

# Critical Issues for the Application of Integrated MEMS/CMOS Technologies to Inertial Measurement Units

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## ABSTRACT

One of the principal applications of monolithically integrated micromechanical/microelectronic systems has been accelerometers for automotive applications. As integrated MEMS/CMOS technologies such as those developed by U.C. Berkeley, Analog Devices, and Sandia National Laboratories mature, additional systems for more sensitive inertial measurements will enter the commercial marketplace. In this paper, we will examine key technology design rules which impact the performance and cost of inertial measurement devices manufactured in integrated MEMS/CMOS technologies. These design parameters include: 1) Minimum MEMS feature size, 2) Minimum CMOS feature size, 3) Maximum MEMS linear dimension, 4) Number of mechanical MEMS layers, and 5) MEMS/CMOS spacing. In particular, the embedded approach to integration developed at Sandia will be examined in the context of these technology features. Presently, this technology offers MEMS feature sizes as small as 1  $\mu\text{m}$ , CMOS critical dimensions of 1.25  $\mu\text{m}$ , MEMS linear dimensions of 1000  $\mu\text{m}$ , a single mechanical level of polysilicon, and a 100  $\mu\text{m}$  space between MEMS and CMOS.

**Keywords:** Microelectromechanical systems, MEMS, inertial measurement, accelerometers, gyros

## 2. INTRODUCTION

MASTER

Modern precision guided munitions that use an inertial measurement unit (IMU) for guidance and control typically rely on the Global Positioning System (GPS) to aid the navigator in removing guidance errors. This marriage of an IMU and a GPS receiver is referred to as a GPS-Aided Inertial Navigation System (GPS/INS). In an environment where the GPS signal is jammed and lost, the IMU will continue to provide input into the munition navigator. However, the navigator's uncorrected errors will grow with time as a function of the IMU quality. Generally, it is accepted that in order to maintain terminal accuracy in a GPS jamming environment, an IMU must contain rotation sensors (gyroscopes) with drift rates of 1 - 10 degrees per hour, and acceleration sensors (accelerometers) with null bias terms of 200 - 1000 micro-g.

The cost, size, and ruggedness of IMUs of this quality have limited their use to (comparatively) expensive ordnance, such as the Joint Direct Attack Munition (JDAM), and the Joint Standoff Weapon (JSOW). Widespread use of GPS-Aided Inertial Navigation Systems would be enabled if a very small, lightweight, inexpensive, and rugged IMU could be fabricated. Silicon microelectromechanical systems (MEMS) is an extremely promising technology that has the potential to achieve these IMU goals. Since inertial sensor cost is typically the primary cost in the production of IMUs, those using MEMS inertial sensors would experience a sharp drop in cost.

The advent of small, rugged, lightweight, and inexpensive inertial navigators would enable the integration of these devices into mass produced munitions, such as artillery shells or small gravity bombs. With a GPS/INS on board, weapon accuracy would improve to essentially GPS accuracy (10 meters circular error precision). This would greatly improve weapon effectiveness and reduce collateral damage.

Though the final goal of this effort is to develop a MEMS IMU which can be used in a munition, there are a range of applications in which MEMS IMUs of lower quality can be used. As shown in Table 1, applications in both defense and

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commercial arenas can be found. In some areas, MEMS accelerometers are already used, such as automotive airbag deployment systems.

Industry	Application	Gyro Bias Stability (deg./hr.)	Accel Bias Stability (micro-g)
Military	Seeker Stabilization <sup>1</sup>	1000	---
Military	Tamper Detection <sup>1</sup>	1000	1000
Military	Environmental Sensing (Stronglink)	100	10000
Military	Stability Control <sup>1</sup>	100	500
Military	Attitude Heading Reference <sup>1</sup>	10	1000
Military	Short Time of Flight Navigation <sup>1</sup>	10	1000
Military	Precision Guided Munition	1	300
Military	Cruise Missile <sup>1</sup>	0.01	50
Military	Strategic Missile <sup>1</sup>	0.001	1
Commercial	Video Image Stabilization	1000	---
Commercial	Automotive Control <sup>1</sup>	1000	1000
Commercial	Automotive Diagnostic <sup>1</sup>	500	1000
Commercial	Automotive Navigation <sup>1</sup>	100	500
Commercial/Military	Virtual Reality Environment Sensor	1000	1000

Table 1. Potential MEMS IMU Applications

### 3. MONOLITHIC INTEGRATION OF MICROELECTRONICS AND MICROMECHANICS

Recently, a great deal of interest has developed in manufacturing processes that allow the monolithic integration of MicroElectroMechanical Structures (MEMS) with driving, controlling, and signal processing electronics. This integration promises to improve the performance of micromechanical devices as well as the cost of manufacturing, packaging, and instrumenting these devices by combining the micromechanical devices with an electronic sub-system in the same manufacturing and packaging process. For example, Analog Devices has developed and marketed an accelerometer<sup>2</sup> which illustrates the viability and commercial potential of this integration. They accomplished this task by interleaving, combining, and customizing their manufacturing processes which produce the micromechanical devices with the processes that produce the electronics. In another approach, researchers at Berkeley<sup>3</sup> have developed a modular integrated approach in which the aluminum metallization of CMOS is replaced with tungsten to enable the CMOS to withstand subsequent high-temperature micromechanical processing. The results of Sandia's implementation of Berkeley's CMOS-first approach have previously been presented.<sup>4</sup>

In order to maintain the modularity of the Berkeley approach but overcome some of the manufacturing challenges of their CMOS-first approach, Sandia National Laboratories has developed a MEMS-first process. This process places the micromechanical devices in a shallow trench, planarizes the wafer, and seals the micromechanical devices in the trench. These wafers with the completed, planarized micromechanical devices are then used as starting material for a conventional CMOS process. This technique is equally applicable to other microelectronic device technologies such as bipolar or BiCMOS. In our facility, both 2  $\mu\text{m}$  and 0.5  $\mu\text{m}$  CMOS technologies on 6 inch wafers are available; the 2  $\mu\text{m}$  process is being used as the development vehicle for the integrated technology. Since this integration approach does not modify the CMOS processing flow, the wafers with the subsurface micromechanical devices can also be sent to a foundry for microelectronic processing. Furthermore, the topography of multiple polysilicon layers does not complicate subsequent

photolithography. A high-temperature anneal is performed after the devices are embedded in the trench prior to microelectronics processing. This anneal stress-relieves the micromechanical polysilicon and ensures that the subsequent thermal budget of the microelectronic processing does not affect the mechanical properties of the polysilicon structures. This anneal can affect the doping profile of commonly used epitaxial starting material; however, this effect can be easily addressed by increasing the epitaxial layer thickness of the starting material.

#### 4. THE EMBEDDED MEMS PROCESS

Sandia's MEMS-first process has been described previously in more detail.<sup>5</sup> Figure 1 is a schematic cross-section of the integrated technology. First, alignment marks are etched onto the surface of wafer in order to provide reference locations for subsequent processing. A shallow trench (~ 6  $\mu\text{m}$  for the single-level polysilicon structures described here) is etched in (100) silicon wafers using an anisotropic etchant. The alignment marks from the top surface of the wafer are used as references to generate another set of alignment marks on the bottom surface of the trench.

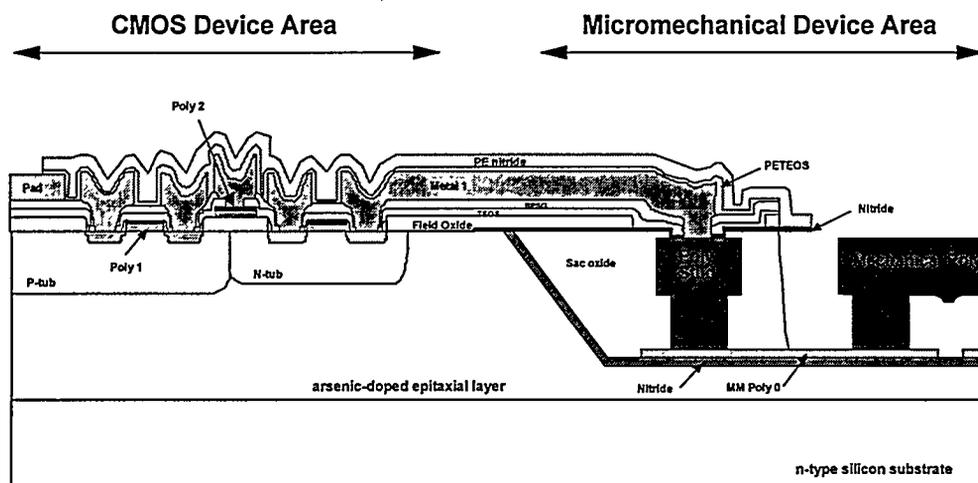


Figure 1. A cross-sectional schematic of the subsurface, embedded MEMS integrated technology.

A silicon nitride film is deposited to form a dielectric layer on the bottom of the trench. Multiple layers of polysilicon and sacrificial oxide are then deposited and patterned in a standard surface micromachining process. Polysilicon studs provide contact between the micromechanical devices and the CMOS; the depth of the trench is sized so that the top of the polysilicon stud lies just below the top of the trench. The shallow trenches are then filled with a series of oxide depositions optimized to eliminate void formation in high-aspect-ratio structures. The wafer is subsequently planarized with chemical-mechanical polishing (CMP). The entire structure is annealed to relieve stress in the structural polysilicon and sealed with a silicon nitride cap. At this point, conventional CMOS processing is performed. The backend of the process requires additional masks to open the nitride cap over the micromechanical layer prior to release of the micromechanical structures.

Photoresist is used as a protection layer over the exposed aluminum bond pads during the release process. The slow etching of the undoped, densified glasses used as sacrificial layers and the ability of this photoresist to withstand long, HF-based etches are presently a factors that impose limits on the design rules used for spacing of release access holes in the structure.

Figure 2 shows a cross-sectional view of an anchor point for the MEMS device within a trench after planarization. The silicon nitride dielectric layer, the ground plane polysilicon, the micromechanical polysilicon and the sacrificial/planarizing layers are easily seen in this Scanning Electron Micrograph (SEM). Completed MEMS next to their controlling CMOS are shown in Figure 3.

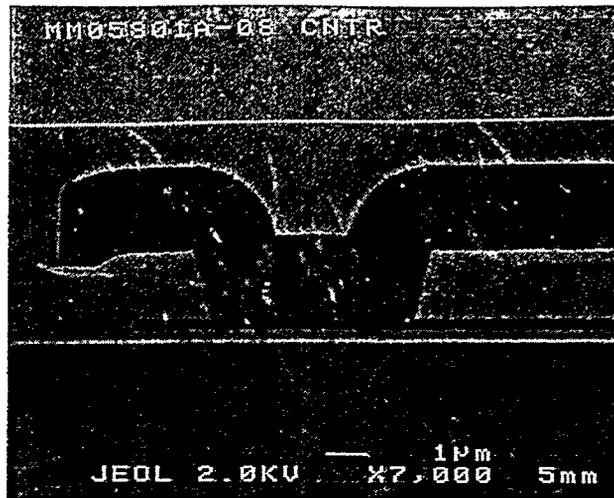


Figure 2. A cross-sectional view of a single-layer polysilicon (with ground plane) structure in a trench. The trench has been refilled with oxide and planarized using chemical-mechanical polishing. This planar structure is ready for standard CMOS processing.

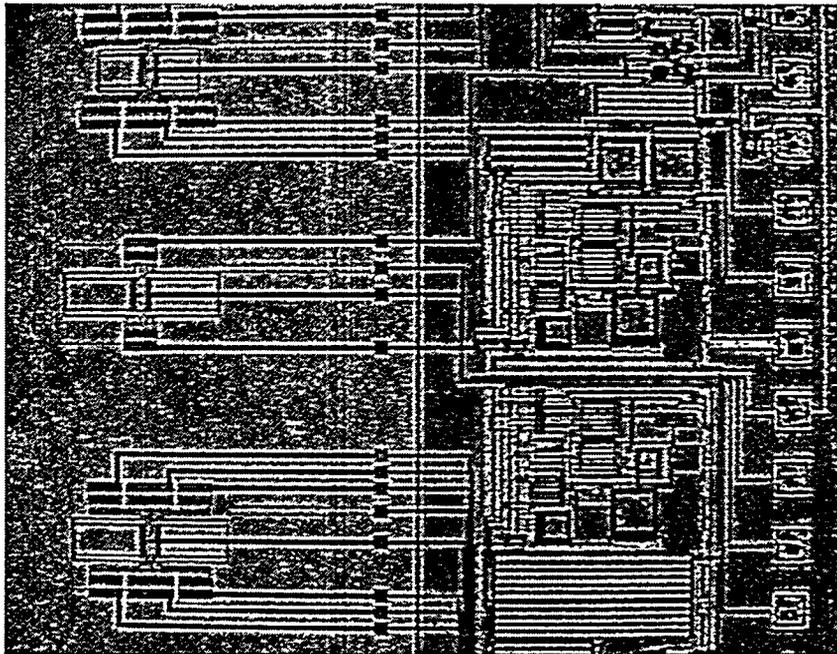


Figure 3. Surface-micromachined polysilicon resonators built in a trench alongside their CMOS sensing electronics. The marks on the bonding pads were caused during wafer-level testing.

This integration process is not limited to the single-level polysilicon process described here. This process can be used with more intricate micromechanical processes such as the three-level polysilicon technology previously developed at Sandia.<sup>6</sup>

## 5. INERTIAL SENSORS

One of the principal commercial products utilizing surface-micromachining is inertial sensors as illustrated by Analog Devices' ADXL150<sup>7</sup> and Motorola's XMMAS40GWB<sup>8</sup>. These accelerometers find their primary application as airbag-deployment sensors in the automobiles, but are also being used as tilt sensors or shock sensors. (In the following discussion, please note the use of  $g$  for the unit of Earth acceleration and the word gram for mass). The Motorola device is a  $\pm 40g$  (full scale) single-axis accelerometer with a noise floor of 400 mg (400 Hz bandwidth, peak) and has an analog

output.<sup>8</sup> The Analog Device accelerometer is available as either a single- (ADXL150) or dual-axis device (ADXL250), has a +/- 50g full scale output, an analog output, and a noise floor of 10 mg (100 Hz bandwidth, rms).<sup>7</sup> It should be noted that the use of peak vs. rms noise specifications along with the difference in bandwidth specifications on each device do not lead to a direct comparison between the devices.

The application of these types of accelerometers to inertial measurement units is limited by the need to manually align and assemble them into three-axis systems, the resulting alignment tolerances, their lack of on-chip A/D conversion circuitry, and their lower limit of sensitivity. In order to overcome some of these limitations, a three-axis, force-balanced accelerometer was designed at U.C. Berkeley<sup>9</sup> and fabricated at Sandia with the integrated MEMS/CMOS described earlier in this paper. As reported by Lemkin<sup>9</sup>, this +/- 25g accelerometer demonstrated an in-plane axis rms noise floor of 110  $\mu\text{g}/\sqrt{\text{Hz}}$  and an 84dB dynamic range at 100 Hz bandwidth. This performance significantly expands the number of applications for surface micromachined accelerometers, but could still use further improvement in order to meet additional application requirements. Additional micromachined inertial components are also being built in the Sandia technology such as the resonant accelerometers of Roessig<sup>10</sup>, the dual-axis (in-plane) rate gyro of Juneau<sup>11</sup>, the Z-axis (out-of-plane) rate gyro of Clark<sup>12</sup>, and the high-shock accelerometer of Davies<sup>13</sup>.

The most direct comparison for devices manufactured in this technology are devices manufactured in Analog Devices' interleaved MEMS/BiCMOS process such as the ADXL250 or the ADXL05 (+/- 5g full scale, 0.6 mg rms noise floor at 100 Hz bandwidth). The smaller dynamic range and higher noise floor of these devices as compared to Lemkin's device is indicative of the limitations of the Analog technology such as its 3  $\mu\text{m}$  critical dimensions for its BiCMOS process, the use of diffused interconnects between the MEMS and the BiCMOS, and the stress-limitations to proof mass size for interleaved processes.

## 6. CRITICAL TECHNOLOGY FEATURES

In pushing the design limits of surface micromachining integrated with controlling electronics, particular features of technologies are critical to one's ability to design sensitive, robust, high dynamic range inertial sensors. Figure 4 illustrates some of these critical technology features for the integrated MEMS/CMOS technology described previously in this paper along with a roadmap for their progression and the first-order benefits of technology progression in that area. This figure uses CMOS as an example of the controlling microelectronic technology, but progressions in figures of merit for other microelectronic technologies such as bipolar or BiCMOS would have similar value.

CMOS CD	MEMS CD	Multi-Level MEMS	Max MEMS Linear Size	MEMS/CMOS Spacing
1.25 $\mu\text{m}$	1 $\mu\text{m}$	1	1000 $\mu\text{m}$	100 $\mu\text{m}$
↓	↓	↓	↓	↓
0.5 $\mu\text{m}$	0.35 $\mu\text{m}$	2	1500 $\mu\text{m}$	20 $\mu\text{m}$
<ul style="list-style-type: none"> <li>•Lower parasitics</li> <li>•Higher sampling rate</li> </ul>	<ul style="list-style-type: none"> <li>•SNR <math>\propto d^3</math></li> <li>•High-aspect-ratio springs</li> <li>•Lower <math>\omega_0</math> &amp; k</li> </ul>	<ul style="list-style-type: none"> <li>•SNR <math>\propto t</math></li> <li>•High-aspect-ratio springs</li> <li>•Increased mass</li> <li>•Z-axis rebalance</li> <li>•Increased robustness</li> </ul>	<ul style="list-style-type: none"> <li>•Increased mass</li> <li>•Increased MOI</li> <li>•Lowered k &amp; <math>\omega_0</math></li> </ul>	<ul style="list-style-type: none"> <li>•Lower parasitics</li> <li>•Increased chip density</li> </ul>

Figure 4. Technology development roadmap for integrated MEMS/CMOS applied to inertial measurement applications.

## 7. CONCLUSIONS

A modular, MEMS-first integrated technology has been applied to inertial sensing applications. Differentiating features of this technology which aid the development of robust, high-dynamic range, low noise floor inertial sensors are the comparatively fine critical dimensions of the technology's CMOS, the use of dielectrically isolated interconnects between

MEMS and the CMOS, and the large proof masses enabled by large, ultra-flat polysilicon structures. The features critical to the continued development of advanced inertial sensors for this and similar integrated technologies are finer microelectronic critical dimensions, finer MEMS critical dimensions, multi-layer MEMS, larger MEMS, and closer coupling of MEMS with the controlling electronics.

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