

EFFECT OF THICK FILM FIRING CONDITIONS ON THE SOLDERABILITY AND STRUCTURE OF Au-Pt-Pd CONDUCTOR FOR LOW-TEMPERATURE, CO-FIRED CERAMIC SUBSTRATES*

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ABSTRACT

Low-temperature, co-fired ceramics (LTCC) are the substrate material-of-choice for a growing number of multi-chip module (MCM) applications. Unlike the longer-standing hybrid microcircuit technology based upon alumina substrates, the manufacturability and reliability of thick film solder joints on LTCC substrates have not been widely studied. An investigation was undertaken to fully characterize such solder joints. A surface mount test vehicle with Daisy chain electrical connections was designed and built with Dupont™ 951 tape. The Dupont™ 4569 thick film ink (Au76-Pt21-Pd3 wt.%) was used to establish the surface conductor pattern. The conductor pattern was fired onto the LTCC substrate in a matrix of process conditions that included: (1) double versus triple prints, (2) dielectric frame versus no frame, and (3) three firing temperatures (800°C, 875°C and 950°C). Pads were examined from the test vehicles. The porosity of the thick film layers was measured using quantitative image analysis in both the transverse and short transverse directions. A significant dependence on firing temperature was recorded for porosity. Solder paste comprised of Sn63-Pb37 powder with an RMA flux was screen printed onto the circuit boards. The appropriate components, which included chip capacitors of sizes 0805 up to 2225 and 50 mil pitch, leadless ceramic chip carriers having sizes of 16 I/O to 68 I/O, were then placed on the circuit boards. The test vehicles were oven reflowed under a N₂ atmosphere. The solderability of the thick film pads was also observed to be sensitive to the firing conditions. Solderability appeared to

degrade by the added processing steps needed for the triple print and dielectric window depositions. However, the primary factor in solderability was the firing temperature. Solderability was poorer when the firing temperature was higher.

INTRODUCTION

Multichip module (MCM) technologies are differentiated from other technologies by their ability to fabricate multilayer interconnection structures that are capable of packaging a higher ratio of silicon area to substrate area than conventional hybrid technologies. An MCM is a package in which the silicon area is generally 30 percent or more of the substrate area. The MCM technologies are not new; however, their applications have expanded recently, particularly in telecommunications applications. Demands for more functionality in a smaller space have exceeded the capabilities of hybrid circuits. Understanding the properties of the materials used to fabricate MCM's can lead to increased packaging density and an ever greater range of applications^[1].

Material suppliers continue to improve quality, processability, and reduce costs for low-temperature co-fired (LTCC) material systems^[2]. LTCC ceramics, often referred to as glass/ceramics, are designed to be fired at lower temperatures, in the 850 – 1050°C range. This permits the use of standard thick film materials, such as silver and gold. It also allows the addition of thick film passive components after firing to eliminate the cost of

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purchasing and mounting passive components^[3]. The behavior of interest in the present study is the effect of firing temperature on porosity. Solderability and joint strength assessments will be presented in a follow-up report.

EXPERIMENTAL

The LTCC test vehicle in this evaluation used the Dupont™ 4569 thick film ink with Au76-Pt21-Pd3 (wt.%) metallization. The test vehicle measures 2.60" x 2.60" x 0.042" thick. A completed test vehicle is illustrated below in Fig. 1.

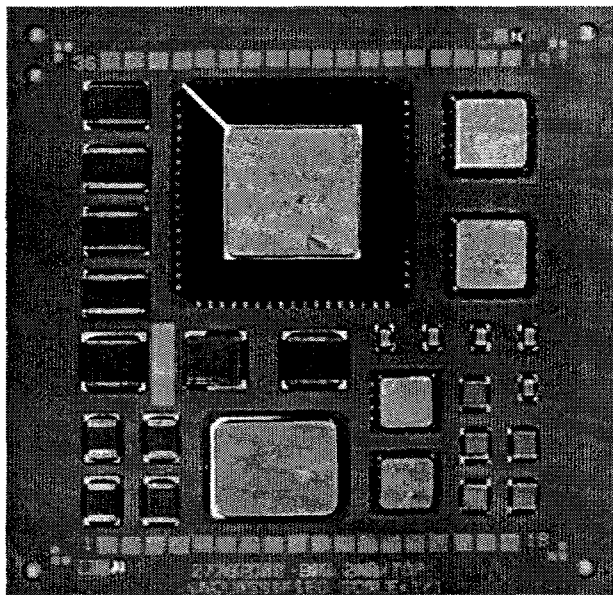


Fig. 1. The populated LTCC test vehicle has 21 chip capacitors and 6 leadless ceramic chip carriers.

The circuit design has a daisy-chained configuration to permit the measurement of electrical continuity during testing. The test components consist of a variety of dummy chip capacitors (0805, 1210, 1812, 1825 and 2225). The chip capacitors used in this study have 100% Sn terminations. There are also four sizes of leadless ceramic chip carriers (LCCC's). The LCCC's have Au castellations with 16, 20, 32 or 68 input/outputs (I/O's) and a 50 mil pitch.

The reflow soldering operation used to populate the test vehicles involves screen printing the solder paste on to the unpopulated test substrate with an 0.008" thick stencil. Sn63-Pb37 solder paste with an RMA flux was screen printed onto the circuit boards. The components were then placed on the paste. The test vehicles were processed through a five zone IR convective reflow machine. The part moves across the heat zones at a line speed of 15 in./min. The peak topside temperature of this board was 221°C. The time above the solder melting temperature

(183°C) was 1 min. 10 sec. to assure adequate solder reflow.

RESULTS AND DISCUSSION

Quantitative image analysis was used to assess the porosity of the thick film layers from the test vehicle for each of the processing conditions. Those conditions included three firing temperatures (800, 875 and 950°C), double or triple printing and with or without a dielectric window. The presence of the dielectric window required additional high temperature firing steps. The thick film pads were metallographically cross-sectioned, mounted and polished. Two edge and two center photos for each of five pads on each board were analyzed. Fig. 2a-c illustrates an SEM/backscattered image of the thick film without the dielectric frame. Note the difference in the microstructure for each of the processing temperatures. The films appear to become more dense at the higher firing temperatures.

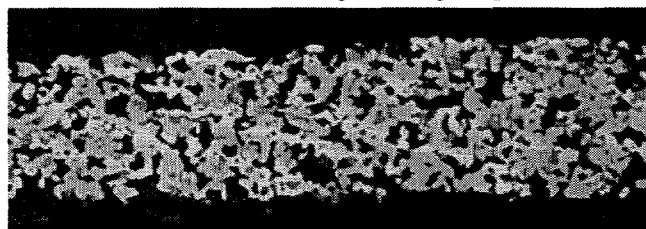
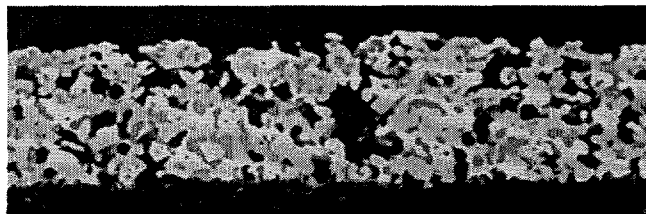


Fig. 2a. SEM/backscattered image of thick film fired at 800 °C.



(b) 875°C



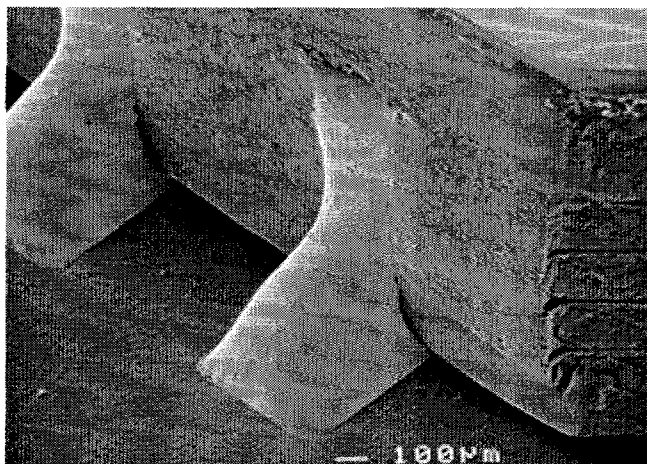
(c) 950°C.

Table 1 illustrates the differences in the thick film porosity for the double and triple printed boards with and without a dielectric window. The porosity of the thick film on the double printed substrates without a dielectric window is 31.2% at 800°C, 26.2% at 875°C and 20.1% at 950°C. In contrast, the porosity of the triple printed substrates, also without the dielectric window, is 26.0% at

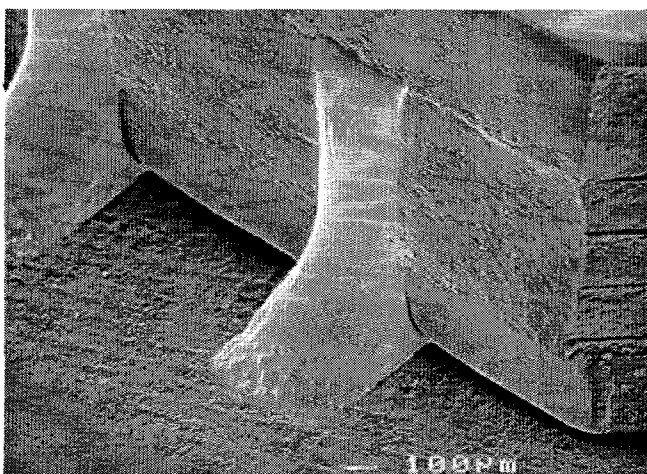
800°C, 24.3% at 875°C and 15.0% at 950°C. These data show that the thick film increased in density as the firing temperature was increased.

A comparison of the thick film porosity is shown in Fig. 3a-b for each of the five pads on the double and triple printed substrates. The trend in porosity was not monotonic when the dielectric was added to the process sequence although the general behavior also suggests that a higher firing temperature decreased film porosity.

Shown below in Fig. 4a-b is a SEM image of a solder joint on the 32 I/O LCCC fired at 875°C with and without the dielectric window. Note the slight difference in the joint smoothness and shape of the solder fillet.



(a)



(b)

Fig. 4. SEM image of a solder joint on the 32 I/O LCCC printed without the dielectric window (a); and with the dielectric window (b).

CONCLUSIONS

Quantitative image analysis has been evaluated on prototype surface mount LTCC circuit boards. The overall porosity of the films was reduced after the 800 and 875°C firings when the dielectric was present than in those samples without the dielectric. The difference was less significant after the 950°C firing step between the two cases. This trend indicates that the heat input resulting from the additional firing step required by the dielectric window had the anticipated effect of further densifying the thick film.

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REFERENCES

1. Jerry E. Sargent, "Materials for Multichip Modules", *Electronic Packaging & Production*, pp. 28-29, Dec. 1996.
2. Donald R. Schroeder, Larry J. Rexing, "LTCC MCM Technology for Military Environments", *MCM '94 Proceedings*, pp. 612-614, 1994.
3. Robert Crowley, "MCM Fabrication Technology Matures", *Electronic Packaging & Production*, p. 57, Sept. 1995.

**Table 1. Thick Film Porosity for LTCC Boards
with and without the Dielectric Window**

Firing Temp (°C)	Double Printed							
	No Dielectric Window				Dielectric Window			
	Mean Area	Variance x # of particles	Maximum Area	% Porosity	Mean Area	Variance x # of particles	Maximum Area	% Porosity
800	7.03 E-06	8.56 E-07	3.13 E-04	31.16	6.81 E-06	8.00 E-07	2.59 E-04	26.78
875	9.17 E-06	9.73 E-07	4.83 E-04	26.23	8.13 E-06	7.81 E-07	3.27 E-04	19.66
950	1.07 E-05	5.52 E-7	3.61 E-04	20.36	7.12 E-06	9.70 E-07	3.13 E-04	23.24

	Triple Printed							
	No Dielectric Window				Dielectric Window			
	Mean Area	Variance x # of particles	Maximum Area	% Porosity	Mean Area	Variance x # of particles	Maximum Area	% Porosity
800	6.06 E-06	6.72 E-07	2.33 E-04	26.02	6.57 E-06	7.67 E-07	2.71 E-04	24.14
875	9.53 E-06	6.86 E-07	2.32 E-04	24.31	9.50 E-06	1.28 E-07	4.55 E-04	23.22
950	6.98 E-06	5.15 E-07	2.99 E-04	14.96	6.62 E-06	8.36 E-07	2.30 E-04	17.64

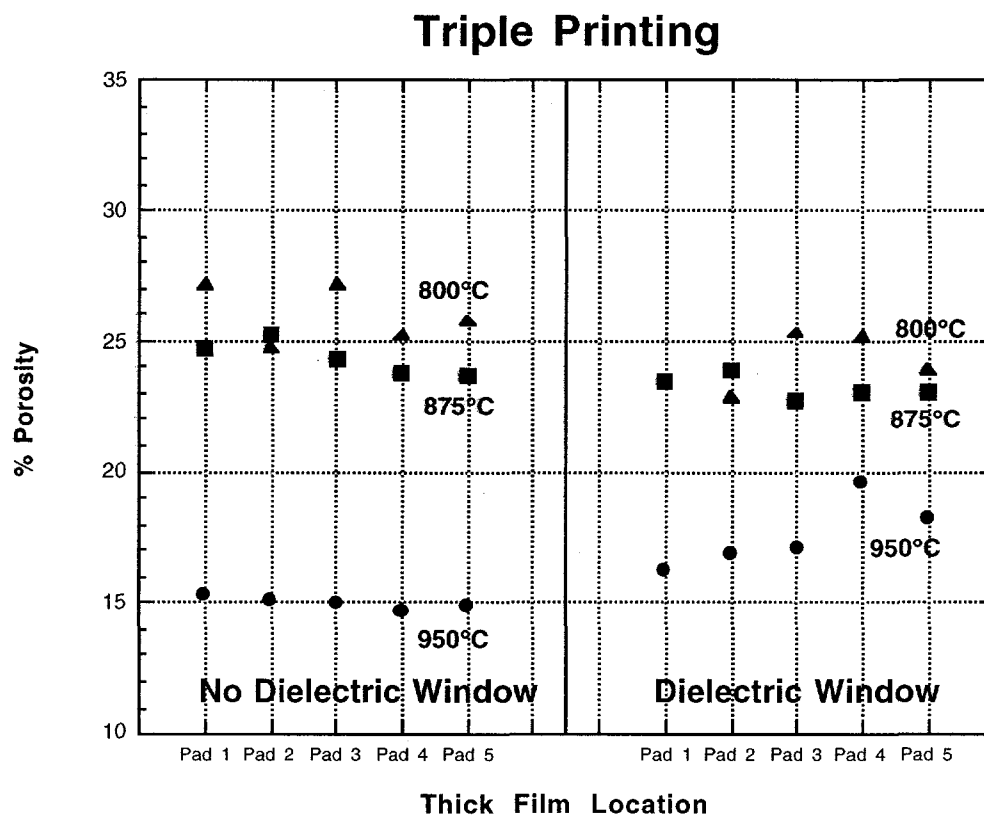
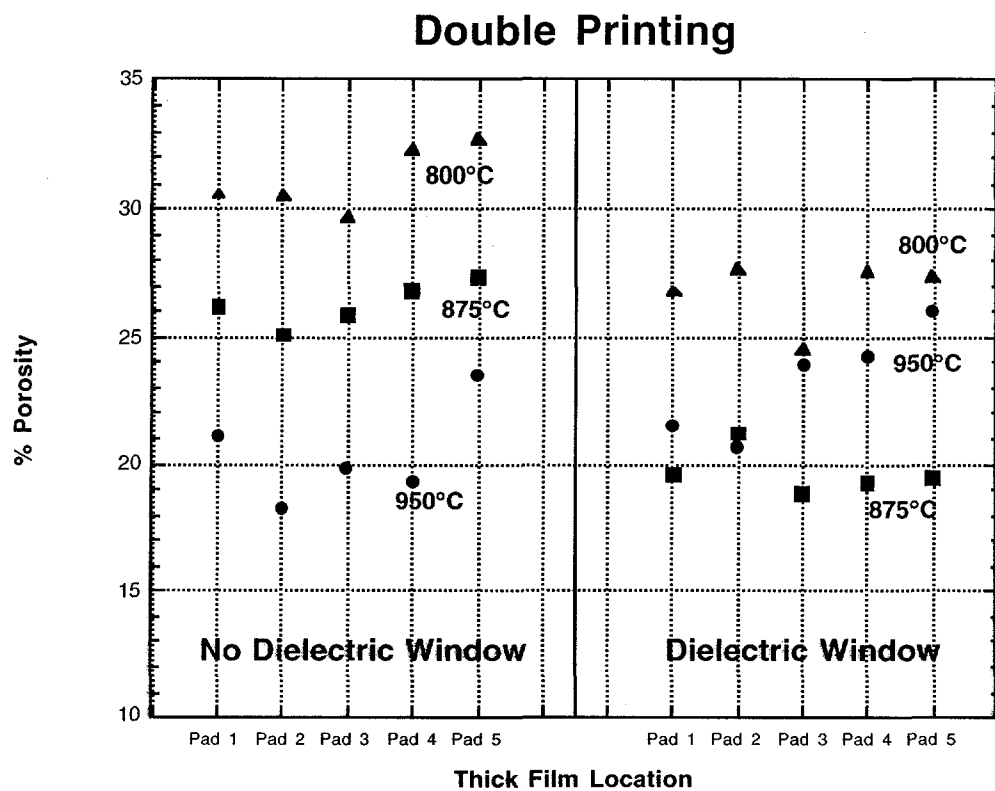


Figure 3. Porosity comparison of each of the five thick film pads for each of the firing temperatures on the double and triple printed substrates with and without the dielectric window.