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Microelectronics Plastic Molded Packaging

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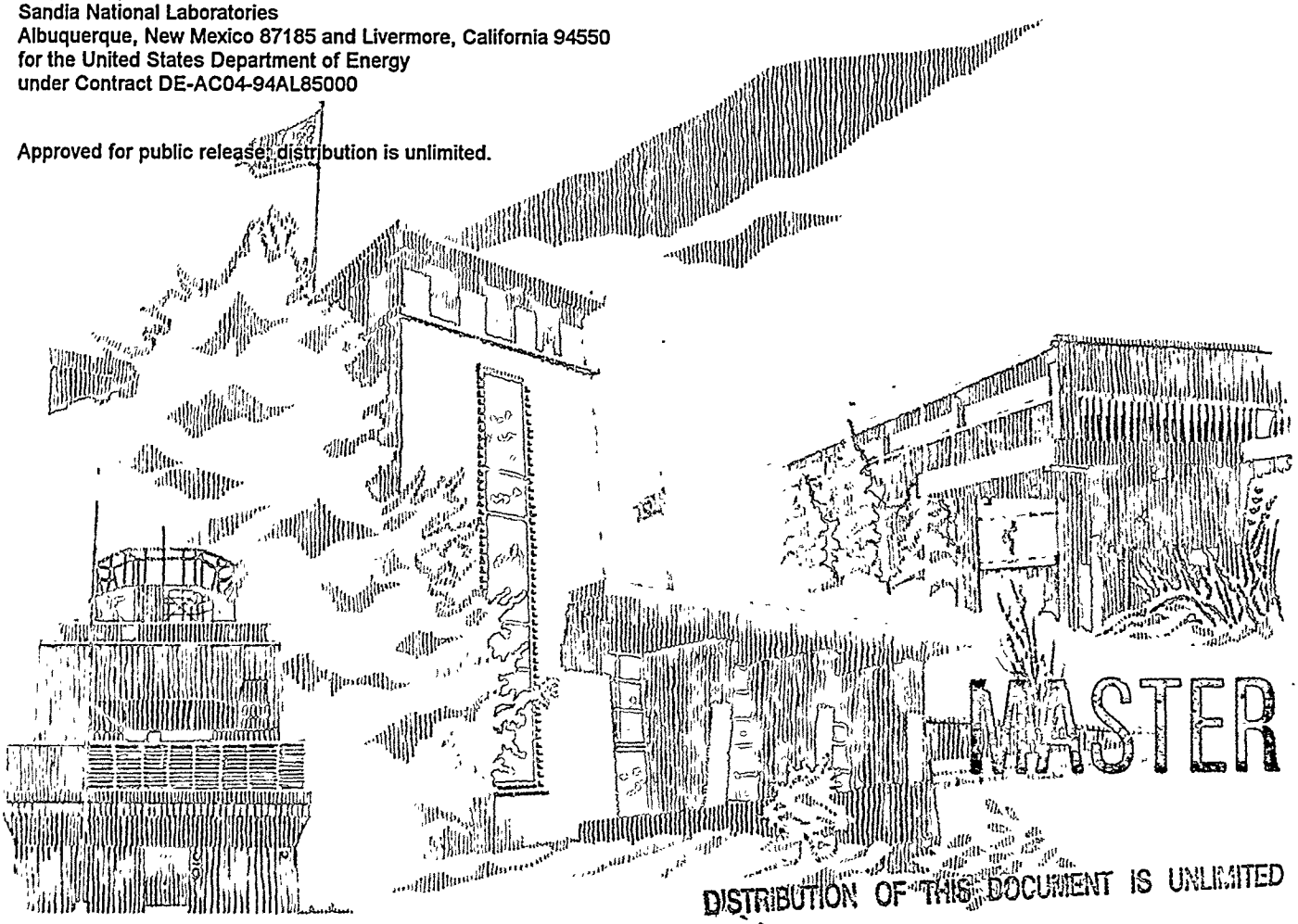

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MICROELECTRONICS PLASTIC MOLDED PACKAGING

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Abstract

The use of commercial off-the-shelf (COTS) microelectronics for nuclear weapon applications will soon be reality rather than hearsay. The use of COTS for new technologies for uniquely military applications is being driven by the so-called Perry Initiative that requires the U.S. Department of Defense (DoD) to accept and utilize commercial standards for procurement of military systems. Based on this philosophy, coupled with several practical considerations, new weapons systems as well as future upgrades will contain plastic encapsulated microelectronics. However, a conservative Department of Energy (DOE) approach requires lifetime predictive models. Thus, the focus of the current project is on accelerated testing to advance current aging models as well as on the development of the methodology to be used during WR qualification of plastic encapsulated microelectronics. An additional focal point involves achieving awareness of commercial capabilities, materials, and processes. One of the major outcomes of the project has been the definition of proper techniques for handling and evaluation of modern surface mount parts which might be used in future systems. This program is also raising the familiarity level of plastic within the weapons complex, allowing subsystem design rules accommodating COTS to evolve. A two year program plan is presented along with test results and commercial interactions during this first year.

Acknowledgment

We would like to especially thank Alex Hsia and Robert Mitchell for their efforts in instrumentation, measurement, and data analysis. They successfully developed and debugged an accelerated testing methodology for high pin count plastic packages in parallel with the experiment itself, a near impossible feat. We would also like to thank Simone Smith for the fine SEM imagery she provided.

Contents

Executive Summary

The primary question addressed by this project concerns the reliability equivalence of plastic encapsulated microelectronics versus ceramic, hermetic integrated circuits when utilized for weapon applications. The project focused on the exposure of plastic encapsulated Sandia-designed assembly test chips to a myriad of environmental specifications for weapon transport and storage, as well as the evaluation of a wide ranging set of temperature/humidity/bias conditions for highly accelerated stress testing which would lead to the development of lifetime predictive models. Additional focal points have included familiarization with the numerous military and commercial specifications addressing plastic devices, and liaison with the commercial industry to determine current field reliability data.

Preliminary Results:

1. Temperature/Humidity/Bias
    - Early problems in test chip design and handling techniques, as well as in commercial wafer thinning, were resolved.
    - Initial long term dormant storage and highly accelerated stress tests were conducted. A consistent story of aging is emerging.
    - Some subsystem design rules—not unlike those now in place to accommodate ceramic devices—must be determined for plastic devices.
    - Failure analysis techniques were developed for decapsulation of plastic packages. Specific F/A techniques for determination of processing defects, damage to glass passivation, opens, shorting, isolated segments, and hot spots were developed and enhanced.
    - The baseline for analysis of package integrity was developed by utilizing C-mode scanning acoustic microscopy. This technique will be used to determine package delamination and cracking defects, as well as wire sweep problems.

2. Military & Commercial Specifications
    - Specifications for high reliability military and commercial applications have been identified, compared, and contrasted.
    - Specifications for plastic and ceramic devices are overlapping except in the areas of dormant storage, temperature extremes, shock, and radiation effects.

3. Commercial Industry Liaison
    - High reliability applications of commercial product reveal equal, or better, results compared to ceramic, hermetic devices.
    - A reliable, commercial plastic packaging foundry was identified, and utilized.
    - A reliable, commercial wafer thinning facility was identified , and utilized.
    - Potential destructive and nondestructive screening and qualification test techniques have been identified from the literature and from commercial contacts.

MICROELECTRONICS PLASTIC MOLDED PACKAGING

Donald R. Johnson

I. Introduction

Plastic encapsulated microelectronics (PEMs), with significant advantages in size, weight, performance, availability, and cost, represent approximately 95% of the worldwide market share for microcircuit sales.[1] Acceptance of PEMs has come in spite of formidable challenges over the last 20 years wherein the technology was considered cheap but unreliable due to corrosion, cracking, and delamination problems. Technology improvements throughout the last two decades focused on the molding compounds, improved fillers, and significant process parameters. The resultant changes have been revolutionary so that not only are low-cost PEMs commonplace but they are also high-quality, high-reliability and high-performance.

Recently, the "Perry Initiative" (Secretary of Defense William Perry, June, 1994) that mandates the use of commercial off-the-shelf (COTS) equipment for the Department of Defense (DoD) has reinforced the utilization of plastic encapsulated microelectronics in both the commercial and defense arenas.[2] Because of this emphasis, new technology will likely be available first, and perhaps only, in plastic encapsulated microelectronics assembled on commercial six-sigma production lines. The concern that this brings to the typical 20-year product life requirement for military systems is found in the inherent obsolescence of the commercial marketplace where today's technology is replaced with new technology every two to three years and the original product then becomes unavailable. In contrast, both the availability and reliability of the traditional hermetic ceramic IC package have decreased because low volume makes it no longer economically feasible to maintain a tightly controlled production line for hermetic packages. Obviously, the continued evolution of the commercial plastic package will compound the critical issues of cost and availability of hermetic packages.

Currently there are many man years of design and development represented with PEMs, and there are hundreds of millions in the field. Aging mechanisms and materials properties are being better defined while there is ongoing modeling of failure mechanisms. Thus, it is reasonable to assume that not only new weapon systems but also upgrades to existing weapon systems will utilize plastic encapsulated semiconductor devices.

II. Scope

The current Microelectronics Plastic Molded Packaging program was structured to pursue, over a two to three year period, the following two goals:

A. **Develop a thorough understanding of materials and property aging for plastic molded device packages—thus leading to standard screening and qualification methodology.**

B. Use of commercial plastic encapsulated semiconductor devices in WR applications.

The basic scope of the program included fundamental research comparing available plastic molding compounds and the parameters of the molding process. In addition, accelerated aging techniques were to be verified as realistic so that developmental qualification of components could take place. The intent was to compare the methodology for accelerated aging to industry field failure statistics as well as the physics of each aging mechanism so that realistic lifetime reliability models could be developed. The vehicle for the basic studies is the Sandia designed and fabricated test IC that has been used jointly with industry for the last 3 years to measure the degradation on a test chip from within a package. These chips allow quantitative monitoring of moisture, ionic, mechanical, thermal, and electrical degradation in both plastic and hermetic packages.

With qualification of vendors absolutely necessary for WR application of PEMs, the program was to define the appropriate environmental, thermal, and shock tests that would be utilized to qualify several potential WR component production lines. The project scope required packaged parts from these lines be exposed to accelerated aging tests verified as appropriate for WR stockpile conditions. A determination must be made regarding the use of COTS components versus the need for customized plastic encapsulated devices.

Ultimately system acceptance for WR piecepart application often surpasses a qualified vendor and a qualified technology. The highest reliability system specifications may require individual screening of parts and thus the scope of the project included the identification, and development, of nondestructive screens based on moisture susceptibility and temperature cycling sensitivity.

A major modification was made to the project plan toward the end of the third quarter when it was determined that the project would not be funded for the second year. This led to a stop on procurement of SRAM devices fabricated by commercial sources, and to the restriction for testing only in those areas that could logically be halted and reported on within this fiscal year. A significant amount of test work would have carried over into year two of the project.

The Project Team consisted of the following participants: M. E. Neuman, Program Contact, 2254; B. T. Meyer, Advanced Microelectronics Project Contact, 1274; David W. Palmer, Project Manager, 1333; Donald R. Johnson, Project Leader, 1333; Alex H. Hsia, Robert T. Mitchell, David W. Peterson, David S. Shen, and James N. Sweet, 1333/Advanced Packaging; James T. Hanlon, 1252/Component Information & Management; and Kenneth A. Peterson, 1275/Failure Analysis.

The Summary Gantt Chart for the program is illustrated below in Figure 1. The results from the FY96 Microelectronics Plastic Molded Packaging Project are presented on a task by task basis in subsequent report sections.

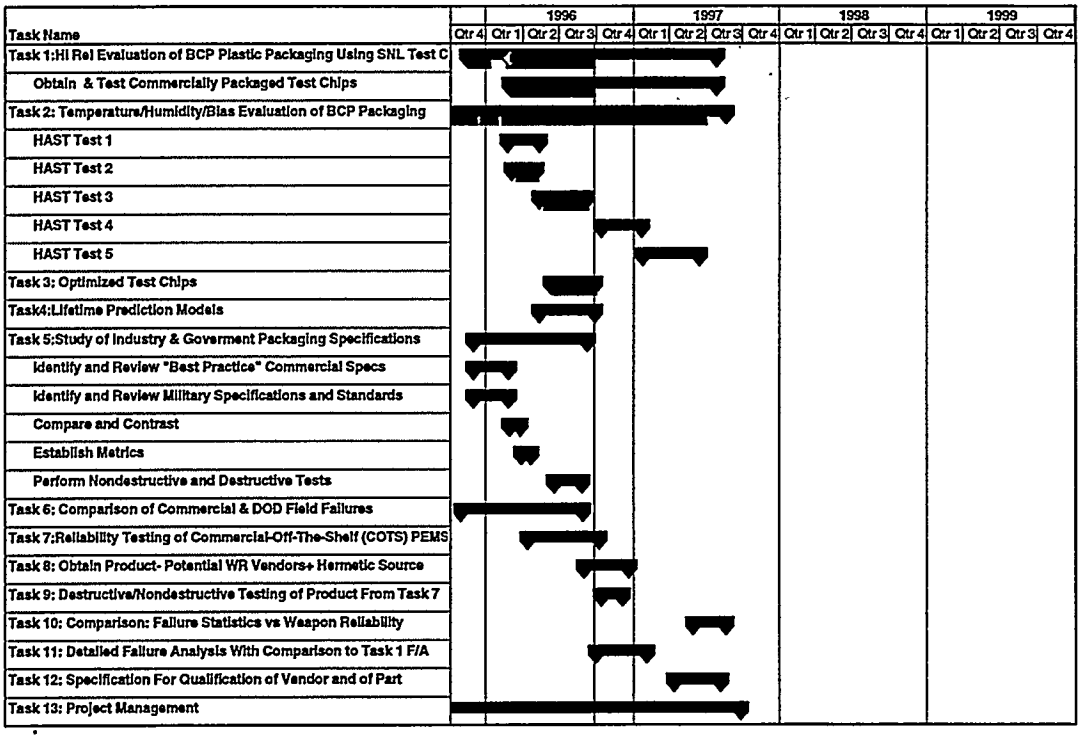


Figure 1. Summary Gantt Chart for Microelectronics Plastic Molded Packaging Project

III. Work Package Agreement

A Work Package Agreement (WPA) was negotiated between the program office and the project office after the project was initiated. The Statement of Work called for "Development of the methodology to be used during WR qualification of plastic molded packages and initial execution of the methodology to qualify potential suppliers." The deliverables enumerated for FY96 included the following specific items with delivery date in ( ); status of each deliverable is shown with the actual date in [ ].

1. **Standard test chip vehicle defined for evaluation (February, 1996)**

   Status: ATC2.6 identified as the primary test vehicle [December, 1995]. This was rooted in the passivated/unpassivated triple tracks available to determine corrosion resistance and moisture sensitivity along with bond pad resistance.

2. **Accelerated aging methods and parameters chosen (March, 1996)**

   a. Temperature/Humidity/Bias (THB) methodology

      Status: Highly Accelerated Stress Tests (HAST) at 159, 140, and 125 °C; 85 and 60 % RH; and 40, 10, and 0 volts bias were chosen as the test parameters [February, 1996].

b. Temperature cycle/shock methodology

Status: Based on transport/storage environments, +155 °C to -65 °C was the identified temperature cycle with one minute change (maximum) between temperatures [February, 1996].

c. Mechanical shock methodology

Status: Hopkinson bar technique for mechanical shock chosen as method for characterizing shock response of plastic packages; 20,000 G's identified as level of shock [February, 1996].

The remainder of the deliverables were set for a September, 1996, timetable. Listed below, these are addressed in the individual task reports.

3. **Initial THB, temperature cycle/shock, and mechanical shock test results reported.**

4. **Initial comparison of commercial with Mil-Spec field results on plastic packages.**

5. **Detailed listing of actual WR aging mechanisms for plastic encapsulated components.**

6. **Preliminary screening methodology for commercial plastic packaging; destructive and nondestructive sampling.**

IV. Summary & Conclusions

The primary question addressed by this project concerns the reliability equivalence of plastic encapsulated microelectronics versus ceramic, hermetic integrated circuits when utilized for weapon applications. On the one hand, the ceramic, hermetic package is probably inherently superior to PEMs except for certain environmental exposure such as extreme shock and vibration. However, the significant reduction in the use of ceramic, hermetic packages has resulted not only in the demise of six sigma manufacturing lines but also to a potential decrease in the overall reliability of ceramic product. In contrast, the preponderance of commercial data reveals PEMs offer a demonstrated field reliability (where six sigma volume manufacturing results in a greater reduction of manufacturing defects than is currently possible with ceramic, hermetic parts) that is equal to if not better than their ceramic counterparts. Thus, while the PEM may not be inherently better than ceramic, it may be a better choice given the prevailing world-wide manufacturing conditions for both plastic and ceramic devices.

Given the lifetime reliability demands of 20 to 40 years, a conservative DOE approach apparently requires a lifetime predictive model especially for moisture related but also for all known failure mechanisms. This is particularly appropriate since the industry experience referred to does not, in general, identify moisture as a current reliability problem, while related laboratory testing of test chips reveals that the predominant failure mode in temperature/humidity/bias exposure of PEMs is bondpad corrosion. The most logical outcome is that plastic encapsulated microelectronics will

be used on an application specific need for future weapon systems, either on a new or upgrade basis, and such utilization will be governed by rigid sub-system design rules (such as moisture and radiation limits) much the same as has been done in the past with ceramic parts (with acceleration and solder type limits) when deemed necessary.

One of the major outcomes of the FY96 Microelectronics Plastic Molded Packaging project has been the definition of proper techniques for performing HAST as well as high temperature storage evaluations with modern surface mount devices of the type which might be used in a future DOE weapons system.

---

[1] Pecht, M. G., Nguyen, L. T. and Hakim, E. B, Plastic-Encapsulated Microelectronics, John Wiley & Sons, New York, 1995.

[2] Wilson, J. R., "Is DOD COTS Initiative Moving Too Fast?," Military & Aerospace Electronics, August, 1996, p. 6.

Task 1

High Rel Evaluation of Best Commercial Practice Plastic Packaging Using SNL Test Chips

Donald R. Johnson

I. Objective

The primary objective of this task was to expose SNL test chips, plastic encapsulated according to best commercial practice, to applicable weapons environmental test specifications. Best Commercial Practice (BCP) represents the best industry has to offer in terms of process control and product quality. The use of SNL test chips was intended to standardize the evaluation.

II. Environmental Test Specifications

The principal guide for determination of environmental exposure conditions was an unclassified Sandia document dealing with transport and storage environments, ES399131.[1] The areas of concern included mechanical shock, thermal shock and temperature cycle, long term dormant storage, and radiation specifications.

Evaluation of the effect of radiation was planned for the second year and thus there are no results to be reported. The thermal shock evaluation was to follow the temperature cycling evaluation which was not completed per the discussion in Section V.

The following exposure levels, for two different weapon system scenarios, were extracted from the referenced environmental specification. The environments were used as guidelines for the limits chosen for testing.

A. Weapon System "A"

- **High Temperature, Long Term**
  - 12 month cycle, ambient 24°C to 53°C
  - Worst case 5 day cycle with maximum skin temperature 66°C
  - Internal heating as much as +7°C
- **High Temperature, Short Term**
  - 24 hour cycle, 32°C to 65.5°C
- **Humidity**
  - Sealed in desiccated compartment, RH<15 % @ 20°C

- **Low Temperature**
  - 12 month cycle, ambient -52°C to 5°C, long term
  - 120 hour cycle, -40°C to -54°C, short term
- **Shock**
  - 20 G to 1400 G

B. Weapon System "B"

- **High Temperature**
  - 66°C for up to 36 months with excursions to 71°C limited to 4 hours in any 24 hour period
- **Low Temperature**
  - -51°C for up to 36 months
- **Humidity**
  - 25% at 20°C
- **Shock**
  - 20 G to 1400 G

Additional information regarding potential weapon environments, along with techniques for testing, was derived through discussions held with personnel from various weapon systems organizations.

III. Plastic Encapsulation

Plastic encapsulation of SNL assembly test chips according to current best commercial practice was a baseline requirement for the project. The packaging foundry chosen was Integrated Packaging Assembly Corporation (IPAC), San Jose, CA.

The molding compound, epoxy novolac with a silica filler, was identified as 6300HJ. This encapsulating resin was considered to be the industry standard in the 1995 time period. The technology for molding compounds was, and is rapidly evolving with constant improvement in the resins, fillers, and other agents for curing, stress-relief, mold release, and flame retardation. Perhaps the greatest improvements in molding compound technology are being made in the epoxy compound used, and especially in the filler size, shape, and content percentage. The 6300HJ material, with a glass transition temperature of 185 °C, served as a good baseline

material for the current project. Improved materials available now through advanced technology may be used for encapsulation in subsequent testing in order to enhance the moisture resistance of the product. Moisture sensitivity of the plastic encapsulant is of particular concern because of its frequently undetected impact on product reliability.

IV. SNL ATC2.6 Assembly Test Chip

The ATC2.6 Assembly Test Chip was chosen as the vehicle by which the commercial encapsulation process could be evaluated. This is a third generation SNL test chip that has been designed to study corrosion resistance, thermal properties, and bondpad resistance. The test chip, illustrated in Figure 1.1, offers 8 sets of aluminum triple track corrosion test structures, 4 of these passivated (with standard 5 KÅ SiN) and 4 unpassivated (cutouts through the passivation layer to expose the underlying triple tracks). Measurements conducted during environmental testing of these chips may include bondpad sheet resistance, gold ball bond resistance, and ball to pad interfacial resistance. Only two connections to the chip are required for biasing all of the triple tracks during accelerated testing. For corrosion experiments, 24 bond outs are required for one side of the 8 triple tracks and 2 bond outs for the commons, making a total of 26 input/output connections. Off-line resistance testing is normally done with the bias removed by sequentially measuring between the three triple track bondpads and the appropriate common bondpad.

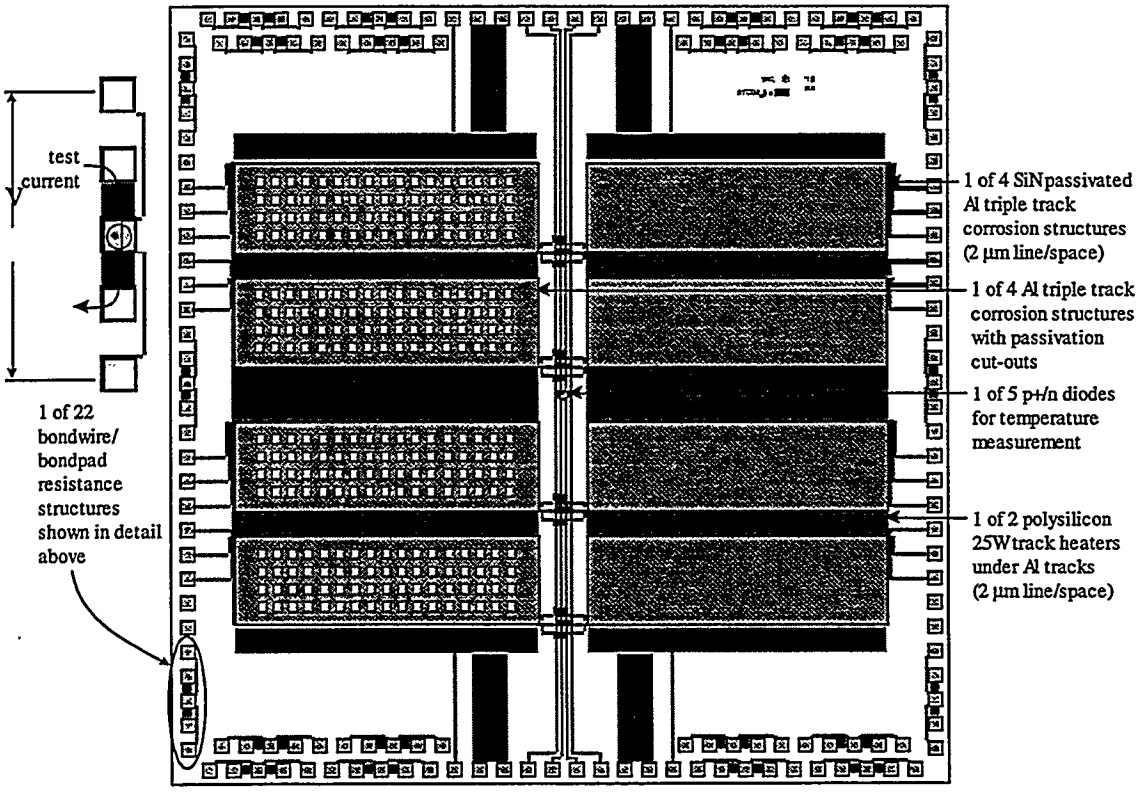


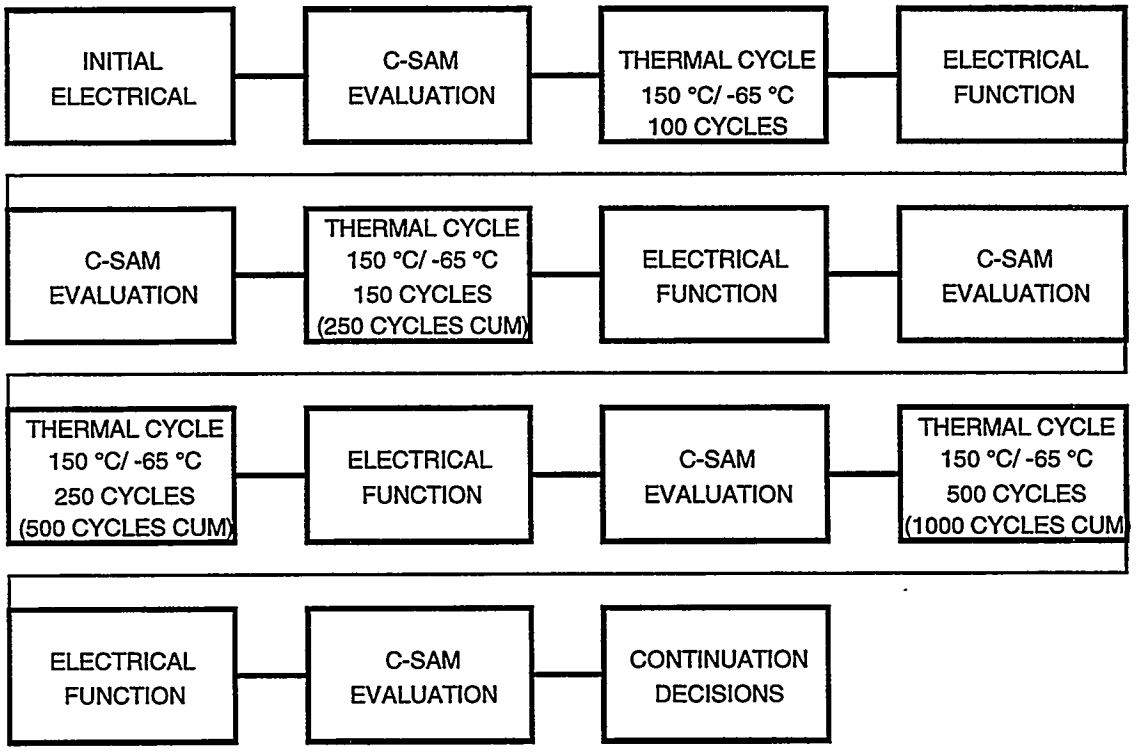
Figure 1.1. ATC2.6 Assembly Test Chip

Additional structural details for this assembly test chip are presented in section IV of the Task 1A write-up.

V. Thermal Cycling Evaluation

While the high temperature requirements of the transport and storage specification were not a concern (commercial devices are typically rated above these values), the low temperature requirements were considered a potential cause for delamination between the die paddle and the epoxy, or between the die and the epoxy. Based on these low temperature requirements observed in the transport and storage environmental specification , a test plan was developed for temperature cycling from +150 °C to -65 °C. The basic plan called for initial electrical measurements of commercially encapsulated ATC2.6 test chips, followed by C-mode scanning acoustic microscopy (C-SAM) to determine the as-fabricated condition of the package with regard to possible delamination and cracking. The plan called for temperature cycling for up to 1,000 cycles with interim testing for electrical response and C-SAM evaluation as may be seen in Figure 1.2.

Figure 1.2. THERMAL CYCLING EVALUATION



Electrical measurements on the as-received devices revealed that the triple tracks were shorted, leaving only the bond pad resistance measurements to be of value. It was decided that the test chips were still usable because the mechanical degradation due to delamination and cracking was of more interest than complete electrical measurements.

Thus, a total of 15 of these plastic encapsulated ATC2.6 test chips were then submitted to Sandia Organization 9752 for C-SAM evaluation. The details of this evaluation are found in the Appendix to this task report.[2]

Following the baseline C-SAM evaluation the packages were submitted to Sandia Organization 9742 for the thermal cycling evaluation. Setup, with dummy parts and trays, was conducted in one of their chambers in order to achieve the proper time at temperature in combination with the required transfer time from hot to cold as stipulated in MIL-STD-883D. During the setup operation a problem was experienced with the chamber; and before the chamber was repaired so the real test could begin it was determined that not only were test funds short but that the program would likely not go into a second year. Thus the temperature cycling evaluation was not begun; however, the plastic encapsulated parts, with baseline C-SAM, are available for test if and when the project is restarted.

VI. Long Term Dormant Storage

The documentation for the long term dormant storage evaluation follows in the write-up for Task 1A.

VII. Mechanical Shock

The mechanical shock requirements were based on earth penetrator program requirements and were listed at 15 - 20K G's according to information obtained from personnel in various weapon systems groups. The test was to be conducted utilizing the Hopkinson bar technique. Discussions were held with personnel from Organization 9742 concerning the test technique. Because of problems with the encapsulated test chips as well as the test plan modification at the end of the third quarter, the mechanical shock tests were not conducted this fiscal year.

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[1] Bell, R. G., Unclassified ES399131, Environmental Specification for MultiApplication Surety Technology (MAST) Demonstration Warhead, Sandia National Laboratories, June, 1995.

[2] Memo, J. H. Gieske to Donald R. Johnson, Ultrasonic C-Scan Imaging of Plastic Molded IC Packages, Sandia National Laboratories, August 19, 1996.

Task 1A: Long Term Dormant Storage

High Rel Evaluation of BCP Plastic Packaging Using SNL Test Chips

David W. Peterson

I. Introduction

The formation of Au/Al intermetallic phases in the interfacial region of a Au ball bonded IC has been extensively studied and documented beginning in the early 70's. These compounds, sometimes referred to generically as "purple plague", are responsible for more IC wire bond failures than any other documented failure mechanism. Intermetallic phases will begin to form during thermosonic wire bonding operations and continue to develop for the life of the product, eventually causing mechanical and electrical failure of the bond through Kirkendall voiding when the time-temperature product is large enough. In principle, changes in resistance of a bond during high temperature storage prior to complete mechanical and electrical failure can be expressed with a simple Arrhenius model, with different activation energies for each intermetallic phase. There is evidence that surface contamination on the bond pad prior to wire bonding, or water soluble additives and/or contaminates within the mold compound, can, in the presence of moisture, accelerate the formation of Au/Al intermetallics. The risk of failure of commercial ICs due to this mechanism is generally very low due to improved materials and processes, relatively benign operating and storage conditions, and short product life cycles. However, the time-temperature product could increase the probability of failure beyond acceptable limits in molded ICs intended for 20-30 year DP applications.

This task does not address all the issues regarding use of commercial PEMs (plastic encapsulated microcircuits) for high rel DP applications, but does develop and apply a test methodology that sheds light on one of the key issues. This methodology is based on high temperature storage (HTS) testing of test chips containing a very sensitive bond pad resistance structure.

II. Au/Al Intermetallic Reactions

The following discussion is taken from Harman[1] and Pecht[2]. At the onset of metallurgical joining of Au and Al during wirebonding, bi-directional diffusion of atomic species across the interface is initiated. There are five principal Au/Al phases or intermetallic compounds formed as a result of this process. Figure 1A.1 contains the binary phase diagram. The $AuAl_2$ phase is colored purple, and was quickly referred to as "purple plague" after its appearance in the early days of IC technology. This phase was generally associated with exposure to high temperatures of Al bond wires on Au thin film pads during the ceramic packaging process, and is seldom observed today due to improved process control. The remaining phases are colored either tan or white, as indicated in Figure 1A.1, but in combination are often gray, brown or black. Vacancies are formed when either the Au or Al diffuses out of a region faster than the other can diffuse in from

the opposite region. These vacancies pile up, eventually forming Kirkendall voids, typically on the Au rich side of the interface. Rates of diffusion vary with temperature, composition of adjacent phases, and number of vacancies in the original metals. Figure 1A.2 shows the intermetallic growth path taken by a binary system as a function of time/temperature product and concentration of each starting component. The path of interest for PEMs is Au>>Al, since Au ball bonding over thin film Al pads is used universally in the transfer molding process.

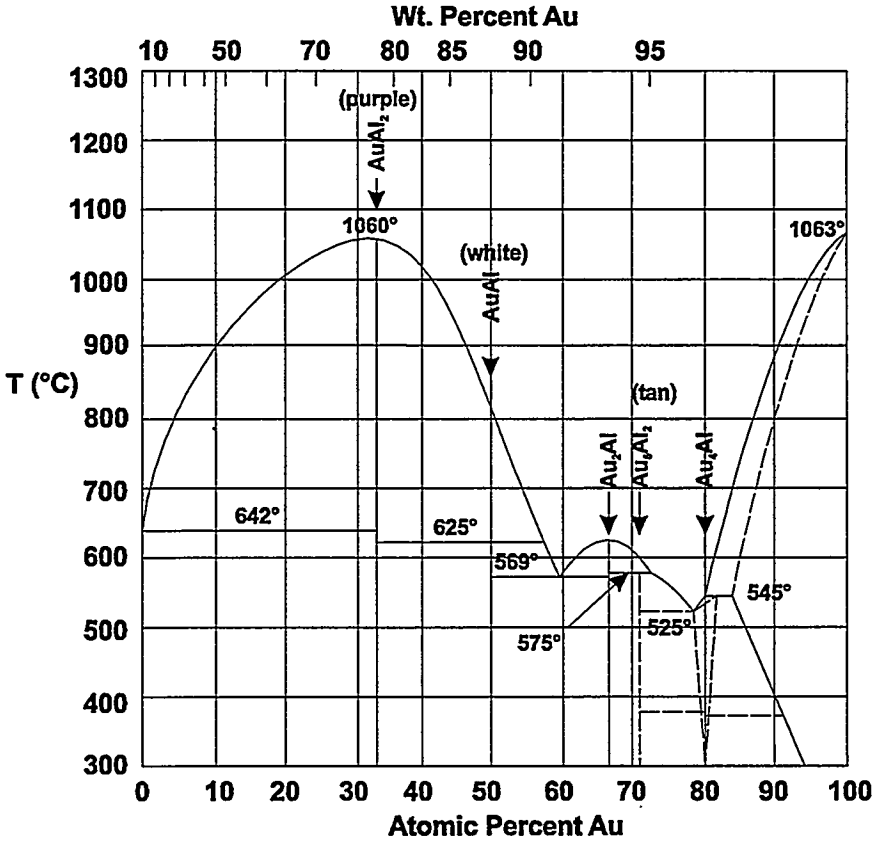

Figure 1A.1. Au/Al phase diagram (after Hansen[3]) showing the five intermetallics.

A. Wire Bond Failure Modes

There are three classical wire bond failure modes associated with the formation of Au/Al intermetallics[1]. In Type I, the thin film Al making up the bond pad voids around the *periphery* of the Au ball resulting in an electrical open, although the bond itself maintains its mechanical integrity. These failures are associated with Au wire on thin film (~1 μm) Al, as used in PEMs. Type II failures occur when Kirkendall voids form *beneath* the bond resulting in loss of mechanical integrity. The bond wire exhibits progressively decreasing pull strength, eventually becoming mechanically detached from the bond pad. This can occur in the Au ball to Al pad region of a plastic molded IC, as in Type I, and also where Al wires are bonded to Au plated surfaces in ceramic hermetic packages. Type III bond failures occur in the intermetallic region during thermal cycle induced flexing of the bond wire. Au/Al intermetallics are stronger than the

pure component metals, but are far more susceptible to brittle fracture during thermal-mechanical flexing of the bond wire. In the case of PEMs, we are primarily concerned with Type I and II failure modes.

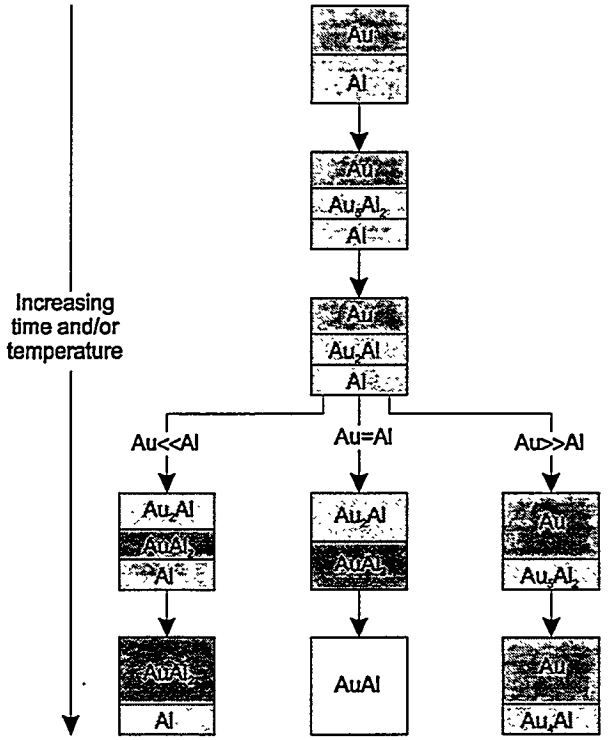

Figure 1A.2. Intermetallic formation path as a function of time/temperature product and species concentration. The final compounds result from the reaction being driven to completion with one component being completely consumed. (after Majni et al[4])

It is well known that halogen compounds can degrade the strength of Au to Al ball bonds. Thomas et al[5] were among the first to observe this effect using devices sealed in various compositions of epoxies containing brominated flame retardants (tetrabromobisphenol-A) that are commonly used in IC molding compounds. Massive wire bond failures occurred within 24 hours at 200 °C. Failure analysis showed a weak laminar microstructure characteristic of an unstable single-phase alloy that has separated, rather than a normal intermetallic compound. Thomas and his co-workers were able to isolate Cl and Br from outgas product from the epoxies used in their experiment, and concluded that these halogens diffused into the bond region from the sides and attacked the intermetallic. Richie and Andrews[6] observed bond failures with similar weak laminar structures caused by Fl from a CF_4/O_2 plasma treatment and even faster failures when Cl from contaminated die attach epoxy was also in the bond interface.

Some researchers believe that H_2O, if not necessary, is at least an active participant in these reactions. Even in the absence of moisture, as in a dry bake, there can be sufficient H_2O evolving from the epoxy to affect the process. Acting as a catalyst or an oxidant, water may cause voiding

and lamellar structure to develop in bond regions at lower temperatures than would otherwise occur.

B. Experimental Approaches to Measuring Bond Degradation

Ahmad[7] et al, studied the effects of bromine flame retardant additives on the degradation of Au/Al bonds. They used a special test chip that provided a modified 4-point measurement of bond resistance in series with an Au bond wire. The experiment examined two mold compounds with varying concentrations of bromine during exposure to 175 °C and 200 °C. In contrast to other studies, Ahmad's change in resistance data was exponential with time, $\Delta R = A \cdot \exp(t/\tau)$, and therefore was plotted as $\log(\Delta R)$ vs. time. (This is the only study found where the time dependency differed from the range n=0 to n=½ using $\Delta R = c[t]^n$). Ahmad calculated activation energy as a function of bromine concentration in both mold compounds and had an interesting observation. The activation energy for both materials converged to ~2.2 eV/atom at decreasing bromine concentrations, but at increasing concentrations (0.4 to 2.8 wt%) they diverged significantly. There appeared to be a difference in the mechanism for degradation between the two compounds. The activation energies at low bromine concentrations are much higher (2.2 eV) than other researchers have reported for bromine free experiments. The authors have no explanation for this anomaly.

Gallo[8] looked at the effect on ball shear force and IC electrical performance of variations in molding compounds, die attach, temperature, and humidity. Ball shear occurs through the Au ball in good bonds, but changes to fracture between the Au ball and Au/Al intermetallic region over time and temperature. The state of bond pad degradation was measured electrically by monitoring parametric shifts of output logic levels set to low logic states (VOL's) on digital ICs during high temperature storage. A shift in output level under constant current is indicative of increasing series resistance in the respective bond wire/bond pad. Molding compounds without Sb_2O_3, and containing an ion scavenger performed the best. The most improved reliability found in electrical testing was for devices with pure Al pad metallization encapsulated with non-Sb_2O_3 (antimony trioxide – a flame retardant synergist) containing molding compounds of high catalyst level and using a low water extractable Cl ion die attach.

Maiocco[9] et al investigated Au/Al interactions in *unmolded* parts for Al films containing Cu and Si additives that are more characteristic of IC metallization processes. Manual 4-point measurements were made by placing current and voltage probes on a single Au ball, a current probe on a second ball and a voltage probe on the Al sheet to which both balls are bonded. This is a difficult and tedious process, but it is the only way of restricting the measurement to the Au to Al interface. Measurements were taken on samples exposed to 77, 107, 150, 187, 223, and 277 °C for up to 3000 hours in argon. Maiocco's data up to ΔR =8 mΩ generally fit the $\Delta R = c(t)^n$ parabolic relation, where n=0.40±0.02. Using the expanded model $\Delta R = c \cdot \exp(-Ea/kT) \cdot (t)^n$, the

activation energy was 0.40±0.01 eV/atom within a 95% confidence interval. Interestingly, there was *no* effect due to Si and Cu additives.

C. Intermetallic Resistivities

Maiocco points out that the most Al rich intermetallics grow during annealing and once the Al is depleted under the Au bond, further intermetallic growth is limited by dissolution of the intermetallic phases of higher Al content and diffusion of Al to the bond from the surrounding film. A single parabolic rate law cannot be expected to accurately describe such a complex process. In addition, the diffusion of Al from the surrounding bond pad creates a depletion region around the bond, which also affects the resistance measurement. And, just as importantly, each of the intermetallic phases vary greatly in resistivity, so that even if the composite intermetallic growth rate were parabolic, the corresponding changes in resistance of the bond would not vary proportionally. Typical resistivities of Au/Al intermetallics are contained in Table 1A.I.

Table 1A.I. Resistivities of Au/Al intermetallics[10].

	Al	$AuAl_2$	AuAl	Au_2Al	Au_5Al_2	Au_4Al	Au
Resistivity ($\mu\Omega$·cm)	3.2	7.9	12.4	13.1	25.5	37.5	2.3

The foregoing discussion was not intended to suggest that all the experimental work regarding Au/Al interactions have been done and the best combinations of molding compound, pad metallization, die attach, and assembly process are common knowledge. It was to provide a background on the kinds of experimental approaches that have been taken in the past to further understanding of the Au/Al bond degradation process. Some feel that the issue is less relevant today due to improvements in molding compounds and assembly process control. But this is a problem that occasionally returns to be rediscovered in new generations of packaging technologies.

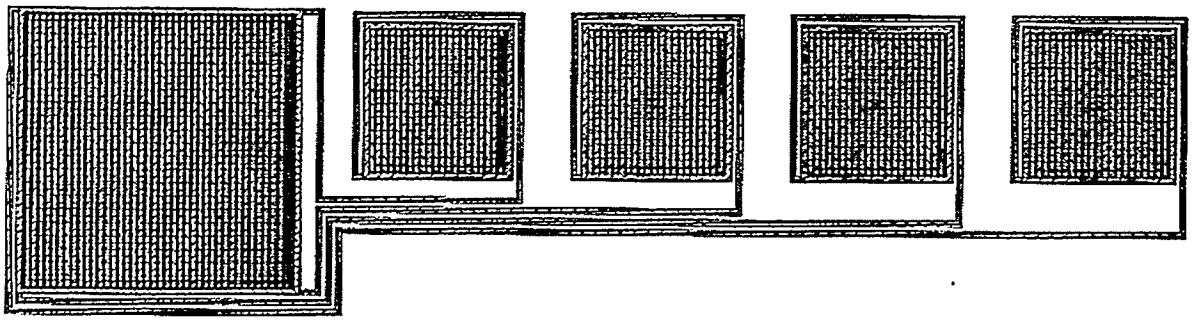

Figure 1A.3. ATC3.0 bond pad placement test structure.

III. Bond Resistance Study

Previous work that correlated changes in bond resistance to bond degradation were hampered for lack of a means for obtaining accurate 4-point measurement data in statistically significant quantities. A technique for measuring interfacial bond resistance using a sheet resistance structure was evaluated using the bond placement detector on the ATC3.0 test chip. (See Figure 1A.3) A current is passed between adjacent corners of a bond pad (large pad in Figure 1A.3), and voltage is measured between adjacent pads on the opposite side. The expected path for current before and after ball bonding, and after the presumed depletion of Al in the pad during thermal aging, is shown in Figure 1A.4. The voltage gradient measured in Figure 1A.4(a) can be used to calculate the sheet resistance in ohms/square using a simple analytical relationship. Once the bond has been placed, as in Figure 1A.4(b), the current path becomes quite complex as it flows through regions of pure Al and Au, mixed intermetallics and voids. Initially, the net effect is a decrease in measured resistance due to the parallel contribution of the low resistance Au ball. As the diffusion process continues, resistance increases until an equilibrium condition is reached at which all the Al within the general vicinity of the Au ball is fully depleted, as in Figure 1A.4(c).

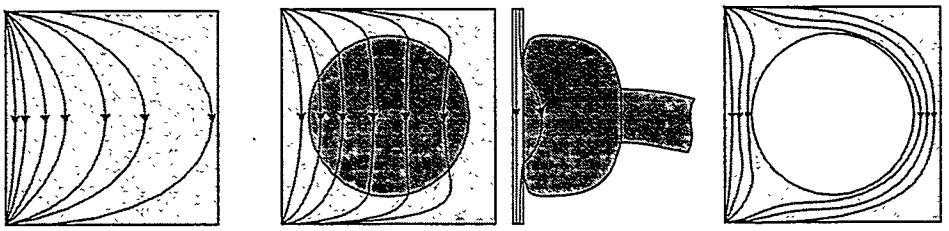

Figure 1A.4. Current flow through bond pad placement structure before (a) and after (b) Au thermosonic bonding, and (c) after complete voiding of Al in pad.

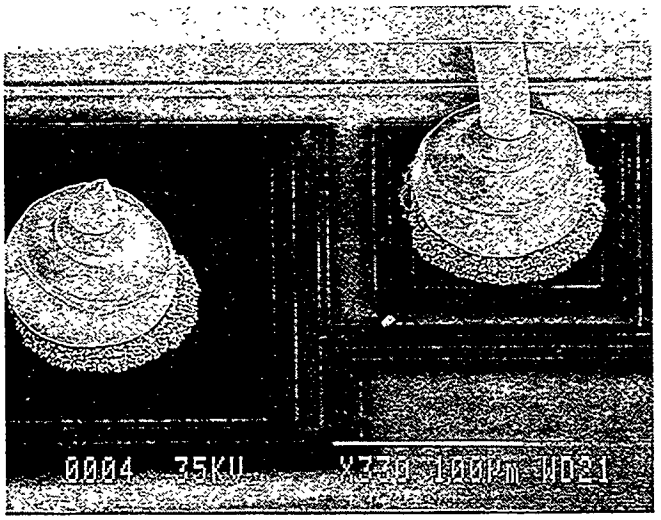

Figure 1A.5. ATC3.0 bond pad position test structure showing intermetallic growth after 30 hours at 300 °C.

In order to test the efficacy of this measurement strategy, a rapid thermal aging experiment was performed using ATC3.0 die bonded out in 40 lead CHP (ceramic hermetic packages). Included were a number of unbonded controls. The formation of Au/Al intermetallic phases was rapid and dramatic, as seen in Figure 1A.5. The corresponding resistance changes are plotted in Figure 1A.6 as the average of eight bonded pads along with two control pads. Prior to bonding, the measurements are proportional to the sheet resistance of the pad. The ATC3.0 bond pads contain both metal 1 and metal 2, with nominal sheet resistances of 30 mΩ and 60 mΩ, respectively, or ~20 mΩ in combination.

Once the bond is placed, the measured resistance decreases due to the parallel conduction path through the Au bond. The parallel conduction path is gradually disrupted at increasing times by voiding in the Au-Al interface. Au diffuses into the Al pad metallization forming disjoint intermetallic regions that tend to be disconnected from the main body of the Al pad. Once the bond becomes fully disconnected, the resistance measurement resembles one of a conducting sheet with a hole in the center. As a result, the ATC3.0 bond pad position structure, with its oversized measurement pad, is less sensitive than a ball bond sized pad. The experimental results confirmed the utility of a sheet resistance test structure for studying bond degradation during high temperature storage.

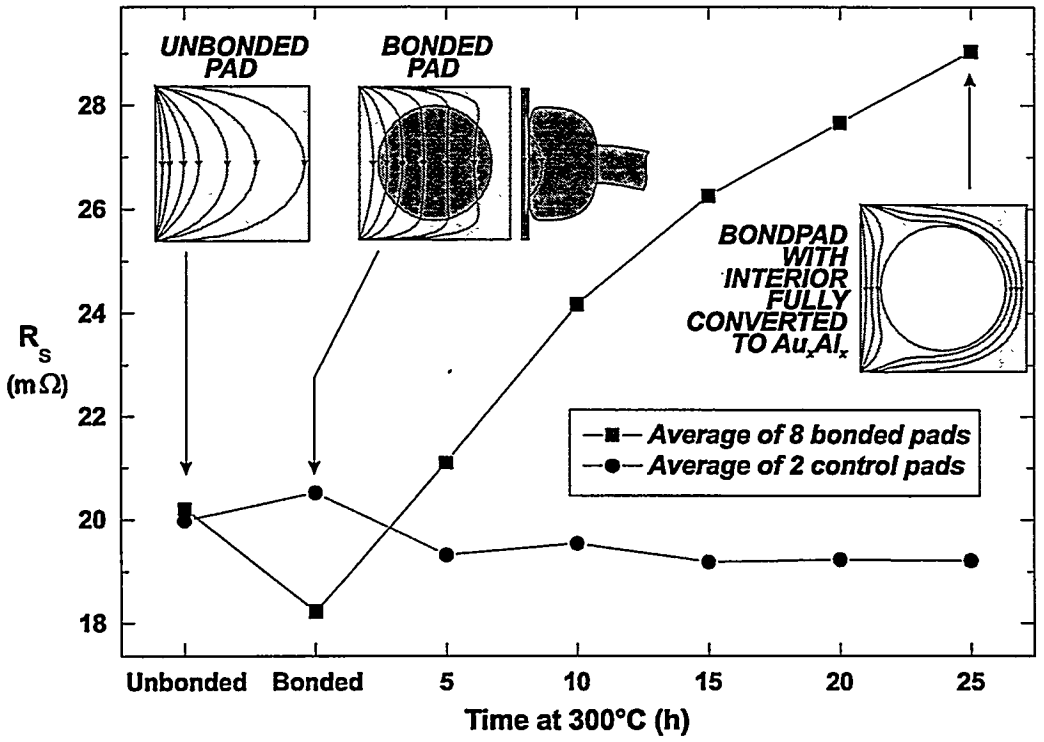

Figure 1A.6. Change in bond pad position pad sheet resistance as a function of bonding and time at high temperature.

IV. Test Chip Design

ATC2.6 is a third generation Assembly Test Chip intended for studying the corrosion resistance and thermal properties of non-hermetic packaging. This chip essentially mimicks the triple track features of the ATC2.5, but includes a number of bond pad resistance test structures, similar to the bond pad position structure discussed above, for studying bond degradation. The chip is ~0.250" on a side and bondpads are 120 μm on 200 μm pitch. The following paragraphs describe each structure in greater detail.

A. Triple track structures

There are 8 sets of interdigitated thin film 2 μm Al line triple tracks which are used to study the ability of chip packaging and passivation to protect the metallization against electrochemical corrosion. Four of the triple tracks are protected with standard 5KÅ SiN passivation, four contain cut-outs through the passivation exposing the biased tracks to overmolding or encapsulant. A schematic diagram of one of the 8 ATC2.6 track structures is shown in Figure 1A.7.

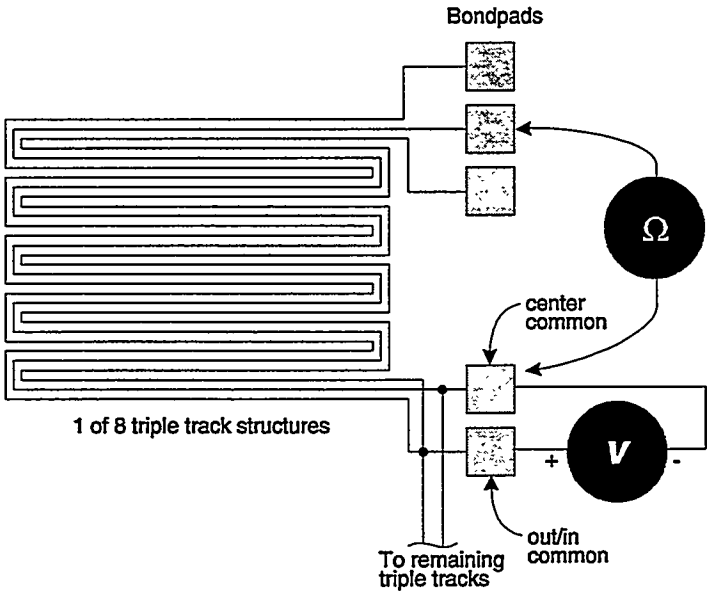

Figure 1A.7. Schematic diagram of triple track structure consisting of three interdigitated tracks, with the outer tracks typically biased anodically with respect to the center (cathodic) track. Track corrosion is detected by measurement of the track resistances, normally with the bias removed.

For corrosion experiments, 24 bond outs are required for one side of the 8 triple tracks and 2 bond outs for the commons, making a total of 26 input/output connections. As shown in Figure 1A.7, only two connections to the chip are required for biasing all of the triple tracks during accelerated testing. Off-line resistance testing is normally done with the bias removed by sequentially measuring between the three triple track bondpads and the appropriate common bondpad. Nominal track resistance is ~3500 Ω.

B. Polysilicon heaters

There are two heater structures consisting of 2 μm line and space polysilicon conductors oriented perpendicular to the overlying triple tracks. Each heater is connected at either end to a bus with three bond terminals to facilitate four terminal high accuracy power measurements. The heaters have a nominal resistance R_h~ 50 Ω and a temperature coefficient $(\Delta R_h/R_h)/\Delta T$ ~ 0.065 %/°C. Typically, 50 W per heater can be dissipated at 50 V and 1 A.

C. Diode thermometers

There are five p^+n diode thermometers, one in the die center and the other four under perimeter bondpads. The center diode has a 4-point measurement connection to minimize series resistance. The bondpad diodes have adjacent substrate pads to facilitate 2-point measurement. Temperature coefficients should be in the range of 2 mV/C°.

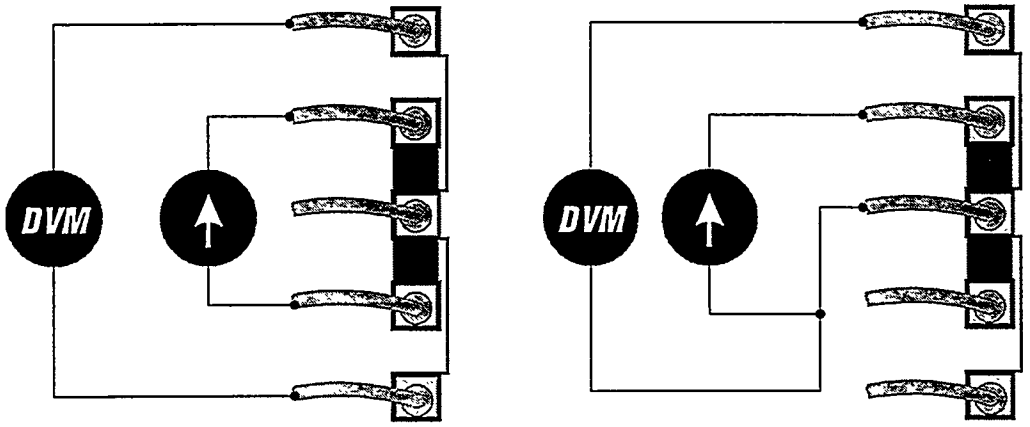

Figure 1A.8. One of 22 bondpad resistance structures showing typical measurement connection for 4-point interfacial resistance of the center bondwire/bondpad (left) and 3-point measurement of the center bondwire continuity.

D. Bondpad resistance structures

Figure 1A.8 shows a close-up of 1 of 22 bondpad resistance structures in two different measurement configurations. The first is a 4-point measurement of the series-parallel combination of bondpad sheet resistance, Au ball bond resistance, and ball to pad interfacial resistance of the center pad. The second configuration shows how to do a 3-point measurement of the center bond wire/bond pad. The 3-point measurement includes the additional series resistance of the bond wire and is subject to measurement "noise" caused by socket contact resistance, but is more effective in measuring the electrical degradation seen by a circuit. The 4-point measurement is inherently more stable and accurate, but does not directly indicate when the bond is electrically open. The intermetallic growth process eventually ceases when no more Al in the bond pad can diffuse into the bond interface, leaving a conducting ring (Al pad with a hole in the center). The measurement data increase at some rate then become asymptotic to a resistance determined by the geometry of the remaining conductive material in the pad. Both measurements

can be made on the same pad during accelerated testing. This structure differs from the ATC3.0 bond pad position structure in creating a uniform sheet of current across the pad rather than producing a non-uniform current density that peaks at the corner source and sink. In addition, the wide current bus allows the use of higher currents, and thus, more accurate measurement of milliohm resistances.

V. High Temperature Storage Experiments

Two high temperature storage experiments were completed, the first at 175°C and the second at 200°C. ATC2.6 die were encapsulated in 160 lead plastic quad flat packs (PQFP) by IPAC, a domestic plastic packaging foundry, using three molding compounds: Dexter 6300HJ baseline, and two experimental formulations, D2 and D3. Both are the same biphenyl resin with the second containing AlN in place of conventional silica filler spheres.

Table 1A.II. Experimental variables for high temperature storage test using ATC2.6 bondpad interfacial resistance test structures.

Molding Compound	Test Temperature	No. ATC2.6s	No. Test Structures
6300HJ	175°C	15	330
6300HJ	200°C	22	572
D2	200°C	14	308
D3	200°C	25	550
CERDIP	200°C	25	200

Table 1A.III. FA removal schedule for ATC2.6 parts during 200°C high temperature storage test. Each "x" represents one part. Times also represent off-line measurement intervals.

Time (h)	CERDIP	6300	D2	D3	Time (h)	CERDIP	6300	D2	D3
24					552	x		x	x
48	x		x	x	600	x	x	x	x
72					648	x		x	x
96	x	x	x	x	696	x	x	x	x
120					744	x		x	x
144	x		x	x	792	x	x	x	x
168					840	x		x	x
216	x	x	x	x	888	x	x	x	x
264	x		x	x	936	x		x	x
312	x	x	x	x	984	x	x	x	x
360	x		x	x	1032	x	x	x	x
408	x	x	x	x	1080	x	x	x	x
456	x		x	x	1128	x	x	x	x
504	x	x	x	x					

Table 1A.II contains the experimental variables. Included in the experiment were a number of control parts packaged in 40 lead CHP. In order to correlate bond resistance changes with visual and mechanical degradation caused by intermetallic growth and void formation, a schedule for systematic removals for failure analysis (FA) was developed. The schedule for the 200°C experiment is contained in Table 1A.III. FA consisted of ball shear and pull measurements after decapsulation with hot fuming anhydrous nitric acid.

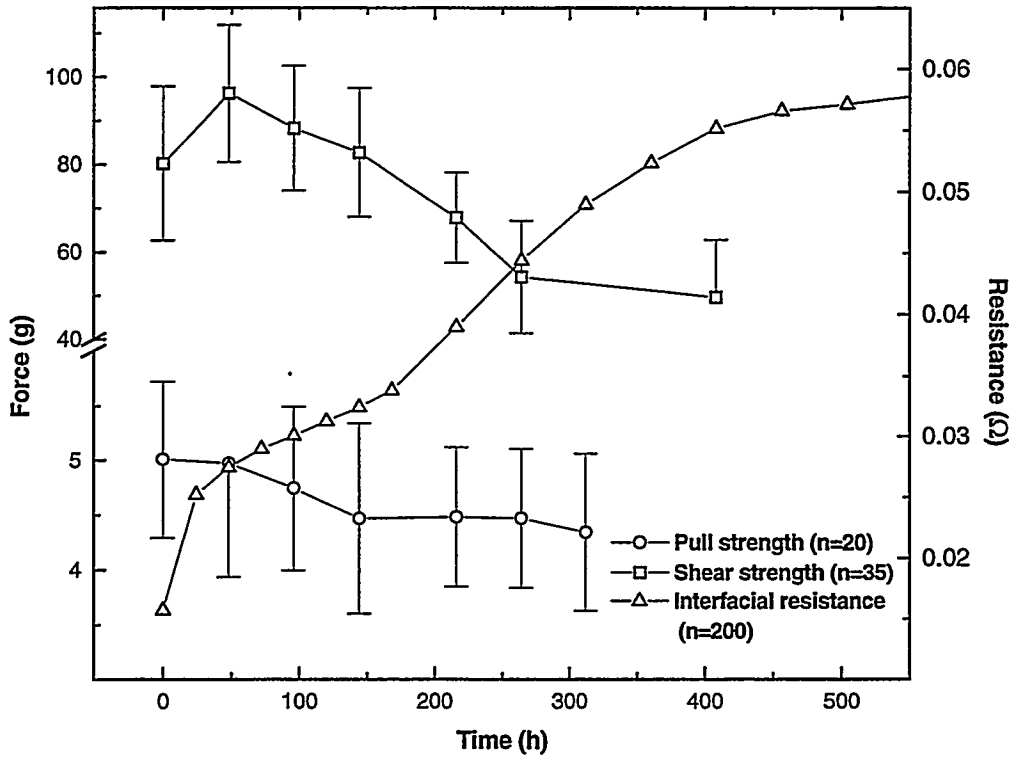

Figure 1A.9. Plot of ATC2.6 average interfacial bond resistance (triangle, right ordinate) as a function of time at 200°C of 200 test structures assembled in 40 lead CERDIP control packages. First 500 h of 1152 h experiment are shown. Overlaid are average bond shear strength (square) and pull strength (circle) data in grams on left ordinate vs. time. Error bars represent one sigma standard deviation.

A. Experimental data

Figure 1A.9 contains a plot of resistance vs. time of ATC2.6 bond resistance structures in the CERDIP control group during high temperature storage testing at 200°C. These data, and all that follows, are from 4-point interfacial resistance measurements using the procedure described in Figure 1A.8. The 3-point measurement data contained too much error due to socket contact problems to be useful. Bond pull and shear strength measurements were made during the course of the experiment and the CERDIP control data are overlaid for comparison in Figure 1A9. At t=24 h the change in resistance averaged over 200 structures was 60%. The temporary increase in

shear strength at the first bond strength measurement interval is not unusual, and is associated with the onset of intermetallic growth. By t=264 h, resistance increased by 75% while shear strength decreased by 30%. In terms of mechanical strength, these bonds were a long time from failing at the last bond strength measurement. However, it is apparent that the interfacial resistance structure is sensitive to both the onset of intermetallic growth where the bond is actually increasing in strength, and to later stages of growth that weaken the bond through voiding.

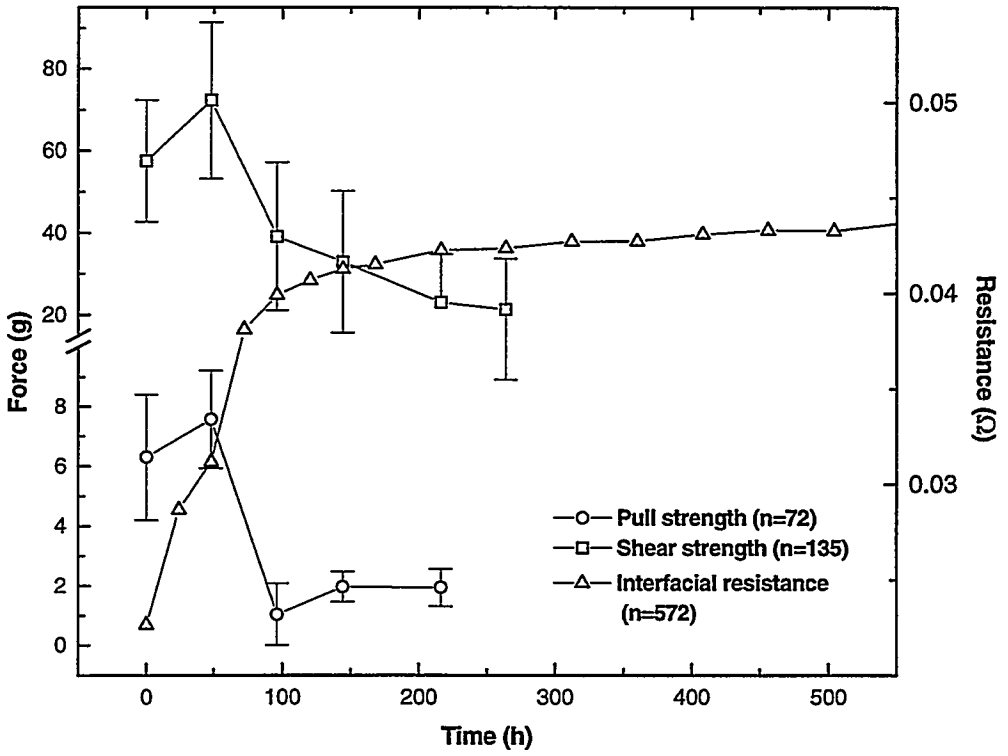

Figure 1A.10. Plot of ATC2.6 average interfacial bond resistance (triangle, right ordinate) as a function of time at 200°C of 572 test structures assembled in 160 lead PQFP packages using 6300HJ epoxy novolac baseline molding compound. First 500 h of 1152 h experiment are shown. Overlaid are average bond shear strength (square) and pull strength (circle) data in grams on left ordinate vs. time. Error bars represent one sigma standard deviation.

Figure 1A.10 contains experimental data for the 6300HJ epoxy novolac baseline molding compound. This molding compound is representative of materials commonly used by high volume IC manufacturers today. Two things should be mentioned in comparing these data against the CERDIP control data in Figure 1A.9. First, the CERDIP control parts have an average starting resistance (~0.016 Ω) two-thirds that of the molded PEM parts (~0.022 Ω). The latter group includes both the baseline and the special D2/D3 formulations plotted in subsequent figures. This is probably due to a reduced time-temperature product seen by the hermetic parts during assembly compared to the PEMs, which typically go though a 1-2 h post-mold cure at

150–165°C. Second, the total change in resistance of the CERDIP control parts is significantly larger than for the molded parts. It is less obvious why this is so. Perhaps compressive force exerted by the epoxy matrix serves to hold the bond together as it degrades, with the net effect of slightly reducing the interfacial resistance.

The change in interfacial resistance of the baseline parts increased by 25% at t=24 h, averaged over 572 test structures, while the bond pull and shear strength initially increased similar to the CERDIP case. The average resistance increased by 75% at t=96 h (compared to t=264 h for 75% increase in control parts) while average bond shear and pull strengths decreased by 30% and 84%, respectively. Bond degradation in terms of electrical and mechanical strength of the baseline parts is striking compared to the CERDIP control parts.

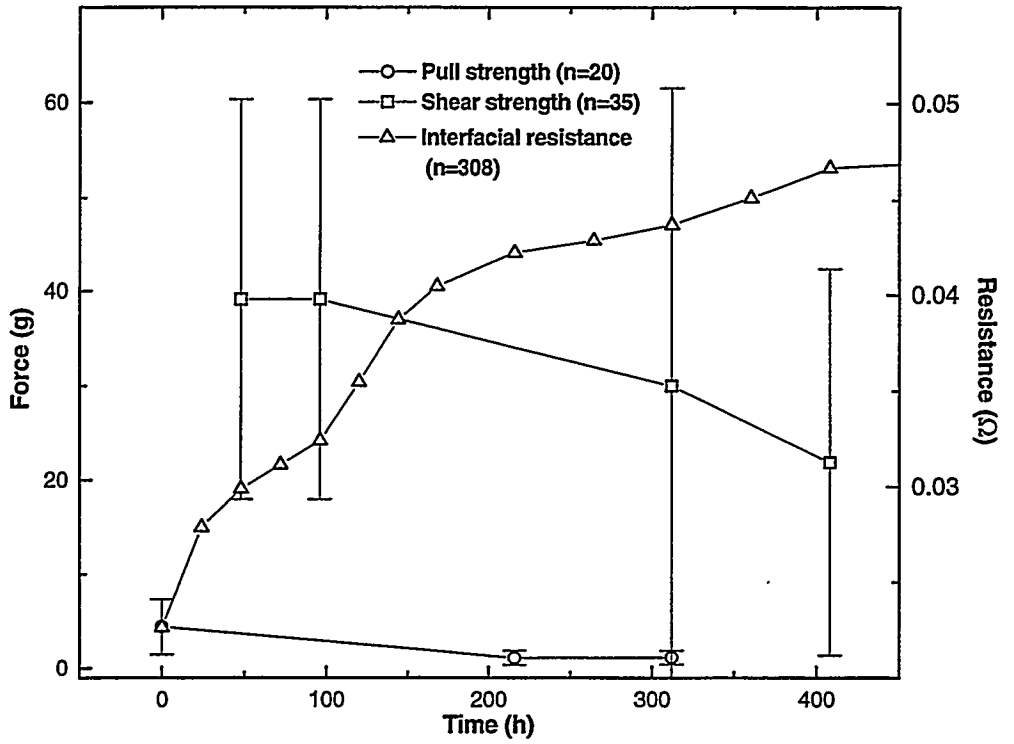

Figure 1A.11. Plot of ATC2.6 average interfacial bond resistance (triangle, right ordinate) as a function of time at 200°C of n test structures assembled in 160 lead PQFP packages using D2 biphenyl resin molding compound. First 500 h of 1152 h experiment are shown. Overlaid are average bond shear strength (square) and pull strength (circle) data in grams on left ordinate vs. time. Error bars represent one sigma standard deviation.

The biphenyl resin D2 and D3 groups are different from the baseline in a number of ways. The biphenyl resin has a lower equilibrium moisture concentration (solubility) than epoxy novolac molding compounds. It is possible that this would have an indirect effect on the rate of bond degradation due to lower moisture evolution during high temperature testing. These specific

formulations also contain proprietary ionic getters that are designed to lock up bromine fire retardant additives and reduce bromine-related bond degradation at elevated temperature. The D3 formulation differs from D2 in containing AlN fillers for enhanced heat transfer rather than silica, which is used almost universally to reduce molding compound CTE.

Experimental data for the D2 and D3 groups are plotted in Figure 1A.11 and 1A.12, respectively. At t=96 h for the D3 parts, bond shear and pull strengths decreased by only 5% and 7%, respectively, with a corresponding 40% increase in interfacial resistance. Both bond strength and resistance data suggest that bond degradation is retarded using biphenyl resin containing ionic getters. Figures 1A.9-1A.12 show a clear correlation between the rate of bond strength degradation and rate of increase in interfacial resistance. This correlation would be extremely useful in evaluating molding compounds using non-destructive resistance monitoring, rather than the current technique of decapsulation and bond shear/pull measurements.

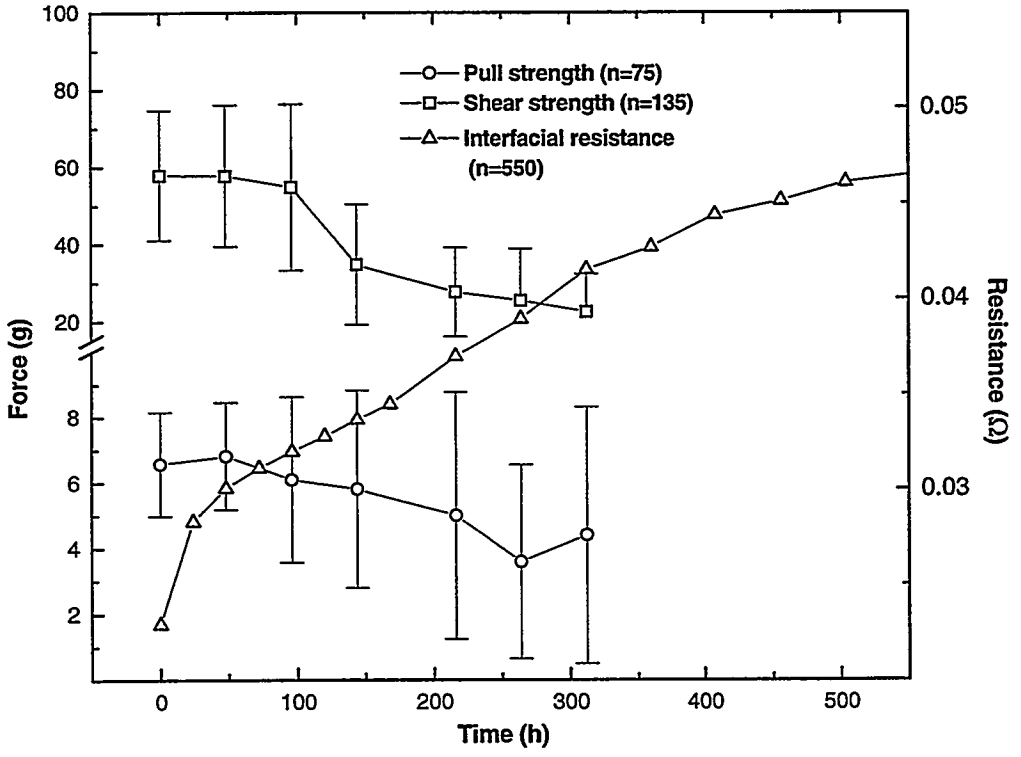

Figure 1A.12. Plot of ATC2.6 average interfacial bond resistance (triangle, right ordinate) as a function of time at 200°C of n test structures assembled in 160 lead PQFP packages using D3 biphenyl resin molding compound. First 500 h of 1152 h experiment are shown. Overlaid are average bond shear strength (square) and pull strength (circle) data in grams on left ordinate vs. time. Error bars represent one sigma standard deviation.

B. Bond shear, bond pull technique

There are two schools of thought regarding measurement of mechanical bond degradation. One supports the use of pull testing, the other shear testing. Pull testing is criticized because a good bond will separate in the wire, it being the weakest point. As the bond degrades, it eventually separates at the interface, leaving intermetallic nodules, such as in Figure 1A.13, and, after longer times, a characteristic "mud flat" of intermetallic on the Al pad. Figure 1A.14 shows a typical mud flat on a ATC2.6 bond pad after 336 h at 175°C. Sometimes the adhesion of the intermetallic to the Au ball is greater than to the oxide dielectric layer beneath the Al pad. We see this condition in Figures 1A.15 and 1A.16. At still longer times at elevated temperature, we have observed damage extend through the oxide dielectric layers to the Si substrate after wire pull strength measurements, as shown in Figures 1A.17 and 1A.18. It is possible that crack initiation sites were formed in the Si during autobonding at the packaging assembly house, however no failure analysis on non-aged parts has been done to confirm this, and the packaging house in question seems convinced that it couldn't happen in their highly controlled process. In any event, bond *pull* testing may be questionable as a process monitoring procedure, as the real strength of the interfacial bond is not measured, but appears to be effective in monitoring changes in bond strength during the progression of an accelerated test. Measurements record the weakest link in bonds during increasing test times, initially the wire and later the interface, forming a useful strength vs. time distribution picture of bond degradation.

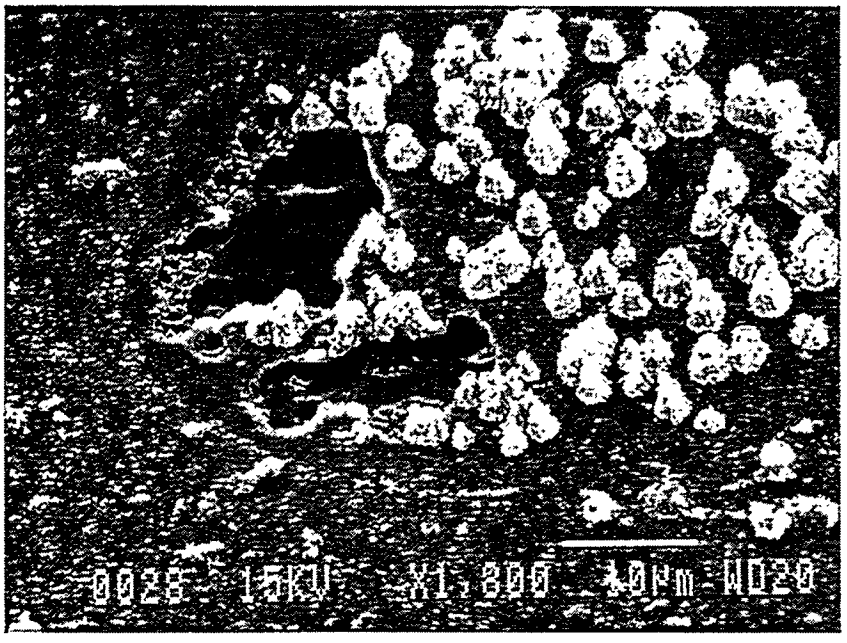

Figure 1A.13. SEM of ATC2.6 SCT213 bond pad showing intermetallic nodules stuck to pad and removal of oxide layer in places after wire pull.

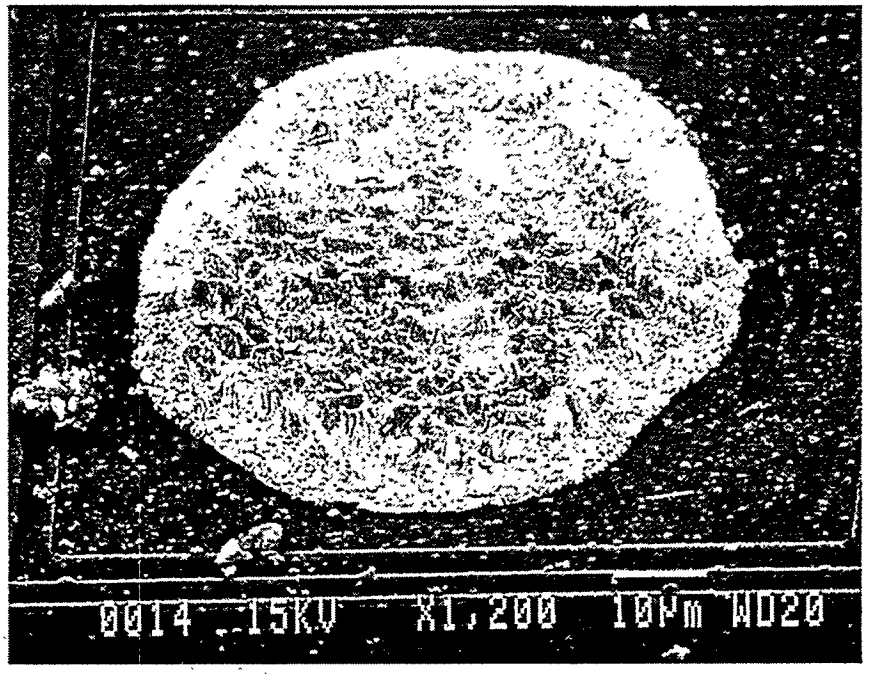

Figure 1A.14. SEM of ATC2.6 SCT172 bond pad after 336 h at 175°C showing "mud flat" Au/Al intermetallic after wire pulled.

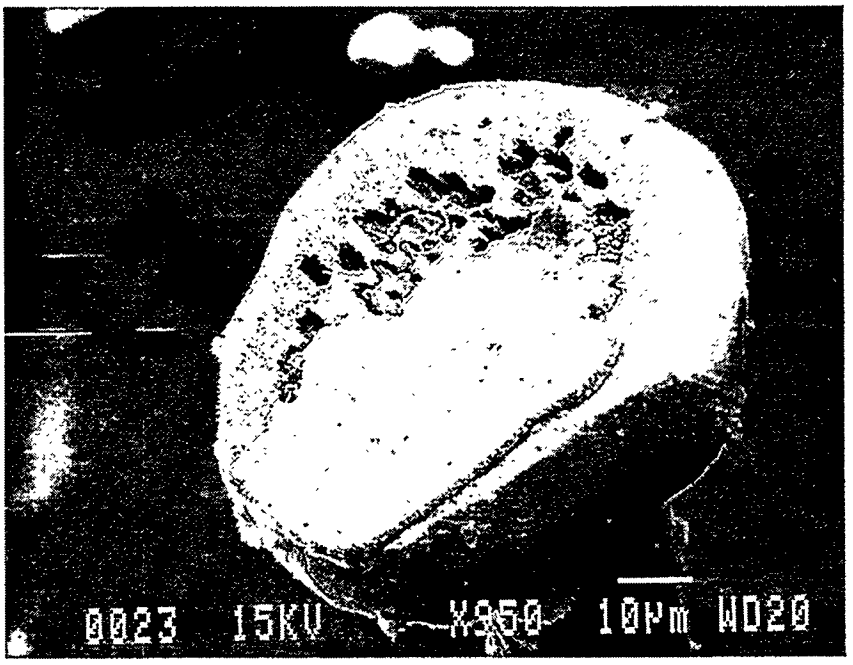

Figure 1A.15. SEM of SCT172 ball bond after 336 h at 175°C showing Au voids formed during intermetallic growth.

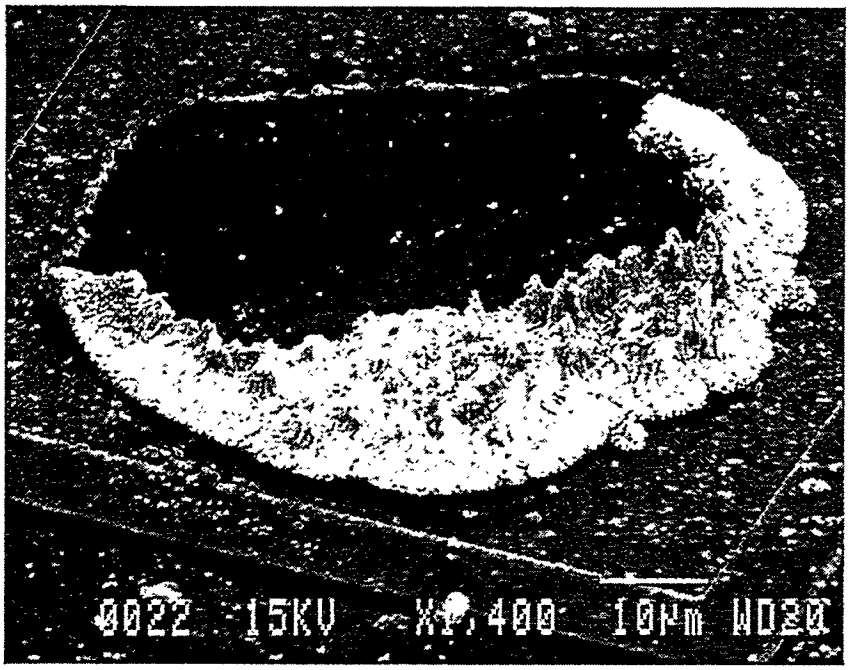

Figure 1A.16. SEM of bond pad corresponding to ball bond in Figure 1A.15. Weakest point in bond has become the intermetallic-to-oxide interface at this point in accelerated testing.

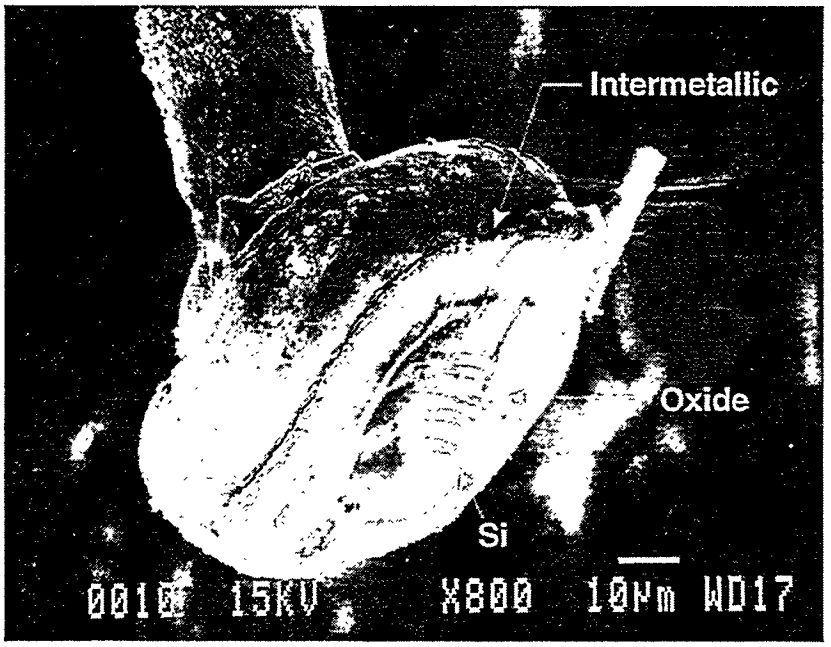

Figure 1A.17. SEM of ATC2.6 SCT171 ball bond after 696 h at 175°C showing cleaved Si adhering to bond after wire pull.

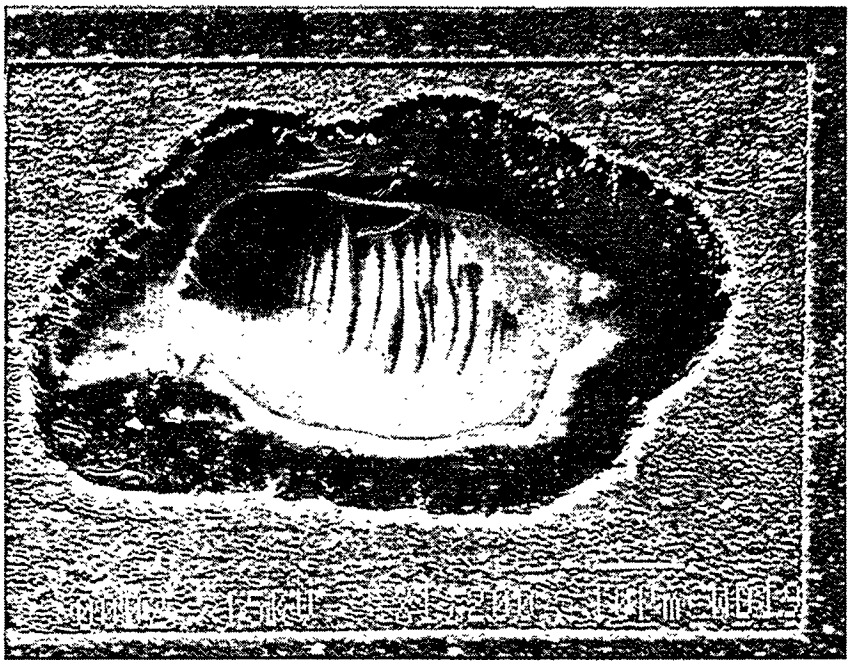

Figure 1A.18. SEM of bond pad corresponding to ball bond in Figure 1A.17.

There are a number of concerns about the validity of the bond *shear* data. The bond shear process on this particular packaged part was difficult due to the proximity of bonds to the decapsulated epoxy side wall and to each other. The ATC2.6 contains a staggered double row of pads on two sides that further constrains access to bonds. In addition, the planarity of the die surface in respect to the tool is critical in ensuring that the shear proceeds through the Au ball at a constant height from the Al bond pad. Many bond shears showed signs of tool contact with Si indicative of a non-parallel shear and consequent measurement error. This may be partly due to the fact that the lead frame can flex during molding so that it is no longer parallel to the bottom surface of the molded package after cure. And lastly, the bond shear tool was recalibrated toward the end of the experiment causing an offset in some of the measurements. (These data points are not shown in Figures 1A.9-1A.12.) Bond shear measurements are grouped into one of four categories: crater, pad lift, ball lift, and ball shear. The last is considered the only legitimate shear, however it becomes an increasingly unlikely result during the course of accelerated testing due to progressive weakening of the interface. The shear data in Figures 1A.9-1A.12 have not been censored for ball-only shear.

C. Effects of humidity acceleration

In addition to the two dry storage conditions of 175 and 200°C, a group of ATC2.6 baseline parts were subjected to HAST at 140°C and 85% RH. Changes in resistance of the bond pad interfacial resistance structures are shown in Figure 1A.19. The 200°C data are the same as in Figure 1A.10, but truncated at ~100 h. Straight (dashed) lines are used to approximate a linear fit to the 175 and 200°C data, although the former is clearly non-linear at early times. There will be more

discussion of this in the next section on calculations of activation energy. The HAST data lie somewhere in between the data for the two dry storage conditions. At very early times the rate of increase of resistance in the 140°C HAST parts is comparable to the 200°C parts. Unfortunately, it was not possible to obtain bond pull and shear data for the HAST parts, but ATC2.5 parts decapsulated in the process of routine failure analysis of triple track failures have shown significant bond degradation. It is not unusual to find wires so weakly attached that the merest touch with a tool dislodges them from the bond pad after relatively short exposure times to HAST conditions.

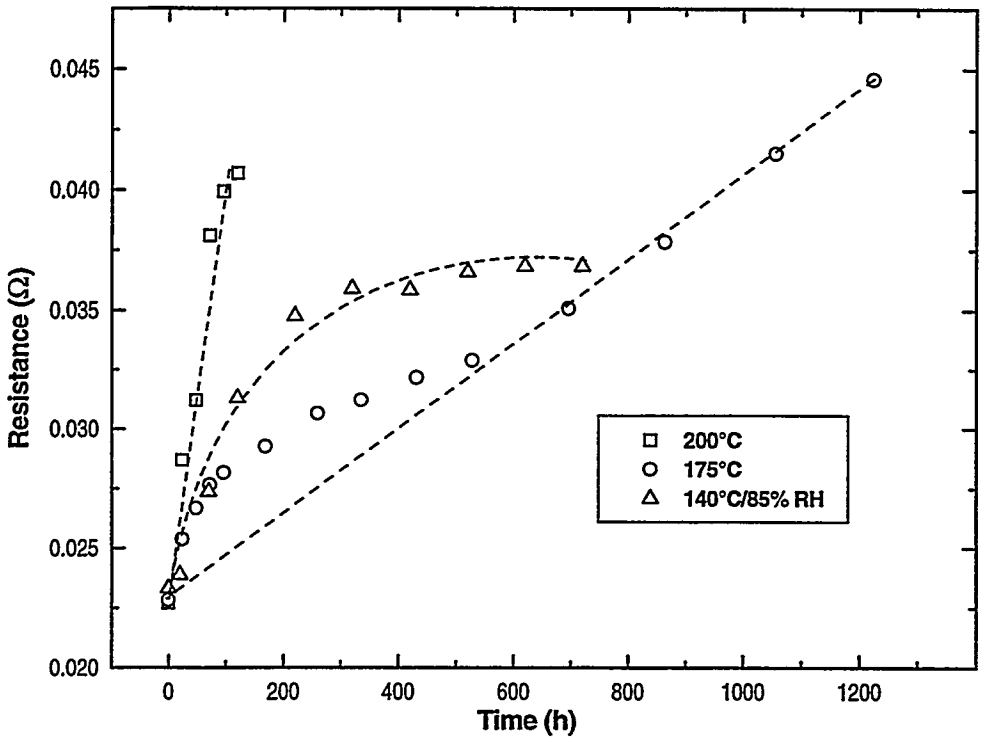

Figure 1A.19. Plot of bond resistance averages as a function of time and accelerated temperature/humidity conditions of ATC2.6 test chips packaged in 160 lead PQFPs using 6300HJ baseline molding compound.

D. Activation energy calculations

As discussed above, Figure 1A.19 contains resistance data from 6300HJ baseline parts exposed to three different temperatures, one that included humidity acceleration. The dashed curves are visual fits to the data and help to illustrate the problem with extracting activation energies for high temperature bond degradation mechanisms. If the two high temperature dry storage curves were linear, as suggested by the dashed lines, the activation energy would be independent of the resistance ratio. In other words, a single activation energy would fully describe the exponential time to fail for any resistance ratio failure criteria using an Arrhenius acceleration model.

Unfortunately, the resistance changes do not proceed in a linear fashion with time, but rather reflect a mix of ongoing diffusion limited processes that are interrelated. The growth rate of one intermetallic phase is affected by the composition of adjoining phases. This causes "bumps" in the resistance vs. time curves as seen in Figures 1A.9-1A.12. Researchers, including Maiocco[9], often plot high temperature testing bond resistance changes vs. the square root of time, looking for a parabolic time dependency similar to that seen in the metallurgical diffusion process itself. If the baseline 175 and 200°C data are replotted in this way, we do see an early parabolic stage at both temperatures. (See Figure 1A.20.) Extracting an activation energy from these data at $\Delta R/R_0$=0.5 and n=½ for the Arrhenius model $\Delta R/R_0 = C\exp[-Ea/kT]t^n$, gives Ea~0.57 eV which happens to be close to Maiocco's 0.4 eV. However, since the fitted lines in Figure 1A.19 are actually *parabolic*, the calculated activation energy will vary with $\Delta R/R_0$. This is also true for Maiocco's data, where an arbitrary value of ΔR=4 mΩ was used as a failure criteria.

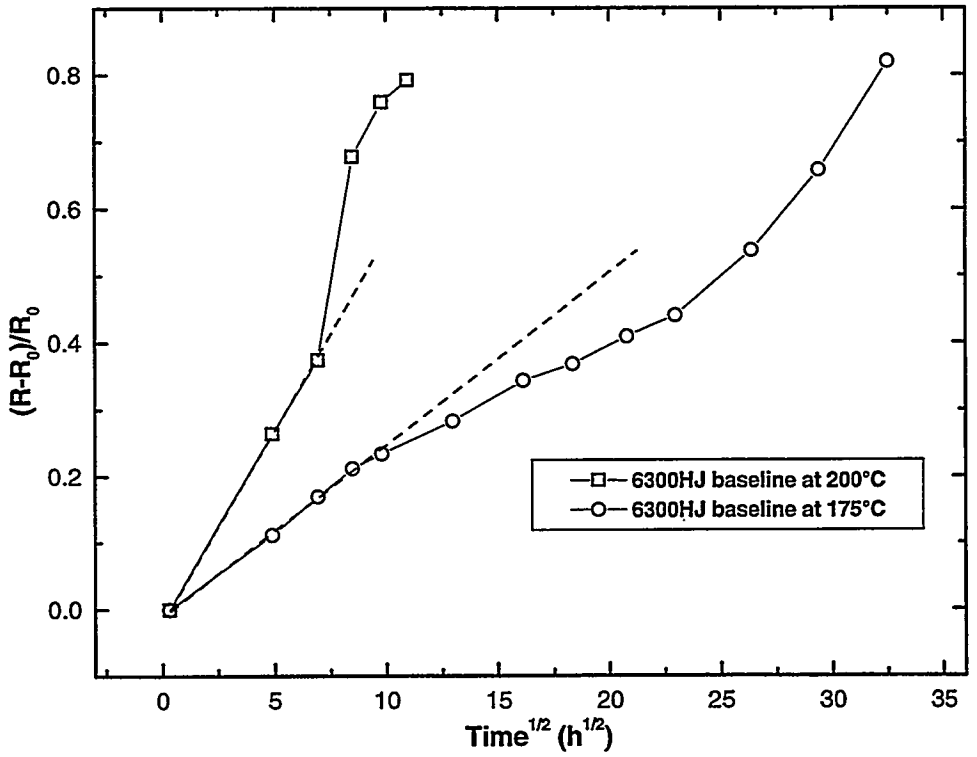

Figure 1A.20. Normalized resistance change as a function of time for baseline molding compound at 175° and 200°C replotted as square root of time to show linear fit (dashed lines) , or parabolic time dependency, at early times.

It would be more meaningful to use a resistance change criteria that correlated to a known and reproducible state of bond degradation observed in bond pull and shear measurements. But even here, an arbitrary bond strength parameter would have to be chosen. Perhaps the best "reference" metric would be a through the bond 3-point resistance measurement, where the effect of bond degradation could be quantified in terms of direct impact on circuit performance. However, the

3-point measurement is exceedingly difficult to do accurately on large numbers of parts in fine lead surface mount packages undergoing accelerated aging due to electrical contact problems.

VI. Conclusions

The primary objective of this task was to investigate a new method for studying the effect of high (accelerated) temperature storage conditions on Au/Al bond degradation in plastic encapsulated microcircuits. Accelerated temperature testing can, in principle, provide data that could be used for life time prediction of Au/Al bonds in PEMs exposed to dormant storage conditions. This is currently done using decapsulation and bond shear/pull testing, where bond degradation is measured in terms of mechanical weakening of the interface. This method provides useful information on the structural integrity of the bond, but is difficult to do routinely or with sufficient samples to provide statistical significance. The ATC2.6 test chip contains bond pad resistance structures that have been shown to provide similar indications of bond degradation far more easily. However, *further study is needed to better understand the correlation between electrical changes and mechanical bond integrity in PEMs.* This is partly due to the innate difficulty in making good bond shear and pull measurements on encapsulated ICs. It would also be helpful to devise a way to measure "through" the bond using a modified 4-point technique, to augment the interfacial resistance technique. This would provide a data point in time where the bond was clearly open electrically.

The data derived from this study are not sufficient to develop a valid empirical acceleration model that could be used for lifetime prediction at use conditions. *A better understanding of the time law and the effects of moderate temperature acceleration are needed.* Data from the literature suggest that the time law of the intermetallic growth process as monitored through changes in bond resistance becomes increasingly parabolic at lower temperatures. There seem to be fewer "bumps" in resistance changes at lower temperatures.

The experimental measurement data show faster bond degradation in baseline parts compared to ceramic control parts exposed to high temperature storage conditions. The combination of moisture and high temperature in HAST further accelerated rate of bond degradation. This is not surprising and is consistent with observations from other researchers. The parts molded using biphenyl resin with ionic getters appear to last longer during high temperature storage testing. Unfortunately, there was not an opportunity to test these parts in HAST to see if the getters also improved performance in high humidity conditions. *These new molding compound formulations hold promise for resolving or ameliorating one of the most vexing reliability issues with PEMs – bond degradation.*

References

[1] G. C. Harman, *Wirebonding in Microelectronics*, ISHM, Reston, VA, 1989.

[2] J. Pecht, M. Pecht, *Long-Term Non-Operating Reliability of Electronic Products*, CRC Press, Boca Raton, 1995.

[3] M. Hansen, *The Constitution of Binary Phase Diagrams*, 2nd Edition, McGraw Hill, New York, NY, 1958.

[4] G. Majni, G. Ottaviani, "AuAl Compound Formation by Thin Film Interactions", *J. Crystal Growth,* vol. 47, pp. 583-588, 1979.

[5] R. E. Thomas, V. Winchell, K. James, and T. Scharr, "Plastic Outgassing Induced Wire Bond Failure," *Proc 27th. IEEE Electronics Components Conference*, Arlington, Virginia, 1977, pp. 182-187.

[6] R. Ritchie and D. M. Andrews, "CF_4/O_2 Plasma Accelerated Aluminum Metallization Corrosion in Plastic Encapsulated ICs in the Presence of Contaminated Die Attach Epoxies," *Proc. 19th Annual IEEE Reliability Physics Symposium*, Orlando, Florida, 1981, pp. 88-92.

[7] S. S. Ahmad, R. C. Blish II, T. J. Corbett, J. L. King and C. G. Shirley, "Effect of bromine in Molding Compounds on Gold-Aluminum Bonds," *IEEE Tran. on Comp., Hybrids, and Manu. Tech.*, CHMT-9, No. 4, Dec. 1986, pp. 379-385.

[8] A. A. Gallo, "Effectors of High Temperature Reliability in Epoxy Encapsulated Devices," *Proc. 43rd IEEE Elec. Comp. & Tech. Conf.*, Orlando, Florida, 1993, pp. 356-366.

[9] L. Maiocco, D. Smyers, P. R. Munroe and I. Baker, "Correlation Between Electrical Resistance and Microstructure in Gold Wirebonds on Aluminum Films," *IEEE Trans. on Comp., Hybrids, and Manu. Tech.*, Vol. 13, No. 3, Sep. 1990, pp. 592-595.

[10] M. Kashiwabara and S. Hattori, "Formation of Al-Au Intermetallic Compounds and Resistance Increase for Ultrasonic Al Wire Bonding," *Rev. Elec. Comm. Lab.,* Vol. 17, 1969, pp. 1001-1013.

Task 2: Temperature/Humidity/Bias Evaluation of BCP Packaging

Accelerated Temperature & Humidity Experiments

I. Introduction

A. Background

A goal of the FY96 work in this area was to evaluate the temperature and humidity performance of some typical plastic packaged IC surface mount parts. In addition, we hoped to be able to carry out accelerated THB experiments at several temperatures and bias voltages in order to determine some approximate acceleration factors. As a result of experimental difficulties, only one test was conducted and the results of that experiment are reported below.

B. Test package

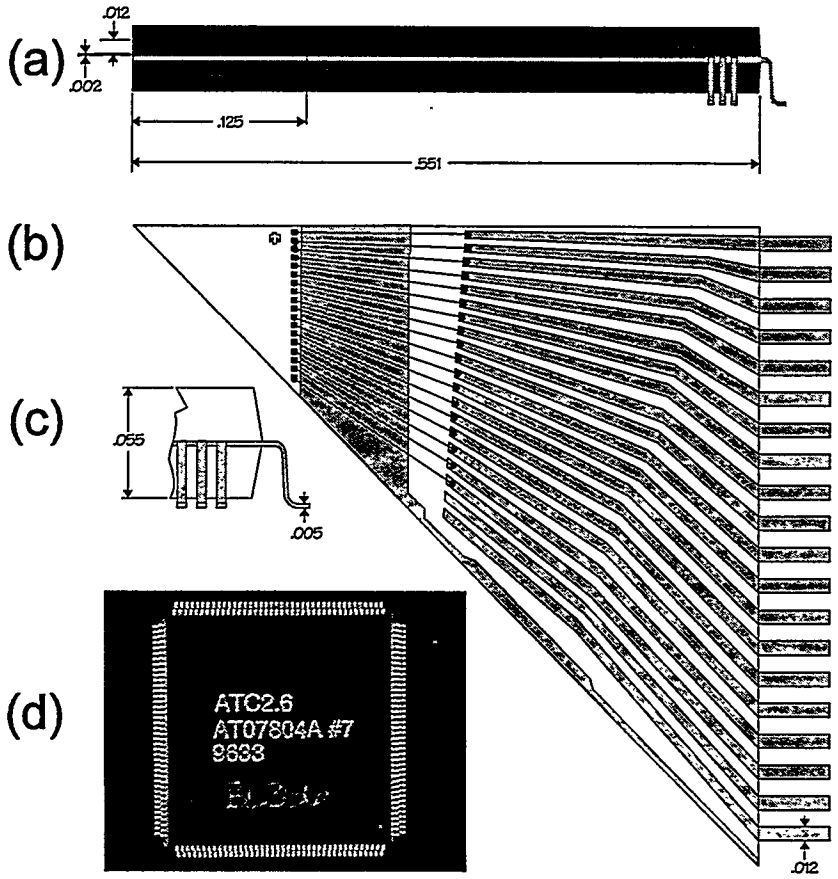

Figure 2.1. Plastic quad flatpack used in the HAST experiment. (a) Side view. (b) 1/8th section showing, die, lead frame and bond wires. (c) Cross-section of package edge showing package leads. (d) Photograph of package top.

Since we were already participating in a DARPA sponsored plastic packaging project, The Low Cost Packaging Technology Reinvestment Program (LCP/TRP)[1], we decided to use the same

baseline test package as we were using in that project. The package was a 160 lead plastic quad flatpack (PQFP) intended for surface mount applications. This package is shown in Figure 2.1.

This is a relatively advanced plastic package which is intended for use in surface mount applications. It is fabricated from materials which are in common use today for high volume plastic package production. The mold compound was Sumitomo's 6300HJ, so the results of the HAST experiment with these parts can be compared directly with our previous results on plastic DIPs molded in a slightly older compound, Sumitomo 6300HD, as reported in Task 4.

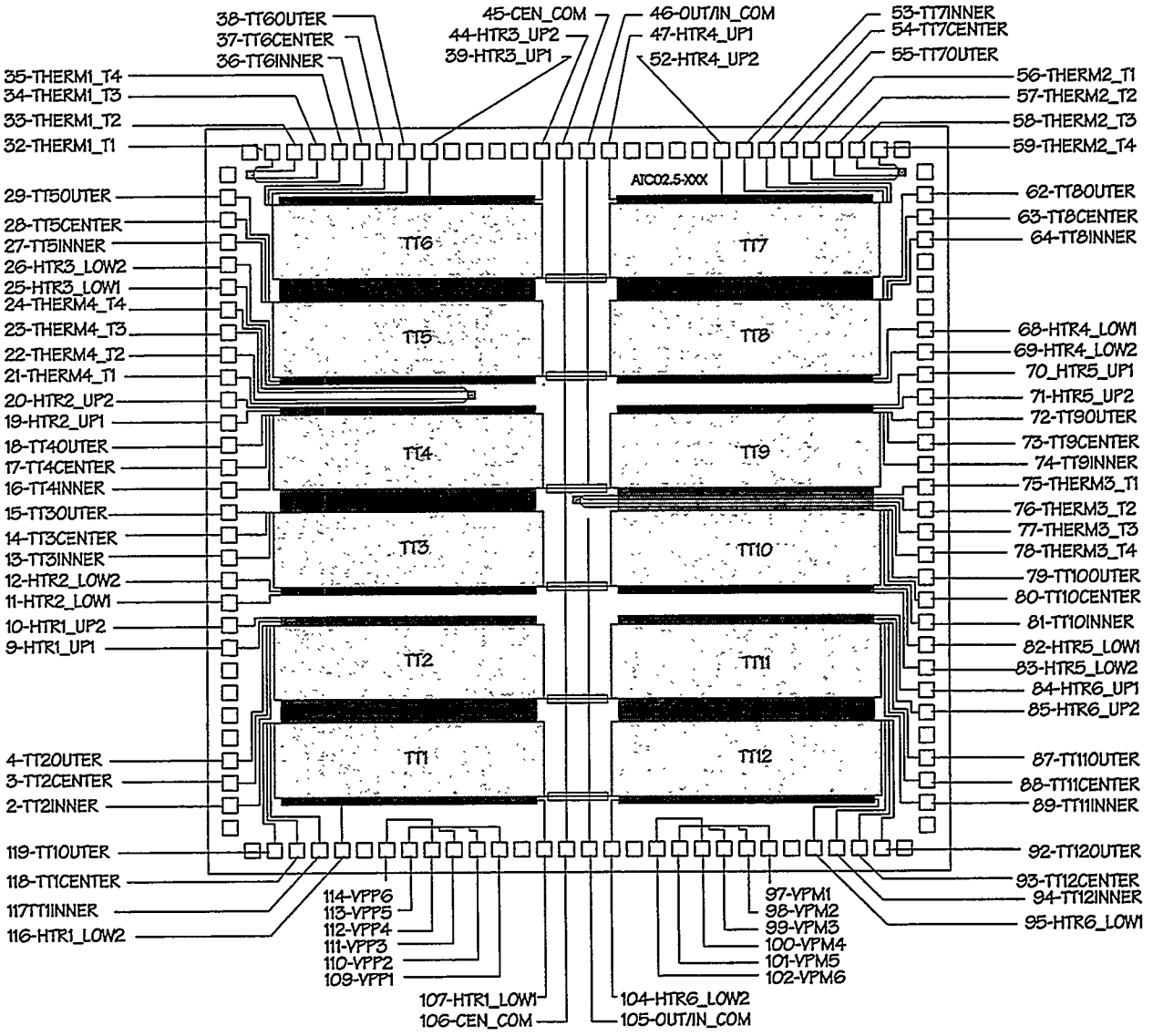

Figure 2.2. ATC2.5 layout showing bondpad designations. Each triple track (TT) has an outer, center, and inner connection. One end of each inner and outer track is connected to out/in common, pads 46 and 105. One end of each center track is connected to center common, pads 45 and 106. Each heater is connected to an upper bus (up) and lower bus (low) with two connections designated 1 and 2.

The IC test chip which was utilized was the ATC02.5, a successor to the ATC01 chips used in the experiments reported in Ref. 8 of Task 4. A diagram of an ATC02.5 chip is shown in Figure 2.2.

The main test features on the die are twelve triple track (TT) corrosion test structures. A diagram of a single triple track is shown in Figure 2.3. These triple tracks are interdigitated 2 μm wide Al metal conductor lines which are biased during a THB test to accelerate corrosion type failures. The usual bias scheme is to bias the center tracks negatively with respect to the inner and outer tracks. Underneath the tracks are parallel 2 μm line and space polysilicon conductor lines which can be used for chip heating in thermal resistance tests. In addition, the polysilicon lines provide realistic topography for the Al conductor lines in the TT structures. The polysilicon and the Al levels are separated by a boron-phosphate-silicate-glass (BPSG) insulator layer about 1 μm thick. The chip passivation is silicon nitride (SiN), approximately 0.7 μm thick.

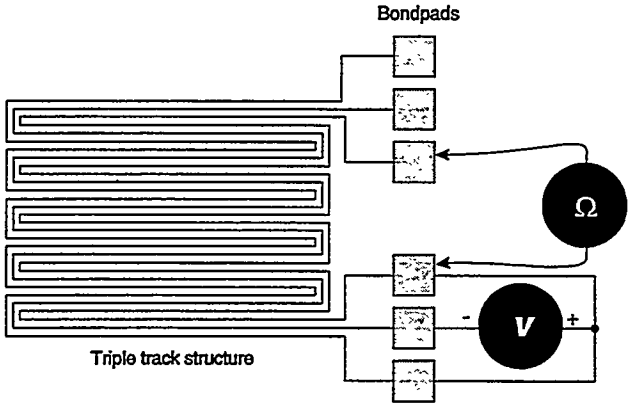

Figure 2.3. Schematic diagram of triple track structure consisting of three interdigitated tracks, with the outer tracks usually biased anodically with respect to the center (cathodic) track. Track corrosion is detected by measurement of the track resistances, normally with the bias removed.

We had originally intended to use the ATC02.6 test chip instead of the ATC02.5. The ATC02.6 triple tracks are similar to those on the 2.5 die, but six of the track structures on one side of the ATC02.6 have cutouts in the chip passivation. The Al triple track conductors which are exposed in the cutout regions are more susceptible to corrosion than are the tracks under the chip passivation. However, in making initial track isolation measurements on packaged parts at a 40 V bias, we found many breakdowns in the ATC02.6 unpassivated tracks. These breakdowns were found to be caused primarily by shorting in unpassivated regions as a result of metal line crushing. This crushing was felt to be a result of particles being deposited onto the die surface during the wafer lapping process and possibly the wafer sawing process also. These particles were not removed prior to assembly and were then driven into the conductors during transfer molding and post-mold cure. A scanning electron microscope (SEM) micrograph of a triple track region with damaged conductors is shown in Figure 2.4.

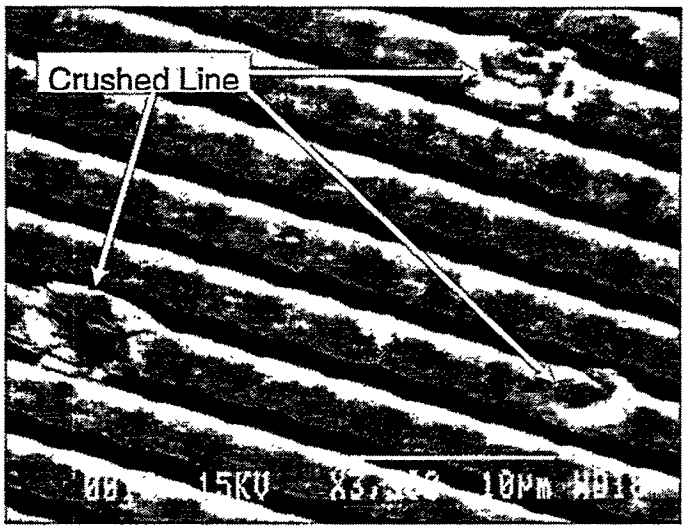

Figure 2.4. SEM micrograph of an ATC02.6 triple track region showing crushed Al metal lines. The plastic above the die was removed by an etching process, as described in Task 11.

II. HAST Experiment

A. General

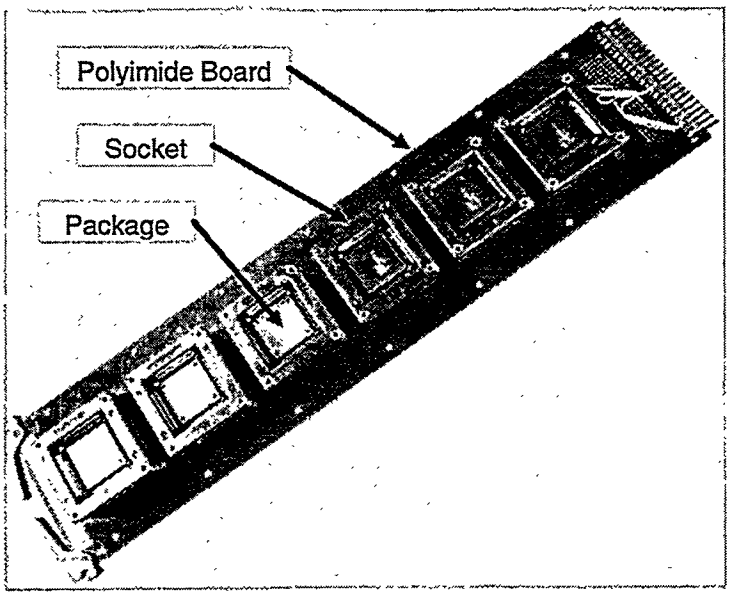

Figure 2.5. Polyimide HAST board with test sockets and ATC02.5 PQFPs mounted in these sockets.

The experiment discussed in this report was conducted at T = 140°C and 85% RH. Parts mounted in sockets on PC boards were biased at either 10 or 40 V, with the center tracks being biased negatively with respect to the outer and inner tracks. In addition, a group of parts with no applied bias, 0 V, was also used. These parts were placed on a tray in the lower region of the

HAST chamber. We assumed that this was equivalent to "zero bias" but no experiment was performed to show that open circuit is equivalent to connecting all triple tracks to the power supply ground. A photograph of a HAST board with test sockets is shown in Figure 2.5. The HAST experiment was interrupted periodically for measurement of the test parts.

B. HAST Procedure

Before any parts were placed in the HAST chambers, the chambers and the test board racks were thoroughly cleaned using isopropyl alcohol. Next the empty test boards were placed into the chambers and the chambers run at 110°C and 95% relative humidity for 10 hours to "sweat" any contaminants from the test boards and to remove any traces of alcohol left in the chambers. Parts were handled using a vacuum wand to load parts in the test sockets. After the parts were loaded on the boards, the boards were placed into the HAST and the 10V and 40V bias power supplies switched on. No significant current was observed to be drawn from either of the supplies and it was verified that power was getting to the three 10V boards and the one 40V board. The chambers were then sealed and the testing started.

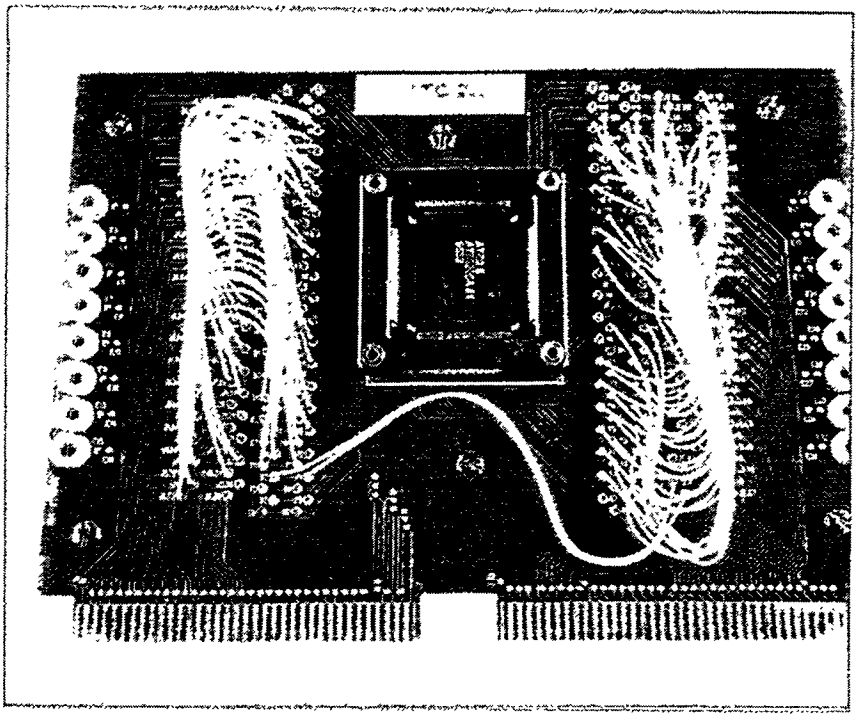

Figure 2.6. Test socket used in the measurement system to obtain electrical data. The edge connector at the bottom of the test board plugs into a socket in the test system.

After each 100 hours of HAST aging time the parts were removed from the chambers for lead cleaning and testing. Lead cleaning was necessary for the quad flat packages to ensure good electrical contact during testing and during subsequent HAST cycles. Initially parts were cleaned using a small brush and a paste made of 600 grit aluminum oxide powder and DI water. After cleaning the parts were rinsed in DI water and dried with nitrogen. After cleaning, the parts were

inspected for bent leads and these straightened. Because this cleaning procedure was not too effective, cleaning is now being performed using low pressure (5 PSI) glass bead blasting. Bead blasting removes oxide from the leads without the use of potentially damaging liquids and with less overall handling. This technique has also cut down on the number of damaged leads substantially. Parts were tested in a spring loaded open top test socket, shown in Figure 2.6, and then returned to the chamber for the next 100 hour cycle. As parts were found to have shorts across the triple tracks, they were removed from the test. As data was accumulated, it was read into a database for easy access and indexing.

C. Part measurements

At a measurement point, the HAST system was shutdown and parts were removed from the board sockets for test. A spring loaded test socket mounted on a PC board, as shown in Figure 2.6, was connected to the test system through an edge connector and cable. Making reliable contact between the test socket pins and the package leads turned out to be the most serious experimental difficulty encountered in the project. In previous programs, we had always used *insertion* packages such as the dual in-line package or DIP. During the HAST exposure, the package leads become coated or corroded, reducing the effectiveness of pressure contacts. With insertion packages, the socket receptacle appears to scrape or scrub the package pins enough to enable a reliable low resistance electrical contact. With the surface mount socket for the 160L PQFP, there was very little scrubbing effect to help maintain electrical contact. As a result, we found that false high resistance or open circuit readings would be produced, especially at longer aging times. In some cases, the package pins would become bent or distorted, preventing a reliable contact in the socket. These causes of high resistance readings are not indicative of real failures because, in an application, the part would be soldered to a PC board.

Various package pin cleaning schemes were tested during the experiment, with none being entirely satisfactory. A commercial pin straightener was used to realign bent pins, with some success. Various abrasive techniqes and cleaners were used on the bottom of the package pins to remove corrosion or coatings. However, since the test socket scrubbed on the pin top surface, these cleaning methods were of limited utility. After the work discussed in this report was completed, we were advised by the National Semiconductor Corp. that a *powder blaster* was useful for pin cleaning in HAST experiments. This tool is similar in concept to a sand blaster but uses very fine abrasive powders instead of sand. Initial tests with a commercial unit indicate that the method has promise for future experiments.

III. Data Analysis

A. Database

A Microsoft Access database was developed for storage and selected retrieval of the data in the HAST experiment. The database stores all of the part measurements in tables, as shown in Figure 2.7.

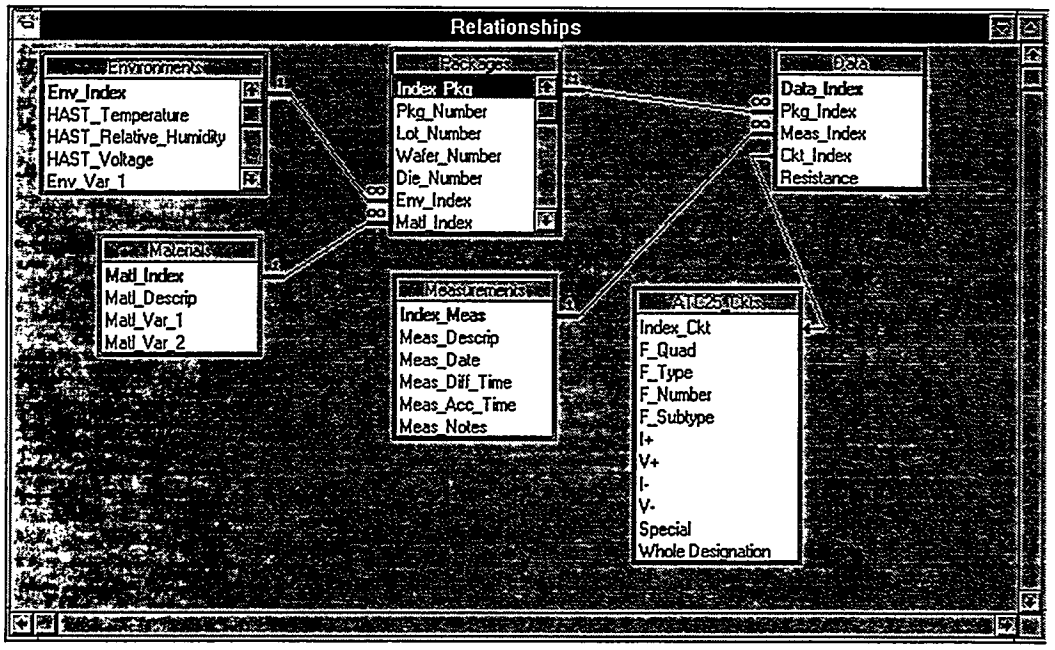

Figure 2.7. Arrangement or schema for tables in the ATC02.5/6 database. The connecting lines indicate relationships between tables in the database.

There are six tables in the database as described below:

1. Environments table

This table stores information about all the environments in an experiment. In our case the bias voltage (HAST_Voltage) was the only environmental variable.

2. Materials table

If there are packages with different materials in an experiment, the information about these materials is stored in this table. In the experiment described in this report, there was only one material combination used in the packages.

3. Packages

This table stores the package numbers for each package in the experiment. Each package is characterized by the die in the package and by the environment and material combination associated with the package.

4. Measurements

This table stores information about the details of package measurements. These details include the date, the differential and accumulated exposure time, and notes about the measurement.

5. ATC25_Ckts

This table contains information about each circuit on the ATC02.5 die. The data collection system writes a circuit identifier on each line of measured data, as given by the "Whole Designation" field in the ATC25_Ckts table. When the data are read into the database from the collection system ASCII output file, the circuit identifier is checked by lookup in the ATC25_Ckts table. If the identifier is valid, the corresponding index is written into the Data table along with the data.

The information in this table is used to query the Data table in order to extract subsets of the data. All of the results reported below were obtained through queries of the triple track data.

6. Data

This table contains a record for each electrical measurement. Each record is characterized by indices for data, package, measurement, and circuit and by a floating point resistance value.

B. Measurements

Electrical measurements were made with a Sandia developed automated test system, designated the Universal Automated Test System or UATS (code name "Albatross").

At its core, the UATS is basically a test instrumentation rack placed under computer control. Its creation stemmed from a need to have a way of rapidly measuring and characterizing simple passive IC structures, such as embedded resistors and capacitors. Formerly, each generation or variation of a die or a package required a considerable investment of time to hand-wire specialized cabling and to code the necessary software for testing. Centered around a relay-matrix and modular code, the UATS cuts down this setup time and presents the user with a simple interface for testing and saving resulting data.

The UATS has several major hardware components, which can be roughly divided into three categories: the computer controller, the test instrumentation, and the relay-matrix. The computer has a GPIB interface which it uses to send commands to and receive data and messages from all of the instruments. The instrumentation includes a currents source, a source-measurement unit, a digital multimeter, a frequency counter, and a LCZ meter. In between the device-under-test (DUT) and the instrumentation is the relay matrix.

The relay-matrix serves as the wire connecting the DUT to the instrumentation. This arrangement allows any connection coming out of the DUT to be electrically connected to any of the instruments' inputs or outputs by simply closing and opening sets of relays. Hence there is no

longer a need to hardwire the instrumentation to the DUT, which lets the user configure the connections with software instead of a soldering iron.

The final piece which ties all the parts together is the software. This code has been written in a modular fashion for easy maintenance and reuse. It is comprised of routines to control the GPIB interface, to make standardized measurements, and to provide a graphical-user interface (GUI) for the user to use in selecting prewritten tests and files. Much of the software is centered around the testing of Sandia's ATC chips, with routines that understand the structures on a die and how to test them. Each die may have multiple packages or multiple pinouts in the same package; all of these are handled through the use of a configuration file. This file is a template in which the user associates the pins of the package with structures on the die. With its built-in understanding of existing ATC chips, the software can take this list and use it to reroute the signals through the relay matrix so that the correct instrumentation is strapped across the correct test structure.

Currently, the UATS is running code to test many variation of Sandia's ATC4.1, ATC4.0, ATC2.6, ATC2.5, and NAT01 chips in quad-flat packs, ceramic DIPS, and flip-chips.

C. Results

For purposes of data analysis, we considered each triple track structure on a die to be an independent entity in the experiment. There were 36 packages in the experiment with 12 triple tracks per package, corresponding to a total of 432 tracks of each type (inner, outer, center), or 1296 total tracks. The initial resistance of an ATC02.5 track of any type was about 2.5 kΩ, assuming no lead resistance. The actual measured initial resistances were distributed in value, as shown in the cumulative distribution plot in Figure 2.8. About 75% of the triple tracks had resistances, $R_{tt} < 3$ kΩ. The long tail in the distribution function at high resistance and the lack of normality in the distribution indicate that at least two mechanisms are producing the observed distribution in resistance values. In this case, we hypothesize that the intrinsic part of the curve occurs at low resistances, as characterized by a standard deviation $\sigma \approx 50$ Ω. The dot-dash line designated *Intrinsic cdf* shows the intrinsic distribution function. This part of the cdf is produced by random variations in resistor values on the chip caused by wafer processing random variables such as ion implant concentration variations. The extrinsic part of the curve at high resistance values is probably caused principally by resistance in the socket to package connection. We have verified this source in sample cases by probing the package directly, using a scrubbing action on the probes to insure good contact. Thirteen of the original tracks measured open circuit in the initial or t = 0 measurement. All of the open tracks except one were on part PMP17. These were legitimate open circuits because some of the tracks on this part measured at a normal resistance, indicating that the center and out/in common busses, as shown in Figure 2.2, were intact and were not the source of the high resistance.

In order to calculate failure fractions at the measurement times, it is necessary to specify the thresholds for the resistance corresponding to track failure. If the distribution of finite resistance values stayed similar to that in Figure 2.8, then the threshold could be chosen as $R_{fail} = 6$ kΩ. However, as time progresses in the HAST, the distribution develops a high resistance tail which could be due either to actual on-chip resistance increases or to increased lead resistance in the

test socket. The distribution of resistance values for all bias voltages at t = 100 h is shown in Figure 2.9. The tail in resistance values now extends to about 20 kΩ.

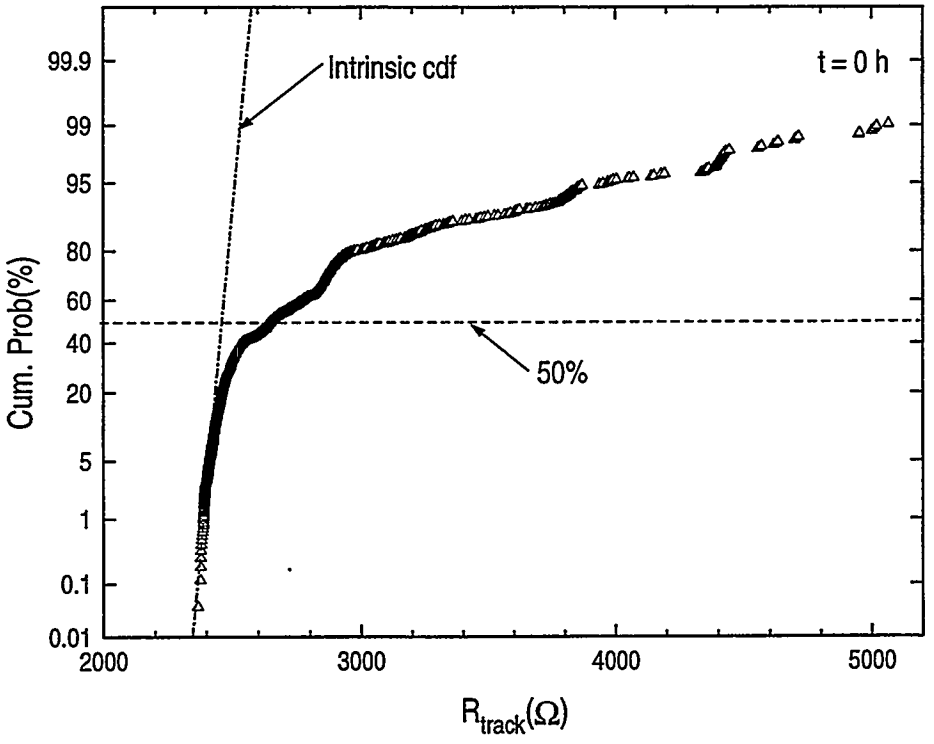

Figure 2.8. Cumulative distribution of initial triple track resistance values. There were 1296 initial triple tracks in the 36 parts at the start of the experiment. The estimated intrinsic cdf function is shown as the dash-dot line.

At each measurement point, one or more parts were removed from the test for failure analysis. The results of this analysis will be discussed in the next section. This removal of test parts causes some uncertainty in determining the track failure fractions at later times because the parts removed are no longer in the test population.

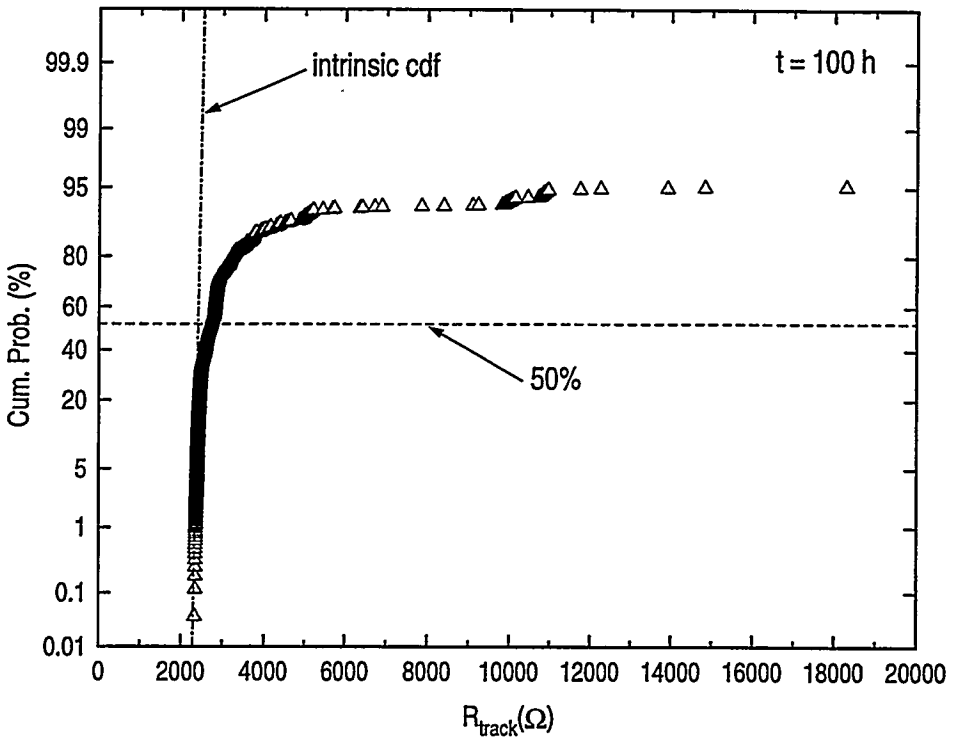

Figure 2.9. Cumulative distribution of triple track resistance values at a HAST aging time of 100 h. The estimated intrinsic cdf function is shown as the dash-dot line.

The distribution of resistance values at the end of the test, t = 800 h, is shown in Figure 2.10. This distribution was measured after the parts had been put through a rigorous cleaning procedure to removed oxide and other deposits from the leads. This cleaning procedure was only used at the 600 and 800 h measurement points and so measurements at earlier times may have been skewed by high socket to package resistances. The maximum measured resistance is limited to about 32 kΩ by the maximum voltage which can be measured by the UATS at the standard measurement current, 100μA.

The distribution of resistances shown in Figure 2.10 indicates that about 31% of the tracks in the parts remaining in the test at 800 h had measured open circuit resistance values. However, the tail of the distribution now extends to about 30 kΩ. If a lower threshold, say R_{fail} = 6 kΩ had been chosen, then the fraction of parts below that resistance value is about 58%, corresponding to a failure fraction of about 42%. Thus, the uncertainty in failure fractions at later times appears to be about 10%.

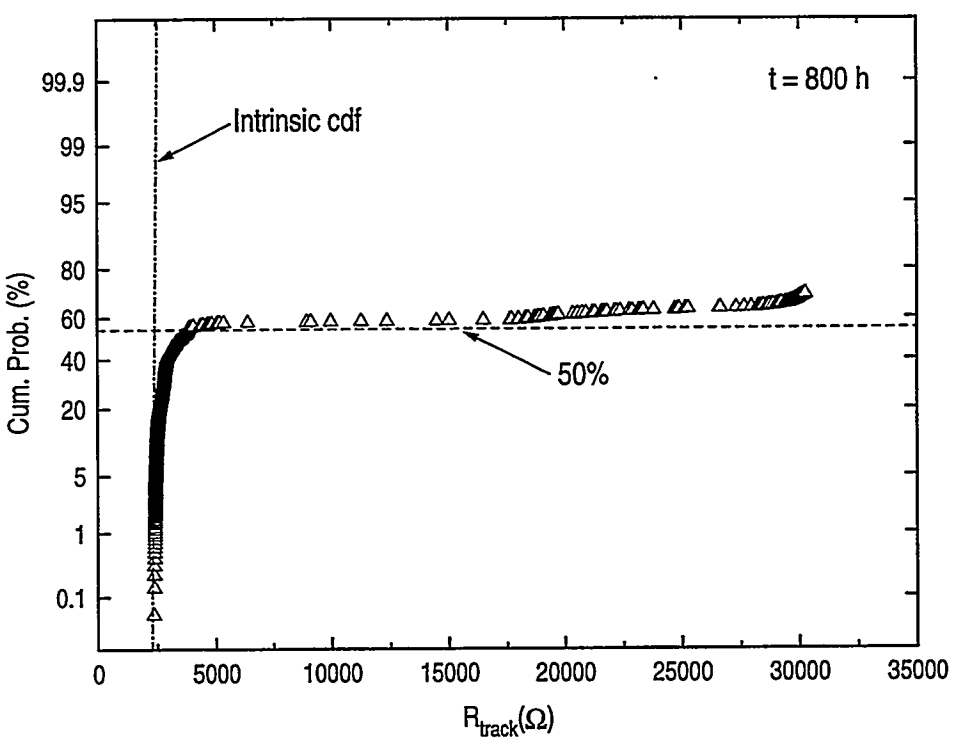

Figure 2.10. Cumulative distribution of triple track resistance values at a HAST aging time of 800 h. The estimated intrinsic cdf function is shown as the dash-dot line.

It is interesting to examine the effect of bias voltage on failure rate. The experimental resistance distribution for the three different bias voltages at t = 800 h is shown in Figure 2.11.

At low track resistance values, there is little difference between the 0 and 10 V groups. Thus, if a threshold failure resistance, R_{fail} = 15 kΩ was used, the 0 and 10 V groups would have the same failure fraction, about 40%. At $R_{track} \approx$ 20 kΩ, the 0 V group starts to have appreciably more high resistance parts than the 10 or 40 V groups. If a high failure threshold is used, R_{fail} = 35 kΩ, then the failure fractions are 14.0, 30.4, and 46.8 for the 0, 10, and 40 V groups, respectively.

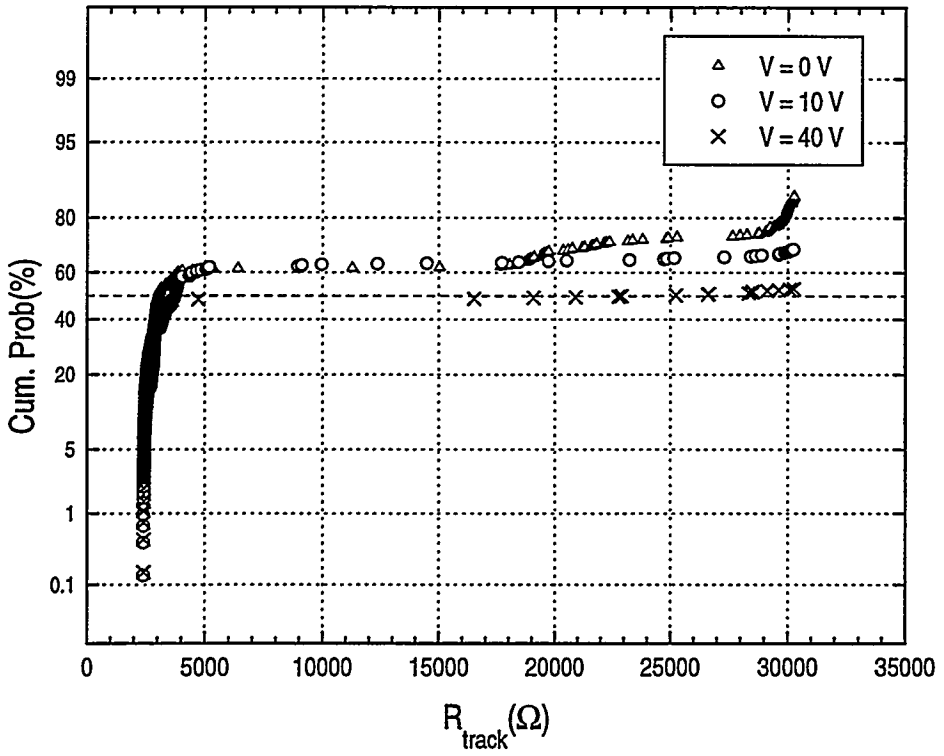

Figure 2.11. Distribution of resistances as a function of bias voltage at t = 800 h. The V = 0 group has a large number of parts with resistances in the 30 kΩ range, indicative of actual resistances in excess of 30 kΩ.

The experimental voltage acceleration factor is determined by fitting the above failure fraction vs. voltage data to a function of bias voltage. A first order or linear fit is shown in Figure 2.12, using Eq. (16) in Task 4. The resulting parameters are a = 1 and b = 0.043, using a reference $V_o = 0V$. These data show a much weaker dependence of failure rate on bias voltage than that reported by Shirley in Table IV-1 of Task 4.

Using data of the type shown in Figure 2.11 for each measurement time, we can draw the experimental failure cdf. This is shown in Figure 2.13. The failure fractions for this graph were calculated using the parts remaining in the experiment at the measurement time. Since some parts had been removed for failure analysis at the later measurement times, there is some ambiguity in the 600 and 800 h data.

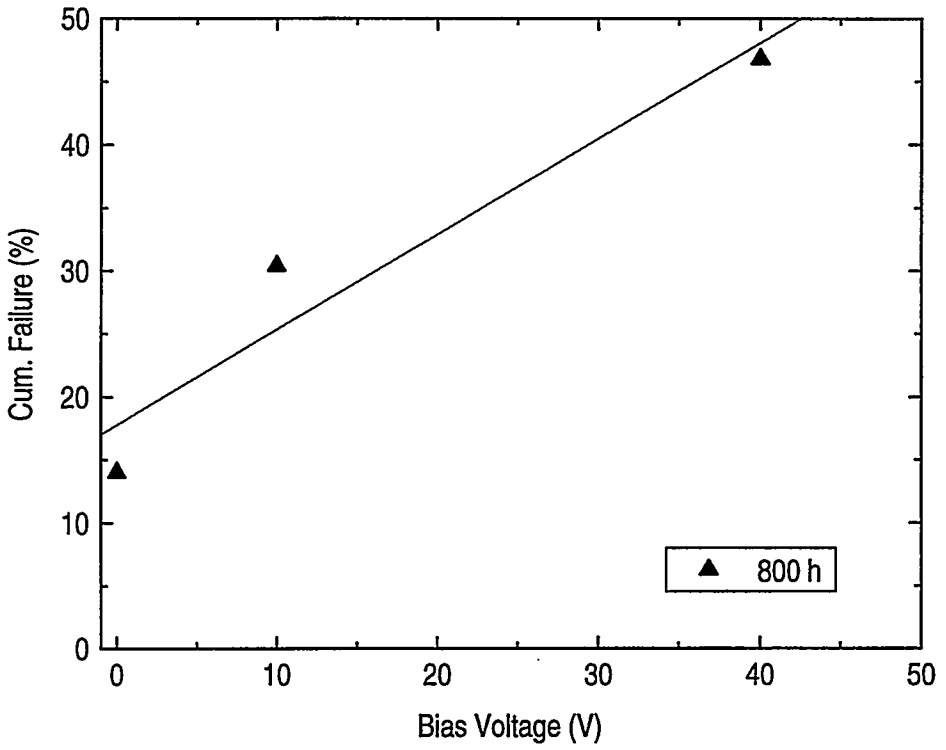

Figure 2.12. Linear or first order fit to the 800 h failure fraction vs. voltage data using a failure threshold, $R_{fail} = 35\ k\Omega$.

The 40 V group has a non-zero initial failure fraction because some of the tracks on two parts were open circuited at the test start, as discussed above. The 0 V group had no failures until the t = 20 h measurement point. To accurately determine the early or extrinsic failure distributions, more parts would be needed.

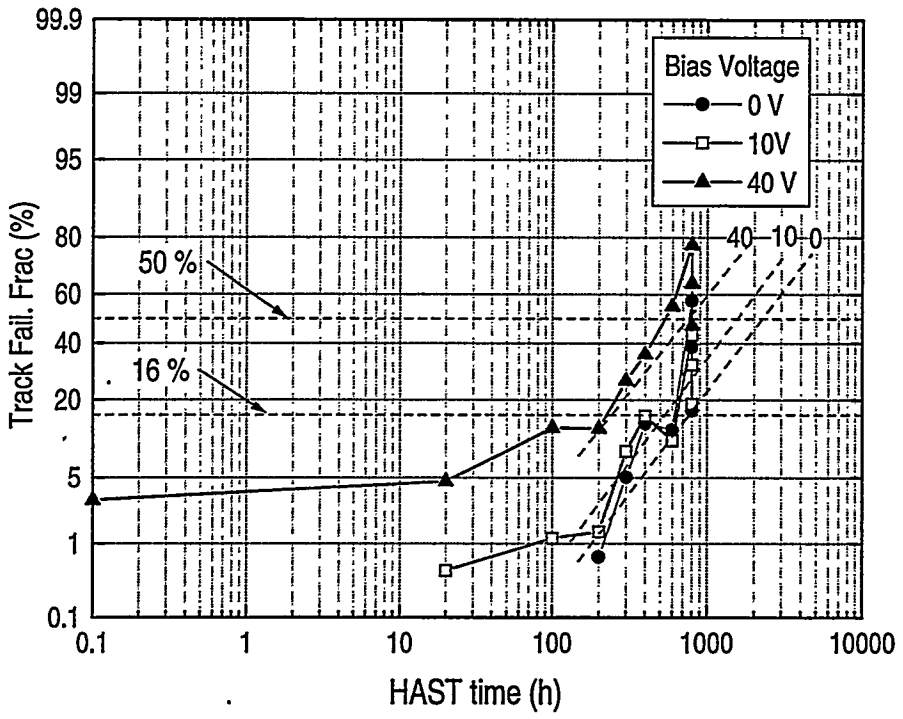

Figure 2.13. Experimental cdf for the 140°C 85% RH HAST. The 16 and 50% failure fractions are shown by the horizontal dashed lines. The data for each voltage group are extrapolated to higher failure fractions using the diagonal dashed lines. This extrapolation has been made "by eye".

At the longest experimental time, 800 h, three electrical measurements were made. In the first, the parts were measured with no cleaning. The package pins were then cleaned and straightened and a second measurement was made. Finally, the parts were cleaned again using a more aggressive procedure and a final measurement was made. A table of values for the three sets of measured failure fractions is shown in Table III-1.

Table III-1. Failure fractions in % for the three voltage groups as measured at the end of the HAST, t = 800 h. Bias voltages are listed in the top row. The left hand column shows the measurement states.

Voltage (V) →	0	10	40
After removal from HAST system	57.6%	43.4%	77.8%
After first cleaning	38.6%	18.9%	62.2%
After second cleaning	17.2%	31.7%	47.2%

From the data shown in Table III-1 it is evident that the measured failure fraction at the end of the test was highly dependent on the package preparation. Hence, the data must be considered as tentative. It is interesting to note that the 10 V group had a small failure fraction, 18.9% after the first clean but on the third measurement showed a failure fraction almost twice as high.

IV. Failure Analysis

During the HAST, several parts were removed and decapsulated for failure analysis at the 200 h point. As shown in the track failure fraction data, Figure 2.13, this time is about equal to the time at which the extrinsic and intrinsic failure modes have roughly the same cdf value. The goal of this analysis was to determine what the failure modes were and to get some idea of their relative frequencies. We expected to see three principal types of failures:

1. Bondpad degradation due to either corrosion or Au-Al intermetallic formation. As discussed in the Task 1 High Temperature Storage (HTS) section, the presence of moisture can significantly accelerate Au-Al bond reaction and degradation.

2. Localized corrosion and track failure due to particle induced damage to chip passivation and underlying Al conductors.

3. Distributed track corrosion resulting from moisture penetration through natural SiN passivation defects or voids. This type of corrosion can appear very similar to the 2nd type if the track opens rapidly.

As an example of the 3rd type of corrosion, an SEM micrograph of a corroded triple track, TT #5, from part PMP17 is shown in Figure 2.14. The corrosion of the Al has resulted in lifting the SiN passivation above the tracks and cracking it. In this case, the center track was open at the initial measurement, while the inner and outer tracks indicated open at time t = 20 h. The extensive corrosion of this triple track probably indicates that there was some chemical contamination or many passivation defects in this region of the die. We have observed this type of corrosion many times in previous HAST experiments using ATCs.

An example of late time corrosion is shown in Figure 2.15. The outer track of structure TT #8 on part PMP22 failed at t = 300 h. The center and inner tracks remained intact until the end of the test, t = 800 h. There is evidence of significant passivation cracking and spallation. The possible outer track failure point is also indicated in Figure 2.15.

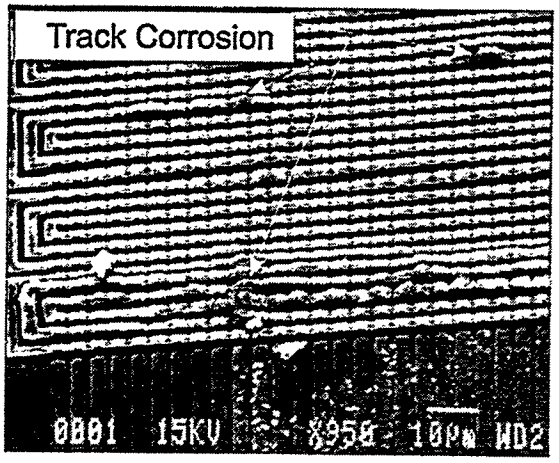

Figure 2.14. Corroded triple track region on track # 5. Corrosion has initiated at several sites on the track and proceeded quite extensively in the bottom site. The center track was open at the initial measurement. The outer and inner tracks were open at the first measurement time, t = 20 h.

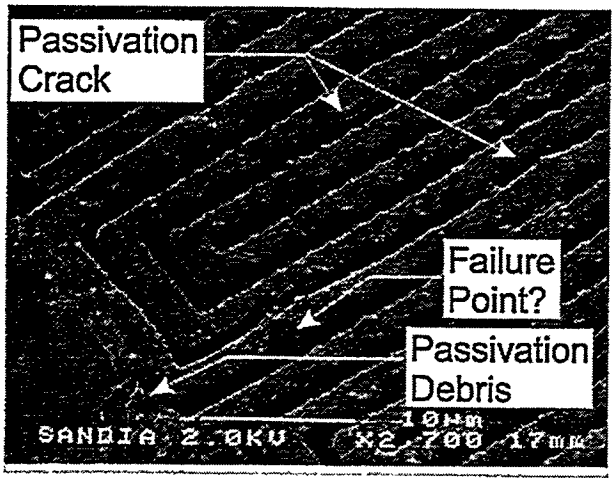

Figure 2.15. Corroded tracks on part PMP22. The outer track measured open at t = 300 h. There is evidence of SiN passivation cracking and spallation. The possible outer track failure point is indicated.

An example of localized corrosion and failure is shown in Figure 2.16, an SEM micrograph of a corroded triple track, TT #12, from part PMP39. This outer track failed at time t = 100 h. The center and inner tracks were still good when the part was removed at t = 200 h. The corrosion probably occurred at a site where the track was damaged by a particle. There is no evidence of the widespread corrosion of the type shown in Figure 2.14.

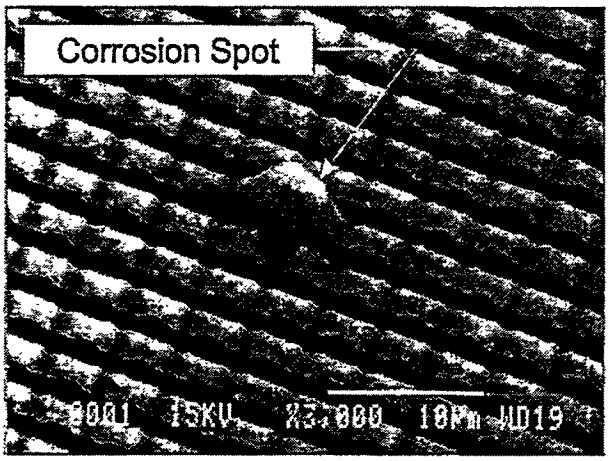

Figure 2.16. Localized corrosion region on part PMP39, TT # 12. This outer track measured open circuited at time t = 100 h. The center and inner tracks remained intact and measured good at the removal time, t = 200 h.

Most of the open circuited triple tracks which we examined at the 200 h point in the test exhibited damaged regions of the type shown in Figure 2.16. This suggests that most of the early or extrinsic failure was caused by particle induced damage.

All of the decapsulated parts exhibited very weak bond pull strength at 200 h. The bonds could be easily broken by a light push with tweezers. In many cases the Al from the bondpad adhered to the Au bond. In other cases, some Si from the die was pulled out and adhered to the Au bond and Al pad on the bond. On some bonds there was visible evidence of a reaction zone forming as shown in the left hand SEM micrograph in Figure 2.17. Other bonds were visually not reacted but were also very weak, as shown in the right hand SEM micrograph.

The low bond strength at 300 h in the 140°C 85% RH HAST is not too surprising. From Figure 1A.12 in the Task 1 chapter, it can be seen that an ATC02.6 bondpad resistance structure shows a significant resistance change at this time under identical HAST conditions. Bond pull and shear tests of bonds aged at 200°C dry conditions showed significant loss of strength at 100 h. From Figure 1A.12 it can be seen that the resistance change of the test structure is about the same for 140°C 85% RH and 200°C 20% RH conditions, so it is logical to assume that the bond strength would be about the same also, as experimentally observed.

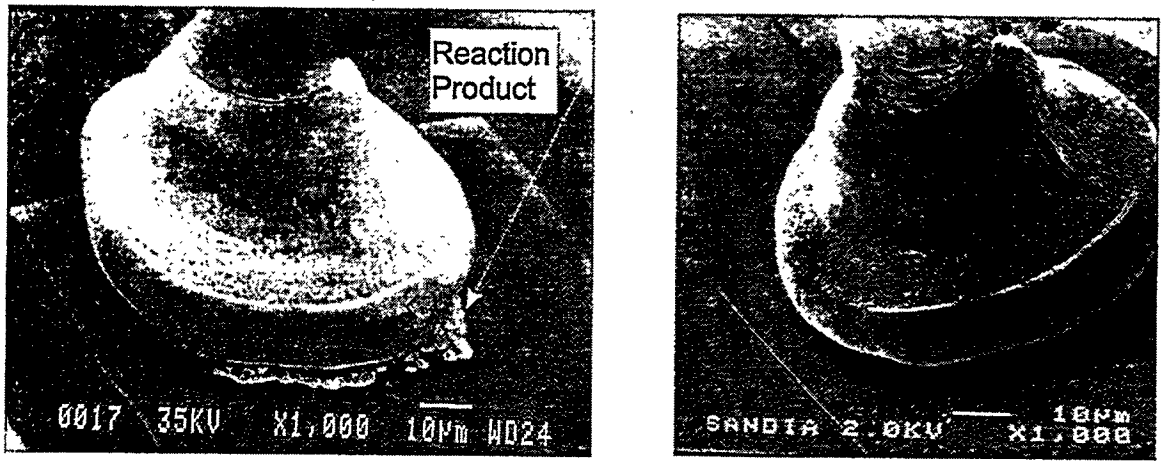

Figure 2.17. Typical Au bonds on Al bondpads from part PMP22 at t = 300 h. The bond on the left shows a visible reaction product region. The bond on the right appears unreacted.

V. Discussion

A. Lifetime prediction for HAST data

Although the HAST data shown in Figure 2. exist only for the given experimental condition, T = 140°C and RH = 85%, it is interesting to extrapolate these results to typical "use" conditions. The Peck parameters, E_a = 0.79 eV and n = 2.66 in Table IV-1 of Task 4 represent conservative values in that they are in the lower range of reported parameters and hence represent the smallest accelerations. Using Eq. (17) in Task 4 or Figures 4.5 and 4.6 in Task 4 together with the measured t_{50} values from Figure 2. yields the following predicted table of t_{50} values at the use conditions given in the right hand column of Table V-1..

Table V-1 Calculated t_{50} values, in hours, found using the Peck acceleration factors from Task 4 and the extrapolated t_{50} values from Figure 2.. One year = 8760 h.

Temp. (°C)	RH (%)	V = 0 V	V = 10 V	V = 40 V
140	85	2,300	1,570	770
85	85	69,460	47,414	23,254
50	85	1,100,900	758,310	371,910
50	50	4,558,600	3,110,170	1,525,370

Several interesting observations may be made from the entries in Table V-1. First, at 85/85 conditions, the predicted t_{50} values are really not experimentally accessible. At 40 V, the predicted t_{50} is 2.6 years and at 10 V, 5.4 years. It would be extremely difficult to run an 85/85 test for these periods of time. Second, at any reasonable "worst case" storage conditions such as 50/85(3^{rd} row of entries), the predicted lifetime is far in excess of any possible actual lifetime.

In high reliability applications, the interest is really in the extrinsic or early failure regime. In our experiment, 10 and 40 V failures were found at the first measurement time, t = 11 h. Using the Peck acceleration factor, this corresponds to a time $t \approx$ 330 h at 85/85 conditions. Current industrial specifications require a very small failure fraction after 1000 hours of 85/85 testing. For example, the Intel specification is < 0.5% failures after 1000 hours of 85/85 exposure[2]. This translates to 0.5% failures after 33 h of HAST at 140°C and 85 %RH. Using this criterion, our 10 V parts would be right at the limit for acceptance. A larger sample set would have been required to accurately measure the early failure rate distribution.

VI. Conclusions

We have demonstrated the ability to perform HAST experiments on modern surface mount parts. The ATC02.5 chip provides an excellent test vehicle which is sensitive to both bond degradation and passivation defect related failure mechanisms. Using high bias voltages it is possible to accelerate failures enough to move t_{50} to under 1000 h of test time at 140°C and 85 %RH. However, it was difficult to accurately determine triple track failure fractions because of variable lead resistance at the package to socket joints. As the HAST proceeds, the package leads become both tarnished and deformed from handling and environmental stressing, with the result that reliable electrical connection becomes harder and harder to establish. In the experiment reported here, we used mechanical abrasion of the leads for cleaning but this introduced additional lead deformation. At the end of the experiment, we tried a bead blasting technique with some success. Currently we are acquiring equipment to make this cleaning process quick and reliable.

From our data, it appears that bond degradation may be the most serious problem at the HAST conditions which we used. Although the mold compound holds the bond in contact with the pad and tends to prevent separation, there is very little native bond strength remaining after about 300 h of HAST aging at 140°C and 85% RH. We would expect that shock and vibration testing at this point would lead to additional failures of weak bonds. This suggests that a thermal cycling stress should be applied at the end of a HAST experiment in order to achieve the largest possible failure fraction in the test population.

.For future work it would be desirable to repeat the experiment at both higher and lower temperatures. This would enable the determination of an activation energy and to verify that the new cleaning procedure provides a means for reliably measuring track resistances in aged packages.

At the time this document was being written, preliminary HAST data on a small group of newly assembled parts which had been carefully cleaned prior to lapping at the National Semiconductor Corp. indicate that the particle induced failure rate has been substantially reduced. Although only six parts were in each of the three voltage groups at 140°C and 85% RH, the cumulative failure

fraction after 800 h is < 1% for the V = 10 V group. This result indicates the extrinsic failure rate has been significantly reduced and that the new bead blaster package cleaning procedure has significantly reduced false open circuit indications. One of the major outcomes of this FY96 PMP research program has been the definition of proper techniques for performing a HAST with modern surface mount parts of the type which might be used in a future DOE weapons system.

[1] L. T. Nguyen, R. W. Giberti, "Plastic Packaging Corsortium - First Year Results", *Proc. of 46th Electronic Components & Technology Conference*, 1996, pp. 1239-1243.

[2] D. Danielson, G. Marcyk, E. Babb, S. Kudva, "HAST Applications: Acceleration Factors and Results for VLSI Components", *Proc. 27th Annual Reliability Physics Symposium*, IEEE, 1989, pp. 114-121.

Task 3

OPTIMIZED TEST CHIPS

Donald R. Johnson

I. Objective

The objective of this task was to identify a need, if any, for optimized test chips for evaluation of the aging characteristics and degradation of the plastic packaged devices that were to be exposed to the various test conditions. Once a need was identified, most likely in the second year of the program, the next step would have been to design and fabricate an optimized test chip for use in subsequent evaluations.

II. Status

No work was conducted on this task during the year.

Task 4

Lifetime Prediction Models

James N. Sweet

I. Introduction

By their nature, lifetime prediction models attempt to predict something like the mean time to failure of a component from one or more variables characterizing the environment in which the component is placed. Examples of such environmental variables are:

1. Temperature (T) - This is a very commonly used variable because most physical and chemical processes in IC packages have a strong temperature dependence.

2. Relative Humidity (RH) - The relative humidity is defined as the partial pressure of H_2O at a given temperature to the saturation pressure at that temperature. Many chemical processes which can lead to IC degradation or failure, are exacerbated by the presence of moisture. In many cases, the degradation rate is a function of the RH external to the package.

3. Voltage (V) - The bias voltage V applied to a part under test may affect the part lifetime. Many chemical reactions are enabled or enhanced by current flow.

4. Acceleration - All components are susceptible to damage produced by mechanical shock. In PEMs, there is no free volume and all bond wires are stabilized by the plastic encapsulant. Hence, PEMs, by themselves, generally perform very well in a high shock environment. Shock induced damage will likely occur at a solder joint between an IC package and the printed circuit (PC) board on which it is mounted.

5. Thermal shock and cycling (T_{high} and T_{low}) - Rapid transitions from a low to a high temperature can produce damage in PEMs. Generally, such tests are characterized by the high and low temperature extremes, T_{high} and T_{low}, respectively.

According to a definition given by Nelson [1], a statistical model for an accelerated life test consists of : (1) a life distribution function which represents the scatter in product life and (2) a relationship between "life" and stress variables, such as those enumerated above. If this relation is known, either from theoretical considerations or from experiment, then it may be used to predict the lifetime at normal or use conditions from a shorter lifetime measured in what Nelson terms "overstress" conditions[2]. We also use the phrase "accelerated aging experiment" to designate an experiment in which parts are run or aged in an overstress condition, with functional test measurements made from time to time in order to determine the dependence of part failure fraction on aging time.

In an overstress condition, a variable such as temperature will be set at a sufficiently high level so as to reduce the lifetime to a measurable value. Overstress experiments have two major goals:

1. Prediction of an actual "use condition" mean lifetime from the measured lifetime(s) at one or more overstress conditions. In order to do this, the dependence of the life distribution function on the stress parameters must be known.

2. Ranking of the performance of functionally identical components fabricated with different materials and/or manufacturing processes. In this type of experiment, the dependence of the life distribution function of the parameters need not be known, but the measured lifetime ratio at the acceleration conditions cannot be directly extrapolated to the corresponding ratio at use conditions. These types of experiments are frequently termed "A vs. B" experiments to indicate that a lifetime comparison is being made between a component fabricated with processes and materials A versus one fabricated with processes and materials B.

In the discussion which follows, we shall be primarily concerned with the state of models which determine the lifetime of PEMs as a function of temperature (T), relative humidity (RH), and voltage (V). For the Ceramic Hermetic Packages (CHP) previously used for DOE Defense Program (DP) systems, RH was not a variable of interest because the CHPs were (hopefully) sealed in a very dry environment. In contrast, all plastic encapsulating materials are permeable to water, and hence a PEM lifetime will depend on the environmental RH which exits external to the package.

At any given stress state, there may be several different degradation and failure modes, each of which has a different dependence on the stress variables. For example, Au wire bonds on Al IC bondpads can degrade at high temperature as a result of the formation of brittle Au-Al intermetallics. Although this failure mode may be exacerbated in very high humidity conditions, it can readily occur at 0 RH. In contrast, failures caused by corrosion of Al conductors in the IC require the presence of moisture and can readily occur at temperatures significantly below those required for bond degradation. An experiment may be designed to study only one of these failure modes or it may look at failures from all possible modes. Nevertheless, we always assume that the observed failures are caused by random or stochastic chemical or physical processes on the IC.

II. Random failure processes

A. Basic ideas

The fundamental assumption underlying all of component reliability evaluation is that failure is caused by random processes which can be characterized, in theory, by statistical distribution functions. These distribution functions are further characterized by several parameters such as the mean and standard deviation of the distributions. Nelson discusses the distributions commonly used in electronics failure analysis in detail [3]. Here we review some basic ideas which are necessary for the understanding of experimental data analysis.

The common assumptions about the part or component failure process are the following:

1. For a group of N identical parts aged at constant stress (constant T, RH, and V), the number, δn, which fail in a time interval dt centered about time t is a random variable. If many identical aging experiments were performed, as characterized by some index i, then the numbers, δn_i, of part failures in the time interval dt in the i^{th} experiment will be distributed about some average value dn. Although the randomness in the failure rate may be associated with the random nature of the failure process, it may also have a contribution from random variations associated with the measurement system. An example of this type of effect is the measurement of an aging caused resistance shift in an IC circuit. There may also be a random change in resistance caused by imperfect contacts in the measurement circuit external to the package under study.

2. This average failure number dn is given by the product of dt and a probability density function (pdf) f(t|s),

$$dn = f(t|s)dt \tag{1}$$

In Eq. (1), t is the random variable and the stress parameter s represents all of the applied stresses. In the work discussed in this report, s represents one or more of the variables; temperature, relative humidity and bias voltage. This representation is conventionally written by showing the list of variables in the stress, s={T,RH,V}.

3. Associated with the probability density function f is a cumulative distribution function (cdf), F, which gives the average or predicted number of parts which fail at or before time t. The cumulative distribution is derived from the pdf by integrating f in Eq.(1) with respect to time from time 0 to the final time,

$$F(t|s) = \int_0^t f(t'|s)dt' \tag{2}$$

In most of the work discussed in this report, the cumulative distribution function will be used. Either the pdf or the cdf can be "fit" to experimental failure data. However, for a small number of failure data, the cdf fit is usually more accurate.

B. Graphical illustration of the failure process

The random processes described above can be illustrated graphically as shown in Figure 4.1. If the part "lifetime" is defined, arbitrarily as the time at which some given fraction x of the parts have failed, then in a series of repeated experiments at a constant stress level s, the time t_x to achieve a failure fraction of x will be a random variable. If the series of measurements is repeated at a number of stresses, the variation of lifetime with stress can be determined experimentally, as shown in Figure 4.1(a). The average behavior of lifetime vs. stress, $t_x(s)$, is shown as the line through the data points. If enough measurements are made, then the pdf at each stress level can be determined, as shown in Figure 4.1(b). If this process could be followed, then confidence intervals on the lifetime vs. stress relation could be established. The dashed curves in Figure

4.1(b) represent the extreme values for the function $t_x(s)$. In practice, it is difficult to do this because of the amount of experimentation required.

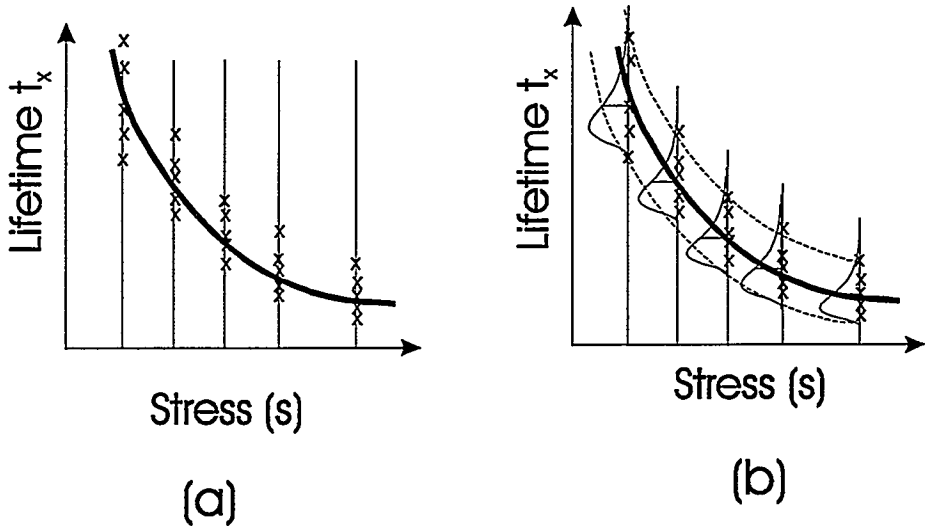

Figure 4.1 (a) Illustration of the derivation of part lifetime vs. stress from a series of repeated experiments at each of several fixed stress levels, indicated by the vertical lines. (b) View of the lifetime vs. stress data as arising from a random process characterized by a lifetime distribution function at each stress level. Confidence levels for the lifetime vs. stress relation are determined from the pdf extremes, as indicated by the dashed curves.

C. Derivation of lifetime from failure rate data

The part lifetime is conventionally defined as the time to a given failure fraction x. This failure fraction is defined as the number of parts Δn which have failed at or before time t_x divided by the total number of parts, N, in the test, or,

$$x = \frac{\Delta n(t_x)}{N}, \tag{3}$$

where $0 \leq x \leq 1$, $0 \leq \Delta n \leq N$, and t_x is determined from data such as those shown schematically in Figure 4.1, as the time corresponding to a cumulative failure fraction x. Frequently, x is expressed in % rather than as a fraction. In this convention, t_{50} is the time to 50% failure.

D. Dependence of lifetime on the stress parameters

The goal of accelerated aging experiments is to determine the functional dependence of the lifetime on the stress parameters, $t_x(s)$, as indicated in Figure 4.1. These experiments have to be run at enough stress values to enable this dependence to be determined. It can be readily seen that this can be experimentally difficult if there are many stress variables and/or the spread in t_x values for constant stress experiments is large.

III. Statistical distribution functions

In most cases, the statistical distribution function or functions which govern the failure process are not known. In addition, they cannot be derived by first principles calculations, starting from the underlying chemical and physical processes which produce the failures. As a result, empirical distribution functions are used with two or more parameters which control the shape and properties of the function. The most common distribution which is used in electronics failure analysis is the lognormal distribution in which the logarithms of the independent variable are assumed to be normally distributed. A brief discussion of this distribution will be presented in order to set a foundation for later presentation and discussion of experimental Highly Accelerated Stress Test (HAST) failure data.

The familiar normal distribution density function (pdf) is given by the relation,

$$f_n(t|\mu,\sigma)=\frac{1}{\sqrt{2\pi}\sigma}\exp\left[-\frac{(t-\mu)^2}{2\sigma^2}\right], \tag{4}$$

where μ is the mean of the distribution and σ is the standard deviation. This function has the property that the independent variable, t, extends over the whole real axis, $-\infty \le t \le \infty$. As a result, it is only appropriate for consideration as a failure probability density function if the mean and standard deviation satisfy the condition, $\mu \gg \sigma$ so that f_n has negligible values for negative t.

The cumulative distribution function, $F_n(t|\mu,\sigma)$ may be derived from f_n using Eq. (4) and replacing the lower limit of 0 by $-\infty$,

$$\begin{aligned} F_n(t|\mu,\sigma) &= \int_{-\infty}^{t} f_n(t'|\mu,\sigma)dt' \\ &= \frac{1+erf\left[\frac{t-\mu}{\sqrt{2}\sigma}\right]}{2} \end{aligned} \tag{5}$$

where $erf(x)=\frac{2}{\sqrt{\pi}}\int_0^x e^{-u^2}du$.

From the definition of the cumulative distribution function, Eq.(2), it can be seen that any function F(t) satisfying the three requirements; F(0) = 0, F→ 1 as t→∞, and F(t) monotonically increasing as t increases can be a candidate cumulative distribution function. Such a function is the cumulative lognormal distribution, found from Eq.(5) by making the substitution, t → ln(t),

$$F_{ln}(t|\mu,\sigma)=\frac{1+erf\left[\frac{\ln(t)-\mu}{\sqrt{2}\sigma}\right]}{2} \tag{6}$$

The lognormal pdf may be derived by differentiating Eq.(6) with respect to t,

$$f_{\ln}(t|\mu,\sigma) = \frac{1}{\sqrt{2\pi}\sigma\, t} \exp\left[\frac{(\ln(t)-\mu)^2}{s\sigma^2}\right] \tag{7}$$

The lognormal pdf looks very much like the corresponding normal pdf, except for the presence of the independent variable, t, in the denominator. However, the lognormal is not symmetrical about μ, and μ and σ are not the mean and standard deviation of this new distribution.

Before making a comparison of these two distributions, it is informative to transform the distribution parameters (μ,σ) to variables which have a more physical meaning. From Eq.(5), the normal distribution, has a value $F_n(t|\mu,\sigma) = 0.5$ at $t = \mu$. In a similar fashion, from Eq.(6), $F_{\ln}(t|\mu,\sigma)$ has the same value when $\ln(t) = \mu$. Thus the first new parameter we introduce is t_{50}, the time to 50% failure in the cdf. The second parameter is chosen as the time at which the normal cdf has a value one standard deviation below the mean. At $t = \mu - \sigma$, the normal cdf has a value, $F_n(\mu-\sigma|\mu,\sigma) = 0.159$. Rounding of this value to 0.16 (16%), yields the second parameter which we designate as t_{16}. In the case of the normal distribution, $\mu = t_{50}$ and $\sigma = t_{50} - t_{16}$. In the case of the lognormal, $\mu = \ln(t_{50})$ and $\sigma = \ln(t_{50}/t_{16})$. The means and standard deviations of the two distributions are summarized in Table III-1. The values for the lognormal distribution were found from the Mathematica symbolic algebra program[4]. From this table, it can be seen that the mean of the lognormal is larger than t_{50}, since the factor multiplying t_{50} in the third row of the lognormal column is greater than unity.

Table III-1 Parameters for the normal and lognormal distributions. The mean is the average value associated with the distribution, while the standard deviation is a measure of the spread in the distribution.

Parameter	**Normal Distribution**	**Lognormal Distribution**
mean(μ,σ)	μ	$e^{\left(\mu+\sigma^2/2\right)}$
standard deviation(μ,σ)	σ	$e^{(\mu+\sigma^2/2)}\left(e^{\sigma^2}-1\right)^{1/2}$
mean(t_{16},t_{50})	t_{50}	$t_{50}\exp\left[\frac{\ln^2(t_{50}/t_{16})}{2}\right]$
standard deviation(t_{16},t_{50})	t_{50}-t_{16}	$t_{50}\exp\left[\frac{\ln^2(t_{50}/t_{16})}{2}\right]\left[\exp\left[\ln^2(t_{50}/t_{16})\right]-1\right]^{1/2}$

It is easiest to see how the two distributions differ by considering an example, using numbers which might be typical for a highly accelerated stress test. In this example, t_{16} = 140 h and t_{50} = 200 h. The resultant pdfs and cdfs are shown in Figure 4.2.

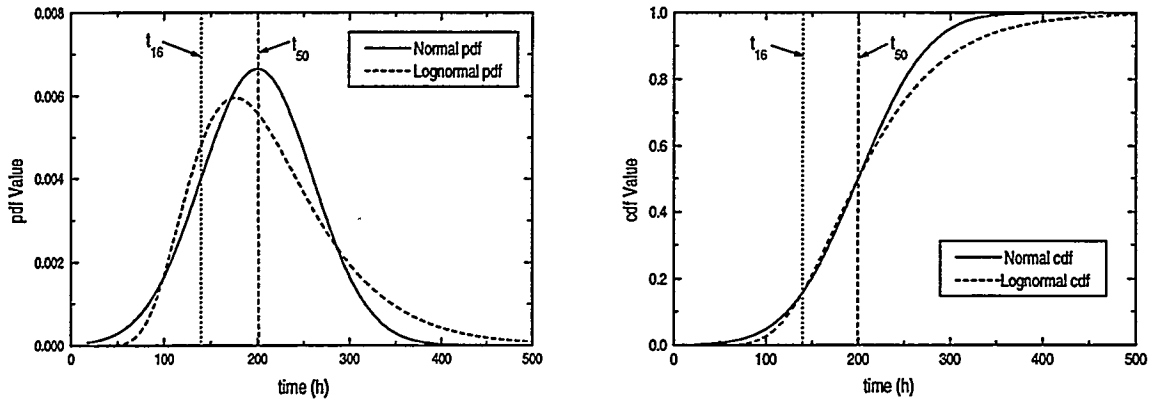

Figure 4.2 Probability density function (pdf) and cumulative distribution function (cdf) for the normal and lognormal distributions with parameters t_{50} = 200 h and t_{16} = 140 h.

In Figure 4.2(a), the density functions are compared. It can be seen that, for small values of t, the normal distribution density function has a larger amplitude than the lognormal but at long times, t>300 h, the lognormal decreases more slowly. The cumulative distribution functions shown in Figure 4.2(b) illustrate this same effect. In this case, the cdfs are equal at t_{16} and t_{50}, by design. At times $t<t_{50}$, the cdfs for the two distributions look quite similar. However, at long times the lognormal cdf is smaller than the normal cdf, indicating that the lognormal has a long "tail". The means and standard deviations of the two distributions shown in Figure 4.2 which are calculated from the relations in Table III-1 are shown in Table III-2. The long tail and increased "width" of the lognormal as compared to the corresponding normal are responsible for the increased values of the lognormal mean and standard deviation. As the ratio of mean to standard deviation increases, the lognormal becomes increasingly asymmetrical and "skewed" relative to the corresponding normal distribution.

Table III-2 Mean and standard deviation for the distributions shown in Figure 4.2. The lognormal has both a higher mean value and a higher standard deviation than the corresponding normal distribution

Distribution	Normal	Lognormal
mean	200	213.1
standard deviation	60	78.5

When experimental data are fit to a theoretical distribution function, it is possible to use either a candidate pdf or a candidate cdf to do the fitting. In the case of the pdf, the observed failure times are sorted and placed into "bins" to make an experimental pdf. The appearance of this pdf depends on how many bins are chosen and so, if there are not many data points in the set, this type of fitting can be fairly arbitrary. In the case of the cdf, the data are first sorted. Then, a theorem from statistics is used which states that, if samples of a random variable with a given pdf are taken, then the corresponding cdf values will be uniformly distributed over the range of the cdf, $0<F<1$ [5]. Thus, if N samples are obtained of the random variable t and these are ordered, by an index i; $t_1<t_2<t_3\ldots<t_N$, then the most "likely" cdf values associated with these N data are, $cdf_i = (i-.5)/N$. This choice of cdf values corresponds to the experimentally observed independent variable or t values being associated with cdf values which are uniformly distributed over the interval (0,1).

In the analysis of experimental failure data, it is conventional to plot the failure fraction vs. time data using a rescaled failure fraction axis so that the data will appear linear if distributed according to the cdf used for the rescaling [5]. If the inverse of the cdf is defined as,

$$t = F^{-1}(p|\mu,\sigma) \tag{8}$$

where F is the cdf function, Eq.(2), and p is the probability or cdf value, $0<p<1$, then this rescaling is achieved by plotting the quantity,

$$h(p, p_{\min}, p_{\max}) = \frac{F^{-1}(p|\mu,\sigma) - F^{-1}(p_{\min}|\mu,\sigma)}{F^{-1}(p_{\max}|\mu,\sigma) - F^{-1}(p_{\min}|\mu,\sigma)}, \tag{9}$$

where p_{min} and p_{max} are the minimum and maximum values on the cdf axis and p is the cdf value corresponding to the failure time t through Eq.(8). It should be remarked that, for a normal or lognormal distribution, $p_{min}>0$ because the inverse cdf is singular at p=0 and similarly for p=1. When the data are plotted in this way, the cdf p axis is labeled with p values and not h values. As a result, equally spaced p values will not be equally spaced when rescaled according to Eq. (9).

As a simple example in plotting and analyzing experimental failure rate data, we assume that a component has a lognormal distribution as shown in Figure 4.2, with t_{16}=140 h and t_{50}=200 h. In an actual experimental aging experiment, the cumulative failure fraction is measured only at discrete times and hence it is not possible to specify exactly at what time(s) a part or parts failed between successive measurements. If the measurement intervals are sufficiently small the failure time(s) may be resolved quite accurately but this is frequently not the case. Here we shall make the simplifying assumption that the cdf is continuously monitored and hence the failure times are precisely determined. We assume there is a group of N=10 parts, not unusual for a HAST experiment. A random sample selected from the lognormal distribution with the given t_{16} and t_{50} produces the data plotted in Figure 4.3. The parent lognormal cdf is shown with the diagonal dashed line. A lognormal was then fit with Mathematica using nonlinear least squares, producing the solid curve characterized by the fit parameters, t_{16} =134.7 and t_{50}=205.9. In this case, although the fit does not look particularly good by eye, the fit parameters are within 5% of the "actual" distribution values. Since there are only 10 data points, it would be very difficult to fit a

pdf to binned data because only a few bins could be used. In general, fitting of a pdf requires many more data points to obtain the same accuracy as a cdf fit.

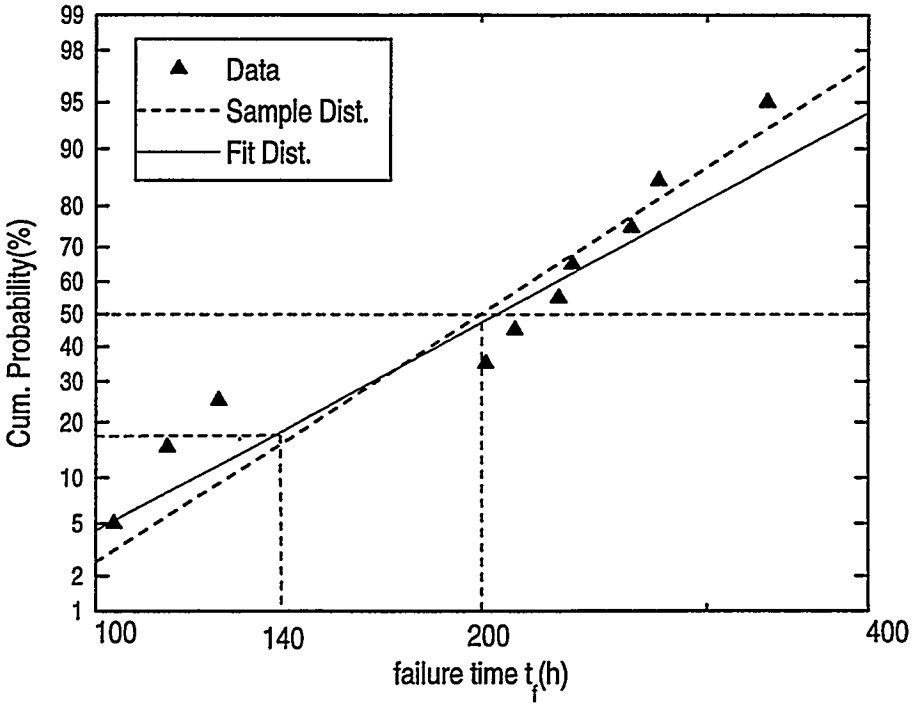

Figure 4.3 Probability plot of the "experimental" failure rate data, as determined by sampling 10 values from a lognormal distribution with t_{16}=140 h and t_{50}=200 h. σ Sampled data set, --- data set parent lognormal cdf with t_{16} =140 and t_{50}=200. ___ fitted lognormal with fit parameters; t_{16} =134.7 and t_{50}=205.9.

In most cases, the component failure process is not described by a single failure distribution because there are multiple failure modes, each with its own associated pdf. Osenbach and Zell describe experiments on accelerated temperature and humidity testing of aluminum ICs, and present many data plots which clearly show two distinct failure regions[6]. The initial part of the distribution is characterized by a very large t_{50} and a small t_{16} and is believed to be associated with local defects which lead to "premature" failures. Such a defect might be caused by a local contamination region caused by improper cleaning or by a handling scratch. These are called "extrinsic" failures because they are not intrinsic to the materials or fabrication process. These extrinsic failures are, in theory, preventable by exercising suitable care in IC fabrication and assembly.

The early failure region is followed by a region in which the experimental cdf increases rapidly. In many cases, such as the Osenbach and Zell[6] experiment, the cdf in this second region is

straight on a lognormal probability plot. The cdf in this region is characterized by a small t_{16}/t_{50} ratio, in contrast to the extrinsic failure cdf. Similar failure data have been reported by Danielson and coworkers for HAST failure of DRAM devices[7]. This type of "two mode" failure has also been reported by Emerson, Sweet, and Peterson for HAST accelerated aging of ATC01 molded and liquid encapsulated parts[8]. Thus, the two mode failure process seems to be quite widely observed.

It is relatively easy to propose models with enough parameters to fit a multimode cdf. However, it is difficult to "prove" that a given model is, in fact, the correct one for describing a given experiment. As stated above, any function which is monotonic and covers the range $0<p<1$ is a candidate cdf. In one such model, which introduces three new parameters, it is assumed that there are two possible failure modes; mode 1 which is an extrinsic or defect related mode affecting a fraction c of the parts and mode 2 which is an intrinsic failure mode affecting all the parts. In a given time interval dt, a part may fail by mode 1, mode 2, or by both modes. If we assume that the mode 1 failure is lognormal with parameters $t_{(1)16}$ and $t_{(1)50}$ and mode two lognormal with parameters $t_{(2)16}$ and $t_{(2)50}$, then a cdf, F_{12}, which describes this process is given by,

$$F_{12}\left(t\middle|c,t_{(1)16},t_{(1)50},t_{(2)16},t_{(2)50}\right)=cF_{\ln}\left(t\middle|t_{(1)16},t_{(1)50}\right)+F_{\ln}\left(t\middle|t_{(2)16},t_{(2)50}\right) -cF_{\ln}\left(t\middle|t_{(1)16},t_{(1)50}\right)F_{\ln}\left(t\middle|t_{(2)16},t_{(2)50}\right) \quad (10)$$

where the $F_{\ln}$ functions are given by Eq.(7) with $\mu=\ln(t_{50})$ and $\sigma=\ln(t_{50}/t_{16})$. It can be easily verified that F_{12} as given in Eq.(10) satisfies the requirements of a cdf. Each of the first two terms in Eq.(10) is monotonically increasing since each is proportional to a lognormal cdf, and hence the sum is also monotonically increasing. The third or product term is itself the product of three factors, each of which is positive and has a magnitude less than unity. Hence the product has a magnitude less than that of any of the individual factors. Thus, the magnitude of the third term in Eq.(10) is less than the magnitude of either the first or second term and so it may be concluded that Eq.(10) represents a monotonically increasing function of t. Finally, as $t\rightarrow\infty$, $F_{\ln}\left(t\middle|t_{16},t_{50}\right)\rightarrow 1$ and so $F_{12}\rightarrow$ c + 1-c $\rightarrow$ 1 as $t\rightarrow\infty$.

The failure model represented by the cdf, Eq.(10), has the virtue that each of the five parameters in the function, $\{c, t_{(1)16}, t_{(1)50}, t_{(2)16}, t_{(2)50}\}$, is physically meaningful. The early time failure mode, mode 1, has a distribution function, $F_{\ln}(t|t_{(1)16},t_{(1)50})$, which is physically meaningful in that the parameters, $t_{(1)16}$ and $t_{(1)50}$ are short or early times relative to $t_{(2)16}$ and $t_{(2)50}$. In addition, it appears reasonable that some fraction of the parts, $c\leq 1$, are afflicted with the condition which can produce an extrinsic mode failure. However, not all of the parameters in the model are "independent" in that they can be uniquely determined by a technique such as least squares fitting. The requirement for parameter independence is discussed in detail by Beck and Arnold[9]. We shall not go into further detail about this issue but simply point out that a reasonable four parameter model with independent parameters is achieved by using c=1 in the expression for F_{12}, Eq.(10). However, the price to be paid is the non-physical nature of $t_{(1)16}$, $t_{(1)50}$. Typically, these times will be much greater in magnitude than those associated with the "late" or intrinsic failure distribution.

In order to clarify and illustrate the use of the model, we reanalyze some of the data reported by Emerson, Sweet, and Peterson[8] on HAST aging of Sandia ATC01 corrosion test chips. These data are plotted in Figure 4.4 along with model fits to the data. In the experiment ATC01 Assembly Test Chips were biased at 40 V and aged at T=140°C and a relative humidity RH=85%. The data shown in Figure 4.4 represent the measured cumulative failure fraction for two groups of molded parts, each with Sumitomo 6300HD mold compound. This compound is similar to the one which we used in the HAST experiment described elsewhere in this report. Each group was identical except for the assembly facility. In each case, the measured cdf was "fit" to a composite lognormal of the form given in Eq.(10). This fitting was done by "trial and error" and does not represent a least squares fit to the data. The fitting parameters are given in Table III-3.

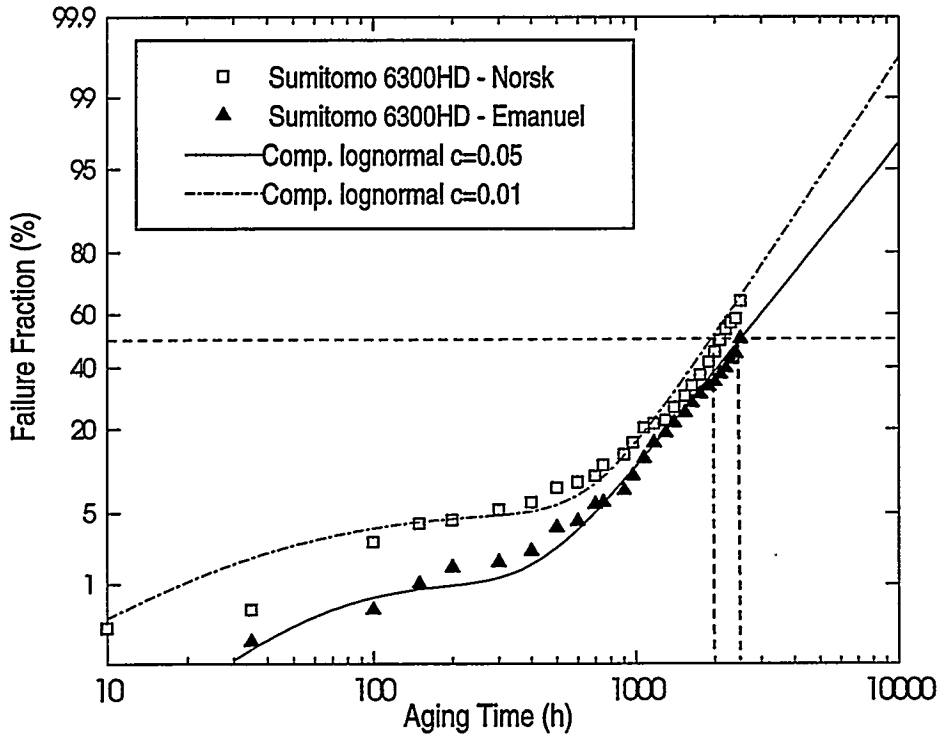

Figure 4.4 Fit of the composite lognormal function, Eq.(10), to accelerated aging HAST data. There were two different assemblers, Norsk Engineering and Emanual Equipment but the mold compound and lead frames were identical for the two groups. The fit parameters are given in Table III-3.

Table III-3 Parameters used to derive the composite lognormal fits to the data in Figure 4.4

Param.	Norsk Engineering.- □	Emanuel Equipment- ▲
c	0.05	0.01
$t_{(1)16}$(h)	20	16
$t_{(1)50}$(h)	50	50
$t_{(2)16}$(h)	1200	1200
$t_{(2)50}$(h)	2400	2500

This fit illustrates some interesting points. In the intrinsic or "long time" region, the two cdfs are essentially identical, indicating that the failures in this region are, in fact, dependent only on the materials in the chip and package which were identical for the two groups. However, at early times, the two distributions are quite different, possibly indicating different contamination levels at the two different manufacturers facilities. In the fit, the c values were chosen by eye as the cdf values at which the two different regions in the experimental cdf curves intersected. The other parameters were then adjusted to produce the plotted fits[4]. We shall examine how such data can be extrapolated to give an estimate of lifetime at use conditions after an examination of acceleration models.

IV. Models

A. Introduction

An acceleration model is a relation which relates the component lifetime at use stress conditions to those conditions used in an accelerated lifetest. In all cases of practical interest, these models cannot be derived from first principles calculations based on laws of physics, chemistry, and materials science. Rather, the models are semi-empirical in nature. The form of the functional dependence of the lifetime on the stress parameters is related to theory in some sense, but the models contain adjustable parameters which are determined by fitting a chosen model to experimental failure rate data.

The fundamental assumption which is made is that the lifetime, t_f, at some generalized stress level s is related to the lifetime at a stress level s_0 by an acceleration factor AF, as given by,

$$t_f(s) = AF(s, s_0) t_f(s_0). \tag{11}$$

The quantity t_f in Eq.(11) can be any definition of a failure time, such as the time to 5% failure in

Figure 4.4. The form of the AF function in Eq.(11) is usually determined by performing accelerated tests at a number of different stress levels and then fitting an acceleration factor relation to these data. The second fundamental assumption is that AF depends on one or more parameters, as expressed by a parameter vector, $p=\{p_1, p_2, \ldots, p_N\}$. Hence, Eq.(11) is usually written symbolically as,

$$t_f(s) = AF(s, s_0 | p) t_f(s_0). \tag{12}$$

A third assumption is that AF can be factored into factors which depend individually only on one stress and one or more of the parameters,

$$t_f(s) = AF_1(s_1, s_{01} | p_1) AF_2(s_2, s_{02} | p_2) .. AF_N(s_N, s_{0N} | p_N) t_f(s_0) \tag{13}$$

This assumption is equivalent to the assumption that all of the stresses act independently in determining the lifetime.

Before discussing specific relations for the acceleration factor function, it is important to note that there are several different interpretations of the function. These interpretations are related to assumptions about the nature of the parameters in the model. In the first interpretation, the parameters are viewed as fixed constants whose values are determined solely from experiment. No subjective or prior information on the values of the parameters is used in their determination. In the second interpretation, the parameters do not have fixed values but are rather characterized by distribution functions[10,11]. This view can arise either because the knowledge of the parameters is not precise or because the parameters are, in fact, actually random variables. Techniques based on the assumption that the parameters in the model are random variables are called Bayes' techniques[11].

B. Stress variables

1. Temperature

The acceleration factor produced by elevated temperature is almost universally taken to be given by the Arrhenius law,[12]

$$AF_T(T, T_0 | E_a) = \exp\left[\frac{E_a}{k_B}\left(\frac{1}{T_0} - \frac{1}{T}\right)\right], \tag{14}$$

where k_B = Boltzmann constant, 8.617×10^{-5} eV/ K, and T is the absolute temperature in K, (T(K)=T(°C)+273.16). The parameter E_a is called the activation energy. Simple first order chemical processes have a rate constant which varies as $\exp(E_a/k_BT)$, but most processes in nature have a more complex temperature dependence than that given by Eq.(14). Nevertheless, many accelerated aging experiments result in a temperature dependence that is well described by Eq.(14).

2. Humidity

The effect of moisture external to a plastic package is to establish a concentration gradient which results in diffusion of moisture into the package until it reaches the IC surface. The equilibrium level of moisture in the plastic is a function of the external temperature, the plastic solubility or saturation coefficient, and the moisture concentration external to the package[13]. The external moisture concentration is usually represented as a relative humidity, RH, defined as the ratio of the partial pressure of water, p, at a given temperature to the saturation pressure at that temperature. The saturated vapor pressure, $p_{sat}(T)$, is the pressure at which water vapor and liquid will coexist without change in the volumes of each constituent. Since $RH = p/ p_{sat}(T)$, and through the ideal gas law, p is proportional to the number of water molecules per unit volume in the vapor, RH is a measure of the water molecule density external to the package. In addition, in a state of thermodynamic equilibrium, the partial pressure of water in the plastic is the same as that in the vapor external to the package, assuming that water is present as a vapor or gas in the polymer. As a result, assuming the temperature at the die surface is the same as the external temperature, the RH at the die surface is the same as that in the environment. However, in the plastic the water is not in the vapor state and the molecular density is not given by the ideal gas law unless the water is in a void region. Nevertheless, it has become common practice to use the external RH as an environmental stress variable for characterizing plastic IC degradation.

In the early years of plastic, the major effect of moisture was to produce corrosion of Al conductors and bond pads on the die. Many studies of IC corrosion lead to the conclusion that the major ingredients necessary for corrosion to occur were; moisture and the presence of ionic contaminants. Given these ingredients, failure rates could be affected by other variables such as bias voltage, the presence of passivation defects, etc. As IC processing improved through the 70's and 80's , contamination levels were steadily reduced and corrosion became less and less of a problem for PEM reliability. In recent years, there have been reports of non-corrosion related IC failures from moisture going into active devices and causing transistor instabilities of various types. In all these cases, the degradation rate presumably was related to the moisture concentration and was governed by some sort of chemical reaction.

Since a chemical reaction is presumably involved, the rate will be governed by the law of mass-action which states that this rate is proportional to the product of constituent densities, each raised to powers equal to the number of a given constituent which is in the reaction[14]. With this in mind, it appears reasonable to use a power law humidity acceleration factor of the form,

$$AF_{RH}(RH, RH_0|n) = \left(\frac{RH}{RH_0}\right)^n \tag{15}$$

For a given reaction model, n may be derived from an analysis of the reaction kinetics. For example, Pecht[15] develops a theory for moisture induced corrosion failures in which the parameter n = 1. In another analysis of Al corrosion[16], the primary chemical reaction is assumed to be the electrolysis of water. In this process, the coefficient of the H_2O term in the chemical reaction equations is 2, and so by the law of mass action, n = 2 for this process. In actual cases, the parameter n is to be determined experimentally. We shall discuss reported fitted values below after considering the effect of bias voltage.

3. Bias voltage

In some instances, the degradation rate is affected by the bias voltage V applied to the circuit. This occurs in situations such as electrochemical corrosion where ions are involved in the reactions associated with the degradation process. In most cases, what is really required is the magnitude of the electric field which is the magnitude of the gradient of the voltage. This gradient depends on both the bias voltage and the spacing and shape of adjacent conductors on the IC surface. These latter quantities are variable and not generally known. Hence, it is not too surprising that voltage acceleration factors are complex and generally dependent on the IC design and technology.

Many empirical or semiempirical models have been proposed for voltage acceleration factors. In some IC failure modes such as dielectric breakdown or hot electron damage, the mean time to failure varies exponentially with the electric field and hence with the bias voltage also[17]. For electromigration caused failures, the failure time scales as the current density raised to a negative power and thus the electromigration acceleration factor varies as V^n, or $AF_V \propto V^n$. Generally, these IC or die related failure modes are not considered to be package related because they can occur at the wafer level and are not related to whether or not a part is packaged or the type of package used.

In the case of electrochemical corrosion of Al conductors, the corrosion rate varies directly as the current between conductors and hence scales as V. However, some types of corrosion do not require bias and so a simple $AF_V \propto V$ relationship is not adequate. A general two parameter voltage acceleration model has been proposed by Shirley.[18] This relation can be expressed as a voltage acceleration factor,

$$AF_V(V, V_0|a, b) = \frac{a + bV}{a + bV_0}. \tag{16}$$

C. Model parameters and their "values"

From the above discussion , we take the general form of the acceleration factor for temperature, relative humidity and bias voltage to be of the form,

$$AF(T,T_0;RH,RH_0;V,V_0|E_a,n,a,b)=\exp\left[\frac{E_a}{k_B}\left(\frac{1}{T_0}-\frac{1}{T}\right)\right]\left(\frac{RH}{RH_0}\right)^n\left(\frac{a+bV}{a+bV_0}\right) \quad (17)$$

There are have been numerous accelerated temperature, humidity, bias (THB) tests carried out over the last 20 years or so. In the following section we shall discuss a selected set of them and present the parameters reported in the various studies. The results of this summary are given in Table IV-1.

Table IV-1 Reported THB parameters for the model given by Eq.(17)

Reference	Reported Mechanism	a	b	n	E_a (ev)
Peck, Ref. 19	Electrolytic corrosion	1	0	2.66	0.79
Hallberg & Peck, Ref. 20	Corrosion	1	0	3	0.90
Lehigh Ref. 21	Corrosion	1	0	1-5	0.88
Shirley, Ref. 18	Passivation defect and transistor failure	0	1	4.64	0.79
Shirley, Ref. 22	Passivation defect and transistor failure	1	0.58	4.64	0.79
Shirley & Shell-DeGuzman, Ref.23	Au ball bond degradation on Al pad	1	0	1	1.1

In Table IV-1, we have rescaled Shirley's reported values, a = 0.24 and b = 0.14 so that the voltage acceleration factor = 1 at V_o = 0V. These values can then be compared to those we report inTAske 2 for the ATC02.5 chip.

Perhaps the most famous synthesis of the "early" THB data was presented by Peck[19] in 1986. In this paper, all published THB data up to the publication data were reviewed and synthesized. No account was taken of bias dependence, so the only variables were temperature and relative humidity. This is equivalent to the assumption that a=1 and b=0 in the voltage acceleration factor in the model, Eq.(17). Peck used as a reference the "standard" acceleration conditions; T_0=85°C and RH_0=85%. He then analyzed all data in which lifetimes were reported at both the reference condition and one or more alternate (T, RH) conditions. The reported failure mode was

electrolytic corrosion failure of Al metallization. Data from 14 sources with 61 reported tests were then fit to an expression of the form, Eq.(17), and the "best fit" values were reported as E_a = 0.79 eV and n = 2.66. Peck reported that the lognormal standard deviation was in the range σ = 0.4-0.5 for all the data reviewed, corresponding to a t_{16}/t_{50} ratio, t_{16}/t_{50} = .67-.82, using the relation, $\sigma = \ln(t_{50}/t_{16})$. In an analysis of more recent data, Hallberg and Peck[20] reported new best fit parameter values, E_a = 0.9 eV and n = 3. In this analysis, only data from the time period 1979-1987 were used because the authors felt that earlier data were suspect, particularly the data for RH = 100%. The authors review five earlier acceleration models and fit these models to the same data sets. They show that their model provides the best overall fit to the included life test data. In addition, their model is "conservative" in that it predicts a smaller enhancement in lifetime at low humidity that the earlier models.

A reanalysis of the Hallberg and Peck data from Ref. 20 was performed in support of the USAF sponsored Reliability without Hermeticity (RwoH) program[21]. In this reanalysis, the data from Ref. 20 were fit by least squares to a model of the type given by Eq.(17) with a=1 and b=0. It was found that the fit was not very sensitive to the exact value of the relative humidity or n coefficient in Eq.(17). The activation energy was determined to be best fit by values in the range E_a=0.8 - 0.9 eV but any n in the interval, n=1 - 5 yielded a "reasonable" fit. The values of E_a and n which yielded the "best" correlation coefficient were, E_a=0.88 eV and n=2.35.

In recent work on THB testing of SRAMs, Shirley reports parameter values for non-corrosion related MOS transistor failures by a "defect" mechanism[18,22]. The parameters reported in Ref. 22 are a=0.24, b=0.14, n=4.64, and E_a=0.79 eV. In another experiment on moisture related Au ball bond on Al bond pad degradation, values n=1 and E_a=1.15 eV have been reported[23].

D. Example acceleration calculations

It is interesting to look at some example acceleration calculations to obtain a feel for the magnitudes of the accelerations obtained in typical accelerated THB tests such as HAST. To obtain a conservative temperature acceleration estimate, we use the smallest magnitude E_a value in Table IV-1, 0.79 eV. Considering as an example, the test data from Figure 4.5, taken at T = 140°C, we obtain the following acceleration relation for temperatures, $T_0 \leq 140$°C,

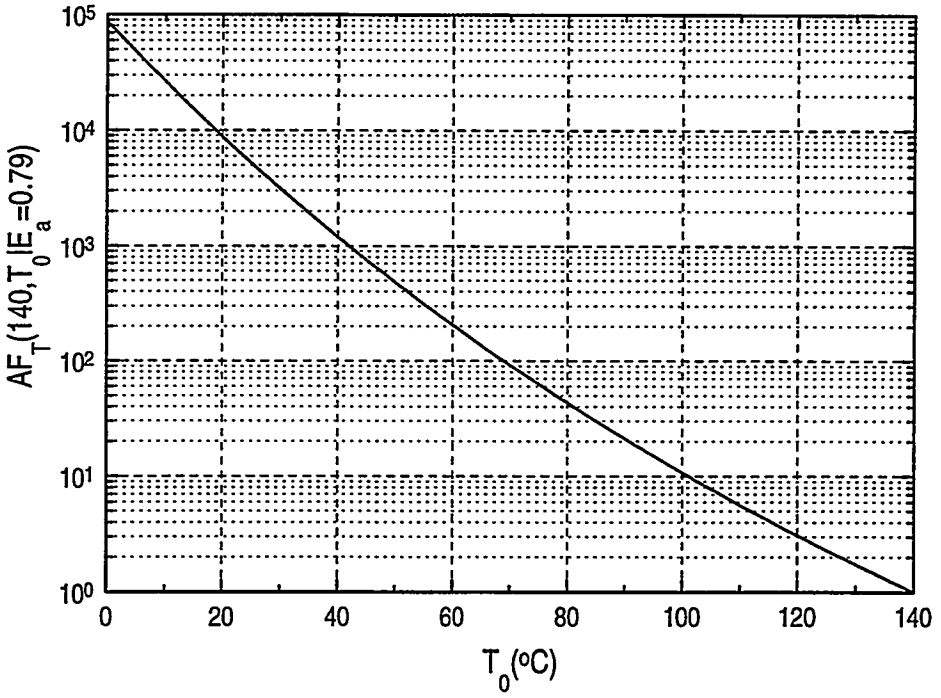

Figure 4.5. Temperature acceleration factor for temperatures $T_0 \leq 140°C$ and $E_a = 0.79$ eV.

From Figure 4.5 it can be seen that the 140°C test represents an acceleration of about 30 over that provided by an "85/85" test at 85°C, 85% RH. Hence, we would predict that the mean time to failure 2000 h in Figure 4.4 would occur at approximately 60,000 h in an 85/85 test. The earliest failure in the Figure 4.4 data at t = 10 h would have occurred at 3000 h in an 85/85 test. A commonly used acceptance criteria in industry for high reliability parts is that no failures occur after 1000 h of 85/85 testing. Based on the assumed activation energy $E_a = 0.79$ eV, we would predict that our tested parts would have been accepted in an 85/85 test.

A graph of the Peck humidity acceleration factor with n=2.66 is shown in Figure 4.6. For a typical weapons application, the average humidity level might be specified as 50%. From Figure 4.6, it can be seen that this represents a factor of four increase in lifetime relative to 85% RH.

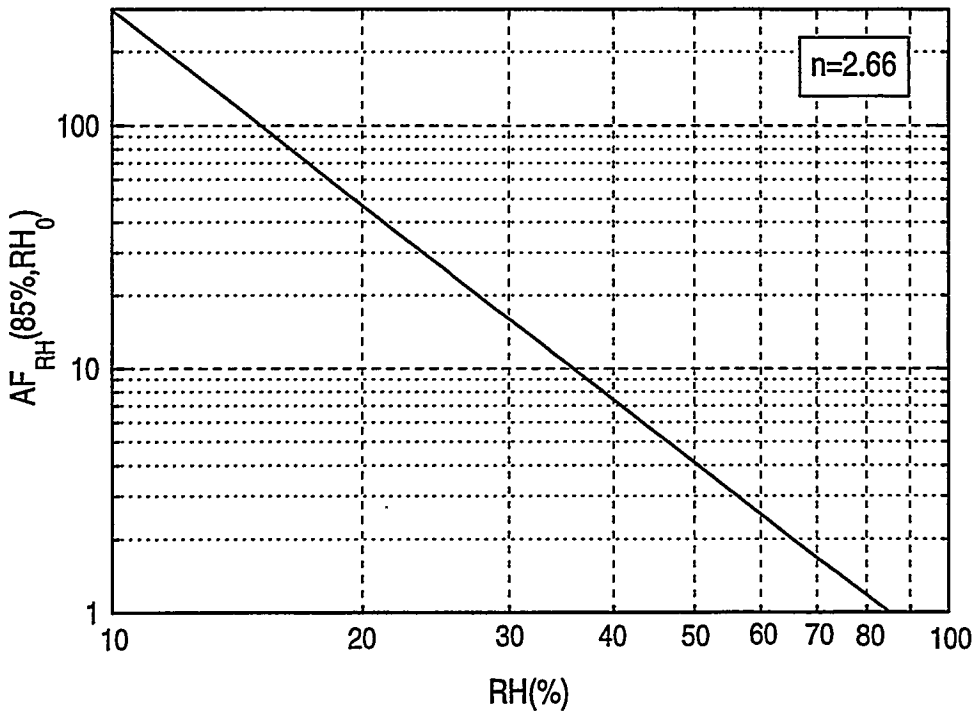

Figure 4.6 Humidity acceleration factor $AF_{RH}(85\%,RH_0|n=2.66)$.

V. Discussion

In this section we have reviewed some of the statistics and phenomenology associated with THB life testing. The Peck model, Eq. (17), is now widely used for lifetime prediction but, as shown in Table IV-1, there is a wide spread in model parameters. In order to make conservative life predictions from accelerated tests, it is conventional to take the smallest values for n and E_a when making extrapolations to lower temperatures and humidities. From Table IV-1, these are the original Peck[19] parameters, n=2.66 and $E_a = 0.79$ eV.

The large variation in reported THB parameters suggests that actual measurement of acceleration factors will be necessary if meaningful lifetime predictions are to be made. While the Peck parameter values provide a starting point for lifetime estimation, there is no way to determine how accurate this estimate is. Another factor which may prevent accurate lifetime determination is the presence of an extrinsic failure region at small aging times. This extrinsic region is sensitive to process variables such as contamination levels and hence will vary from run to run and manufacturer to manufacturer. Unless the intrinsic wearout region can be reached in a life test it is effectively impossible to determine lifetimes at storage and use conditions by extrapolation.

References

[1] W. Nelson, Accelerated Testing; Statistical Models, Test Plans, and Data Analysis, John Wiley, NY, 1990, p. 51.

[2] W. Nelson, ibid, pp. 16-17.

[3] W. Nelson, ibid, Chapter 2.

[4] All calculations in this report were done with the symbolic algebra computer program, Mathematica version 2.2, Wolfram Research Inc.. The program is described in; S. Wolfram, Mathematica, a System for Doing Mathematics by Computer 2nd Ed., Addison Wesley, CA, 1991.

[5] R. B. D'Agostino, M. A. Stephens, Goodness-of-Fit Techniques, Marcel Dekker, NY, 1986.

[6] J. S. Osenbach, J. L. Zell, "Corrosion of Thin Film Aluminum Metallization: Conformal Coating Materials", *IEEE Trans. Components, Hybrids, Mfr. Technol.*, Vol. 16, 1993, pp. 350-359.

[7] D. Danielson, G. Marcyk, E. Babb, S. Kudva, "HAST Applications: Acceleration Factors and Results for VLSI Components", *Proc. 27th Annual Reliability Physics Symposium*, IEEE, 1989, pp. 114-121.

[8] J. A. Emerson, J. N. Sweet, D. W. Peterson, "Evaluating Plastic Assembly Processes for High reliability Applications Using HAST and Assembly Test Chips", *Proc. of 44th Electronic Components & Technology Conference*, 1994, pp. 191-195

[9] J. V. Beck, K. J. Arnold, Parameter Estimation in Engineering and Science, John Wiley, NY, 1977.

[10] E. Gonno, G. Deleuze, M. Brizoux, C. Robert, "Bayesian Approach of Failure Rate Estimation in Field Conditions Through Accelerated Testing", *Proc. of 43rd Electronic Components & Technology Conference*, 1993, pp. 116-123.

[11] J. V. Beck, K. J. Arnold, Parameter Estimation in Engineering and Science, John Wiley, NY, 1977., pp. 158-165.

[12] W. Nelson, op cit. , pp. 76-77..

[13] C. G. Shirley, C. E. C. Hong, "Optimal Acceleration of Cyclic THB Tests for Plastic-Packaged Devices", *Proc. 29th Annual Reliability Physics Symposium*, IEEE, 1991, pp. 12-21.

[14] C. Kittel, H. Kroemer, Thermal Physics, 2nd Ed., W. H. Freeman, 1980, pp. 266-272

[15] M. Pecht, "A Model for Moisture Induced Corrosion Failures in Microeoelectronic Packages", *IEEE Trans. Components, Hybrids, Mfr. Technol.*, Vol. 13, 1990, pp. 383-389.

[16] *RwoH Semi-Annual Technical Report*, MCC Technical Report HHVE-198-92(Q), Microelectronics and Computer Technology Corp., 1992, Section 4.3, "Modeling and Predicting (Lehigh)",pp. 63-67.

[17] A. G. Sabnis, VLSI Reliability, *VLSI Electronics Microstructure Science, Vol 22*, Academic Press, San Diego, 1990, see p. 165 and chaps. 3-6.

[18] C. G. Shirley, "THP Reliability Models and Life Prediction for Intermittently-Powered Non-Hermetic Components", *Proc. 32rd Annual Reliability Physics Symposium*, IEEE, 1994, pp. 72-78.

[19] D. S. Peck, "Comprehensive Model for Humidity Testing Correlation", *Proc. 24th Annual Reliability Physics Symposium*, IEEE, 1986, pp. 44-50.

[20] O. Hallberg, D. S. Peck, "Recent Humidity Accelerations, A Base for Testing Standards", *Quality and Reliability Engineering International*, Vol. 7, 1991, pp. 169-180.

[21] *RwoH Semi-Annual Technical Report*, MCC Technical Report HHVE-088-92(Q), Microelectronics and Computer Technology Corp., 1992, Section 4.3, "Modeling and Predicting (Lehigh)",pp. 82-88.

[22] C. G. Shirley, J. T. McCullun, "Component Reliability", *45th Electronic Components & Technology Conference Technical Seminar*, 1995, p. 53

[23] C. G. Shirley, M. Shell-DeGuzman, "Moisture-Induced Gold Ball Bond Degradation of Polyimide-Passivated Devices in Plastic Packages", *Proc. 31st Annual Reliability Physics Symposium*, IEEE, 1993, pp. 217-226.

Task 5

Uniformity of Commercial Molded Products Tested Relative to Weapon Specifications

David S. Shen

I. Objective

The primary objective of this task is to seek out and evaluate the numerous specifications and standards that exist for plastic encapsulated microcircuits (PEM). Specifically, it is to compare and contrast the high reliability specifications used by industry with those of the military. Although it can be argued that the requirements of commercial and military products and processes differ significantly, there are still areas where the two overlap. It is in these areas where using commercial off-the-shelf (COTS) products that have proven reliability and significant cost savings can benefit the Department of Defense (DOD) and the Department of Energy (DOE). This chapter will cover MIL-STD-883D and JEDEC 22-B (replaced by JEDEC 22-A100-A through JEDEC 22-C101) and 26-A.

II. DOD Standards and Specifications

A study of various DOD standards reveals a daunting web of specifications relating to microelectronics and PEMs. Some of the more applicable standards include:

MIL-STD-883	Test methods and procedures for microelectronics
MIL-I-38535	General specification for integrated circuits manufacturing
MIL-HDBK-217	Reliability model
MIL-I-19500	General specification for semiconductor devices
MIL-I-38534	General specification for hybrid microcircuits
MIL-I-38510	General specification for microcircuits

A. MIL-STD-883D

MIL-STD-883 establishes uniform methods, controls, and procedures for testing microelectronics devices suitable for use within military and aerospace electronic systems including environmental, mechanical, and electrical tests. It was intended to describe in one standard all of the test methods of a similar character which now appear in the various joint-services and NASA microelectronics device specifications. Although intended primarily for devices utilizing hermetic (ceramic) packaging, some of the test

methods in MIL-STD-883 are directly applicable to plastics. Thus, it has been widely cited as a de facto military standard for PEMs. Unfortunately, it fails to address the reliability and failure mechanisms unique to plastic devices.

MIL-STD-883 is itself a massive document encompassing 105 test methods over 652 pages. Among these tests, several are cited in this study which have similarities with commercial specifications. They are listed in Table 5.1.

Method Number	Test Description
1004.7	Moisture Resistance
1005.8	Steady State Life
1008.2	Stabilization Bake
1010.7	Temperature Cycling
1011.9	Thermal Shock
1015.9	Burn-In Test
1016	Life/Reliability Characterization Tests
2009.9	External Visual
2010.10	Internal Visual (Monolithic)
2012.7	Radiography
5005.13	Qualification And Quality Conformance Procedures

Table 5.1. Selected tests in MIL-STD-883D[1].

As stated previously, the purpose of these tests and specifications is to establish a uniform set of test methods, controls, and procedures to qualify microelectronics devices for use within military applications. Unfortunately, these specifications can prevent the adoption of continuous improvements and the use of state-of-the-art technologies by manufacturers that consistently produce high quality, high reliability components. This can be attributed to the added cost and time required to meet these specifications with each incremental improvement. Table 5.2 illustrates the additional costs and times for a few common integrated circuit (IC) devices..

Device	Part Number	Price	Discriminator	Lead Time (weeks)
Memory 28ns LSI Error Detection and Correction	IDT7140LA45FB	$129.56	883	8-10
	IDT7140LA45J	$22.50	Plastic Commercial LCC	4
Logic 45ns LSI Dual Port RAM	Am29C660B/BZC	$87.10	883	4
	Am29C660BJC	$34.47	Plastic Commercial	2
Analog SSI Dual Line Driver	SNJ55110AJ	$4.13	883	10
	SN75110AN	$0.65	Plastic Commercial LCC	6

Table 5.2. Costs and Lead Times for Common IC devices[2].

The additional costs and lead times aside, of greater concern is the limited availability of new devices in traditional hermetic packages. As more and more manufacturers switch production and processes to PEMs, the costs and times to deliver hermetic packages will become even more prohibitive. The critical issue then becomes the extent to which PEMs can maintain reliability in the harsh, long-term environments typical of military and aerospace applications. Industry, in an effort to develop uniform standards and qualify PEMs in high reliability systems, has begun to establish specifications and effective screening methods that address plastic packages. These standards are discussed in the next section.

III. Commercial Standards

The manufacturing base of plastic devices is estimated at greater than 98% of all integrated circuits produced.[3] This transition from hermetic to plastic packaged devices is due largely to the lower cost, lower size and weight, and increasing ease of manufacturing of PEMs. As in most industries, high volume production allows manufacturers to institute statistical process control (SPC) and total quality management (TQM) procedures leading to continuously increasing yields, quality and reliability. This is very similar to the qualified manufacturers list (QML) specifications set forth in MIL-I-38535. In addition to manufacturing improvements, there have also been significant improvements in materials and handling of PEMs. These include the reduction of ionic contaminants on die and in the plastic molding compounds; improvements in die passivation to minimize pin holes and defects; improvements in lead frame and chip pad surface treatment and design; and the use of additional coating to prevent moisture ingress. The sum of the improvements has led to levels of quality and reliability that meet and even surpass comparable hermetic devices. Unfortunately, the wide acceptance and use of PEMs in high reliability systems has also led to individualized standards and specifications. In an effort to bring uniformity to plastic standards, the Electronic Industries Association (EIA) and the Joint Electron Device Engineering Council (JEDEC) produced a series of test methods intended solely for PEMs.

A. JEDEC 22-B (JEDEC 22-A100-1 through JEDEC 22-C101)

JEDEC 22 was an attempt by the EIA to describe in one standard, test methods of a character similar to those which now appear in the various device specifications, so that these methods may be kept uniform.[4] The first iteration of JEDEC 22 focused on test methods and procedures for solid state devices used specifically in transportation and automotive applications. The goal was to specify suitable laboratory conditions at the device level that could be correlated to conditions existing in the field. Unlike MIL-STD-883, however, these tests were designed to address the failure modes and reliability issues specific to PEMs. Some of the tests are listed in Table 5.3.

Test Method (All are EIA/JESD 22)	Test Description
A100-A	Cycled Temperature Humidity Bias Life
A101-A	Steady-State Temperature Humidity Bias Life
A102-B	Accelerated Moisture Resistance
A103-A	High Temperature Storage Life
A104-A	Temperature Cycling
A106-A	Temperature Shock
A108-A	Bias Life
A110	Highly Accelerated Stress Test (HAST)
B101	External Visual

Table 5.3. Selected Tests in JEDEC 22-B.

B. JEDEC26-A

The need to establish a test methodology for PEMs operating in harsh environments led to the adoption of JEDEC 26-A, a General Specification for Plastic Encapsulated Microcircuits for Use in Rugged Applications.[5] The standard established uniform procedures and defined general requirements for the quality and reliability assurance of PEMs. JEDEC 26-A utilizes the tests outlined in JEDEC 22 in specific test sequences and sample sizes to allow for qualification and periodic process control monitoring.

Although commercial standards for high reliability PEMs seem well suited to qualifying PEMs for certain military applications, simply relying on commercial specifications and purchasing COTS devices is not a realistic solution. A uniform standard is needed which will address the unique applications of PEMs in the DOD/DOE and commercial industries. The formation of JEDEC, which includes military, industrial, and academic members, is a step in the right direction.

IV. Comparisons

Although the focus tends to be on the differences between military and commercial standards, there are actually numerous similarities which can serve as a foundation for specifications that meet the needs of the DOD/DOE and industry. The table below compares various test methods outlined in MIL-STD-883, JEDEC 22-B/26-A, and the Plastic Package Availability (PPA) Program sponsored by the Defense Logistics Agency (DLA).

Table 5.4 illustrates that the differences in test standards are subtle.

Test Description	MIL-STD-883D	JEDEC 22-B/26-A	PPA Program
Temperature Cycling	Method 1010.7 (A) -55C to 85C (B) -55C to 125C (C) -65C to 150C	Method 104-A -40C to 125C	-65C to 150C
Thermal Shock	Method 1011.9 (A) 100C / 0C (B) 125C / -55C (C) 150C / -65C	Method 106-A (A) 85C / -40C (B) 100C / 0C (C) 125C / -40C (D) 150C / -50C	-65C to 150C
High Temperature Storage Life	Method 1008.2 100C for 1000 hours	Method 103-A 150 C for 1008 hours	175C for >1000 hours
Cycled Temperature Humidity Bias Life	Method 1004.7 25C to 65C 80% to 100% RH	Method A100-A 30C to 65C 90% to 98% RH	N/A
Mechanical Shock	Method 2002.3 (A) 500 g for 1.0 msec (B) 1500 g for 0.5 msec	Method B104 (A) 500 g for 1.0 msec (B) 1500 g for 0.5 msec	N/A
Biased Humidity Life	N/A	Method A101-A 85C/85% RH 1000 hour	85C/85% RH
Bias Life	Method 1005.8 125C for 1000 hours	Method A108-A 125C for 1000 hours	125C for 4000 hours
External Visual	Method 2009.9	Method B101	

Table 5.4. Comparison of Various Test Methods and Standards

V. A New Perspective

In June of 1994, Secretary of Defense William Perry issued a memorandum which stated a new policy to streamline DOD purchasing practices and procedures. The purpose was to leverage the use of best commercial practices and where appropriate, commercial parts to reduce the cost of military systems, while maintaining comparable levels of quality and reliability. In particular, there was a push for the System Program Offices (SPO) to use PEMs in military applications using commercial specifications. Additionally, the DOD is in favor of a process that requires justifying the use of a military standard when a comparable commercial specification is available.

The solution could be the use of best practices in the selection and use of PEMs. The selection of qualified manufacturers and devices is the key element in successfully utilizing PEMs. As noted before, this process was primarily governed by MIL-STD-883 and MIL-I-38535 in the

past, but more emphasis is now being placed on commercial specifications. Benefits to adopting a best practices solution include the elimination of multiple and costly audits of vendor/technology combinations and an improvement to system quality and reliability. A standardized evaluation process, similar to the one shown in Figure 5.1, can be used to select PEMs for military applications. The flow is not covered in-depth in this paper but is thoroughly discussed in reference [6].

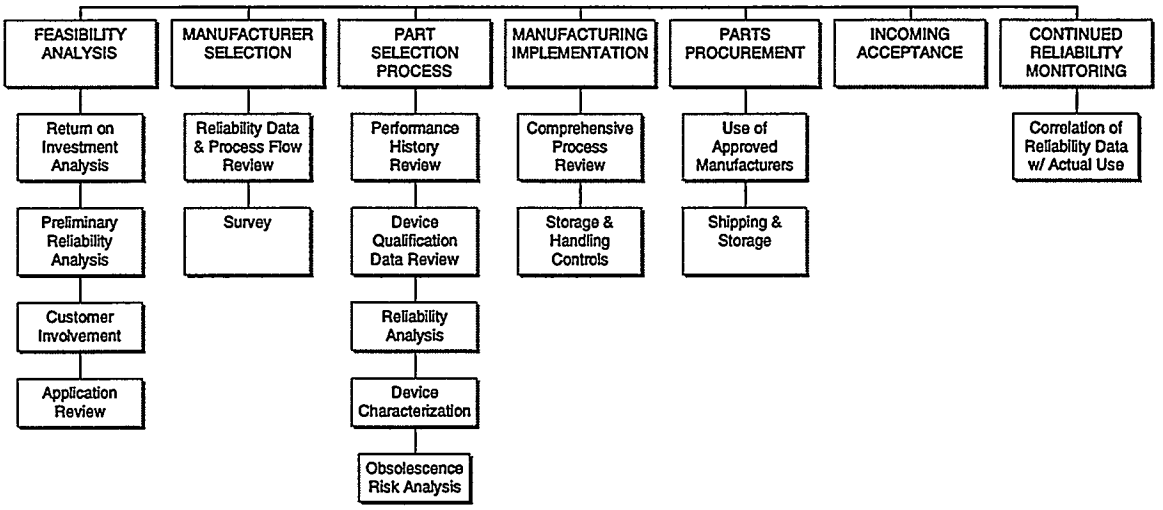

Figure 5.1. PEM Usage Implementation Process Flow[6].

As hermetic devices become more costly and less available, the need for integrated circuits in military applications will have to be met using qualified PEMs. Today, it is not uncommon to find PEMs operating in harsh environments including automotive, avionics, and space without any degradation in quality or reliability. The use of military standards in the near term seems certain but a transition to best practice commercial specifications will be necessary to meet the cost, time, availability and reliability goals of future DOD and DOE applications.

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[1] MIL-STD-883D, "Test Methods and Procedures For Microelectronics", Information Handling Services, DODSTD Issue 96-04.

[2] "Procuring and Using Plastic Encapsulated ICs," CALCE Electronic Packaging Research Center, University of Maryland. June 1993.

[3] "Components Engineering Best Practices; Selection and Use of Plastic Encapsulated Microcircuits," Lockheed Martin. November 1995.

[4] JEDEC Standard No. 22-B, "Test Methods and Procedures for Solid State Devices Used in Transportation/Automotive Applications," Electronic Industries Association. September 1987.

[5] JEDEC Standard No. 26-A, "General Specification for Plastic Encapsulated Microcircuits for Use in Rugged Applications," Electronic Industries Association. April 1990.

[6] "Components Engineering Best Practices; Selection and Use of Plastic Encapsulated Microcircuits," Lockheed Martin. November 1995.

Task 6

Comparison of Commercial and DoD Field Failures

James T. Hanlon

I. Objective

The objective of this task was to compare field failure rates experienced by DoD systems using ceramic encapsulated, hermetically sealed integrated circuits to field failure rates experienced by commercial systems using plastic encapsulated parts.

II. AT&T Field Experience

During FY 93 and 94, Sandia sponsored a program at AlliedSignal Federal Manufacturing & Technologies (AS/FM&T), *AT&T Component Evaluations,* in which SNL and AT&T were participants. During this project, Mike Luvalle, Chun K. Chan and Michael Tortorella of Bell Laboratories researched and summarized AT&T field reliability experience with "WP components." These are commercial (as opposed to Mil Spec) components obtained through AT&T's Total Quality Management Program. In particular, WP integrated circuits are all plastic encapsulated.

Early in this study, LuValle made a comparison between the failure modes seen in an AT&T system built primarily with straight commercial parts, with some WP and KS (AT&T equivalent to SA(Sandia Apparatus)) parts and data from our stockpile surveillance failure mode data base. Mike concluded that, "A statistical test for a difference in the pattern of failures ... in both databases implies that there is no statistically discernible difference between the way failures that occur distribute themselves across the failure modes." In layman's words, to the accuracy available, the distribution of failure modes in our stockpile components, including hermetic, ceramic IC's, is the same as that found in straight, commercial parts.

Chan and Tortorella developed field failure statistics for WP components operating in controlled, central office and uncontrolled, remote terminal operating environments. Because of the limited amount of data available and the low failure rates found, they were not able to distinguish a significant difference between failure rates in the two environments. Nor were they able to find a significant, storage-related failure rate difference between components with mean installation wait times of 120 and 400 days.

They compared their findings in the AS/FM&T study to Rome Air Development Center (RADC) published, non-operating failure rates for JAN Mil-grade (ceramic, hermetic) parts[1], shown in the following table.

Table 6.1. Non-operating Failure Rates for Various Components. [1]

(1 FIT = 1 Failure in 10^9 Hours)

Component Type	JAN Mil-Grade Non-Operating Failure Rates (RADC-TR-85-91), FIT
Digital TTL SSI	1.7
Linear IC < 30 transistors	5.6
Silicon Transistor	1.5
Silicon Diode	2.5
Resistor	0.3
Capacitor	1.2

Unfortunately, the AT&T failure rate information is proprietary and cannot be released outside of Sandia Labs. It is published, along with additional information, in Sandia Report SAND95-0723, "Factory and Field Data on AT&T WP Components."[2] It can be said here that the WP component operating failure rates on these same groups of components are quite similar to the Mil-Grade non-operating failure rates.

Using the Peck model[3], an acceleration factor of 2 was found to relate the AT&T 60°C, 30% RH operating conditions to 35°C, 80% RH non-operating storage conditions. That is, the failure rate of a part in storage would be twice that of a part in the operating environment. Chan and Tortorella concluded from their study that the failure rates for WP (commercial, plastic encapsulated) and JAN Mil-Grade components is comparable in both operating and storage environments.

III. Honeywell Field Experience

Honeywell is a major player in the commercial and military avionics systems business. They have about 60% of the commercial market share, supplying product to Boeing, Airbus, Douglas and other commercial and business aircraft manufacturers. In conjunction with the tri-service sponsored Plastic Package Availability Study[4], they analyzed data from a commercial avionics system that they first fielded using Mil-Std-883B grade, hermetic integrated circuits and then, in 1990, switched to the equivalent, commercial plastic integrated circuits. The typical air transport requirement has systems operating 8 hours per day in the air, 315 days a year in 3g Vibration, ambient temperatures from -40 to +70° C (parts temperatures to 90°C), and humidity 0 to 100%. Intended product life is 20 years.

John Fink from Honeywell presents the following comparison of commercial plastic IC's and Mil-Std-883B grade IC's from that study.

Table 6.2. Commercial Plastic vs. Mil-Std-883B Ceramic Field Failures. [4]

Device Grouping	Hermetic 50% χ^2 Failure Rate/Million Op. Hrs.	Plastic 50% χ^2 Failure Rate/Million Op. Hrs.	Plastic/Ceramic Ratio
Digital SSI/MSI	0.0167	0.0109	0.52
Digital µProcessor/Memory	0.2017	0.1462	0.45
Linear	0.0156	0.0257	1.65

Note that a Plastic/Ceramic Ratio < 1 means that the plastic parts had a lower field failure rate than the ceramic parts. John's statistician tells him that the difference in individual data on each device grouping is not significant. However, the overall system average failure rate is significantly lower when using plastic parts.

IV. IT&T Aerospace experience

ITT[5] has designed, built, and is now successfully shipping SINCGARS, a ground mobile and Army helicopter airborne radio system, and MINTERM, an analog and digital voice and data encryption device for ground mobile service, using production hardware populated with non military components. Both of these programs had formerly been built with military components. Use of selected commercial parts from qualified manufacturers is transparent in manufacture. System failure rates in pilot evaluation are half that predicted by Mil-Handbook-217. There are no field failures in 16K and 15K operating hours respectively. Performance, quality and reliability using commercial parts is transparent.

V. General Dynamics experience

General Dynamics[6] is also making SINCGARS. They have established a parts control program, qualified suppliers and done over 9 million hours of qualification testing. Like ITT, they are using primarily commercial parts rated from -25 to +85 or -40 to +85°C and lot sampling to assure that they meet the wider limits required. They find that careful program planning and execution coupled with extensive system level testing of components provides Best Commercial Practice (BCP) parts that perform as well in the operating environment as and are more reliable than their traditional military counterparts and result in from 50% to 70% cost savings. Their lab test mean time before failure (MTBF) experience for this unit is "above the growth line" predicted from another radio they build with all Mil-Spec parts.

They are designing GDLS SINCGARS SIP, an improved version, with 95% commercial components, mostly surface mount, and their early MTBF testing demonstrates that it is at least as good as a radio built from Mil-Spec parts.

VI. Rockwell/Collins Avionics experience

Rockwell/Collins[7] Tri-Service Precision Lightweight Global Positioning Receiver (PLGR) made from surface mount, commercial PEM's, initially went to the field in 9/93. There were 35K units in service by their summer of 1995 report. Environmental requirements include -20° to +70° C (but they operated to -40° C at last year's Winter Olympics), humidity, vibration, and salt fog. Reliability has been demonstrated by the US Army, with an 11,514 hour point estimate for MTBF (based on 1 observed failure). Cost savings were 8.5:1 over mil screened parts, but use of mil parts would require redesign for through-hole technology and increase the unit size. No formal qualification process was used on suppliers, they were selected on basis of experience. After 254 million component hours, the Worst Case Failure Rate (counting 38 ASICs whose FMA is in progress as all bad for total of 46 PEM failures) produces a rate of 0.181 failures per million operating hours. This is at least 60% lower than Mil-Handbook-217H prediction. Overall failure level is approximately equal to that predicted for Mil screened parts.

VII. Lucas Electronics experience

Lucas Electronics[8] is a large, multinational company located in Birmingham, England, with 46,000 employees. It does $860 million business in aerospace and $2900 million in automotive sectors. Lucas makes electronic control systems for civil airplane engine control (in ceramic, Mil Spec parts) and for automotive engine control (in plastic commercial parts). Automotive environments are comparable to airplane environments, and Mil-Spec and plastic commercial component failure rates are also comparable (0.01 to 0.04 failures per million operating hours). Lucas is evaluating plastic encapsulated devices for use in aerospace systems.

VIII. Rome Laboratory, Reliability Analysis Center, experience

Dan Fayette of (Air Force) Rome Laboratory[9] reported (at the 1996 Advanced Electronics Acquisition, Qualification, and Reliability Workshop, 8/21/96) on their Best Commercial/Industry Components and Practices Initiative in which they are comparing the reliability of circuit boards assembled using commercial components and processes to those assembled using full Mil Spec components and processes. The boards include RF, digital and analog components using through hole and surface mount packages.

Findings to date are as follows. The Commercial and Military *processes* are effectively the same except for military inspection and burn-in. The resulting boards are comparable in quality and reliability. They are in the process of doing accelerated testing including temperature and humidity soak, vibration, thermal shock and HAST. The performance of commercial and military boards and parts looks comparable, with the exception that commercial, plastic parts subjected to the standard military line, post production temperature shock (-65° to +150° C

thermal shock, 20 cycles) showed some delamination. Moral, don't just continue to use old processes. Dan's current conclusion, in light of Rome Lab's conservative stance, is that it is OK to use commercial, plastic parts in benign system environments.

IX. TI Experience With Plastic and Ceramic Packaged Parts

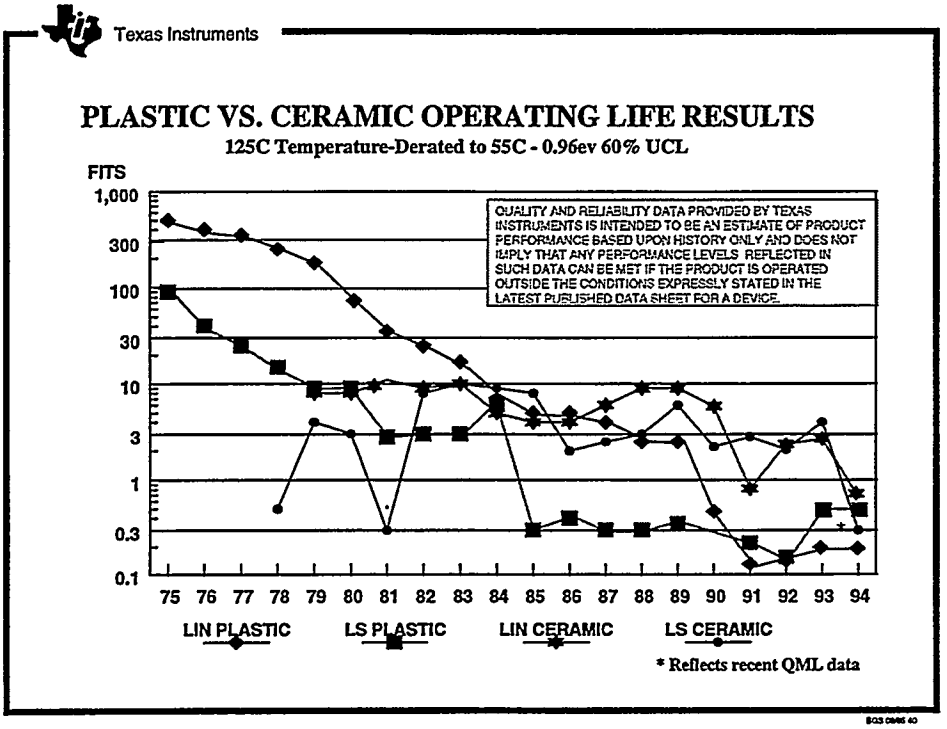

Figure 6.1. Texas Instruments Plastic vs. Ceramic Operating Life Results

Figure 6.1 summarizes Texas Instruments[10] accumulated experience from 1975 through 1994 on accelerated operating life for digital and linear integrated circuits in plastic and ceramic packages. Note that in 1984, LS (TTL logic) plastic crossed over LS ceramic and has been consistently better since that time. In 1986, LIN (linear) plastic crossed over LIN ceramic and has been consistently better since that time. In 1994, the failure rates for the ceramic parts made a considerable improvement and essentially merged with the rates for their plastic counterparts. This coincides with the change from QPL, where the product was made on separate military production lines controlled by DESC, to QML where the product was made on commercial lines.

X. A comment on Mil-Handbook-217

The following was contributed by Dr. Michael Pecht, professor and director of the CALCE Electronic Packaging Research Center at the University of Maryland during a course on Advanced Plastic Encapsulated Microcircuits, 3/19/96. Pecht is quite adamant about why some government programs are not using PEMs today. He is a member of the committee that advises on Mil-Handbook-217, so he has first hand experience to speak from. In brief, he presented much evidence and personal experience that Mil-Handbook-217 deliberately underestimates the

true field reliability of PEMs by a factor ranging from 60 to 600, depending upon input parameters. In addition, Mil-Std-454, used by most DoD contractors, ranks Industrial Grade and Commercial Grade ICs as 4th and 5th choices in order of preference and calls them "non-preferred." It does make allowance for their use in "ground, benign environments," but it negates even that concession by requiring that reliability predictions be prepared in accordance with Mil-Handbook-217. This leads military program managers to believe that the risk of using PEMs is too high, much greater than it actually is.

Fortunately, the DoD seems to have realized its mistake. Mr. Decker, Assistant Secretary (Research, Development, Acquisition) signed a new Army Policy on February 15, 1996 which says in part, "...Use of any reliability specification, standard or handbook (military or not) in an RFP, even for guidance, requires a waiver using the existing waiver process for military specifications and standards. In particular, MIL-Handbook-217, "Reliability Prediction of Electronic Equipment", is not to appear in an RFP as it has been shown to be unreliable and its use can lead to erroneous and misleading reliability predictions."

XI. Conclusions

The collective field experience, from both the commercial and military sectors, is unanimous. Wherever modern, BCP plastic parts are used, they are found to be equally as reliable as their Mil-Spec, hermetic ceramic counterparts. This holds true regardless of the environment and the operating duty cycle. Reliability prediction models that portray plastic parts as inferior to hermetic ceramic parts are simply not in touch with reality! The only question that remains unanswered about the use of plastic parts in military applications is their long term dormant storage behavior.

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[1] D. W. Coit and M. G. Priore, *Impact of Nonoperating Periods on Equipment Reliability*, RADC-TR-85-91.

[2] J. T. Hanlon, *Factory and Field Data on AT&T WP Components,* Sandia Report SAND95-0723, May 1995

[3] D. S. Peck, *Comprehensive Model for Humidity Testing Correlation*, International Reliability Physics Symposium, 1986, page 44.

[4] J. W. Fink, Honeywell Inc., Minneapolis, MN, *Honeywell's Experience with Plastic Parts,* Proceedings, 1995 Advanced Technology, Acquisition, Qualification, And Reliability Workshop, pp. 3-20.

[5] Curt Ulliman, and E. Jacoby, ITT Aerospace, Fort Wayne, IN, *ITT's Commercial Parts Program,* Proceedings, 1995 Advanced Technology, Acquisition, Qualification, And Reliability Workshop, pp. 55-74.

[6] F. Fernandez, R. Kempton and F. Smith, General Dynamics, Tallahassee, FL, *SINCGARS Best Commercial Practices (BCP) - The Next Generation,* Proceedings, 1995 Advanced Technology, Acquisition, Qualification, And Reliability Workshop, pp. 75-81.

[7] D. A. Emerson, Rockwell Collins Defense Electronics, Cedar Rapids, IA, *Plastic Encapsulated Microcircuit (PEM) Reliability and Cost Effectiveness Study,* Proceedings, 1995 Advanced Technology, Acquisition, Qualification, And Reliability Workshop, pp. 21-30.

[8] Dr. R. M. Newman and C. Hughes, Lucas Electronics, United Kingdom, *Civil Engine Control - The Challenge for Plastic Packaging,* Proceedings, 1995 Advanced Technology, Acquisition, Qualification, And Reliability Workshop, pp. 31-44.

[9] D. F. Fayette, J. Reilly, N. Koziarz, B. McKinney, J Nagy, and D. Gilmour, Rome Laboratory, and K. Martin, Maden Tech Consulting, Inc., *Assessing Best Commercial/Industrial Components and Practices for Air Force/DoD Systems,* 1996 Advanced Technology, Acquisition, Qualification, And Reliability Workshop, presentation 2.6.

[10] This figure supplied by Joe V. Chapman, Government Relations/Facilities Manager, Military Products, Semiconductor Group, Texas Instruments.

Task 7

Commercial IC Product for Accelerated Aging

James T. Hanlon

I. Objective

The objective of this task was to obtain commercial integrated circuit (IC) product in plastic molded packages and perform accelerated aging to establish methods for fixtures, data handling, failure analysis, and part traceability.

II. Choice of IC Product

The product identified for this task, after some negotiation, was a 1 Mb, Static Random Access Memory (SRAM). The choice of SRAM was recommended by our systems sponsors as something likely to be used in a Sandia design. It is also a highly testable structure; failures can be mapped to individual word and bit lines, cells, and transistors.

Sandia has a contract with Unisys for the use of their component engineering Commodity Management Organization. We obtained a recommendation from Unisys that we use either Motorola's MCM69P618 or IBM's IBM041813PQK. Both are 64K x 18 Pipelined, Synchronous Burstable Fast Static RAM. They are supplied in a 100 pin, Thin Quad Flat Pack (TQFP) package. Unisys has successfully completed all of the work necessary to qualify both of these products. The only step remaining for complete Unisys qualification is for their utilization in system design. Data sheets for both are available.

Because of budget limitations, commercial devices were not procured and accelerated aging was not performed

III. Recommended Accelerated Aging Sequence

There are several studies being run on the long term dormant storage behavior of PEMs at this writing. The one formulated by Northrop-Grumman and the Computer-Aided Life-Cycle Engineering (CALCE) Electronic Packaging Research Center (EPRC) at the University of Maryland is closely aligned to the concept of our project. It is described as "...a plan to develop acceleration transforms for highly accelerated temperature-humidity stress testing of PEMs under non-operating conditions. A design of experiments analysis will be conducted. Root-cause analysis will be conducted on all failures to identify the failure site, failure mode and failure mechanism. Physics-of-failure based acceleration transforms will be developed for metallization corrosion failures, which will account not only for the effects of the elevated temperature-humidity environment, but also for the damage from temperature cycling and assembly and for the effects of package construction. In this study, parts will first be preconditioned as in assembly and then exposed to a simulated long term storage environment consisting of HAST, temperature cycling, and salt fog exposure." The Northrop-Grumman/CALCE experimental design is outlined fully in documents available from J. T. Hanlon.

Because this plan is supported and ongoing, I have recommended that the accelerated aging sequence performed in our task be aligned with that of the Northrop-Grumman/CALCE study. They are willing to perform the various C-SAM and E-SEM inspection steps on our parts. At the end of the study, we would share our data to the mutual benefit of all concerned. Accelerated tests have already begun at this writing, and they plan to complete their final acceleration model by December, 1997 and to distribute a final report by June, 1998.

CALCE has invited Sandia to become a Sponsoring Member of this project for a $50K contribution. They have made me a member of their "Technical Advisory Panel." Especially in light of the lack of support for our internal study next year, it would certainly be in Sandia's best interest to become a Sponsoring Member of the CALCE/Northrop-Grumman project!

IV. A Brief Survey of Other Studies Under Way on Long Term Dormant Storage of Plastic Encapsulated Microcircuits

In addition to the CALCE/Northrop-Grumman project, there are other ongoing programs looking at dormant storage reliability of PEMs at CALCE; John Hopkins University, Applied Physics Laboratory (the Navy F/A-18 Program); Naval Weapons Center, China Lake; Texas Instruments; TRW; Midsco; and by the U.S. Army Missile Command, MICOM, Redstone Arsenal.

The following CALCE studies, A through E, were reported in the notebook furnished with the CALCE Short Course, Plastic Encapsulated Microelectronics, March 19-20, 1996.[1]

A. CALCE Study of Parts Stored at Distributor

CALCE studied a group of 20 plastic dual in-line packages (DIPs) and 30 ceramic DIPs that had been stored for 12 years on grounded shelves in ESD packing in a distributor's warehouse in Massachusetts, heated in winter but not cooled in summer. The environment was 20° to 40°C, 20% to 100% RH in the summer and 15° to 20°C, 20% to 100% RH in the winter. There was no moisture protection for the parts, and they were never operated. The ceramic DIPs were 3 different devices from 2 different manufacturers. Seven of the 30 ceramic DIPs had visible lead seal fracture, one of these failed gross leak test, but all of them passed functional electrical test. The plastic DIPs did not exhibit visual cracking and passed functional testing. There was no delamination at the epoxy-to-die interface, but some between the leadframe and the epoxy. This delamination is associated with the lead frame trim and form operation of the era, which has since been improved. The plastic DIPs exhibited no evidence of metallization corrosion, metallization defect formation, wire fatigue, or die cracking.

B. CALCE Study of Parts Used/Stored in Commercial Electronic Assemblies

CALCE obtained 10 television circuit board assemblies produced between 1983 and 1986 with 2 plastic DIPs and many passive components and connectors on each assembly. These had been operated for 3 to 6 hours per day, for 10 to 13 years, in an average relative humidity of 70%, between -18° and +37°C ambient temperature. The boards were not moisture protected, and there was dirt and oil present to some extent on all of them. In addition, there were 2 more boards of the same description that had not been

operated. Damage found on the boards (FR-1 paper phenolic and very moisture absorptive material) included copper trace delamination, solder fatigue, microstructural coarsening in solder joints, and an increase in connector contact resistance. The plastic DIPs did not exhibit package cracking, delamination at the epoxy-die interface, wire fatigue, die cracking, or intermetallic formation. They were subjected to accelerated aging (temperature cycle and HAST) to bring them to the equivalent of 20 years life. At that point there was no additional delamination, but some evidence was found of electrochemical migration (dendritic growth), stress driven diffusive voiding, and Kirkendall voiding.

C. CALCE Study of Remanufacturing Center Parts

CALCE obtained 52 plastic DIPs of two types with 1992 date codes from the DELCO Remanufacturing Center that had been stored outdoors in open sheds in Kokomo, Indiana. This facility experienced diurnal temperature swings between 15° and 35°C and average daily temperatures between 20° and 24°C, 45% to 85% in the summer and between -4° to 10° C, 32% to 70% RH in the winter. These parts were selected in order to give a good representation of the effects of long term storage on very current technology. There was leadframe/encapsulant delamination in 4 of these parts and encapsulant/top-of-die delamination in one as found using C-SAM. There was no evidence of package cracking or corrosion, wire or wirebond failure, or excessive intermetallics.

D. CALCE Sonobuoy Study

CALCE obtained a total of 44 Sonobuoys manufactured with plastic DIPs in 1984, 1989, 1992 and 1994. The 1984 units had been stored for a year in a controlled warehouse in Virginia, then shipped and trucked to a storage warehouse in Norway for 8 years of storage, and finally returned by ship to Crane, Indiana via Norfolk, Virginia, where they were stored outside in containers exposed to the environment. The 1989 units had been stored in a controlled warehouse in Virginia for 6 years and then returned to Crane where they were stored outside in containers. The 1992 and 1994 units were stored in a controlled warehouse.

Sonobuoy boards were visually examined and cross-sectioned for board and metal delamination, solder joint cracks, and corrosion. One, seven year old board stored in Norfolk and Crane exhibited corrosion, no other failures were found. Seventy nine parts of five types removed from sonobuoys passed functional electrical testing.

E. CALCE Study of Automotive Assemblies

John Fink of Honeywell supplied CALCE with four automotive electronics assemblies that came from 1982 model cars found in a Minnesota junk yard. Presumably, these saw both thermal cycling, humidity and salt spray during life. CALCE found no evidence of corrosion on the PEMs from these boards.

F. John Hopkins University, Applied Physics Laboratory, Navy F/A-18 Study of Long Term Dormant Storage of Plastic Encapsulated Microcircuits[2]

The Navy F-18 carrier aircraft uses PEMs in its Inertial Reference GPS box and in its Radar. In use, these parts will be powered only about 9% of the time, so the Navy is concerned about their long term reliability.

The study involved 92 PEMs from 12 manufacturers, both analog and digital, mostly DIPs but one SOIC, with date codes ranging from 1967 to 1994. They had never been installed on boards and were stored in uncontrolled environments. They were given an external visual inspection, X-ray, electrical test, bake out to estimate moisture content, another electrical test, C-SAM exam, and then destructive analysis.

Conclusions are as follows. The older parts exhibited worse external damage. Only 2 PEMs exhibited corrosion, and both were 28 years old. Two exhibited excessive intermetallics, one was 18 years old and the other was 28 years old. The 18 year old with excessive intermetallics passed electrical test. All but 8 exhibited some delamination on C-SAM examination, only one on the top of the die. Corrosion was not observed on this one unit. Delamination was not time dependent. Regardless of age, all parts were saturated with moisture and this bore no relationship to corrosion.

As a result of this study, its author Anthony Casasnovas reported that he was not overly concerned about the dormant storage reliability of plastic encapsulated parts of modern vintage.

G. Naval Weapons Center - China Lake Study[3]

PEMs were installed in a ground tracking IR camera for Tomahawk missiles. No degradation has been found after 6 years of storage in a missile storage environment. No evidence of corrosion has been found in 25 of 25 decapsulated PEMs.

H. Texas Instruments Studies[3]

Study #1 included HAST testing to determine acceleration transforms. Tests were conducted on 1987 datecode TI74LS00N DIPs. Parts were stressed under normal bias, dissipating less than 10 milliwatts of power. 180 units underwent 130°C, 85% RH HAST; first failure occurred after 500 hours, 51% had failed within 2,000 hours. 180 units underwent 120°C, 85% RH HAST, first failure occurred after 1,000 hours, 52% had failed within 4,000 hours. All HAST failures were traced to bond pad corrosion. 180 units have been exposed to 85°C, 85% RH; and 0 of 180 have failed by corrosion after 70,000 hours.

In Study #2, two Circuit Card Assemblies were exposed to: 200 temperature cycles from -55° to +92°C, 336 hours of 85°C/85% RH, 30 operating temperature cycles from -55° to +92°C (under power), and 672 additional hours of 85°C/85% RH. One card was a military type with 34 plastic DIPs from 3 different manufacturers substituted for ceramics. The other was a notebook computer board with 53 PEMs (DIP, QFP, SOJ,

TSOP, TO, SOIC) from 12 manufacturers. All PEMs met the requirements with no degradation.

I. TRW F-22 Study[3]

Nineteen different PEMs from 9 manufacturers on each of 67 boards were subjected to all combinations and permutations of: burn-in at 125°C for 111 to 525 hours, 518 temperature cycles from -65° to +150°C, 96 hours of autoclave at 121°C, 100% RH, 240 hours of HAST at 125°C, 85% RH, 5 volts bias. Some boards were coated with paraline, some with uniseal, some were uncoated. Only one of the 1,273 PEMs in the study, on a uniseal coated board, failed as a result of the environmental exposure. The failure mechanism was bond pad corrosion; delamination and cracking were observed by acoustic microscopy

J. Midsco Study[3]

Fourteen plastic packaged bipolar junction transistors from each of two manufacturers, rated for 0° to 70°C operation, were subjected to 1,000 hours of HAST at 130°C, 85% RH, under 5 volts reverse bias. No changes in V_{CEsat}. Changes in breakdown voltage are statistically insignificant. I_{EBO} stayed below 10 nA. No failures were found.

K. MICOM, Redstone Arsenal Study

The following study was reported by Ronda Brantley at the 1996 Advanced Electronics Acquisition, Qualification, and Reliability Workshop, 8/22/96.[4] Ronda's co-author is Dr. Noel E. Donlin, of MICOM, probably the most outspoken conservative, anywhere, on the topic of plastic package reliability.

The Army-MICOM, Product Assurance Directorate, and Rome Labs are partnering on this study. It consists of storing CMOS CD4011 14 pin plastic DIPs in 5 locations that simulate actual missile system storage environments. These locations are outdoor sheds, where wind and rain may enter, at Redstone Arsenal, Rome Labs, on a PREPO Ship, at Eglin Air Force Base (Florida panhandle), and at the Yuma Proving Grounds. There are 1,500 parts in the study from 5 different manufacturers, installed on circuit cards. The cards are housed in Hellfire missile storage boxes during field exposure. Circuits are electrically tested at -55°, -40°, 25°, 85°, and 125°C. Plans are to test them initially and then at yearly intervals. Parts are transported to and from the test sites by FEDEX.

Initial test showed three margin failures. These units were left in the test. So far, 991 units have been tested at the 1 year point with 6 electrical failures (out of spec). Five of these failures were at 125°, 1 at all temperatures. Three of these parts were baked and retested and passed (it was not reported whether the failure was confirmed after it was found and before bake.) Three others, not baked, were retested and passed. The failed parts have been returned to the test.

They also plan to add plastic LM324 quad op-amps to this program in the future. And they plan to do failure analysis on catastrophic failures and perhaps also on parametric

failures. They decided not to put ceramic parts in the test because they had a good history on them.

L. 1996 Advanced Electronics Acquisition, Qualification and Reliability Workshop - Panel Discussion

Bob Knowl from Ford noted that their automotive electronics are operating in a 10% on, 90% off mode. The major field return categories are Electrical Overstress, Electrostatic Discharge Damage, and No Trouble Found. Intermetallics and corrosion are way down the list. Their environments include hydrocarbon fumes and air pollution gasses, for example 15 years of exposure in Los Angeles. But they get back nothing due to gas contamination. They field 5 to 6 million cars in a year. An engine controller failure rate of 100 ppm would "set off alarms." Their component failure rates are in the single digit ppm level or less. In his experience, PEMs are as good as hermetics. Ford's largest failures are connectors, then circuit board problems.

V. Summary and Conclusions

The original objective of this task was to obtain commercial, plastic packaged IC product and perform accelerated aging on it. Appropriate IC's were identified, but funding was cut off before procurement and the actual aging work was begun.

The Northrop Grumman/CALCE program is closely aligned to the concept of our project, and it actually will wind up testing far more types and variations of commercial IC's than we had planned. Because of that, I had recommended that we adopt their test methodology and share data with them.

In addition to our work, there are many other projects, some currently ongoing, by CALCE, the Navy, TI, TRW, Midsco, and MICOM focused on the long term dormant storage reliability of plastic encapsulated parts. They all involve operating parts, as opposed to Sandia's test chips. Thus far, no catastrophic failure modes suggestive of early end-of-life have been found in any modern PEMs. A definitive, validated acceleration transform for PEMs in dormant storage has yet to be completed, but the Northrop-Grumman/CALCE study promises to have one available by December, 1997.

VI. Recommendations

The Sandia program has an opportunity to make a unique contribution to the body of ongoing work on dormant storage because of the unique sensitivities of our test chips. But whether we are a player or not, the dormant storage question is of such importance to so many military manufacturers and customers that it will be answered, probably in less than two years.

Because of our own vital interests, we need to have these answers properly formulated and directed to DOE weapons systems environmental conditions. We should, at the very least, become a sponsoring member of the Northrop-Grumman/CALCE study so that we can exercise some influence over it. If sufficient funding is available, we should continue our tasks associated with evaluation of Sandia test chips, and if possible take responsibility for some of the test work on commerical IC's for the Northrup-Grumman/CALCE study as well.

[1] As reported in the notebook furnished with the CALCE Short Course, *Plastic Encapsulated, Microelectronics*, University of Maryland, March 19-20, 1996.

[2] A. Casasnovas and J. W. White, The John Hopkins University, Applied Physics Laboratory, *The Navy F/A-18 Program and Plastic Encapsulated Microcircuits: Long Term Dormant Storage Study,* 1996 Advanced Electronics Acquisition, Qualification, and Reliability Workshop, Sponsored by the Army Research Laboratory, Shaumburg, IL, August 21-22, 1996, presentation 3.1.

[3] As reported in the notebook furnished with the CALCE Short Course, *Advanced Plastic Encapsulated Microelectronics*, Shaumburg, IL, August 20, 1996.

[4] R. Brantley and Dr. N. E. Donlin, US Army Missile Command, Product Assurance Directorate, Redstone Arsenal, *MICOM Long Term Dormant Storage in Harsh Environment Program: Concepts and Test Results,* 1996 Advanced Electronics Acquisition, Qualification, and Reliability Workshop, Sponsored by the Army Research Laboratory, Shaumburg, IL, August 21-22, 1996, presentation 3.5.

Task 8

OBTAIN PRODUCT – POTENTIAL WR VENDORS & HERMETIC SOURCE

Donald R. Johnson

I. Objective

The objective of this task was to obtain plastic encapsulated microelectronics representing best commercial practice from three potential WR vendors as well as to obtain the same device from a ceramic, hermetic source.

II. Status

This task would have been initiated late in FY96, and would have essentially been a second year task based on results and information from the work accomplished the first year. Because of budget limitations and the apparent zero funding for FY97, work on the task was not initiated.

III. Summary and Conclusions

The work envisioned for this task must be accomplished prior to the utilization of plastic encapsulated microelectronics for weapon applications. Potential WR vendors must be identified, and their process line and final product qualified through detailed screening and testing.

Task 9

DESTRUCTIVE/NONDESTRUCTIVE TESTING OF PRODUCT FROM TASK 7 & TASK 8

Donald R. Johnson

I. Objective

The primary objective of this task was to perform both destructive and nondestructive testing on the commercial product acquired through preceding Tasks 7 and 8. Results from this would allow identification of screening and qualification procedures that may be necessary for utilization of plastic encapsulated semiconductors for stockpile applications.

II. Status

Because Tasks 7 & 8 were essentially FY97 tasks, and because of budget limitations in the current fiscal year, no actual destructive/nondestructive testing was performed in their behalf. However, in conjunction with Tasks 1 and 5, there was a significant effort expended on determination of what techniques were most frequently used in commercial practice along with what tests were required by similar high reliability applications, albeit industrial or military.

III. Summary and Conclusions

It is mandatory that destructive and nondestructive testing techniques be selected and adapted for specific failure mechanisms and defects at specific defect sites in order to be effectively used for screening and qualification. Both the defects and the defect sites are dependent on the product line and the product processing technology. Parameters for nondestructive evaluation must be chosen so that failures due to overstress occur only at potential defect sites, and so there is minimal effect on the remaining useful life of the component. Failures should be classified as to the failure site, the consequence of the observed failure, and the failure mechanism. This approach is critical for assessing the effect that one failure at a specific site has on other failures at different sites or with different mechanisms.

Task 10

FAILURE STATISTICS VERSUS WEAPON RELIABILITY

Donald R. Johnson

I. Objective

The primary objective of this task was to compare the accumulated failure statistics from the tests conducted in the various evaluation tasks to the requirements for weapon reliability in stockpile.

II. Status

This was a second year task, and not enough testing was conducted during this first year to accumulate sufficient failure statistics.

Task 11

Failure Analysis of Plastic Molded Test Chips

Kenneth A. Peterson

I. Introduction

Plastic-encapsulated ATC2.6 devices which were intended for highly accelerated stress testing (HAST) failed prematurely and were submitted for failure analysis. The package was a 160 lead, gull-wing, surface mount, epoxy-molded quad flat pack. The same package was used for ATC2.5 devices which were studied because of similar failure modes. ATC2.6 devices in 40 pin ceramic dual in-line packages (DIP) were also examined as a way to gain information about the overall mechanisms. The silicon chips were fabricated at Sandia, thinned at an outside vendor, and assembled and molded at another outside vendor.

The failure analysis (FA) approach involved examination of any electrical data supplied, collection of additional data in bench-testing, and decapsulation of the part, followed by specific failure analysis techniques. The FA techniques employed include electrical testing, optical microscopy, ultrasonic imaging, scanning electron microscopy (SEM), voltage contrast (VC), resistive contrast imaging (RCI), fluorescent microthermal imaging (FMI), focused ion beam (FIB) cross-sectioning, and active and passive laser trimming. Further deprocessing of parts for removal of silicon nitride passivation and silicon dioxide dielectric was also performed. Many electrical indications of failure were elusive--disappearing immediately or otherwise changing nature following decapsulation. Mechanical damage to the triple track portion of the circuit appeared to be the primary mechanism for failure, although the causes for such mechanical damage have not been isolated. This damage was gross in early parts, and less severe in later parts. Corrosion of aluminum lines may also account for some of the failures observed.

A typical indication of a problem was that the common pin for the center conductors was shorted to the common pin for the outboard conductors, indicating a breach of the isolation somewhere within the triple track structure. (See Task 1A, Section IV for detail of triple track structure.)

II. FA Technique

A. Electrical measurement of triple tracks

For both device types, the center conductors to all triple tracks were common at the end of the structure which terminated near the center of the chip, and the inner and outer conductors for all triple tracks were common at the same end of the structure. The perimeter traces to triple tracks were pinned-out individually.

In addition to electrical information supplied on breakdown voltages and resistances for center common and outboard common conductors, electrical measurements on individual triple track elements were useful. These consisted of measurements between outside pins connected to individual center and outboard conductors, and measurements from end to end on individual triple track conductors. A schematic of how this was helpful in isolating potential flaws is shown in Figure 11.1.

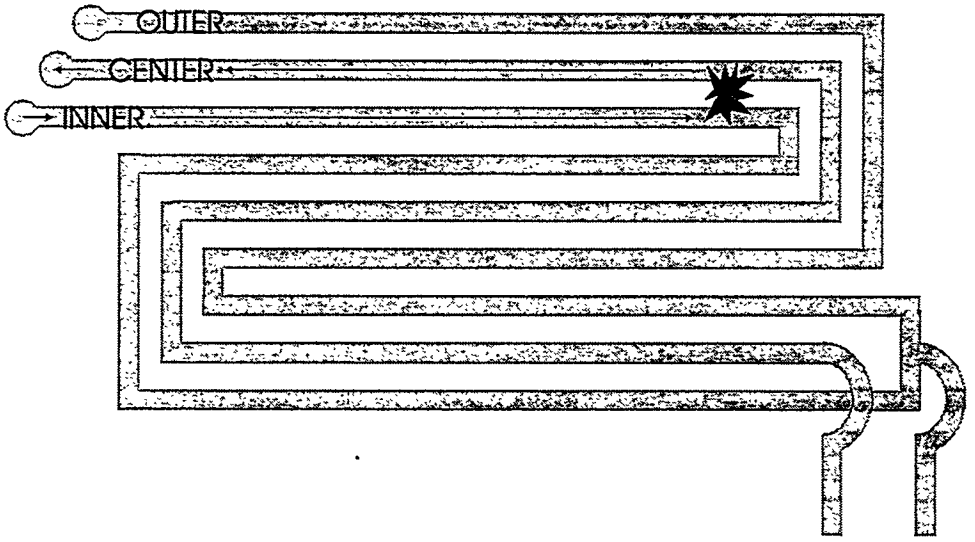

Figure 11.1. Schematic current path for a single short between center and inner conductor in triple track structure.

For the illustrated short between the center and inner conductors, a relatively low resistance was expected, based on the number of squares in the current path. A higher center-to-outer conductor resistance was measured, since the current path consisted of the entire outer conductor to the point where it was bussed to the inner conductor, the inner conductor from this point back to the flaw, and the center conductor from the flaw back to it's i/o pin. This measurement was complicated somewhat by multiple flaws, when present, and was complicated a great deal when the behavior of flaws was altered by decapsulation or subsequent stimulation. A typical assortment of such measurements in Table 11.1 illustrates the utility of this information. Unusual behavior is flagged by underlined, bolded data. Other resistances were the result of current paths through defective triple tracks via the busses.

Table 11. 1 A Sample of Track Resistances Prior-to and Following Decapsulation

Globbed 40DIP ATC2.6 bussed conductors (ALL) and individual center-to-outer/inner (TT#) conductor resistances in K Ω unless otherwise noted.

TT ID#	ALL	ALL	2	2	1	1	8	8	7	7	6	6	5	5	4	4	3	3
PIN ID#	8-13	28-33	1-2	2-3	4-5	5-6	15-16	16-17	18-19	19-20	21-22	22-23	24-25	25-26	35-36	36-37	38-39	39-40
s/n gb128 Pre- Decap	*0.41*	*0.41*	5.7	5.7	5.8	5.8	5.7	5.7	5.7	5.7	5.7	5.7	5.6	5.6	*0.82*	*4.2*	*400*	*400*
s/n gb128 Post-Decap	4.9	4.9	10.7	10.7	10.8	10.8	10.3	10.3	*8.9*	*8.9*	10.2	10.2	10.2	10.2	*0.90*	*5.75*	OPEN	OPEN
s/n gb131 Pre- Decap	*1.0*	*1.0*	6.2	6.2	4.3	5.3	6.2	6.2	6.2	6.2	6.3	6.3	6.3	6.3	6.3	6.3	6.3	6.3
s/n 1gb31 Post-Decap	OPEN	1.07	6.7	6.7	*4.6*	OPEN	6.3	6.3	6.3	6.3	6.4	6.4	6.4	6.4	6.8	6.7	6.8	6.7
s/n gb132 Pre- Decap	*0.47*	*0.46*	5.7	5.7	5.8	5.8	5.7	5.7	5.7	5.7	5.7	5.7	5.7	5.7	5.7	5.7	5.3	4.9
s/n gb132 Post-Decap	*0.06*	*0.06*	*0.22*	*0.47*	*4.4*	*0.33*	5.3	5.3	5.3	5.3	5.4	5.4	5.4	5.4	5.8	5.7	*6.2*	*4.0*
s/n gb133 Pre- Decap	*2.9*	*2.9*	8.2	8.2	*280*	8.2	8.2	8.2	8.2	8.2	8.3	8.3	8.3	8.3	8.2	8.2	*2.6*	*5.4*
s/n gb133 Post-Decap	*1.7*	*1.7*	*1500*	*0.96*	*55.0*	7.5	7.0	7.0	7.0	7.0	7.1	7.1	7.1	7.1	*1000*	*7.4*	OPEN	*5.5*
s/n gb134 Pre- Decap	*3.5*	*3.5*	8.8	8.8	8.9	8.9	8.8	8.8	8.8	8.8	8.8	8.8	8.8	8.8	8.7	8.7	*5.3*	*1.8*
s/n gb134 Post-Decap	*2.5*	*2.5*	11.0	11.0	11.1	11.1	10.5	10.5	10.5	10.5	10.5	10.5	10.5	10.5	110.	10.9	OPEN	*3.4*
s/n gb135 Pre- Decap	*3.1*	*3.1*	8.9	8.9	8.9	8.9	8.8	8.8	8.8	8.8	8.7	8.7	8.7	8.7	8.7	8.7	*5.8*	*2.7*
s/n gb135 Post-Decap	*1M*	*2M*	*10M*	OPEN	*10M*	*10M*	*10M*	*10M*	*10M*	*10M*	*10M*	*10M*	*10M*	*10M*	*10M*	OPEN	*10M*	*3.0*

B. Decapsulation of plastic encapsulated devices

Just prior to the first FA, parts were sent to an outside lab for decapsulation in a hot sulfuric acid jet-etcher. The result was a very clean decapsulated part, but visual inspection revealed attack of the aluminum lines in the unpassivated regions of triple tracks, which was unacceptable. A second attempt was made to modify decapsulation conditions to save these fine aluminum traces, but without success.

An in-house technique for decapsulating plastic encapsulated devices employed a B&G nitric acid jet etcher. The technique was developed for ATC04 test chips as well as early ATC2.5's and ATC2.6's.

The plastic part itself made a seal against a rubber gasket which permitted vacuum aspiration of acid against the plastic above the die. An equipment program which worked well for these initial samples included a 30 second warm-up to the 95 C etch temperature, where 25 etch pulses (of ~1 second duration each) were performed, followed by a 30 second rinse. When the machine cycle was complete, parts were removed from the etcher within 6 seconds and immersed in an ultrasonically agitated bath of acetone for about 30 seconds. Following that, parts were rinsed in a secondary bath of flowing deionized water for several minutes, followed by a rinse in the primary bath for 5 to 10 minutes. Thorough drying in a stream of nitrogen was the last step. An example of a very successful decapsulation to the edge of a die is shown in Figure 11.2 on page 11-12.

Several parts were decapsulated for the purpose of wirebond tests. When wirebonds were to be tested, the ultrasonic excitation was replaced by slight manual agitation in a bath of acetone. This reduced the surface cleanliness with respect to residual encapsulant, but removed any confusion associated with possible damage due to ultrasonic agitation of wirebonds.

Occasionally, conditions required an adjustment to this cycle. The most extreme of these changes was for parts exposed to extended high temperature storage, which increased by more than a factor of ten the etching time required to reveal the die surface. In the worst cases, a cycle employing 90 etch pulses was used as many as ten times to clear the surface of the die. In this case, a manual rotary grinder was also employed to remove material overlying the die, prior to the beginning of etching. When the wirebond test was the motive for decapsulation, the end point for the grinding was when the surface of the die at the center was just-touched.

Another technique which showed promise for decapsulating plastic molded parts involved the mechanical separation of the encapsulant from the chip at an elevated temperature. This technique sacrificed the interconnect to the die, and would require probing. The backside of the die was reached in a grinding operation. When the part was heated, the plastic became somewhat pliable and may be manually pried away from the chip surface. This may be useful as a way to preserve the material adjacent to a mechanical defect on the surface of the IC.

C. Decapsulation of Glob-Top devices

Glob-Top devices (fabricated by attaching a test chip in a 40 pin ceramic dual inline package (DIP) and filling the package cavity with liquid encapsulant, which is subsequently cured) were decapsulated using fuming, anhydrous, hot sulfuric acid. A beaker of fuming sulfuric acid was heated at 300 °C for several hours on a hotplate to be sure it was anhydrous. The ceramic DIP part was immersed for a period of 20 seconds. This time was critical, because the die attach polymer was also attacked, and there was some uncertainty about the effect of silver particles on the performance of subsequent failure analysis. While this technique was being developed, some devices were nearly detached from the package. Following the acid immersion, the part was removed for several seconds, which allowed some convective cooling, and rinsed in ultrasonically agitated acetone. Under the best of circumstances, this still constituted a severe thermal quench. As with the molded parts, these globbed parts were also rinsed for several minutes through two deionized water baths and dried in a stream of nitrogen.

D. Delayering of decapsulated devices

Once the IC surface was exposed, it was sometimes helpful to remove the silicon nitride coating and the insulating glass from the IC. The silicon nitride was removed in a reactive ion etcher, using a flow of 25 sccm CF_4 and 25 sccm O_2 for a duration of 5 minutes. Following that, a glass etch at room temperature was performed for two minutes with mild agitation to remove the insulating glass.

E. Isolation of circuit elements using Laser Cutter

The Florod laser in Department 1275 was used to isolate circuit segments for analysis. Triple track lines were usually severed at the extremes where the serpentine doubled back so as not to be above heater lines. One drawback was unintentional laser-induced bridging to heater lines or to the substrate which confused analysis.

III. Results

A. Plastic Molded ATC2.5's

ATC2.5 devices were tested to determine the cause of infant mortality failures which prevented their use in HAST tests. ATC2.5's were completely passivated in the triple track region, so direct contact of encapsulant with aluminum traces was inhibited.

1. S/N SCT115 (ATC2.5)

This sample was supplied as one of the original failures, showing a 1.24 KΩ short between I/OCom-CCom. Following decapsulation in a nitric acid jet etcher, this short was measured at 1.36 KΩ. Electrical measurements with a multimeter indicated that all triple track center terminals showed a similar, albeit high, resistance to the center bus (6.8-7.3 KΩ) except triple track #7, where the resistance was 3.7 KΩ. The circuit was powered at three sequentially increasing voltages, while the whole surface of the die was examined for hot spots, using FMI. Settings of 5 V (3.5 mA), 5.5 V (3.8 mA), and 6 V (4.2 mA) did not produce any hot spots associated with defects. Using the fourth setting, 10V (7.1 mA) resulted in an image with a faint hot spot which did not involve any undesirable change to the sample. This image is shown in Figure 11.3 and the corresponding SEM images are shown in Figure 11.4 and Figure 11.5. This defect was similar to those identified optically on several other samples. A FIB section of this area did not show structure which could identify the origin of this blemish (Figure 11.6).

2. S/N SCT113 (ATC2.5)

Electrical measurements on this part indicated multiple defects in triple tracks which were also mechanically blemished. Laser cutting illustrated that excising suspect triple tracks restored electrical isolation between busses for triple track center and adjacent lines. Extensive cutting was performed to attempt to locate flaws on three triple tracks. Increases and decreases in

resistance illustrated problems cleaning out the kerf of the cut. One defect which was almost certainly a source of electrical shorting could not be isolated by this technique.

3. S/N SCT 108 (ATC2.5)

One defect which was isolated using the laser cutter turned out to be a processing defect, not caused by electrical stress to the part. This defect is shown in a FIB cut image in Figure 11.7. Another processing defect which affected the heater lines and caused several adjacent lines on various samples to stand out in optical examination was observed as shown in Figure 11.8. Using FIB cross-sectioning and imaging, this was shown to be incomplete removal of polysilicon from selected spaces between lines as shown in Figure 11.9. While this did not significantly degrade heater performance, it was important to rule it out as contributing to triple track shorting.

B. Plastic Molded ATC2.6's

One challenge, which suggested additional future work is needed, was the disappearance of shorts associated with triple tracks. These occurred both for plastic molded and for globbed parts. Work on ATC2.6's which were stressed to failure with voltage ramps illustrated this. One part was monitored through the decapsulation process. The original resistance of the failed part at room temperature was 2.78 kΩ. During the etch cycle in the jet etcher, the resistance climbed as high as 3.4 kΩ due to the increasing temperature, and was intermittently open by the end of the acid rinse of a second etch cycle in the etcher. It registered 45 kΩ in the acetone rinse, and rose from 8 kΩ to 34 kΩ as it was rinsed in water. Finally, it registered 58 kΩ as dried. The nitride was then removed in a plasma etcher, following which the short was permanently open. Some shorts disappeared immediately upon decapsulation. Certain shorts were preserved following decapsulation, but were no longer shorted when parts were examined 24-168 hours later. Some parts were seen to open during the testing on individual tracks, first evidenced by a continuously changing resistance, followed by complete open. Some parts opened in a way which suggested that a defect which later became an electrical discontinuity within a track line may have been shorted while the part was encapsulated.

1. S/N SCT08 (ATC2.6)

This sample was supplied as one of the original failures, showing a 1,922 Ω short between I/OCom-CCom. Following decapsulation in a nitric acid jet etcher, this short was measured at 3.6 KΩ. Electrical measurements with a multimeter indicated that all triple track center terminals showed a similar, albeit high, resistance to the center bus (~6,400 Ω) except triple track #1, where the resistance was 1,590 Ω. Optical examination of triple track #2 showed two prominent clusters of damaged lines, but the depth of field was insufficient to get a good look. SEM images of these two areas are shown in Figure11.10, Figure 11.11, and Figure11.12. This type of defect was also seen in triple track #8 on the passivated side of the sample.

An attempt to image a temperature rise from this powered short using FMI at 5V (1.3 mA) was unsuccessful. The voltage was stepped to 7 V, which altered the part and resulted in a current of 7 mA. Another scan was performed at 5V (5.5 mA), resulting in a hot spot being sighted in triple

track #3, shown in Figure 11.13 and Figure 11.14. This manufactured short was different in appearance from the inherent defects seen.

2. S/N SCT09 (ATC2.6)

This sample originally showed a 1.79 KΩ short between I/OCom-CCom, which was measured to be 2.73 KΩ after decapsulation in a nitric acid jet etcher. Measurements showed each triple track center to CCom resistance to be in the vicinity of 8.6 KΩ, except on TT1, where it was 2.15 KΩ. Numerous blemishes were apparent on triple tracks when the sample was observed optically. These blemishes affect areas under glass, whether on the side with passivation cutouts, or on the other side. SEM images of some of these blemishes are shown in Figure11.15, Figure11.16, and Figure 11.17.

An attempt to image a temperature rise from this sample using FMI at 5V (1.8 mA) was unsuccessful. A second scan of the entire die was performed using 6V (2.2) mA, but no signal was observed.

3. S/N SCT58 (ATC2.6)

This sample was stressed by 1333 with the intention of producing a failure. Failure occurred when the voltage was ramped to ten volts, resulting in a 3,670 Ω short between I/OCom-CCom. A second reading was made immediately following decapsulation, which indicated that this trace was open. A subsequent reading in 1275 indicated a 3,685 Ω short. An attempt to image a temperature rise from this powered short using FMI at 6V (1.6 mA) was unsuccessful. The voltage was stepped to 8 V (2.1 mA) for another scan, and then to 10 V (2.7 mA). After a few seconds at 10 V, the part was altered. A subsequent scan at 5V (6.7 mA) revealed a prominent hot spot as shown in Figure 11.18. The corresponding physical location is shown in the SEM image of Figure 11.19, and Figure 11.20. The appearance of this site was not that of the inherent defects which were earlier observed optically.

C. Glob-Topped ATC2.6 Parts

As a check on mechanical damage resulting from the molding process, test chips were supplied packaged in 40 pin ceramic dual inline packages (DIP), where the package cavity was filled with a liquid encapsulant ("glob"), which is subsequently cured. Unexpectedly, these parts also exhibited breakdowns under voltage ramping when tested by 1333. Some of these were analyzed in a batch mode, checking detailed resistances only after decapsulation. Another group was monitored for the effect of decapsulation on performance. A few parts were not analyzed further due to hairline cracks in the ceramic package which was likely due to a thermal shock inherent in the decapsulation process. The main difference in the effect of decapsulation, was the alteration of some shorts to opens. Also, slightly more than 90% of all anomalies which made a trace stand out from the normal traces on a circuit occurred on tracks 1-4, which have passivation openings on the ATC2.6 chip. Fewer than 10% occurred on tracks 5-8, which are completely passivated.

1. S/N gb122

Serial Number gb122 exhibited one misplaced wirebond with a weakened neck region (Figure 11.21) and another broken wirebond, which cannot be separated from decapsulation. It also exhibited several contaminated tracks, both in the unpassivated region and outside as shown in Figure 11.22.

2. S/N gb124

Serial number gb124 broke down at 60V, but changed during decapsulation and indicated problems in tracks 3 and 4, as shown in Table 11.2. The sample was characterized in the SEM and found to have an anomaly in triple track 3 which was an open circuit. This is shown in Figure 11.23. An SEM view (Figure 11.24) of this defect showed it to be a particle embedded in the surface, giving rise to a crack (Figure 11.25). This particle was analyzed using energy dispersive analysis of X-rays and was found to contain silver. The main source of silver in this system would be the conductive loading material in the die attach. The deprocessing might free silver, but embedding it in the surface can't be explained.

Table 11.2 Track Resistances for S/N gb124 Prior-to and Following Decapsulation

Globbed 40DIP ATC2.6 bussed conductors (ALL) and individual center-to-outer/inner (TT#) conductor resistances in K Ω unless otherwise noted.

TT ID#	ALL	ALL	2	2	1	1	8	8	7	7	6	6	5	5	4	4	3	3
PIN ID#	8-13	28-33	1-2	2-3	4-5	5-6	15-16	16-17	18-19	19-20	21-22	22-23	24-25	25-26	35-36	36-37	38-39	39-40
s/n gb124 Pre-Decap	*4.5*																	
s/n gb124 Post-Decap	*0.79*	*0.79*	6.3	6.3	6.3	6.3	6.1	6.1	6.0	6.0	6.0	6.0	5.9	5.9	*5.4*	*4.6*	*0.27*	*4.4*

3. S/N gb126

Serial number gb126 broke down at 85V and showed similar behavior to s/n gb124, as shown below in Table 11.3. A section of line which showed a voltage contrast anomaly is shown in Figure 11.26. Another SEM image of this section of line is also shown in Figure 11.27 and Figure 11.28. This appearance suggests that corrosion of this area may have occurred. Additional work is needed to correlate the appearance of lines involved in HAST testing.

Table 11. 3 Track Resistances for S/N gb126 Prior-to and Following Decapsulation

Globbed 40DIP ATC2.6 bussed conductors (ALL) and individual center-to-outer/inner (TT#) conductor resistances in K Ω unless otherwise noted.

TT ID#	ALL	ALL	2	2	1	1	8	8	7	7	6	6	5	5	4	4	3	3
PIN ID#	8-13	28-33	1-2	2-3	4-5	5-6	15-16	16-17	18-19	19-20	21-22	22-23	24-25	25-26	35-36	36-37	38-39	39-40
s/n gb126 Pre-Decap	*1.1*																	
s/n gb126 Post-Decap	OPEN	*0.43*	*0.49*	*01.6*	*02.5*	*04.0*	5.9	5.9	5.9	5.9	6.0	6.0	6.0	6.0	*1.7*	*4.0*	6.4	6.4

4. S/N gb136

Serial number gb136 failed before a test voltage ramp was applied. The table below indicates problems with track #1 and track #6 which were preserved through the decapsulation process. The defect on track #6 was among the 10% of electrical anomalies found in tracks 5-8, where the conductor is completely passivated. Some very obvious flaws were evident in both tracks and were not induced by the decapsulation. Figure 11.29 shows severe mechanical damage at the surface in track #1. Figure11.30 shows a severe mechanical damage site on track #6. Figure 11.31 shows heater line involvement which was not lined up with the damage site shown in the previous image. The "swirl" was an artifact of the electrical interaction of the sample with the beam.

Table 11.4 Track Resistances for S/N gb136 Prior-to and Following Decapsulation

Globbed 40DIP ATC2.6 bussed conductors (ALL) and individual center-to-outer/inner (TT#) conductor resistances in K Ω unless otherwise noted.

TT ID#	ALL	ALL	2	2	1	1	8	8	7	7	6	6	5	5	4	4	3	3
PIN ID#	8-13	28-33	1-2	2-3	4-5	5-6	15-16	16-17	18-19	19-20	21-22	22-23	24-25	25-26	35-36	36-37	38-39	39-40
s/n gb136 Pre-Decap	*0.08*	*0.07*	5.6	5.6	*2.1*	*2.2*	5.6	5.6	5.6	5.6	*0.6*	*0.8*	5.3	5.3	5.5	5.5	5.5	5.5
s/n gb136 Post-Decap	*0.10*	*0.79*	6.3	6.2	*2.4*	*6.2*	5.6	5.6	5.6	5.6	*0.6*	*0.8*	5.3	5.4	6.0	6.0	6.2	6.2

5. S/N gb129

Serial number gb129 broke down at 15V and was tested prior to decapsulation and was seen to have anomalous resistance readings between the two buss connections to the triple tracks, and between inner and outer tracks on triple track #1. Decapsulation increased all the measured resistances, including triple track #1 to change, and caused an open circuit to appear in triple track #2 as well as one of the common connections. The latter was linked to a failed wirebond. The open in triple track #2 was believed to be a mechanical defect which was held closed by the encapsulant. Passive voltage contrast was observed on triple track #2 to reveal open locations shown in Figure 11.32. An enlarged view of such an open site is shown in Figure 11.33. The corresponding site is shown in Figure11.34 following removal of silicon nitride and glass. Only the irregular portion of the aluminum line has been removed by the deprocessing. Figure 11.35 shows a very recent result involving electrical coupling of some circuit features to some heater lines, pointing to the possibility of heater line involvement in the voltage breakdowns.

Table 11. 5 Track Resistances for S/N gb129 Prior-to and Following Decapsulation

Globbed 40DIP ATC2.6 bussed conductors (ALL) and individual center-to-outer/inner (TT#) conductor resistances in K Ω unless otherwise noted.

TT ID#	ALL	ALL	2	2	1	1	8	8	7	7	6	6	5	5	4	4	3	3
PIN ID#	8-13	28-33	1-2	2-3	4-5	5-6	15-16	16-17	18-19	19-20	21-22	22-23	24-25	25-26	35-36	36-37	38-39	39-40
s/n gb129 Pre-Decap	*0.67*	*0.69*	5.9	5.9	*5.3*	*4.6*	5.8	5.8	5.8	5.8	5.9	5.9	5.9	5.9	5.9	5.9	5.9	5.9
s/n gb129 Post-Decap	OPEN	3.2	OPEN	OPEN	8.2	7.4	8.3	8.3	8.3	8.3	8.4	8.4	8.4	8.4	8.8	8.7	8.8	8.8

IV. Conclusions

The mechanical damage on all samples exhibited similar behavior, but the source of each type has not been conclusively defined. Particles from extended storage combined with mechanical lapping of the die backsides and the ensuing plastic molding have been suggested, but cleaning and encapsulating in a curable liquid have produced defects with similar behavior. A sequential evaluation of mechanical treatments and the propensity to fail could clarify this further. The shorting locations on ATC2.6's heavily favored triple tracks 1-4, which have passivation openings. This was true even when direct disturbance of these regions was not observed. There were differences between the details of plastic molded ATC2.6's and globbed ATC2.6's, the most prominent being the post-decapsulation behavior of suspected defects (turned to electrical opens on globbed circuits).

Electron beam techniques for isolating defects were inherently more successful on open leads than shorted leads, but revealed the electrical behavior of several defects. Fluorescent microthermal imaging pinpointed a few defects and shows promise for future work. These techniques were used to attempt to isolate the defects responsible for the electrical failure from among a large number and variety of physical defects following decapsulation. The experience gained from working with these problems will undoubtedly expedite future examinations.

V. Future work

Future work is proposed to include an extension of techniques employed for the devices in this report to quantify the source of the mechanical damage seen on circuits and to characterize HAST testing effects on the test chip's structures. Analysis on future devices could be conducted without several of the pitfalls which were encountered in this failure analysis due to familiarity established in this work. A more extensive electrical test prior to decapsulation (with heater lines pinned out, in the case of globbed ATC2.6's) would be a routine addition to analysis, for the purpose of looking more closely at the possibility of z-axis shorting. The time essence of certain types of defects would receive more attention, using less batch processing during FA. Repressurization and localized heating of suspected healed defects may help to reveal the precise locations of several types of defects. Decapsulation techniques which preserve the material adjacent to the test circuit surface would permit morphological and compositional examination of this topography for particles to determine the sequence of defect appearance. Additional work with thermal imaging (IR and FMI) will be more effective with a more aggressive approach to isolation of defective regions. Electrical isolation performed in the FIB would avoid the molten reconnection of current paths which confused certain analyses.

Additional attention to property changes in polymeric encapsulant with temperature and environment are warranted, based on the results of decapsulation for a study of wirebond properties.

Simulation of direct corrosion for a detailed look at the effect on the insulating layers and aluminum lines (mechanical rearrangement of aluminum lines) would be useful.

VI. Acknowledgments

This work was supported by Ken Peterson, 1275, as project leader, by Pai Tangyunyong, 1275, particularly for FMI analysis, and by Jim Rife, 1275, for FIB and SEM analysis.

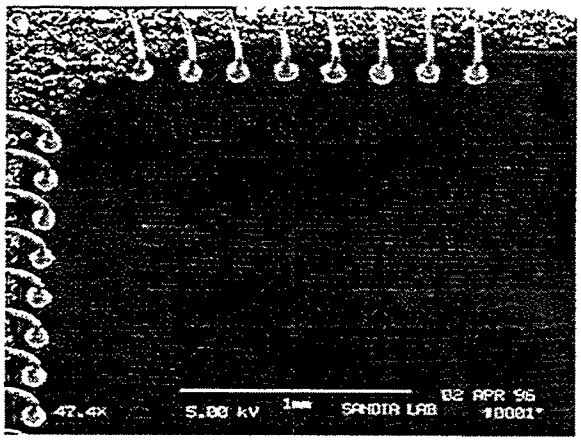

Figure 11.2. Decapsulated test chip.

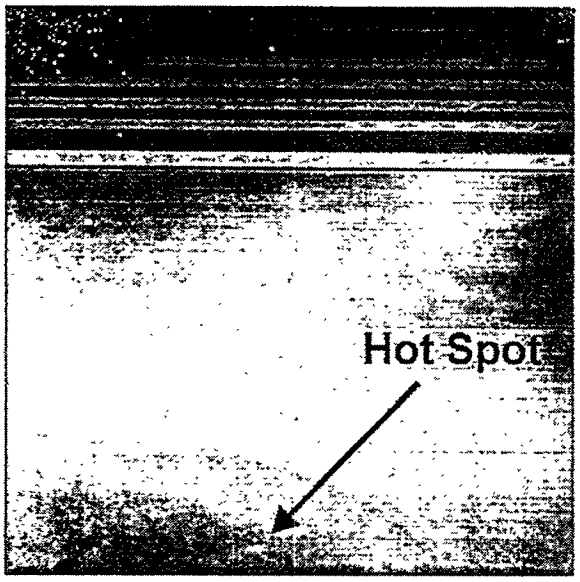

Figure 11.3. FMI image of the hot spot associated with a short circuit in a triple track on S/N SCT115.

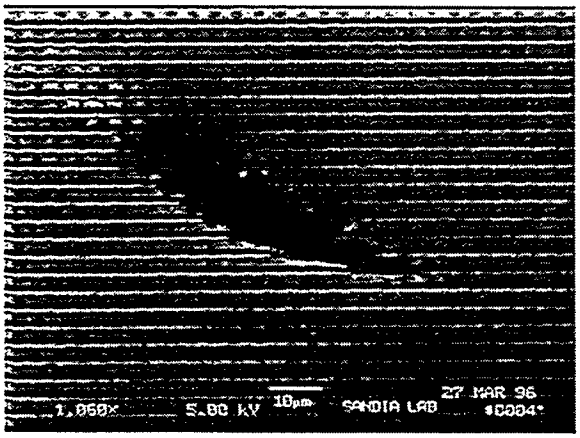

Figure 11.4. Defect responsible for FMI hot spot on S/N SCT115.

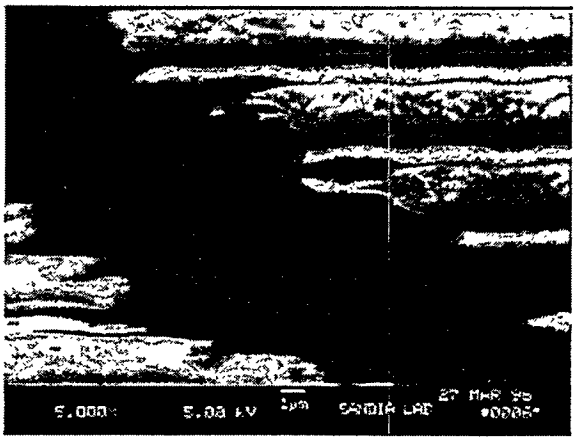

Figure 11.5. Higher magnification view of FMI hot spot on S/N SCT115.

Figure 11.6. FIB cross section of defect associated with FMI hot spot on S/N SCT115.

Figure 11.7. FIB cross-section of processing defect shorting adjacent lines on S/N SCT108.

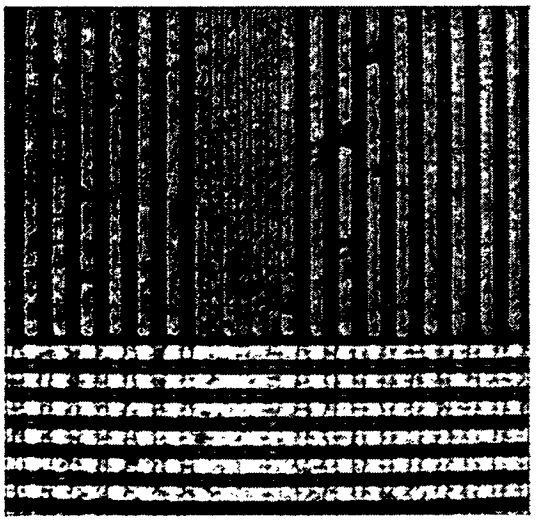

Figure 11.8. Optical image of heater line anomaly on S/N SCT108.

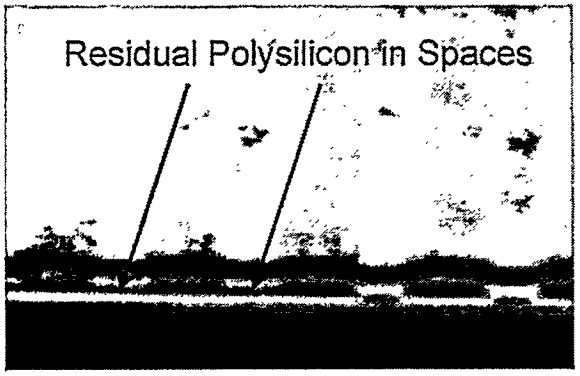

Figure 11.9. FIB cross-section of heater line anomaly on S/N SCT108 showing incomplete removal of polysilicon.

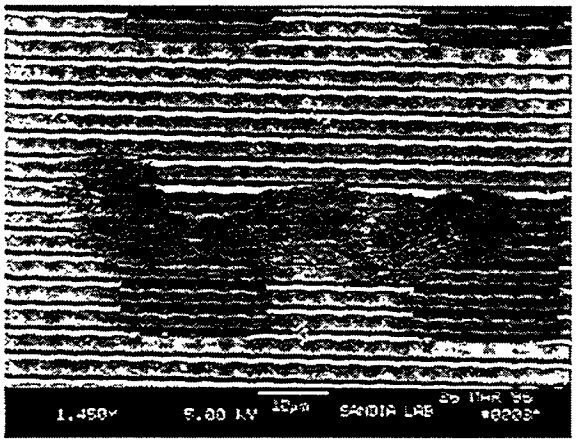

Figure 11.10. Mechanical damage in failing triple track of S/N SCT08.

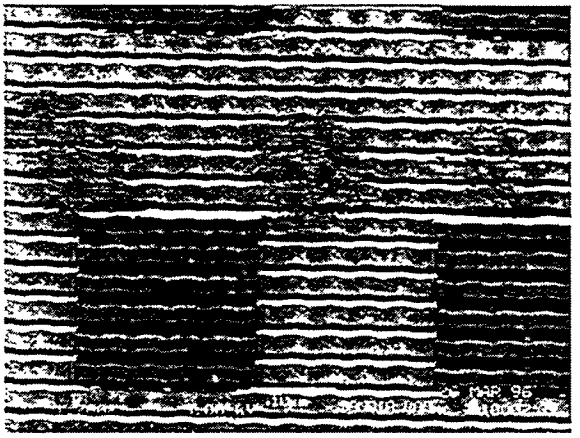

Figure 11.11. Additional mechanical damage in failing triple track of S/N SCT08.

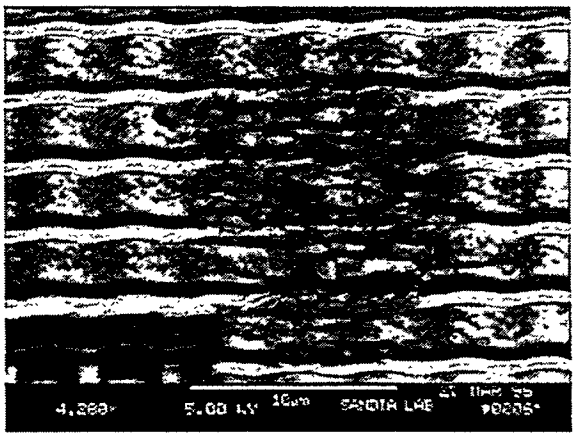

Figure 11.12. Higher magnification of defect in failing triple track of S/N SCT08.

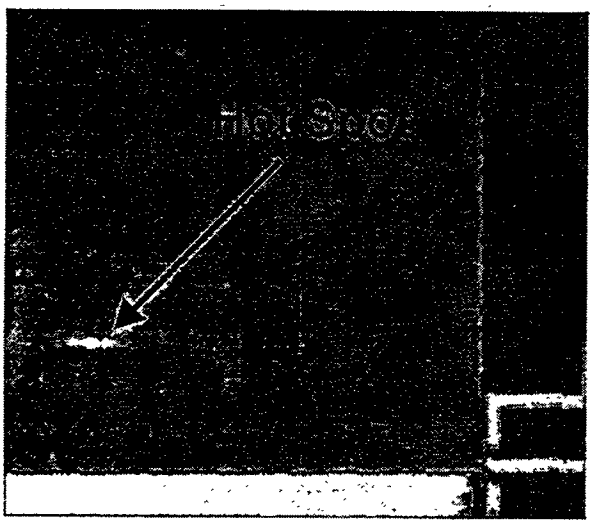

Figure 11.13. Hot spot imaged using FMI in failing triple track of S/N SCT08.

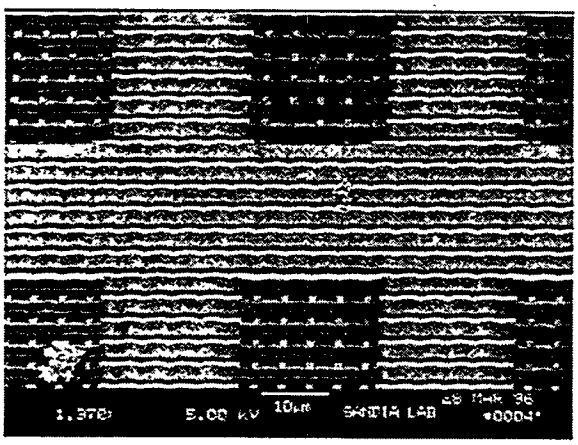

Figure 11.14. Defect associated with FMI hot spot on S/N SCT08.

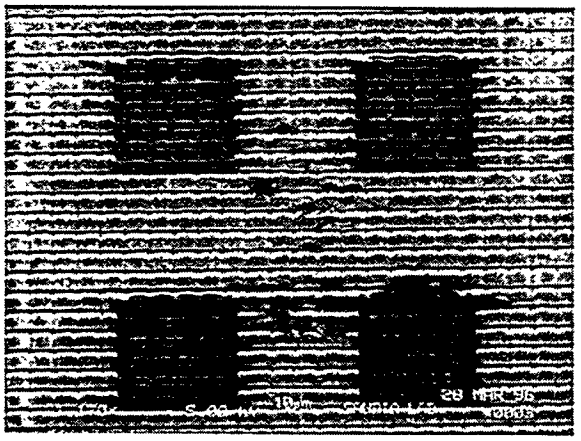

Figure 11.15. Mechanical damage in failing triple track of S/N SCT09.

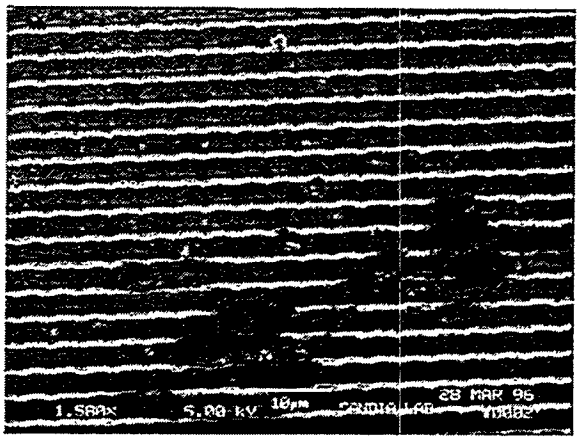

Figure 11.16. Additional mechanical damage in failing triple track of S/N SCT09.

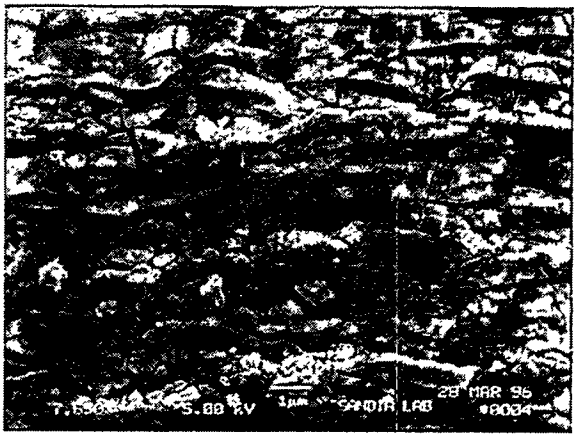

Figure 11.17. Magnified view of mechanical damage in failing triple track of S/N SCT09.

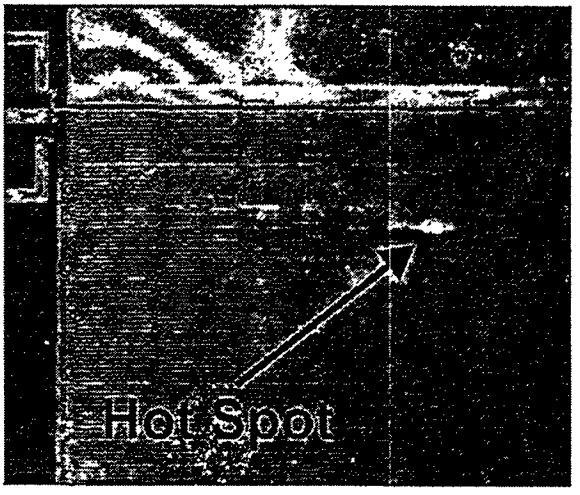

Figure 11.18. Hot spot in FMI of S/N SCT58.

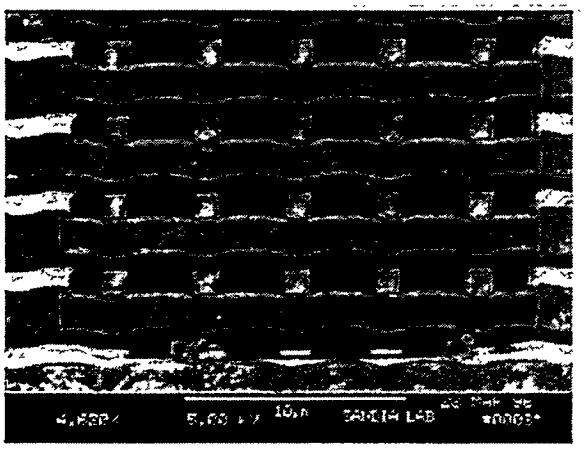

Figure 11.19. SEM image of site of FMI hot spot on S/N SCT58.

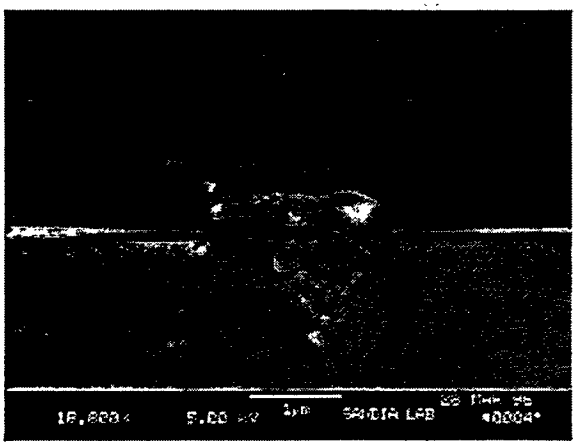

Figure 11.20. Increased magnification of site of FMI hot spot on S/N SCT58.

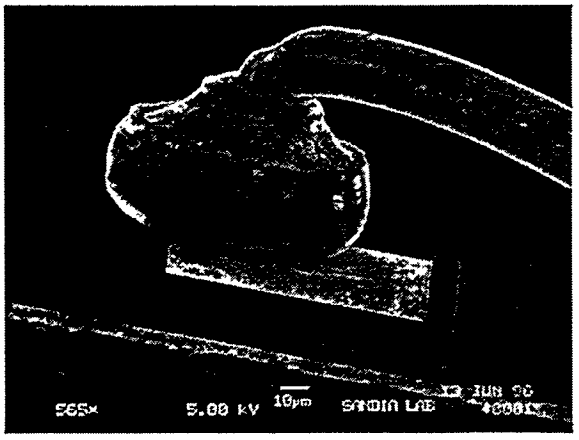

Figure 11.21. Misplaced wirebond on S/N gb122.

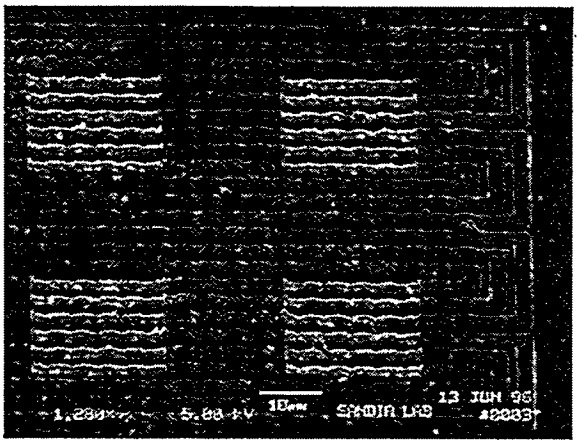

Figure 11.22. Contamination on triple track structure on S/N gb122.

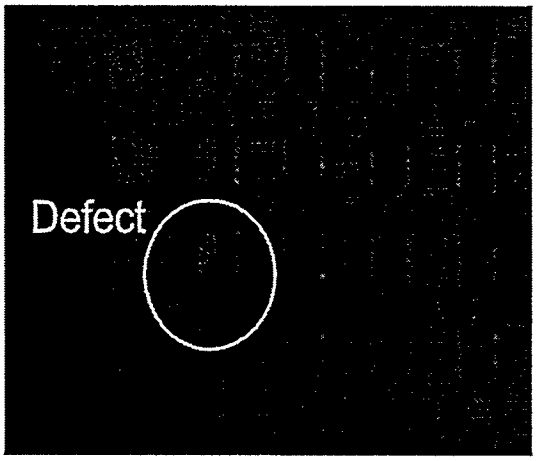

Figure 11.23. Open circuit indicated by voltage contrast discontinuity on S/N gb124.

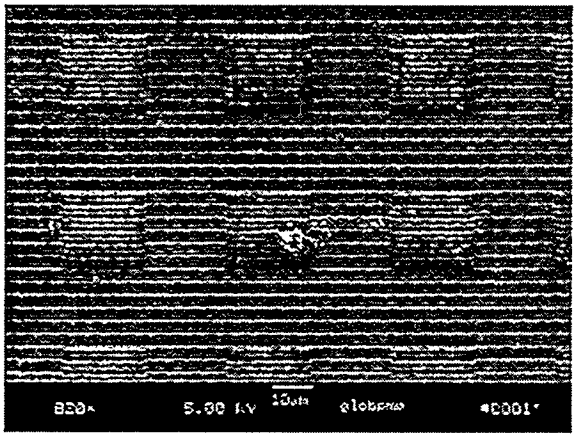

Figure 11.24. Site associated with open circuit on S/N gb124.

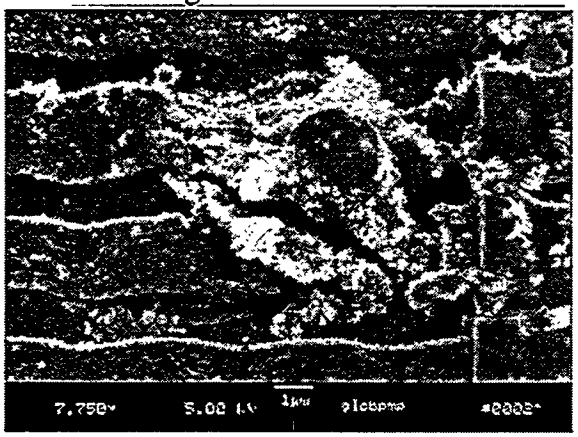

Figure 11.25. SEM image of crack in triple track conductor on S/N gb124.

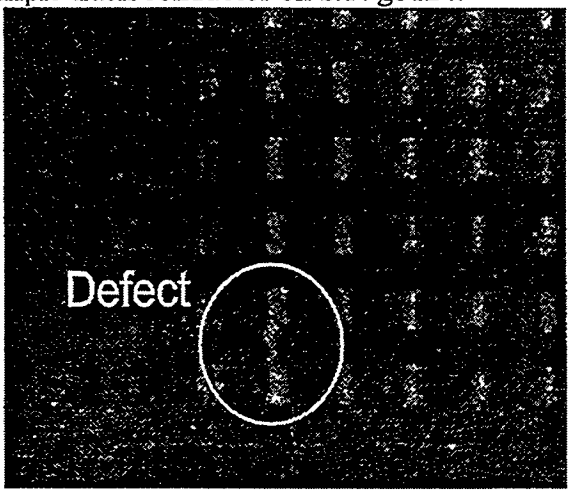

Figure 11.26. Anomaly in voltage contrast image of failing track on S/N gb126.

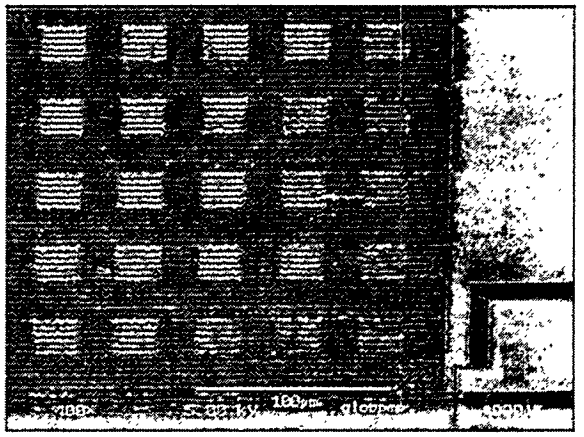

Figure 11.27. SEM of site of voltage contrast anomaly on S/N gb126.

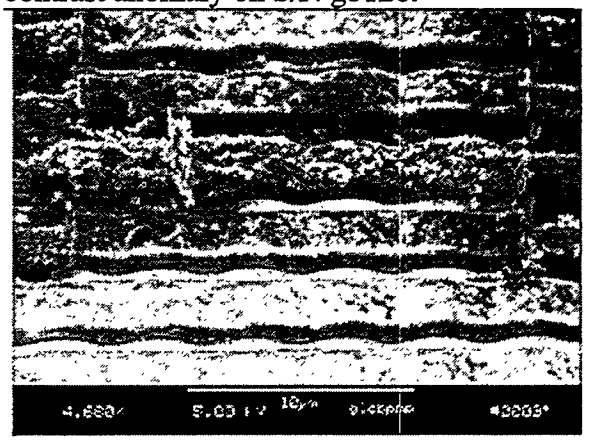

Figure 11.28. Increased magnification view of anomaly associated with triple track conductor on S/N gb126.

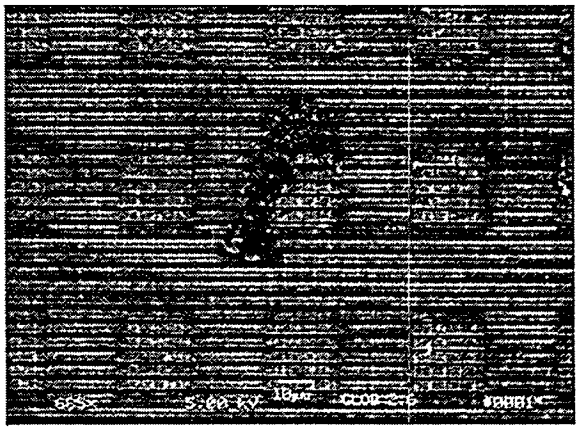

Figure 11.29. Mechanical damage on side of S/N gb136 with passivation openings.

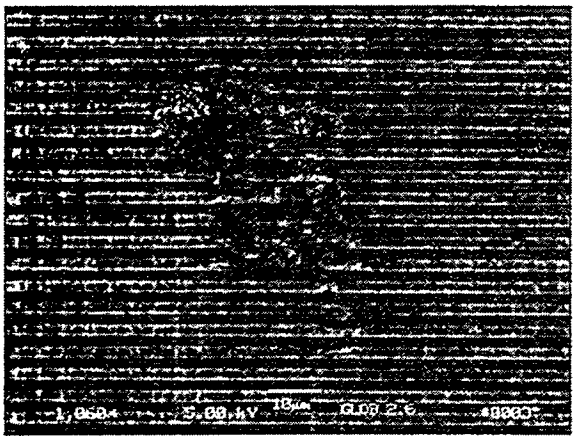

Figure 11.30. Mechanical damage in triple track on side of S/N gb136 without passivation openings.

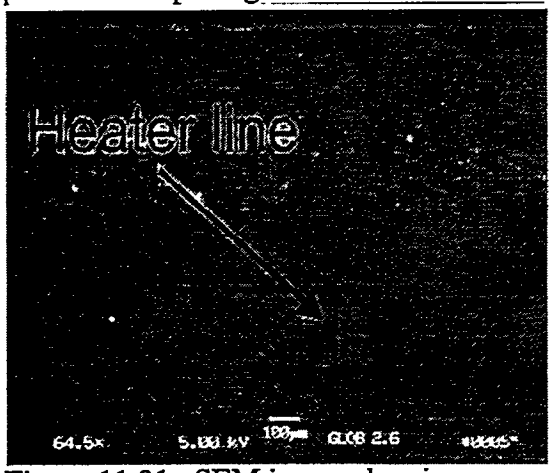

Figure 11.31. SEM image showing a potential difference of a single heater line.

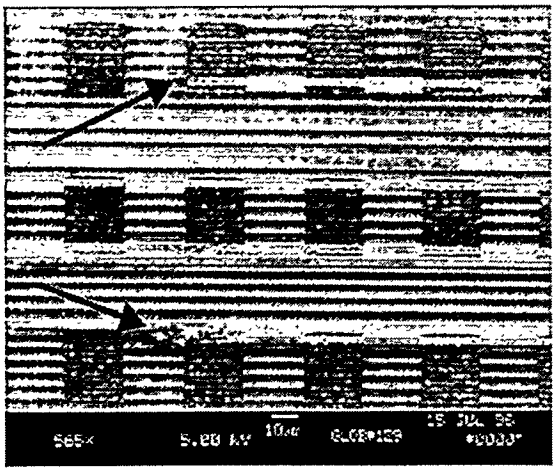

Figure 11.32. Passive voltage contrast indication sites of electrical discontinuity in failing triple track of S/N gb129.

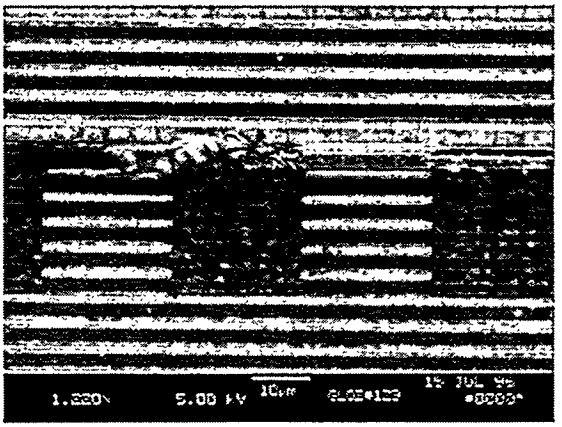

Figure 11.33. Increased magnification SEM of a single discontinuity on S/N gb129.

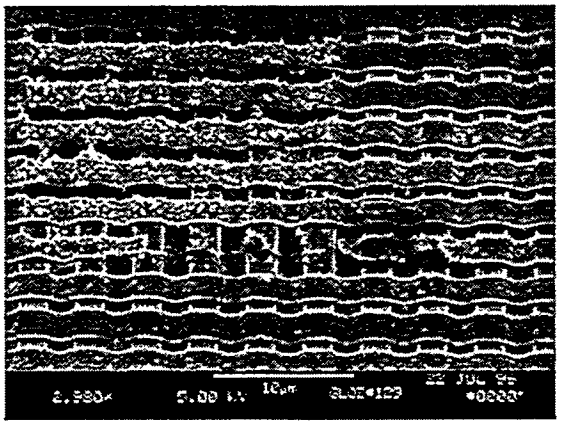

Figure 11.34. Site of electrical discontinuity on S/N gb129 following delayering..

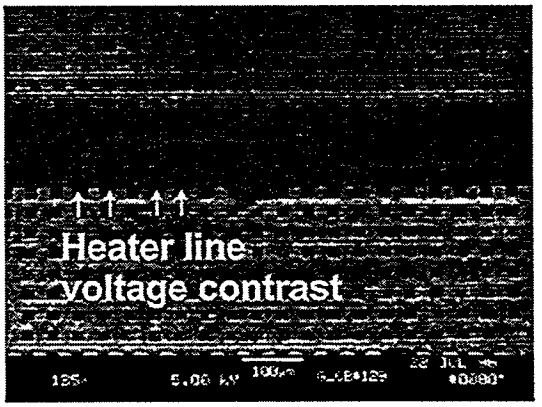

Figure 11.35. Passive voltage contrast of intermittent heater line connections.

Task 12

SPECIFICATION FOR QUALIFICATION OF VENDOR AND OF PART

David W. Palmer and Donald R. Johnson

I. Objective

The objective of this task was to provide a detailed specification, based on the test and evaluation results of a proposed two year program, for the qualification of commercial off-the-shelf (COTS) plastic encapsulated integrated circuits (ICs) with regard to vendor materials and processes, and manufacturing lots.

II. Introduction

Not enough work has been performed on this investigation to define procedures for qualification of plastic molded IC packaging. External communication and high end computer companies have shared field data with Sandia indicating that commercially packaged product can meet high reliability requirements for decade lengths of time; this is promising but does not provide a foundation for predicting lifetime, modeling aging and prioritizing stresses.

By performing accelerated aging studies using sensitive assembly test chips as the molded ICs, a predictive lifetime model is to be constructed. Accelerated aging includes (1) time-high temperature-high humidity tests with several values of each variable, and (2) thermal mechanical temperature cycling. In addition, detailed failure analysis is used to determine the most prevalent aging mechanisms that will lead to field failure. A predictive model based on these results plus statistics continually gathered from the field will form the basis for purchase specification and qualification procedures. The considerable, closely related work being done under DoD support should continue to be synergetic with DOE studies, with the final documentation being in agreement, and complementary in areas of non-overlap (earth penetrators and strategic radiation levels, for example).

Enough work has been performed to date in this study, previous research and DoD supported work to make preliminary educated guesses about the possible outcomes and their impact on nuclear weapon designers. It is important to note that this change in packaging is considerably more significant than a switch from one ceramic package to another (for example the switch 15 years ago from DIP / flat packs to leadless chip carriers). Each of these switches was accompanied by 10s of man-years of studies and judgments (at Sandia and Kansas City). Such in-depth investigation had proven necessary because of unexpected consequences of even these "little" changes. Such in-depth investigations were possible back then because of a shared sense of mission and the high value placed on reliability. Times have changed. Today's attempt was to take only a small number of measurements but by using test chips to make the measurements extremely quantitative, thus allowing construction and validation of detailed analytic models. Reliance would then be on the models for predictions based on specific weapon environments and extrapolations of initial field aging measurements.

III. The Questions:

A. *Given a packaging line that has demonstrated six sigma for commercial packaging, does this quality extend into the DOE specific specifications of temperature extremes, extended dormant storage, radiation effects, and extreme accelerations (artillery firing and earth penetrators)?*

If yes, then only a small sampling of the production lot is needed for exposure to the lifetime weapon environments for part and production qualification. To the extent that nuclear weapon non-commercial requirements can not be assumed to be tightly controlled by the commercial vendor the difficulty rises. However, the accommodation can take place with design rules imposed at the subsystem level. For example, the well understood ceramic packages have many subsystem design rules: orientation rules for high acceleration, desiccant in the potting rules to prevent lead corrosion, acceptable rework temperatures and times.

In this spirit, it would not be unexpected to have some heat capacity or insulation requirement to prevent very rapid temperature swings of a subsystem, or a foam encapsulation requirement to prevent package cracking during some mechanical shocks, or a seal and desiccant balance to prevent condensation on parts during dormant storage. Measurements to date do not indicate that subsystem design rules would be any more numerous or extreme with plastic than with ceramic, only unfamiliar to the nuclear weapon designer. It is also possible that some stringent specification precludes the use of a commercial part in some situations just as we performed special packaging on some components in the past. For example: parts with crystal oscillators required considerably more hermeticity in their sealing than standard ceramic parts can give, and high frequency semiconductor devices often require "hydrogen free" packages today. It is also clear at this early stage of the investigation that placing packaged sensors (test chips) within the subsystem in such a way that the inevitable degradation of the IC component can occasionally be monitored when the subsystem is addressed is a very necessary way of operating in the future. Exact aging data on the health of packaged weapon parts will allow full faith in stockpile readiness calculations.

B. *What do the extensions of 6-sigma look like based on 1 year of study?*

The following are just possible concerns which define the range of possibilities not the final specification answers.

1. **Temperature extremes:** Weapons tend to have specifications of -55 to 150 C compared to commercial parts that are more typically -25 to 100 C. Several packaging materials aimed at the auto industry have recently been qualified for the -55 to 150 C range. Subsystem thermal mass or insulation may be requested to prevent rapid temperature fluctuation (thermal shock). This is particularly important if a fast swing to high temperatures occurs after years of equilibrating to high humidity at low

temperatures. Certain common epoxy and filler materials will prove better at these temperature swings than others and may become the preferred materials for military and automobile uses.

2. **Dormant Storage:** Nuclear weapons tend to sit on the shelf for years rather than the months seen in commercial systems. There is little data on commercial parts stored in high humidity environments for years. It may be necessary to use encapsulants, seals, or desiccants to prevent surface condensation of humidity from occurring on part leads. This is not unlike similar requirements with ceramic parts today. In addition, as stated in the previous paragraph, prevention of rapid temperature shock seen at the part level may be necessary.

3. **Radiation effects:** Recent measurements have shown that post burn-in response to total gamma radiation can be an order of magnitude worse than on non-burn-in parts. The distinction is a bit more extreme for plastic than for ceramic parts, but exists for both. An intermediate "cool-down" dwell may be necessary after burn-in to get rid of built-in mechanical stress on the gate oxide or perhaps a minimum length of time between burn-in and stockpile will have to be implemented. Some commercial trends are aimed at eliminating long burn-ins, this may also help.

4. **Extreme accelerations:** Plastic seems to be supreme in extreme accelerations with no free bond wires to vibrate and die attach material to give way. However, the optimal thickness of the plastic package must be considered in this process.

C. *How would a written specification be used?*

1. The specification would call out what test structures or chips would be used to evaluate a manufacturing line, followed by which accelerated aging procedures will bring out the equivalent aging of these parts during stockpile and use. For example, a manufacturing line could be qualified by sending 100s of silicon IC test chips in wafer format to the facility. The returned packaged parts would receive initial sensor readings and then be submitted to a series of accelerated aging processes with regular sensor readings. In this way, each manufacturing line could be compared to a growing database. For example, mechanical damage caused by assembly operations would be quantitatively determined by readings taken upon receipt of the packaged product. Similarly, susceptibility to corrosion would become a numerical result after extensive HAST tests using the triple tracks on the test chips.

2. Once a line is qualified using test chips, the qualification of each manufacturing lot becomes an issue. Remember that the present procedures on ceramic parts call for a small number of parts (30) taken for destructive tests and a few nondestructive screens to be performed on all the parts to be used (for example, fine leak test and PIND). To the extent that the manufacturing line is determined to be six sigma for all our weapon specifications, the procedure may consist of doing absolutely nothing, since handling the devices to find the 1-in-a-million defect would cause even more flaws. However, if the vendor's quality control does not influence the subtle radiation/

package induced IC degradation then it may be necessary to perform an incoming screen on each manufacturing lot to determine if it is within specification.

3. The commercial world often makes small changes for cost reasons that they think have little effect on product performance. For example, the cure time in the mold may be decreased by 10% or a different mold release additive may be added to the molding compound. It is probable that communication of such changes will not be made to the weapons complex with each delivery since this is beyond the spirit of COTS. Therefore a specification calling out regular monitoring with test chips or routine destructive sampling of delivered parts will be necessary.

D. *How does the DOE complex become as expert with commercial packaging as with the military spec packaging?*

Time is part of the solution. Investigations such as the first year of this one can go a long way to connecting DOE engineers with the studies and experts in the commercial packaging world. However, as pointed out earlier in this discussion, even "minor" ceramic packaging changes generated studies with 10s of man-years of effort by yesterday's DOE. In contrast, this major change in packaging is being studied in only a cursory fashion to date.

One possibility is creating a plastic molding prototype capability within the complex to let engineers get their hands dirty with the technology. In fact with SEMATECH support the initial steps in this direction have been taken. A highly instrumented commercial molding press has been located at Sandia and a run of molding using Sandia test chips is underway. However, in contrast 4 or 5 ceramic packaging facilities existed through the years at DOE facilities. The largest was run for 8 years by Bendix (AlliedSignal) and employed approximately 100 people. Hands on expertise ran deep in the Complex.

E. *Should we try to establish deep expertise in commercial technology?*

Yes. How should this be done? The most cost effective route is not yet clear. The current study, if continued, should put Sandia in a better position to propose the solution to the Complex.

IV. Screening For Qualification

Screening may be defined as an audit process utilized to ensure that the product's manufacture and materials conform to the control limits of the qualified production process.[1] This audit may involve the early detection of out-of-tolerance product parameters along with resultant defects. Screening may be used to qualify a manufacturing line or to systematically monitor in-coming product from that line. This approach assumes that the weak population (e.g., weak wire bonds, weak die attach, weak solder joints, etc.) can be eliminated, thus leaving a high-reliability final product.[2] Screening has been the way of life for "mil spec" ceramic packaged devices. All manufacturer's lots receive destructive tests on a significant number of parts and visual, electrical, leak test, PIND, and burn-in on all parts. If the lot fails to meet some sampling criteria

then often the complete lot receives an ad hoc screen to allow shipment despite failure. Commercial parts see only sample HAST testing by the manufacturer.

Preferably screening of COTS components would not be required for a fully qualified line. If, however, screening is deemed necessary, then a choice must be made between nonstress and stress screens. Nonstress screens are typically non-contact tests that are used to detect defects; the non-contact approach is used rather than bring on failures through applied loads. These screens may include visual inspection, radiography, and acoustical microscopy, as well as functional and parametric electrical tests. A few viable examples of such screens and the potential defects exposed are presented in Table 12.1.

SCREEN	DEFECT EXPOSED
Weight After Humidity Soak	Encapsulant Porosity
Radiography	Wire sweep, broken wires, contamination and extraneous metal
Acoustic Microscopy	Delamination, voids, cracks, inclusions
Functional Test	Shorts, opens, broken wirebonds
Visual	Surface defects, foreign material, misaligned leads, dimensional problems

Table 12.1. Possible Screening -- Nonstress

Stress screens on the other hand expose defects by application of thermal, mechanical, or electrical loads, which may or may not be representative of service loads. Additionally, these loads may be applied at an accelerated level to reduce time-to-failure, and may result in more than one failure mechanism at more than one site. Stress screens may be grouped into wearout or overstress screens.

Wearout screens, such as temperature cycling and vibration, are known to activate fatigue, diffusion , and tribological mechanisms. These screens ultimately lead to an accumulation of damage at defect sites sufficient to cause failure in weak product. The problem that should be noted is that a fraction of the useful life of non-failed product is also consumed by wearout screens due to damage accumulation. Screening parameters must be carefully chosen so that the remaining useful life of the screened product meets longevity and reliability requirements.

In contrast to wearout screens, the overstress screens, such as bond pull test and thermal shock, result in catastrophic failure because the stress level at a defect site exceeds the local strength. Often a defective product that would fail early in service life due to one of the wearout stress mechanisms may be detected by employing an overstress screen. While an overstress screen

prompts instantaneous failure rather than damage accumulation, this screen must be cautiously implemented in order not to cause yield problems on the product line.

Effective screens must be chosen and adapted for specific defects/failure mechanisms at specific defect sites. Whatever screening technique is employed, the required product life must not be compromised. When and how to screen any product is likely to become an economic decision. Screening may result in significant penalties in capital, operating expense, cycle time, and induced defects. The ultimate decision regarding screening will likely be influenced by the desired quality level, an evident but unresolved problem, product technology, package type, and product application. Correlation between failures occurring during screening and early field failures may offer a valid justification for continuing to screen. However, no incidence of found defects may result in no screening at the component level but increased emphasis in "design for testability" so that system failures can be immediately traced to the component level.

The defects observed in plastic encapsulated semiconductors are typically ascribed to poor base material quality, out-of-control manufacturing processes, and contamination on the process line. Based on the high volume production processes combined with automatic assembly, the alternatives to screening for PEMs include statistical process control and closed loop feedback control. Defects are frequently found to be different from one manufacturer to another, and from one process to another within the same manufacturing location.

While high reliability applications may ultimately result in screening of product by the customer, it is deemed most desirable to eliminate such procedures as soon as possible. Screens that do not result in failures are serving no useful purpose, and those that induce a high percentage failure rate are quite costly. Thus, identification of potential failures intrinsic either to the packages or to the manufacturing processes is necessary for the screening to be considered effective. Ultimately the goal is to continually improve the methodology for process control, and thus reach the product level wherein screening techniques are considered totally unnecessary!

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[1] Pecht, M. G., Nguyen, L. T., and Hakim, E. B., Plastic-Encapsulated Microelectronics, John Wiley & Sons, New York, 1995.

[2] Pecht, M. G., Editor, Handbook of Electronic Package Design, Marcel Dekker, Inc., New York, 1991.

APPENDIX

Memorandum Detailing Ultrasonic Imaging of Plastic Packages

Sandia National Laboratories
Operated for the U.S. Department of Energy by
Sandia Corporation

Albuquerque, New Mexico 87185-0615

date: August 19, 1996

to: Donald R. Johnson, 1333, MS 1082

from: John H. Gieske, 9752, MS 0615

subject: Ultrasonic C-scan Imaging of Plastic Molded IC Packages

Ultrasonic through transmission and pulse-echo examinations of 15 plastic molded IC packages were performed to characterize package uniformity for defects. All defects such as voids, disbonds, and delaminations were characterized in the original packages before thermal cycle tests were to be performed. The baseline C-scan images were obtained to display all non-uniformities or disbonds within the package; i.e., within the lead frame area, the top of the die surface area, the bond area of the die attachment to the lead frame paddle, and the surface area of the paddle to the plastic package.

A schematic of the package cross section is shown in Figure 1. The cross sectional view shows the location of the different material interfaces within the thickness of the package. The baseline C-scan images provide the initial characterization of the package material interfaces for which comparisons of ultrasonic C-scan images can be made after various stages of the thermal cycle tests. The C-scan images can show how much degradation of the bonds at the interfaces occurs at any point during the thermal cycling tests by displaying the location and

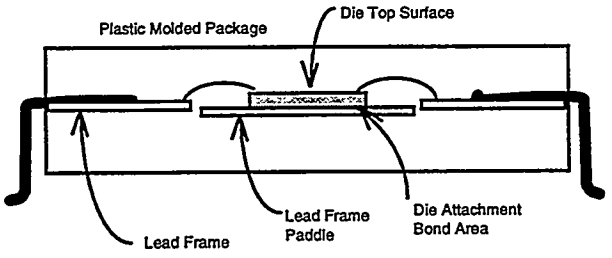


Figure 1. Plastic molded IC package cross section.

area of disbonds as they initiate and enlarge.

Through Transmission Examinations

A characterization of all interfaces within the package can be made with a Through Transmission (TT) examination as shown in Figure 2. The amplitude of the through transmission signal is a measure of the ultrasonic energy lost in the single path through the thickness of the package. Ultrasonic energy is reflected at each interface encountered

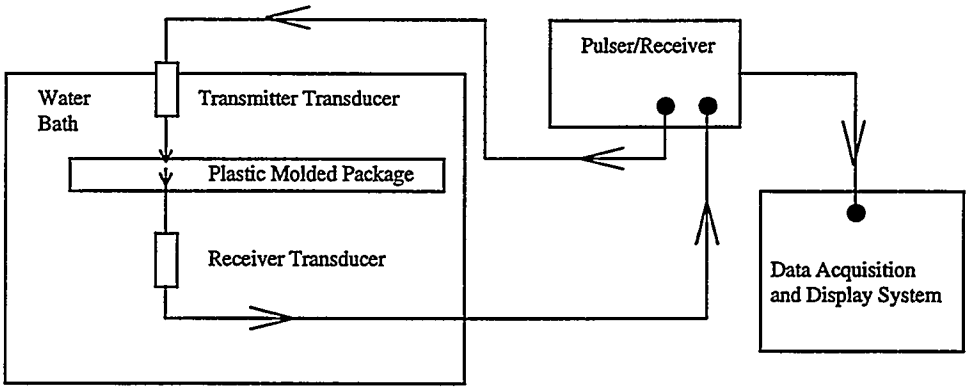


Figure 2. Through transmission examination of the plastic molded IC package.

depending on the acoustic velocity and density difference of the materials at the interface. When a disbond or delamination occurs, almost all the energy is reflected and as a result a very low signal is recorded by the receiver transducer. Areas of small defects or voids also reflect or scatter the energy by varying amounts so that small non-uniformities within the materials or bonds within the package will also be detected.

The variation of the signal amplitude recorded by the receiver transducer as the pair of transducers is scanned over the area of the package provides an image of the uniformity of all interfaces of the package. Figure 3 displays the Through Transmission (TT) amplitude and Time-of-Flight (TOF) images for 3 test packages. The 3 test packages were not part of the 15 packages to be used for the thermal tests but they illustrate the capabilities of characterizing the packages by the TT examination. The TOF plot displays the changes in the delay of the pulse due to acoustic velocity differences of the materials in the package. The TOF plot shows the location of components of the package that may not appear in the amplitude plot. For example, the die attachment area is clearly seen in the TOF plot but it is not seen in the amplitude plot. The amplitude plot, however, shows clearly small bond non-uniformities that are not seen in the TOF plot.

In Figure 3, the amplitude plot of SCT04 and SCT06 shows a green area in the die attachment area surrounded by the blue area of the die attachment and paddle. The green area is where a slightly larger amplitude signal is transmitted through the package than at the surrounding area. These variations may be due to the bond differences at the die top surface, or the bond of the die to the paddle, or the bond of the paddle to the plastic package. The TT test can not distinguish which interface is non-uniform but viewed with subsequent pulse-echo data, a determination of the failing interface usually can be made. The amplitude plot of SCT100 in Figure 3 shows that only a small area of the die is attached through the thickness of the package and a large area around the paddle is disbonded.

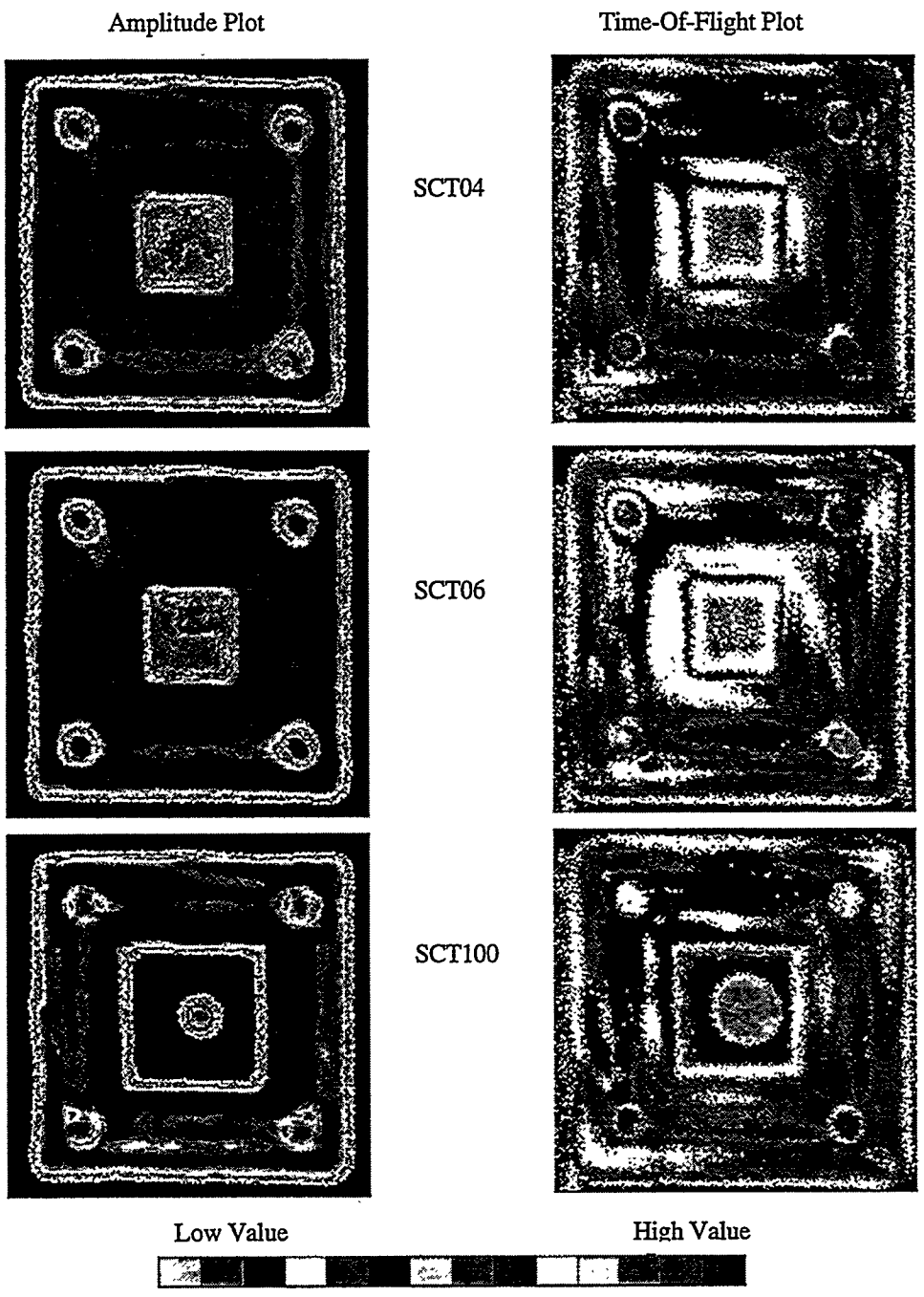


Figure 3. Through transmission amplitude and time of flight plots for 3 test packages.

Similar images for 3 packages ,SCT127, SCT128, and SCT134, taken from the group of 15 thermal cycle packages are shown in Figure 4. The images displayed are typical of all 15 packages. The diagonal yellow area in the paddle cavity is due to the presence of the diagonal ground lead of the paddle to the lead frame. The baseline images for all 15 packages showed that they are all fairly uniform and no disbonds, delaminations, or other defects in the packages were detected. The 15 package examined were: SCT121, 123, 124, 127, 128, 134, 135, 138, 139, 142, 151, 152, 153, 154, and 158.

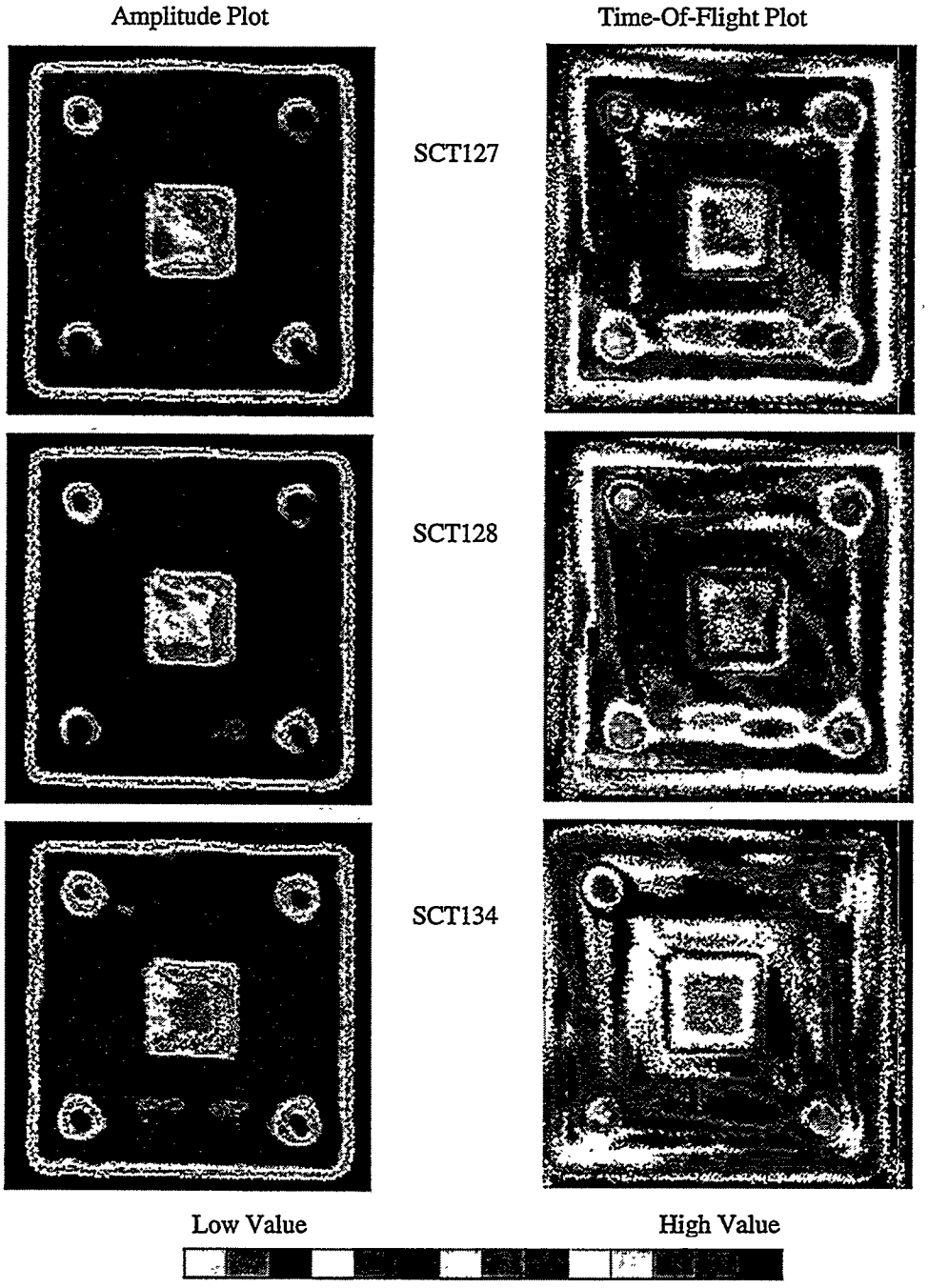


Figure 4. Through ; used in the thermal

Pulse-Echo Examinations

The 15 packages were also characterized with a pulse-echo examination from the top of the package (die-side) and from the bottom of the package (paddle-side) The pulse-echo examinations can display non-uniformities present in a single interface. However for multiple

layer materials, the pulse-echo data for deeper layers can be masked by defects in the shallower layers. Therefore, scanning the package from the top and also from the bottom provides the most appropriate data to characterize all the interfaces.

The pulse-echo data is obtained with the same instrumentation shown in Figure 2 except that only one transducer is used. Figure 5 shows a schematic of the ray path of the ultrasonic energy as the wave pulse travels perpendicular through the thickness of the package. As is

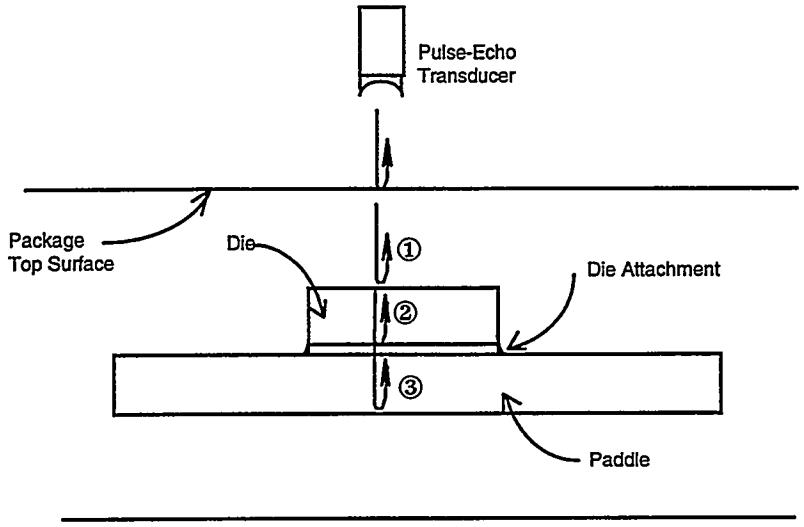
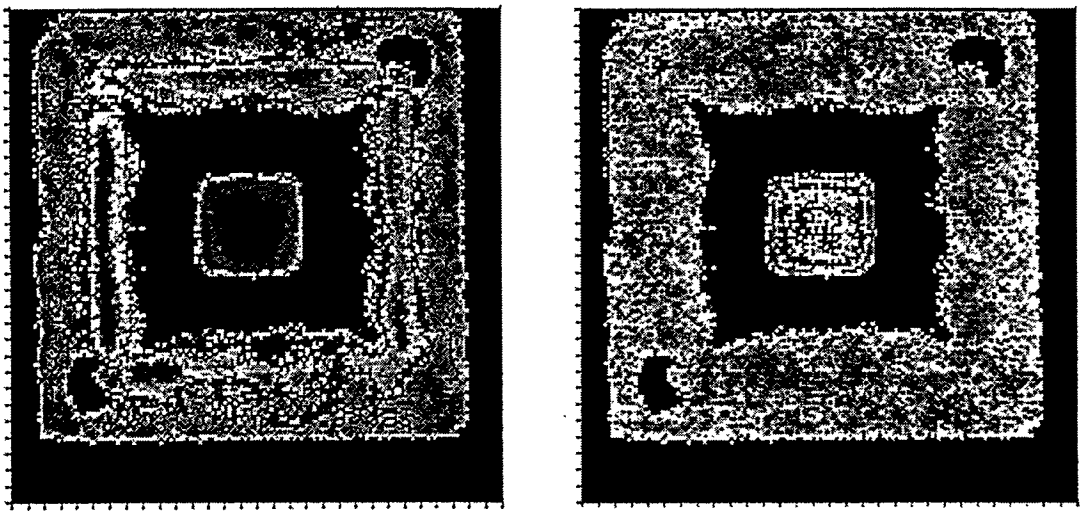


Figure 5. Pulse-Echo reflections at material interfaces within the package.

true with the TT examination, the amplitude of the reflected pulse is a measure of the material differences at the interface. When a disbond occurs, a large amplitude signal is reflected. By scanning the interface with a focused transducer of a small spot size, the material uniformity of the interface can be plotted. Figure 6 shows the pulse-echo amplitude plots of the SCT06 package as it was scanned from the die-side of the package. Figure 6(a) shows the amplitude uniformity of the first echo ① as shown in Figure 5 which characterizes the bond interface of the plastic package at the top of the die and at the top of the lead frame. Figure 6(b) shows the



(a) (b)

Figure 6. Pulse-echo amplitude plots showing uniformity of material interfaces at the lead frame (a) and at the top of the die (b).

uniformity of the bond interface at the top of the die by gating out the first echo ① and displaying the amplitude of the second echo ② from the die attachment area. Areas of low signals for echo ② would indicate disbonding at the top of the die.

Figure 7 shows a scan from the paddle-side of the package of SCT06. Here, low amplitude signals indicate poor bonding of the die attachment to the paddle. The small magenta spot in the image at the die attachment area of Figure 7, indicates a small void in the die attachment.

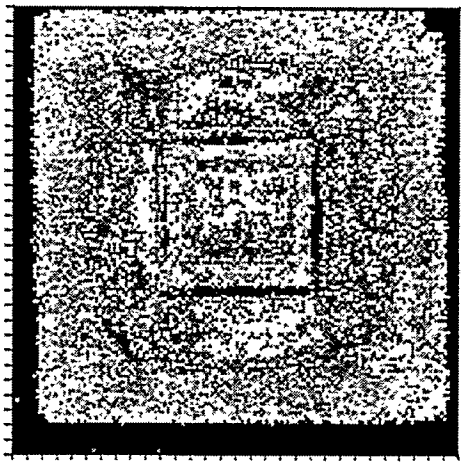
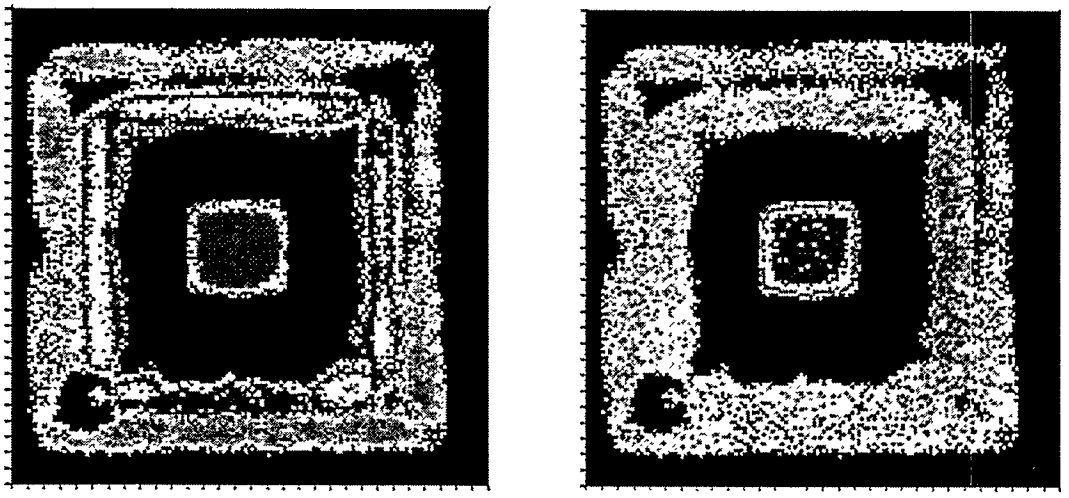


Figure 7. Pulse-echo amplitude plot from the paddle-side of SCT06 showing the uniformity of the die attachment.

Figure 8 shows plots of the pulse-echo data obtained for the die-side of SCT134 which is typical of all 15 thermal cycle packages. The data indicates a uniform bond at the top of the die and a fairly uniform interface at the leadframe. No anomalies in these two areas were detected in any of the 15 packages used for the thermal cycling tests.
Figure 9 shows the pulse-echo data obtained from the paddle-side of the die for SCT134.



(a) (b)

Figure 8. Pulse-echo plots of the lead frame and die interfaces obtained from the die-side of package SCT134.

Here, the bond interface of the die attachment shows some non-uniformity at the right side of the die shown in blue where a lower signal amplitude is recorded. This area may be of concern if a disbond develops at this area during the thermal cycle tests. However, the data does show that a bond exists and it may be adequate for the life of the package.

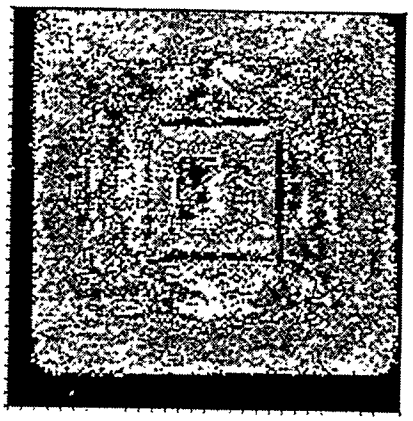


Figure 9. Pulse-echo amplitude plot showing the die attachment interface for SCT134.

Conclusions

The through transmission examinations provide C-scan images that are simple to interpret for disbonds and delaminations that occur in the IC package. However, the through transmission examination can not discern which interface may be failing. The pulse-echo examination can provide added information as to which interface is failing but interpretation of the data can be ambiguous in some cases. Comparison of the through transmission images and the pulse-echo images at the various stages of the thermal cycle tests can indicate when degradation of a bond interface occurs, which interface is failing, and the area of the failure.

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