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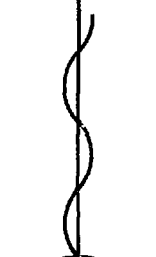

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A MULTIWIRE PROPORTIONAL CHAMBER SPECTROMETER FOR NUCLEON-NUCLEON EXPERIMENTS

by

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ABSTRACT

A flexible low resolution spectrometer is being built for a program of experiments to be done at the LAMPF Nucleon Physics Lab. The bend angle of charged particles through an 18D36 magnet will be determined by multiwire proportional chambers (MWPC) with 2-mm wire spacing. The general design of the chambers and of the associated electronics for readout and encoding are discussed. Some results obtained with a prototype systems are given.

I. INTRODUCTION

This report gives a description of a data collection system as it will be used in medium energy physics at the Los Alamos Meson Physics Facility (LAMPF). It is designed for a variety of scattering experiments at the Nucleon Physics Laboratory (NPL), chiefly in the nucleon-nucleon (N-N) field.

The system is a magnetic spectrometer, using Multiwire Proportional Chambers (MWPC's) to collect the information on the particle trajectories. The number of active wires is planned to be 1184, hence the requirement for a well-designed amplifier/logic and encoding system. The design aspects and the actual realization are described in Sections 5 to 7.

The system also includes conventional scintillation counters with the associated logic, which is necessary for a proper triggering of the read-out of the MWPC's and to get precise information on the time-of-flight of the traversing particle.

For nucleons of $\approx$200-800 MeV, the average multiple scattering angle due to the detectors is of magnitude of a few mrad. Therefore chamber separations of 1 meter with wire separations of S = 2 mm provide angular uncertainties $\approx 1/500$, comparable to the multiple scattering error. Such a geometry with the LAMPF 18D36 pool magnet gives an overall length for the spectrometer of ≈ 4 meters. The solid angle of the spectrometer (for a single momentum) is of the order of 5 msr for chambers with areas in the range 20x20 to 50x50 cm^2.

MWPC's are also outstanding for their counting rate capabilities, up to 10^5 Hz/wire. This is important since LAMPF has a 6% duty factor and will operate at high intensity. The use of eight wire planes in the spectrometer requires high detection efficiency, ϵ, for each plane. With MWPC, $\epsilon \geq 99.5\%$ can be obtained as has been verified by our preliminary measurements.

The low duty factor at LAMPF makes considerations on timing and buffering worthwhile. The macroscopic duty factor is defined by 500 μsec beam pulses at 120-Hz rate. It is important that our data acquisition system be capable of recording several events per macropulse. In order to ease the inherent limitations of computer speed, we shall use a Micro-programmed Branch Driver[1] developed at LAMPF, which is capable of buffering incoming data during the macropulse and transferring it to a PDP-11 computer during beam-off periods. In addition, the MBD frees the computer for processing and

recording of the data. In order to diminish the time required for recording all the data associated with a single event, we have developed a fast intermediate buffer called the Scratch Pad Memory (SPM) which reads and stores the wire chamber data during the operation of the analogue to digital converters. The system is ready for another physical event after the ADC's have been read into CAMAC and the SPM has been filled.

II. SYSTEM LAYOUT

A. Physical Layout

The system layout, as shown in Fig. 1, is chosen so that the different goals of several N-N experimental can be attained without major changes.

a. Measurement of the energy distribution of the neutron beam is proposed in Experiment 56 by momentum analysis of the proton produced in the forward direction by the n-p charge exchange. Figure 1 shows the setup as it is planned for Experiment 56. Neutrons are produced in a 10-cm-long liquid-deuterium target at a chosen angle θ_1 to the proton beam. The neutron beam emerges from the end of the collimator at a distance of ≈ 8 meters from the LD_2 target and passes through a monitor system comprised of a charged particle veto counter, a polyethylene radiator, and two range telescopes. Charged particles in the beam or originating from the radiator will be removed by the sweep magnet M1. We plan to use a sweep magnet inside the beam channel to remove charged particles originating directly from the neutron source.

In the liquid hydrogen target (LH_2), a small fraction of the beam is converted to protons by charge-exchange scattering. The nominal length of the LH_2 target cell is 10 cm, with a comparable diameter. Momentum analysis of the protons by means of the magnet M2 then gives information on the momentum distribution in the incident neutron beam. In Experiment 56 the spectrometer system is set at the nominal angle $\theta_2 = 0°$ with respect to the neutron beam.

b. The same setup, since it has sufficient solid angle (≈ 5 msr) can be used to measure the angular distribution of backward angle n-p scattering (LAMPF Proposal #125). The analyzing magnet (M2 in Fig. 1) and the MWPC's form a rigid entity; the spectrometer, which is mounted on a movable stand[2] and rotates about a pivot under the LH_2 target.

The design also includes provision for optical alignment and accurate replacement of chamber housings after repair or maintenance. The system can be used without major changes in the pion production Experiment No. 129, or in Experiment No. 65 where a polarized target is intended to replace the LH_2 target.

The magnetic analysis is to be done with a 18D36 H-frame magnet with "pancake" coils. The nominal field is B = 18kG in a 6-in. gap and allows a bend angle $\alpha = 22°$ for 800-MeV protons. We hope to obtain a precision of < 5 mrad for the angular measurement and so obtaining $\Delta p/p = \Delta\alpha/\alpha = 5/384 =$ < 1.3%. The bend angle is obtained by reconstruction of the proton trajectory using the information obtained from the MWPC's (W1....to W4). The sensitive area of the chambers is $\approx 20 \times 40$ cm^2 for W1 to W3 and $\approx 40 \times 60$ cm^2 for W4. The geometrical resolution for four x or four y chambers can be estimated by means of the root-mean-square deviation for detectors of uniform response and of extent $\pm S/2$ in x, for example. For a single such detector $(\Delta x)^1_{RMS} = \pm S/\sqrt{12}$, and for four detectors (adding in quadrature) $(\Delta x)^4_{RMS} = \pm S/\sqrt{3}$, or ±1.15 mm, considered as a standard deviation. Using chamber spacing of 1 m, the standard deviation in angle for four detectors is then ±1.15 mrad. Multiple scattering will bring the uncertainty in angle up to values ranging from 4.6 to 1.7 mrad for proton energies in the range 200 to 800 MeV, respectively.

Since we don't use the MWPC in autotriggering mode, a set of three scintillators (S0, S1, S2) is used to give a trigger signal. S0 eliminates residual charged particles from the neutron beam. The time difference between S1 and S2 gives the time of flight of the analyzed particles. This information will allow us to distinguish protons and deuterons of the same momentum. For 1460-MeV/c protons and deuterons, the difference of the time of flight is ≈ 6 nsec. The trigger logic will be discussed in more detail in Section 3.

B. Organization of the Data Flow

The block diagram in Fig. 2 shows the different elements used in the data collection. We distinguish a section of NIM electronics to furnish the necessary trigger signal for bona fide events which

includes fast logic and analogue circuits. An Inhibit circuit prevents interference between closely spaced events.

Also shown is a system of elements to collect the addresses of the struck wires. The transfer of this data takes place via the bus line that leads to the Scratch Pad Memory. This process is initiated by an output pulse from the Master Gate coincidence circuit (called EVENT) which is transmitted to the Scratch Pad Memory (SPM) which issues the ENCODE ENABLE signal to the first chamber, W1, which then transmits in a sequential manner the 16-bit data words of each hit to the SPM. When the data from W1 have been read, the ENCODE ENABLE signal proceeds to W2, and so forth until the last data word of W4 has been transmitted. At this point, ENCODE ENABLE returns to the SPM and if analog data input is completed, the INHIBIT is lifted, and the system may accept a new event. As noted earlier, the SPM acts as a fast intermediate buffer between the MWPC data flip-flops and input to the computer, and allows recording of the MWPC data to proceed in parallel with encoding of the analogue data and readout to the MBD.

Each MWPC data word has the following composition: 8 bits provide the hit pattern as recorded by the active module; 3 bits provide the binary address of each grouping of 64 wires, called the Super Module; and 2 bits provide the identification of one out of four chambers, for a total of 16 bits. Analogue and MWPC data are joined together sequentially at the level of CAMAC to form the event data. The analogue data comes first with a maximum of 8 each 8 bit words. Then follows a number of 16 bit MWPC data words which may vary in number from 6 to 32 or more. In the ideal case, there would be 8 MWPC data words corresponding to 1 hit on each of the 8 signal planes.

The PDP-11 computer performs several functions which we will not dwell on in this report. The incoming events are buffered and stored on magnetic tape for later detailed analysis. A fraction of the events are subjected to calculations including tests for point of origin, continuity through the magnet, calculation of polar scattering angle, and approximate calculation of momentum. These correlated preanalyzed data are buffered, stored on a rotating disk memory, and subject to recall for on-line display diagnostic purposes.

III. NIM AND CAMAC ELECTRONICS

Figure 3 shows a schematic block diagram of NIM electronics associated with the scintillators and MWPC's. An important function of the electronics system is to produce a coincidence output from the Master Gate which represents the occurrence of a bona fide event. This coincidence output is called the EVENT pulse. It initiates the conversion of analogue information to digital form and starts the MWPC data collection by the Scratch Pad Memory. This signal represents a good event by the following criteria: absence of a charged particle in S0, presence of two time-correlated signals in S1 and S2 coming within approximately 50 nsec of each other, and the presence of at least 6 out of 8 of the OR-ed fast outputs from the MWPC planes. The signature of a valid event is therefore: $(\overline{S0}\cdot S1\cdot S2) \times (W1x\cdot W2x\cdot W3x\cdot W4x)_{3/4} \times (W1y\cdot W2y\cdot W3y\cdot W4y)_{3/4}$, where the subscript denotes majority coincidence of 3 out of 4.

The scintillation counter system also provides the following analogue information: elapsed time between S1 and S2 on a 50-nsec time scale, (TOF 1, 2); the pulse height in S1 (PH1); and the pulse height in S2 (PH2). At a later stage of the program additional time differences or pulse heights may be measured. The signal TOF 1,2 allows us to distinguish between particles of the same momenta but different masses.

The central unit of the system is the Master Gate, which gives an output pulse when the inputs satisfy the conditions stated above with a further constraint being the absence of a busy signal from the INHIBIT flip-flop (F.F.). The output of the Master Gate is then fanned out and shaped to perform the following functions.

a. It forms the WRITE GATE pulse which strobes the hit pattern into the individual F.F. associated with each wire.

b. It sets the INHIBIT F.F. which holds off further triggers until such time as the current event is stored.

c. It is used as the start pulse for the TAC's and to open the fast linear gates.

d. It strobes the ADC's which then begin conversion of the analogue signals.

e. It goes to the SPM as EVENT pulse to set the EVENT QUEUED F.F. which issues the ENCODE ENABLE signal to the MWPC and initiates the readout of the MWPC data into the SPM.

f. It is also scaled.

When all ADC's have completed conversion, a signal is sent to the Priority Interrupt Register to inform the MBD that an event is ready for servicing. The MBD then reads in the analogue information contained in the octal scaler, packing two ADC's per 16-bit word and buffering it in its own memory. The SPM is then interrogated and if all the wire addresses have been read into the SPM, the system is reenabled by resetting the INHIBIT F.F. and then the contents of the SPM are emptied into the MBD memory via a specially designed CAMAC input gate (Sec. 7).

Communication with the computer for the purpose of experiment control (start, stop, etc.) and monitoring (display of histograms, checking of various transducer outputs, etc.) is established via switch registers (not shown) in CAMAC. The required function is toggled into the switches and a LAM is generated by pressing a button on the switch register. The MBD then takes action appropriate to the specified function.

IV. MULTIWIRE PROPORTIONAL CHAMBERS

Multiwire proportional chambers have been described in the past in many articles of which the review of Charpak[3] is specially recommended. Our use of the MWPC follows proven practice of the scientific literature. In our application, MWPC's with wire spacing of 2 mm are used to provide spatial information on the particle trajectory. Their high rate capability and high efficiency are of great importance.

Figure 4 shows a scale drawing representing the MWPC chambers W1 through W3, all identical. These chambers are comprised of 7 G-10 fiberglass-epoxy laminate planes each 3/16 in. thick. Associated with each signal plane are two high-voltage planes. The printed circuit boards for signal or H.V. connections are cut from 3/32-in.-thick copper coated G-10 laminate and are bonded with an epoxy resin[4] into depressions milled into the appropriate G-10 planes. The specifications for W1, W2, and W3 (all identical) are as follows:

Dimensions of open area: 19.9 cm x 39.1 cm corresponding to 96 x 192 active wires.

Gap between sense plane and H.V. plane = 4.7 mm (3/16 in.).

Planes: G-10 fiberglass-epoxy laminate 3/16 in. thick. (The dimensions are chosen so that deformations due to the wire stress are negligible.)

Wires: Sense Wires:

Gold-plated tungsten, 20 μm diam.

Tension: 60 g weight.

Separation: S = 2 mm.

H. V. Wires:

Cu-Be, silver coated, 50 μm diam.

Tension: 160 g weight.

Separation: S = 1 mm.

H. V. isolation: 10 MΩ resistor between supply and groups of 32 wires.

Windows: 25 μm mylar sheets fastened with Scotch tape.

Gas Seal: Neoprene O-rings 1.5 mm diam.

The chamber W4 is similar to the W1-W3 series, except that it is larger as follows:

Dimensions of open area: 39.1 cm by 64.7 cm corresponding to 192 by 320 active wires.

Planes: Fiberglass-epoxy laminate 1/4 in. thick (6.35 mm).

Other aspects are the same.

We are making two sizes of MWPC's, namely the small size corresponding to W1-W3, and the larger size corresponding to W4. W1 and W2 could have been smaller, but this was not done in order to retain the benefit of interchangeability. It is planned to use fewer than the maximum number of wires in W1 and W2. The number of active wires to be used is as follows:

Chamber	No. Horizontal	No. Vertical	Sum
W1	64	96	160
W2	96	128	224
W3	96	192	288
W4	192	320	512
		Total	1184

Gas Mixture: For all chambers we expect to use the magic gas mixture developed at CERN[5] consisting of:

74.3-vol. % argon

25.0-vol. % isobutane

0.7-vol. % freon 13 B1

We expect to bubble the argon through methylal at -12°C as a measure to increase the effective lifetime in high-radiation fields.[6] This gas mixture allows us to run the chamber W1 at ≈3800 V.

Each MWPC chamber is located by means of two tooling holes (one being shown in Fig. 4) which provide position reference in the winding process and in the aluminum housing of the chamber.

The winding of our chambers takes place at LAMPF on a winding machine[7] which rotates the planes on a shaft such that the wire is wound on to the plane as a flat helix. The wire is drawn from a spool with frictional loading.[8] We have fabricated a special winding plate which fastens to the shaft of the winding machine. The plate carries tooling pins, such that the wires are wound parallel or perpendicular to the line defined by the pins. In this way we control the conformity of the wires from the winding process to insertion in the chamber housing. After the wires are wound, they are glued to the G-10 plane with an epoxy resin.[9] After hardening, the wires are soldered[10] and the plane may then be removed for cleaning.

V. THE AMPLIFIER/LOGIC CARD

The millivolt sized signals appearing on the individual wires must be amplified, shaped, and delayed to match the Master Gate conditions and transmitted in digital form to the encoding circuits. These functions are provided by the 8-channel amplifier/logic card which will sometimes be described by the term Module. The general function of the unit is based on the circuit described by Larsen.[11] Figure 5 provides a schematic diagram together with the corresponding time diagram.

The following functions are realized:

1. The comparator amplifier provides a TTL level output for the duration of time that the input signal exceeds the preset threshold.

2. A FAST DISCRIMINATOR OUTPUT signal is derived as an OR-ed function of any input which exceeds the threshold.

3. The shaped signal from the fast discriminator output also initiates a monostable element for a delay time during which the fast coincidence logic can make a decision on the validity of the event. The D-edge F.F. is activated if the Write Gate pulse from the Master Gate in the fast electronics overlaps the trailing edge of the monostable output. In our system, a monostable delay of 680 nsec is required. This value derives chiefly from 220 ft of signal cable between the spectrometer location and the electronics trailer.

4. When the D-edge F.F. is activated, a Module Active signal is issued indicating that one or more of the 8 channels is active.

5. The summed output of any monostable element from a given plane is available for inspection providing analogue information on the number of inputs that are activated in a given plane.

6. The gating of the information to the data bus is accomplished by a Module Select signal returned from the encoding electronics.

7. The module being encoded is cleared individually by the Module Clear pulse. This pulse is presented to all the modules of an active Super Module (refer to Sec. VI and the Appendix for definition of these terms) but is accepted only by the one that is currently active.

8. Finally, a Master Clear function is provided which can reset any and all modules of the entire system whether or not they are receiving Module Select signals.

It may be mentioned that all amplifier/logic cards and encoding electronics associated with each chamber are physically located within the aluminum housing of the given chamber. The chambers are connected to each other and to the SPM in the electronics trailer by a cable containing 16 data lines and 4 control lines. Each line is a twisted pair activated by balanced drivers and uses differential receivers. On each chamber is a common adjustment for threshold, mentioned in Item 1. above. The threshold offset for each comparator may be trimmed individually as shown in Fig. 5. There is also an adjustment at each chamber for the monostable delays.

VI. THE ENCODING SYSTEM

The essential feature of the encoding system is its hierarchical structure, a concept suggested originally by Kirsten.[12] The realization is facilitated by the availability of integrated circuit (e.g., Fairchild 9318) priority encoders which provide a 3-bit binary output in response to the highest of 8 inputs. When the highest priority

input disappears, the device gives an output corresponding to the next highest input, and so forth. The device also has an output signifying when any input is active. The priority encoder is used together with a decoder which can take the 3-bit code and activate the suitable one of the 8 outputs, and send back a signal to the source with highest priority for the purpose of enabling or gating data. In addition to its 3 inputs, the decoder has a fourth which gates it on, or enables it.

We have three levels or organization. The lowest level is the amplifier/logic card, called Module in the context of encoding. As described earlier, it services 8 wires and its output is an 8 bit pattern which is impressed directly on the 8-wire bus when the module is enabled by the Module Select signal. The next level of organization is the Super Module (SM) which consists of 8 Modules, a priority encoder (PE), and a decoder (see Fig. 6a). When one or more modules of the SM are active, the PE puts out a binary code corresponding to the address of the highest priority module. Module 6 has higher priority than Module 5, and so forth. The SM is enabled by receiving a SM Select signal at the fourth input of its decoder which then sends out a Module Select signal to the highest priority module.

An active SM priority encoder sends out a signal to the priority encoder of the highest level of organization, which is the Chamber (refer to Fig. 6b). The Chamber consists of 8 Super Modules with a total of 512 wires, a PE, and decoder. The Chamber also contains gating circuits that accept and transmit the Encode Enable signal from the SPM, line drivers, and a hard wired 2-bit code for chamber identification. The chamber PE and decoder service the 8 Super Modules in a fashion similar to what happens in the SM as described above.

An active chamber does not put out any MWPC data to the data bus until it receives an ENCODE ENABLE signal from the Scratch Pad Memory. When this occurs, the net result is to put 16 bits of information onto the data bus corresponding to the highest priority module in the chamber. Two bits relate to chamber designation, 3 bits provide Super Module identification, and 3 bits provide module identification, all of the preceding information being in binary form. The other 8 bits provide the hit pattern experienced by the 8 wires associated with the module.

The 16 bits of data make up a data word and are transmitted to the Scratch Pad Memory. This unit provides the Encode Enable signal and originates the Module Clear signal. The SPM will be described in greater detail in Section VII with a block diagram of the major functions in Fig. 7. In the following, reference will be made to certain functions of the SPM in relation to the encoding process prior to full explanation.

We shall now go through the encoding process in proper time order. The process begins with one or more charged particles traversing the spectrometer and giving rise to signals from scintillators and MWPC's which cause the Master Gate coincidence circuit to fire (refer to Fig. 3). The NIM Master Gate then issues an EVENT pulse which immediately sets the INHIBIT F.F. and also sets the EVENT QUEUED F.F. in the SPM. The following things now happen. First, the Encode Enable line goes high and, after a 1-μsec time delay, the first Module Clear pulse is sent out. Now, referring to Fig. 6b, the ENCODE ENABLE (ENC EN) level is stopped at, and enters, the first chamber in which at least one module is active. This occurs by action of the Chamber Active signal at gates in the ENCODE ENABLE line.

The following events now happen in the chamber. The ENC EN and CHAMBER ACTIVE signals form the CHAMBER SELECT. This signal activates the Tri-State output line drivers to the data bus and the appropriate 2 bits of Chamber code and 3 bits from the Chamber priority encoder are put on the bus. The CHAMBER SELECT signal activates the Chamber decoder which selects the highest priority Super Module, thereby gating the associated 3 bits to the now-open data bus. The SM decoder sends out the Module Select signal to the highest priority Module, thereby gating the 8 bit module hit pattern on to the data bus.

The first data word reaches the SPM in the electronics trailer after 1/3 μsec transmission time and waits to be read. It is strobed into (written into) the SPM by the first Module Clear pulse on its way out of the SPM. The Module Clear pulse finally traverses the distance between trailer and spectrometer, passes the open gate (Fig. 6b) into the active chamber where it seeks out and resets the

active module. At this point the module with the next highest priority is selected and puts its information on the 16 bit data bus. On entering the chamber, the Module Clear pulse immediately generates an Acknowledge Clear pulse which goes back to the SPM to perform the functions of incrementing the SPM address counter, writing the second data word into the SPM, and generating the next Module Clear pulse to reset the second active module. And so the system proceeds until all active modules have been read and reset.

At this point the Chamber Active signal goes low, thereby blocking entry of the Encode Enable signal into that chamber and allowing the ENC EN signal to proceed to the next active chamber. When data from the last chamber has been read, the ENC EN signal returns as Return Encode Enable (RTN ENC EN) to the SPM (refer to Fig. 7) where it causes the final Acknowledge Clear pulse to reset the EVENT QUEUED F.F. The MBD receives information of this condition by reading the status lines of the CAMAC Input Gate (refer ahead to Section VII). The MBD then instructs the CAMAC Output Register to reset the INHIBIT F.F. in the NIM system, and the system is again ready to accept a new physical event. The dead time of the system is defined by the average time the INHIBIT F.F. is set divided by the beam-on time of the macropulses.

VII. THE SCRATCH PAD MEMORY AND THE CAMAC INPUT GATE

The two circuits described in this section are special designs, the first to speed up data taking, the second input the data into the MBD through CAMAC.

A. The Scratch Pad Memory

One of the requirements of our system is the ability to take data of a few events during one macropulse. We use a fast intermediate buffer called the Scratch Pad Memory[13] (SPM) to speed the data acquisition. The time to record one event in the SPM is approximately 0.4 μsec plus round trip transmission time between the MWPC's and the location of the SPM which is 0.68 μsec in our case. It therefore is expected to take approximately 10.8 μsec to record 10 MWPC data words in our system. The saving of time derives from the fact that the SPM can operate during the time that the ADC's are running down and being accumulated in the octal scaler. The ADC's are 10-bit units working at 40 MHz, which implies ≤ 25 μsec run down time plus a little more for settling and reading into the MBD via CAMAC. As soon as the analogue data has been read and the SPM filled, the F.F. on the amplifier/logic cards will have been cleared, and the inhibit of fast coincidence functions lifted and the system is ready for a new physical event.

Figure 7 shows the logic block diagram of the Scratch Pad Memory. The main elements are an addressed memory of 32 words, an associated address counter which keeps track of the actual number of stored words, and two F.F. -- The EVENT QUEUED F.F. and the SPM Status F.F. -- which control the write and read process.

The EVENT Q'd F.F. is set by the EVENT pulse originating from the Master Gate in the NIM logic. Its output being high signifies that an event is waiting in the queue for encoding, or is in the process of being encoded. The output is used as ENC ENABLE signal. After having enabled the encoding at each chamber in turn, it returns to the SPM as a signal called RTN ENC ENABLE where it is used together with the ACK CLR to reset the EVENT Q'd F.F. Moreover, the output of the EVENT Q'd F.F. initiates the storage process into the SPM if the latter is empty, which can be seen from the presence of the MT signal issued by the Status F.F.

The status of the EVENT Q'd F.F. is part of the so-called SPM status word, which consists of 7 bits, 5 bits of the actual memory address, the EVENT Q'd bit, and the MT bit.

The SPM Status F.F. tells the CAMAC Input Gate (IN GT) when the SPM is filled, be it that the SPM is full (31 words stored, which is signaled by address 31 and the WRITE pulse of the last word) or that the encoding is completed, as signified by the ENC DONE signal (derived from RTN ENC EN). The Status F.F. changes level on receipt of one of these signals. The Input Gate, therefore, no longer gets an answer to its signal CHECK MT, which means that the SPM has valid data to offer. The read-out through the IN GT can proceed until the last word at address 1 has been read and acknowledged by TRANSFER ACK. This signal returning from the IN GT now decrements the address to 0 and the delayed TRANSFER ACK clears the Status F.F. The CHECK MT signal can then be returned again to the IN GT having

the meaning of an END OF BLOCK for the next word read.

The address counter is controlled in the following way.

The storage begins at addresss No. 1, with a special pulse "load 1" that sets the counter to 1. This happens when an event is signaled for further encoding by the EVENT Q'd F.F. and the SPM Status F.F. says that the SPM is empty. One μsec later the WRITE pulse strobes the first data word into the memory. This same pulse is used as MOD CLEAR, the pulse that resets the module whence came the first data word, and advances the encoding by one step. The MOD CLR returns to the SPM as ACK CLR. It is delayed 250 nsec to let the new data settle, and is checked by two gates which impose the considtions for the SPM still to be in its empty state and the RTN ENC EN not having returned yet. After passing these tests, the delayed ACK CLR increments the address counter and 80 nsec later writes the data word into the memory. It proceeds further as new MOD CLR to start the next step. This process goes on until the gate for the incrementing pulse is closed by RTN ENC EN and another gate opens to issue the ENC DONE pulse to the Status F.F.

For the read-out, the decrementing of the address counter is done by the TRANSFER ACK signal, which in essence is the S2 pulse of the CAMAC cycle in the IN GT. However, before allowing this signal to decrement the address counter an and-gate verifies that the address has not yet reached 0.

As already stated, the occurrence of the address 0 signifies the end of the read-out process. If the encoding had not been finished within the first 31 words, the second part of the MWPC words begins loading at this time. Otherwise the SPM is ready for a new event.

B. The CAMAC Input Gate

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The two circuits described in this section are special designs, the first to speed up data taking, the second input the data into the MBD through CAMAC.

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is pulsed, notifying the MBD (see Fig. 3). After reading the last register of the octal scaler, the SPM status is read via the IN GT and, when the SPM is found to be full, the MBD lifts the Inhibit level via the Output register, freeing the system for another event. Meanwhile, the read-out of the SPM ensues.

B. The second string of operations concerns the treatment of the MWPC data up to the point it is stored in the SPM. The Master Gate signal initiates that sequence of operations by sending the EVENT pulse to the EVENT Q'd F.F. The SPM immediately sends out the ENC EN signal and shortly thereafter the first encoded word arrives at the SPM. There it waits if the data of the previous event is still in the SPM. As soon as the MT signal appears, the storage process begins (Fig. 7). With the first WRITE (into SPM) signal also the first MOD CLR is created which returns with the next word as ACK CLR. After a delay of 250 nsec, this signal increments the address counter of the SPM and, after a further delay of 80 nsec, creates new WRITE and MOD CLR pulses. This process goes on until the last word is transmitted, and the EVENT Q'd F.F. is reset by RTN ENC EN. The Status F.F. is set indicating SPM FULL, which allows the MBD to lift the INHIBIT.

The data collection of the current event can now be terminated by the transfer of the MWPC words from the SPM through the IN GT to the MBD. The last-in MWPC word will be transferred first. The last transferred word is forced to value zero.

At this time the MBD checks to see if the number of words currently residing in its memory buffer is larger than some present value N_1. If so, it enables interrupts on another PIR input and the next end of macropulse will trigger a block transfer of the contents of the MBD buffer to the PDP-11/20. If not, then the MBD exits and waits for another event. This allows transfers to take place while the beam is off. If the number of words in the buffer exceeds some number $N_2 > N_1$, than a transfer is initiated immediately rather than wait for an END of Macropulse.

One may ask when the system is ready for a new event. This is the case when the encoding is done. At that moment, the Status F.F. goes to SPM FULL, and the MBD reenables the system. If a new event appears while the MBD is reading out the SPM, the new MWPC data will wait on the amplifier/logic cards until the SPM is empty, the analogue data waits in the octal scaler, and the LAM waits in the PIR until the MBD has finished with the previous event.

IX. PERFORMANCE OF A PROTOTYPE MULTI-WIRE PROPORTIONAL CHAMBER SYSTEM

In order to better understand the problems associated with MWPC sonstruction and operation, a complete prototype chamber with its housing and encoding electronics was built and extensively tested before proceeding with the fabrication of the final system. This section contains some of the results obtained from the tests made with the prototype system.

A. Description of the Prototype Chamber

The chamber consisted of two mutually perpendicular signal planes with 64 wires each with wire spacing S = 2 mm. The gap width between the signal and high voltage wires was 4.76 mm. The signal wires were 20-μm-diam. gold-plated tungsten. For the high-voltage planes, three different types of wires were tested: a) 75-μm-diam. nickel wire, b) 100-μm silver-plated copper-beryllium wire, and c) 50-μm silver-plated copper-beryllium wire. The 50-μm copper-beryllium wires were used in the final design since no appreciable difference in chamber performance was noted for the different H.V. wires.

One peculiarity of the prototype design was the fact that only three H.V. planes were used; hence the two signal planes shared a common H.V. plane. This allowed an investigation of the influence on chamber performance of the orientation of the H.V. wires with respect to the signal wires. No difference was observed between the configuration in which the wires of both H.V. planes seen by a signal plane were either parallel or perpendicular to the signal wires. Some problems were experienced, however, in the configuration where the wires of one H.V. plane were parallel and the other perpendicular to the signal wires.

The use of the so-called magic gas mixture 74.3% argon, 25% isobutane, 0.7% freon 13B1 was adopted. It has been noted previously that a larger isobutane percentage lowers the pulse height, but also reduces the multiplicity of adjacent wires firing. This conclusion is consistent with our observations.

The use of methylal[6] as an additive to avoid polymerization of the isobutane and freon will probably be necessary in the high intensity LAMPF beams. We are not yet able to prove the advantages of this ingredient. However, we observed on one occasion that, with its introduction, the knee of the efficiency plateau shifted towards higher voltages by ~ 300 V. The plateau length did not change, contrary to the results reported in Ref. 10.

B. Results of Measurements on the Prototype Chamber

A collimated beta source and two thin plastic scintillation detectors rigidly connected together and capable of being moved in two dimensions over the sensitive area of the chamber were used to investigate some of the properties of the chamber. Figure 11 gives a schematic view of the setup. Those properties of particular interest to us were efficiency and uniformity of response, although we made measurements on the timing characteristics as well.

1. Chamber Efficiency. Using a collimated beta source (^{207}Bi), we measured the efficiency of the chamber which we define for the horizontal plane, $\varepsilon_H = \frac{H \cdot V \cdot S1 \cdot S2}{V \cdot S1 \cdot S2}$, where H and V represent the horizontal and vertical planes, and similarly for the vertical plane. The results are shown in Fig. 12. Efficiencies of 99.7% were routinely obtained with high voltages above 3.5 kV. Also shown is a plot of the singles counting rate as a function of H.V. The shape is the same as is normally observed.

2. Uniformity of Response of the Chamber. Figure 13 shows the result of efficiency measurements made at different positions in the chamber. Aside from a decreased efficiency at the extreme edges of the chamber, the chamber response was found to be uniform to within a fraction of a percent.

3. Spatial Resolution of the Chamber. Figure 14 shows the results of a wire number spectrum for a given location of the collimated source and scintillator trigger system. Wire Nos. 0-63 correspond to the vertical plane and 64-127 to the horizontal plane. The widths of the distribution are consistent with the size of the collimators used for the measurement.

4. Time Response of the Chamber. By using the signal from S1 as a start pulse for a time-to-amplitude converter and taking the first fast discriminator output for a given plane as a stop pulse, the time spectrum of an entire plane was obtained as shown in Fig. 15. The shape and position of the peak changes with chamber high voltage, in accord with an explanation based upon decreased electron drift times with increasing high voltage.

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We acknowledge the direct support of the LASL Physics and Electronics Divisions to the realization of this project. The help of I. Bijarchi in fabrication and procurement has been indispensable to our progress. We have had useful conversations and assistance from D. Lee, and from E. R. Martin at an early stage of the development.

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7. We are indebted to Dr. R. E. Mischke of MP-Div. for putting at our disposition the LAMPF winding machine. Many thanks are due to M.P. Dugan for help with the winding work.
8. At the time of writing, we are changing to wire loading by hysteresis motor. Measurements by resonant wire method indicate an improvement in spread of tensions among the wires.
9. We used an epoxy composed of Shell Epon 828 resin (50% by weight) + Versamid 140 catalyst (50% by weight) + 8 drops Cyanamide Beetle 216-8 wetting agent for every 20 gms of mixture. We are are indebted to E. Eaton of CMB-6 for help in choosing this composition.
10. For soldering signal wires we use: DIVCO 276 lead free solder (melting temperature 430°F), Division Lead Co., Sommitt, Ill.; H.V. wires are soldered with ordinary soft solder.
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13. D. Brown, paper submitted to the 1973 IEEE Symposium on Nuclear Science.
14. LASL E-Div. CAMAC module No. 3003 developed by D. Brown and A. Greenwood.

APPENDIX

GLOSSARY OF ABBREVIATIONS FOR THE MWPC ELECTRONICS SYSTEM

ACK CLR - Acknowledge clear (Chap. VII, Figs. 6,7). Signal derived in the MWPC from MOD CLR, that returns to the SPM initiating the next storage operation.

CHAMBER - (Fig. 6b). Ensemble of the encoding elements, supermodules and modules. It can consist of a maximum of 8 supermodules. In our case, it coincides with any one of the physical chambers W1 to W4. Its address is given by 2 bits, which are issued to the data-bus with the SM and MOD address.

CHECK MT - Check empty (Chap. VII, Figs. 7, 8). Signal issued by the IN GT to sense the status of the Status F.F. Its return, END OF BLOCK, signifies the end of valid data.

ENC EN - Encode Enable (Figs. 2, 6, 7, 8, 9).
With SPM: The ENC EN signal is issued by the EVENT Q'd F.F. in the SPM after receipt of an EVENT signal. It is issued to all MWPC's in turn enabling the encoding. Its return clears the EVENT Q'd F.F. and sets the SPM status F.F. to full, indicating the SPM is ready for read-out.
Without SPM: Signal now issued by the IN GT to the MWPC's to encode the data. It is daisy-chained (Figs. 2, 6b) through all MWPC's and its return (RTN ENC EN) indicates that the encoding is done.

END OF BLOCK - (Figs. 7, 8). Signal derived from CHECK MT when the SPM Status F.F. is in the empty state. Its reappearance after the read-out of the SPM means the end of valid data.

EVENT - (Figs. 2, 7, 9). Signal issued by the Master Gate to the EVENT Q'd F.F. in the SPM. It signals the presence of a valid event.

EVENT Q'd - Event queued indicates that there is data in the Module F.F.'s waiting to be transferred to the SPM.

FAST OUT - (Chap. II, Figs. 2,3). Signal issued by each MWPC plane separately to the majority gates in the NIM logic (Fig. 3) indicating the MWPC plane being active.

IN GT - CAMAC Input Gate (Chap. VII, Figs. 2, 8, 9). Interface between MWPC and CAMAC or Scratch Pad Memory and CAMAC.

LAM - Look At Me (Fig. 9).

MAST CLR - Master Clear (Figs. 6, 7). Signal activated in the IN GT by push-button or CAMAC command F(9), Z or C; resets all F.F.'s.

MBD - Micro-programmed Branch Driver. (Figs. 2, 9). Interface between CAMAC and PDP 11/20.

MOD - Module (Chap. V, Figs. 5, 6a, 10). Lowest element in the encoding system, also called Amplifier/logic card; a group of 8 modules forms a supermodule. A selected module issues an 8-wire pattern unencoded on the data bus. Its address is encoded by a supermodule and issued by that one on the data bus.

MOD ACT - Module Active, signal issued by any active module (Fig. 6a).

MOD CLR - Module Clear (Chap. V, Figs. 6a, 7, 8).
With SPM: Signal derived from the WRITE pulse that strobes data into the SPM. The signal is issued to all modules of a selected SM but resets only the one that had been selected to give its information on the data bus.
Without SPM: Signal issued by the IN GT which acts as reset signal as described above.

MOD SEL - Module Select (Fig. 6a). Signal enabling a module to impress its 8 bit pattern on the data bus.

MT - Signal from Q-output of the SPM Status F.F. which indicates that the SPM is ready to accept data. The opposite condition of the F.F., FULL, indicates that the data in the SPM is ready to be transferred to CAMAC.

MWPC - Multiwire Proportional Chamber (Figs. 1, 2, 4, 9, 10).

PE - Priority Encoder (Figs. 6a, 6b). Integrated circuit used to transform highest of 8 inputs to a 3-bit binary address.

PIR - Priority Interrupt Register (Chap. IX, Fig. 2). The CAMAC module that issues a LAM signal on receipt of the EVENT signal from the Master Gate on its first entrance. A second sub-unit is used to initialize data transfers to the PDP 11/20 at the end of a beam macrocycle when the MBD buffer is sufficiently filled.

RTN ENC EN - Return Encode Enable (Figs. 2, 7, 8, 9). ENC EN signal returned to the SPM or IN GT.

With SPM: In this configuration, the RTN ENC EN clears the EVENT Q'd F.F. and sets the Status F.F. to full. This means that the encoding is done and the SPM readout can begin.
Without SPM: As soon as the signal arrives from the daisy-chain, it stops the Q signal, which signifies the end of valid data.

SM - Supermodule (Chap. VI, Fig. 6b). Second level ensemble in the encoding hierarchy. It consists of 8 molules and is a subensemble of the next bigger ensemble, the CHAMBER. If selected, it issues in turn the coded addresses of its modules on the data bus (3 bits).

SM ACT - Supermodule Active (Fig. 6b). Signal issued by SM priority encoder.

SM SEL - Supermodule Select (Fig. 6b). Signal issued by the chamber decoder.

SPM - Scratch Pad Memory (Chap. VII, Figs. 2, 7, 9).

TRANSFER ACK - Transfer Acknowledged (Figs. 7, 8). S2 part of the CAMAC command F(0)A(0) in the IN GT, sent back to the SPM, to tell it that the data have been read. This signal decreases the address counter in the SPM, if this one has not yet arrived at 00000. In this latter case, it clears the Status F.F.

WR GT - Write Gate Signal (Fig. 2).

FIGURES

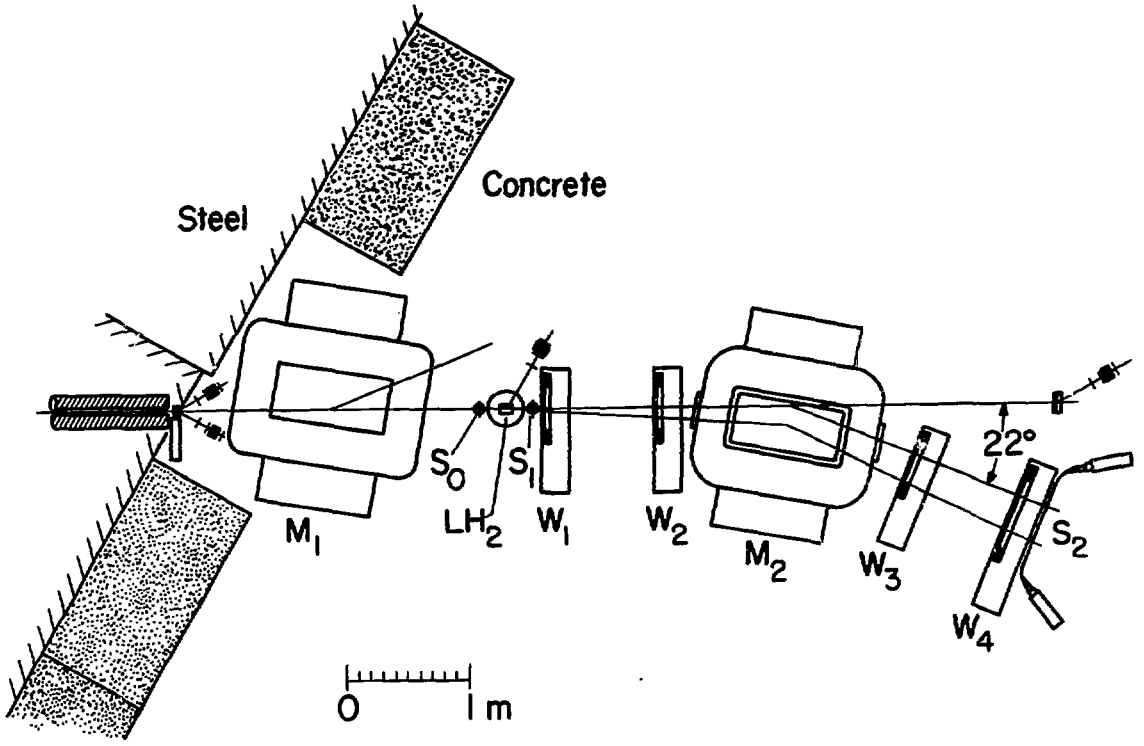


Fig. 1. Plan view of the spectrometer as it will be set up in the neutron beam at the Nucleon Physics Laboratory at LAMPF.

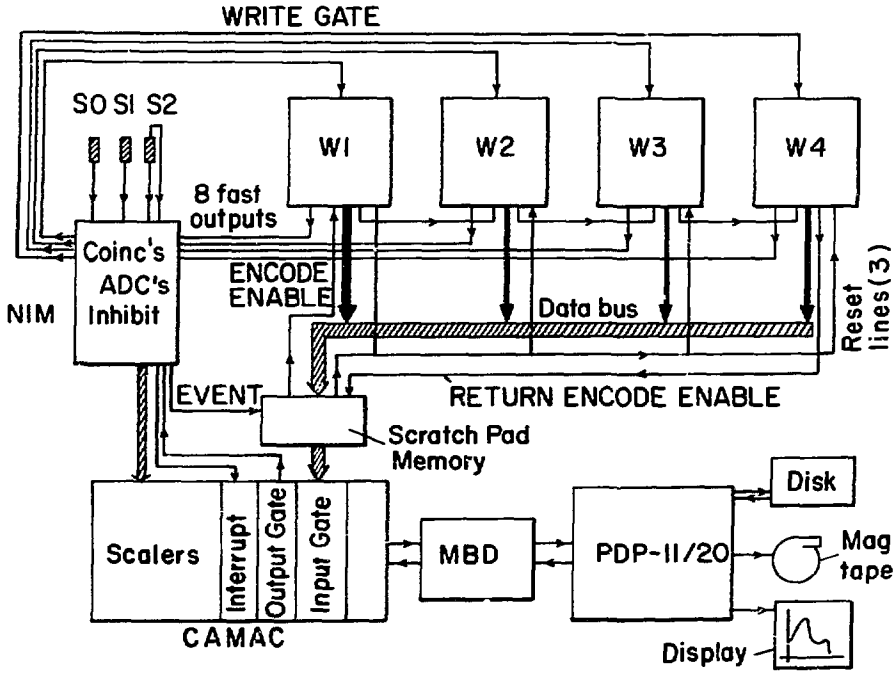


Fig. 2. Block diagram of the data collection system.

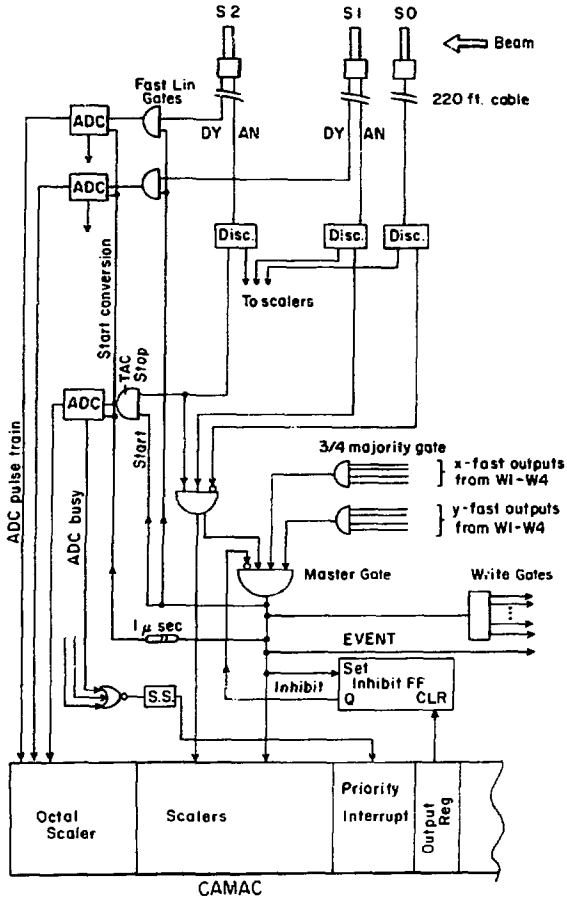


Fig. 3. Schematic diagram of the fast logic and analog electronic system.

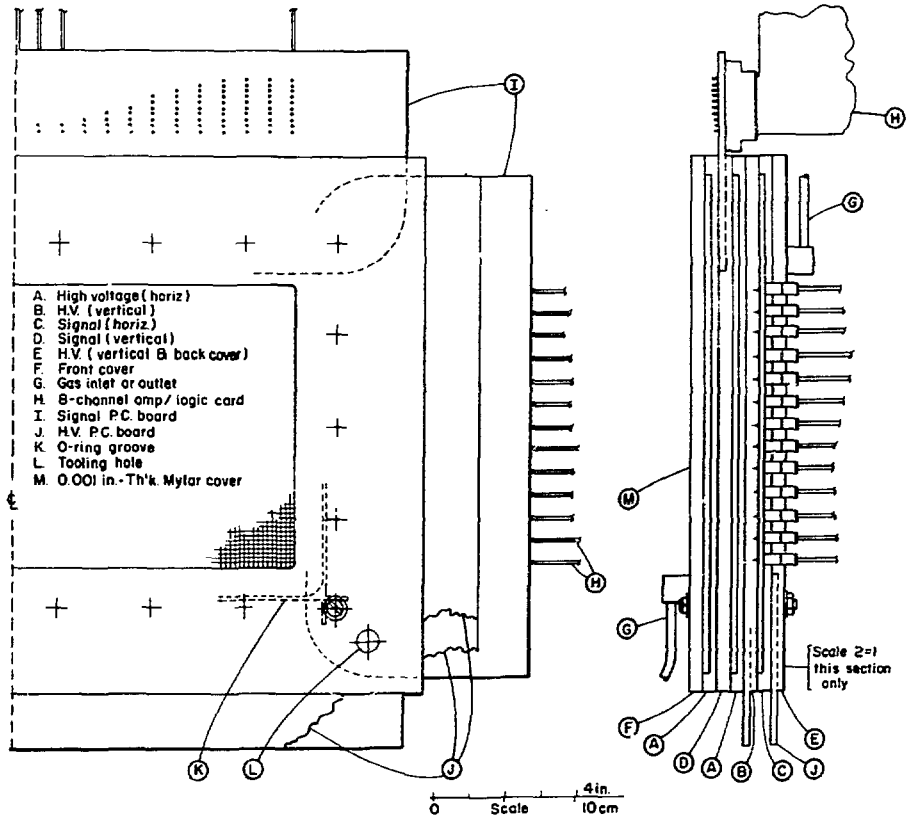


Fig. 4. Scale drawing of one of the MWPC W1 through W3. Half of the front view of the G10 planes is shown.

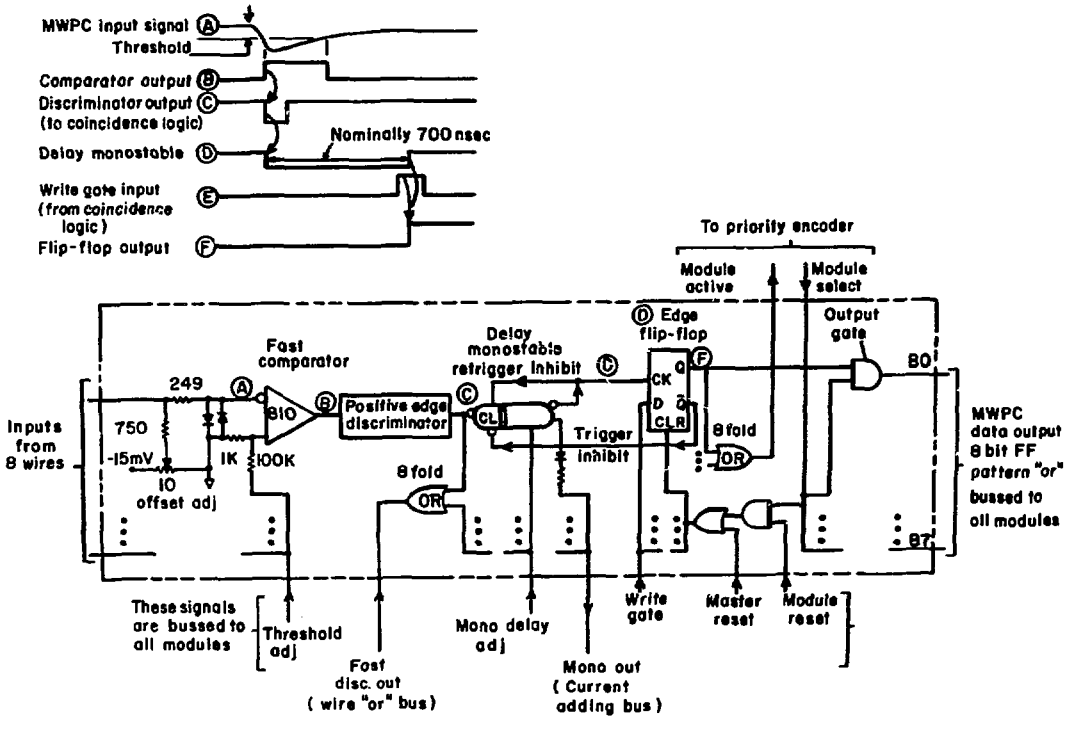
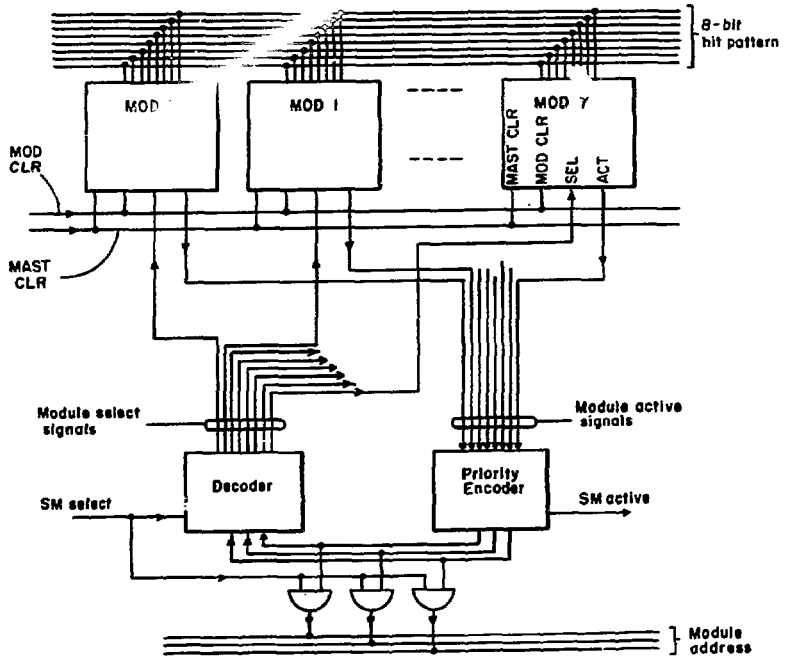
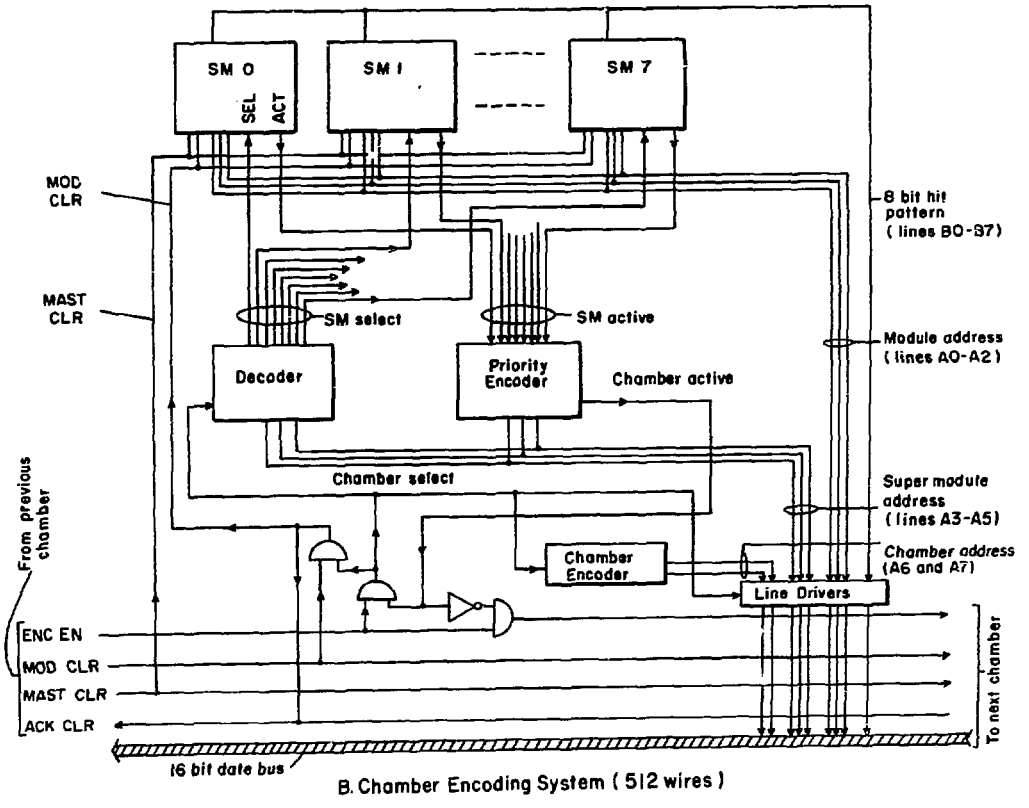


Fig. 5. Schematic diagram of one channel of 8-channel amplifier/logic card with timing diagram.



A. 64 Wire Super Module Encoder



B. Chamber Encoding System (512 wires)

Fig. 6. Schematic diagram of the encoding system.

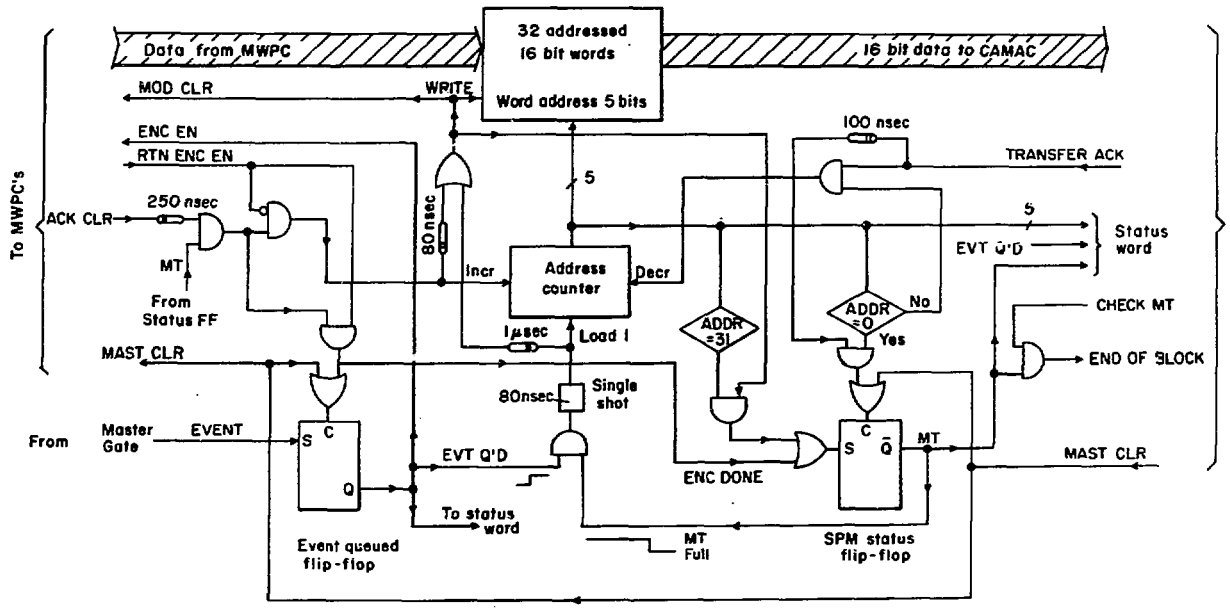


Fig. 7. Schematic diagram of the Scratch Pad Memory.

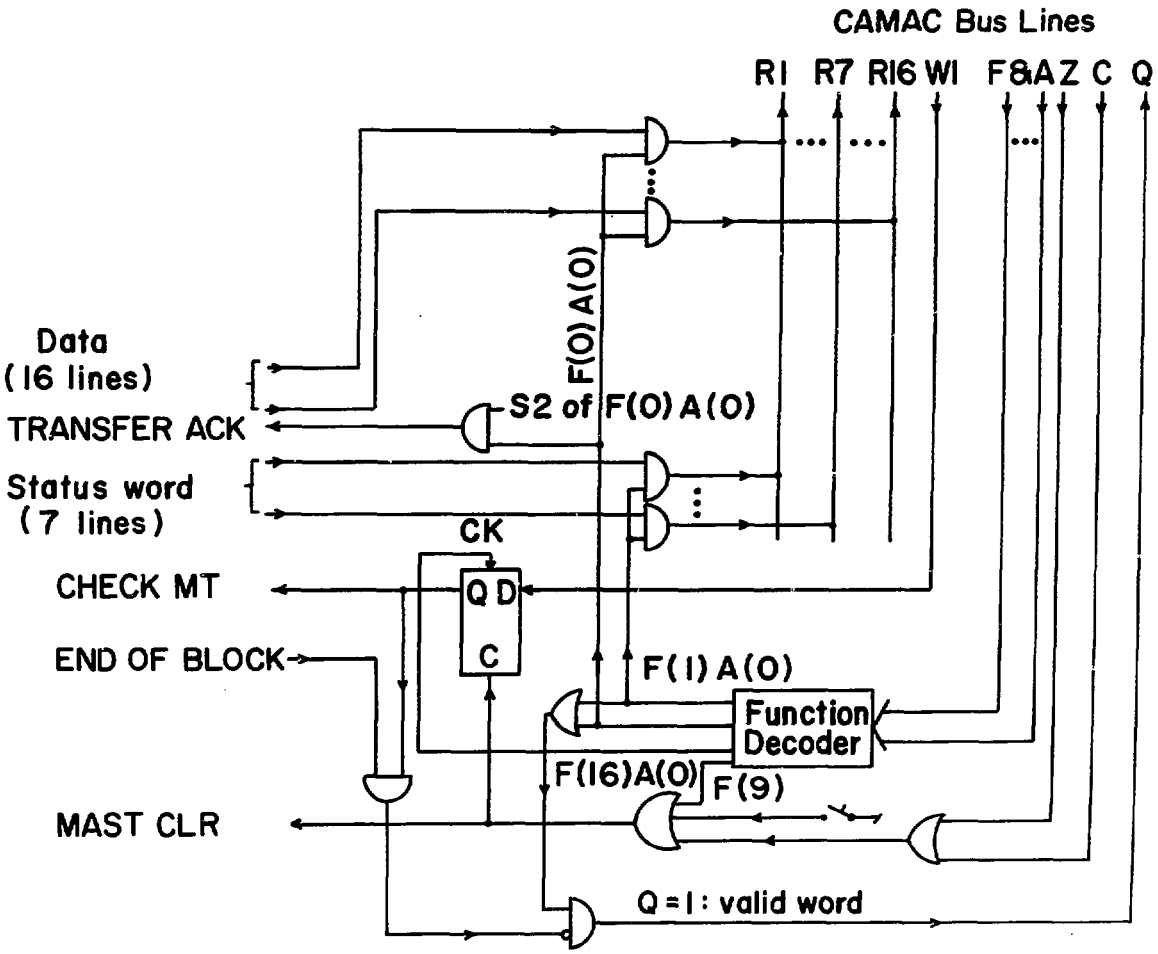


Fig. 8. Schematic diagram of the CAMAC Input Gate.

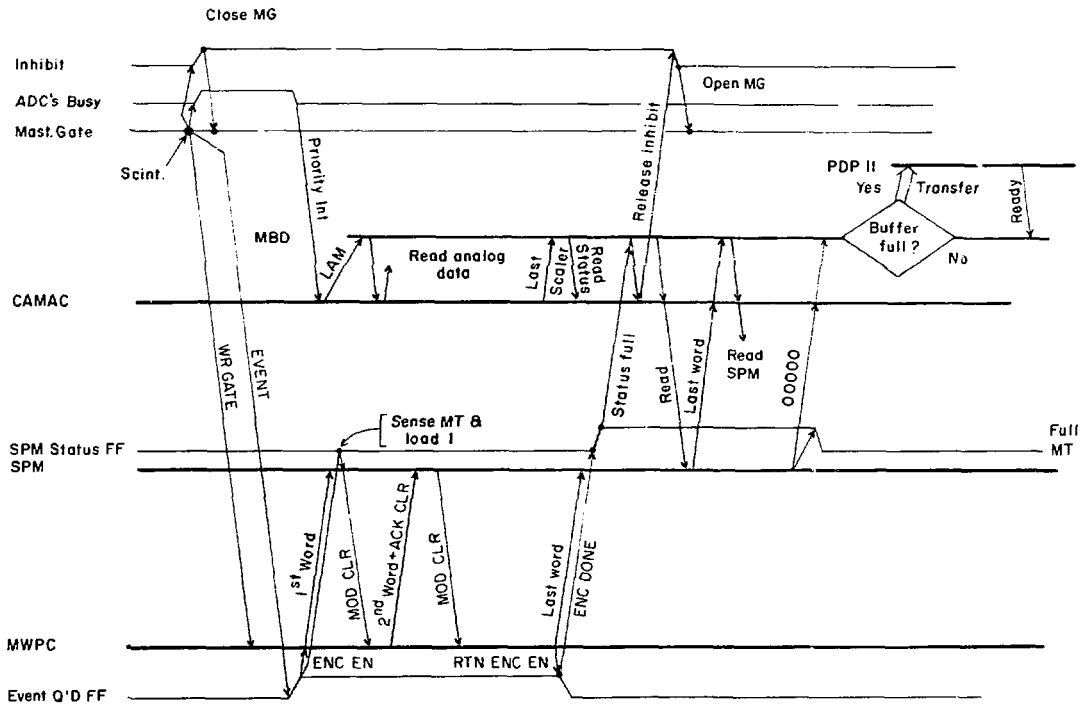


Fig. 9. Time table of the data collection process.

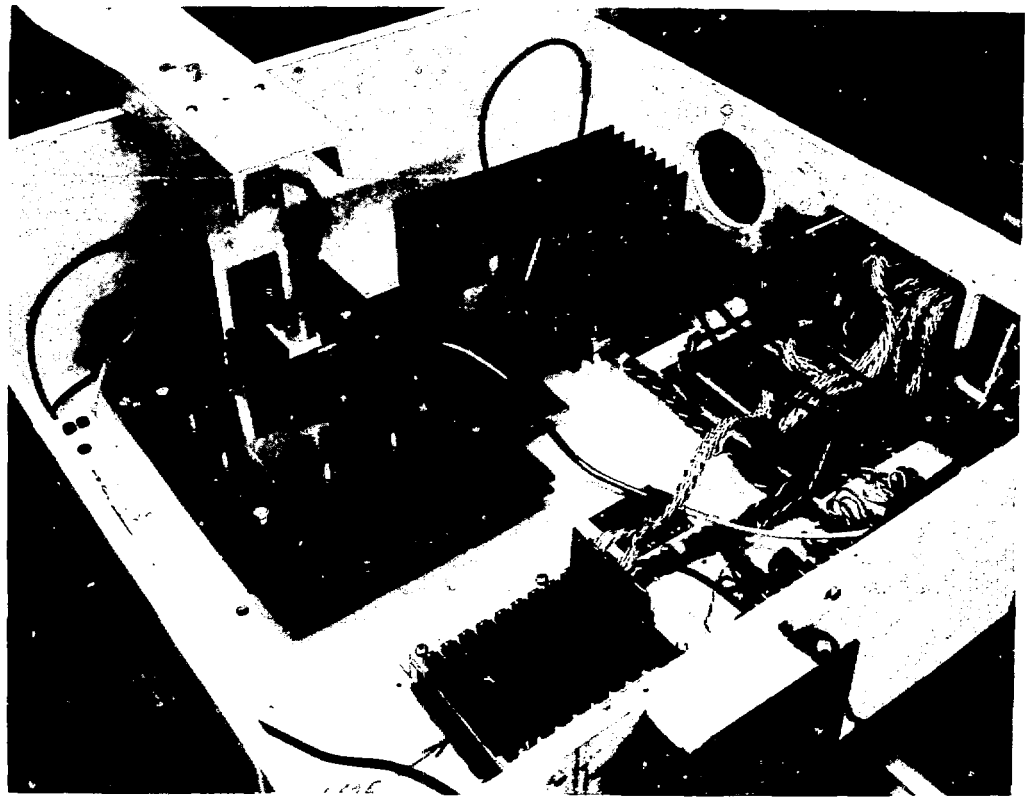


Fig. 10. Photograph of protype chamber in its housing.