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A CMOS Variable Gain Amplifier for PHENIX Electromagnetic Calorimeter and RICH Energy Measurements*

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Abstract

A variable gain amplifier (VGA) has been developed for equalizing the gains of integrating amplifier channels used with multiple photomultiplier tubes operating from common high-voltage supplies. The PHENIX lead-scintillator electromagnetic calorimeter will operate in that manner, and gain equalization is needed to preserve the dynamic range of the analog memory and ADC following the integrating amplifier. The VGA is also needed for matching energy channel gains prior to forming analog sums for trigger purposes. The gain of the VGA is variable over a 3:1 range using a 5-bit digital control, and the risetime is held between 15 and 23 ns using switched compensation in the VGA. An additional feature is gated baseline restoration. Details of the design and results from several prototype devices fabricated in 1.2- μ m Orbit CMOS are presented.

I. INTRODUCTION

Very wide dynamic range energy measurements are possible with scintillation or other detectors using photomultiplier readout. In many cases, the range possible with the photomultiplier exceeds the capabilities of the electronics. For the electromagnetic calorimeters planned for PHENIX, the dynamic range of energies to be measured is 20,000:1, and it is difficult to make multi-channel, compact integrated circuits that allow measurement of energies over such a wide range. If the photomultipliers and/or detectors vary in gain, then even more dynamic range is needed. For most detectors of this kind, the gains are matched by using an individual programmable high-voltage supply for each photomultiplier. These high-voltage supplies are considerably more expensive than bulk high-voltage supplies and a distribution network. If the gains of the different channels can be equalized in the electronics with no loss of dynamic range, then considerable cost savings can be realized for a detector with thousands of channels.

Of the many detectors planned for PHENIX, three (lead-glass electromagnetic calorimeter, lead-scintillator electromagnetic calorimeter and RICH) will use similar electronics for energy or charge and timing measurements, and energy-sum formation for trigger generation. Energy (or charge in the RICH case) measurements from these detectors will be made by integrating the signal from the

photomultipliers (or a fast preamplifier in the case of the RICH), sampling the integrator output at the beam clock frequency using an analog memory and double correlated sampling of the appropriate samples following digitization. This method was used successfully for the WA98 lead glass calorimeter [1].

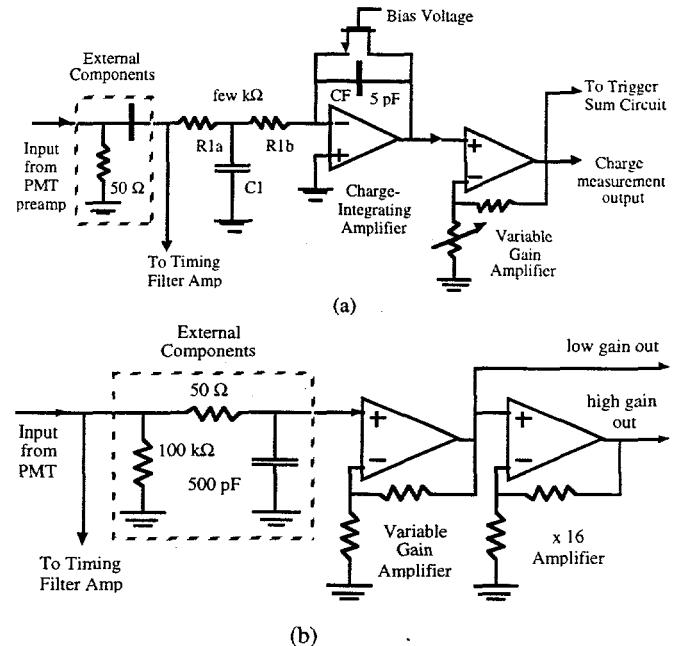


Fig. 1. (a) Active integrating amplifier system. (b) Passive integrating amplifier system.

Two types of integrating amplifier architectures have been investigated for these PHENIX applications [2]. The active integrating amplifier system shown in Fig. 1(a) was used in WA98 and will be used for the RICH detector. The RICH detector will use a fast gain-of-10 preamplifier following the photomultiplier tube. That preamplifier will drive a long cable, so it is important that the integrator provide a proper 50-ohm termination like that provided by the circuit of Fig. 1(a). A passive integrator amplifier system like that shown in Fig. 1(b) is being developed for the two electromagnetic calorimeters. The integration of the charge is performed externally to the integrated circuit (IC), which results in improved noise performance relative to the active integrator circuit using comparable amplifiers; however, the termination is not suitable for long cables. These amplifier systems will be implemented as 4-channel ICs that will also include constant-fraction or leading-edge discriminators, time-to-amplitude converters, DACs, etc. The dual gain ranges are required to get the needed dynamic range. It is planned to use

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an 11- or possibly a 12-bit ADC with high and low gains (separated by a factor of 8 or 16) to give a dynamic range of 16,000, which is slightly greater than the needed energy range.

For the lead-scintillator detector, bulk HV supplies will be used, and it is planned that a simple screening of the photomultiplier tubes will allow grouping into sets exhibiting no more than a 3:1 variation in gains. Thus the variable gain amplifier (VGA) must be capable of adjusting the electronics gain over a 3:1 range, or else dynamic range will be lost for some channels, as the ADC does not have excessive range. The VGA must also equalize the gains prior to summing channels and discriminating on the result to provide local or global energy sum triggers. The HV supplies for the lead-glass calorimeter already exist, so the VGA is not absolutely required for that application, but may be useful. For the RICH detector, the needed dynamic range is much less (250:1), but gain matching is needed for charge sums for trigger formation.

II. VARIABLE GAIN AMPLIFIER CIRCUITS

There are a number of requirements for the VGA beyond adjusting the gain over a 3:1 range. For the energy (or charge) sum circuitry, the gains must be matched to about 6%. For discretely programmable gains, there would need to be a minimum of 21 different gains since $1.06^{20} = 3$. Since the sums must be made and discriminated on every bunch crossing (~ 106 ns), the VGA output must rise and settle in considerably less time. Based on simulations of the trigger-sum processing circuits, the VGA must have a maximum 20 ns risetime for all gains. The VGA must have an output dynamic range greater than 3 V to match the analog memory unit (AMU) and ADC, and an output offset voltage (from both low and high gain channels) less than 100 mV to preserve AMU/ADC dynamic range. This corresponds to an input offset of 0.5 mV. The wideband equivalent input noise voltage spectral density of the VGA must be less than $6 \text{ nV/Hz}^{1/2}$ to limit the rms output noise to less than 1 least-count of the ADC for the high gain range.

A simplified schematic of the VGA is shown in Fig. 2. Gains are digitally controlled (5 bits) from 4 to 12 by selecting combinations of fixed resistors which are switched in or out. The switched resistors are binary-weighted, which gives evenly spaced steps in resistances, but produces larger steps in gain at the minimum gain than at the maximum. The maximum incremental gain step is 6%. Ideally, the gains would be controlled by resistor ratios, which are quite accurate; however, the CMOS transmission gates used as switches have non-zero impedances. The switch impedances were designed to be less than 10% of the fixed resistor to minimize the gain uncertainty. Also, the switch impedances were binary-weighted to preserve the binary weighting of the overall resistor network and therefore preserve the smooth variation of gain steps. This was done by scaling transistor sizes in some cases and using multiple switches in parallel in others. Another advantage of this configuration, with one side of the switches grounded, is that there is very little gain variation with output voltage. The output voltage can range over nearly the full supply voltage, but the range of voltages seen by the switch is limited first by the voltage division between the opamp output and input and then by voltage division between the fixed

resistor and the switch. This is important because the CMOS switch impedance will change with the applied voltage and therefore the gain would change, resulting in non-linearity. Calculations indicate that the worst case gain change would be less than 0.5%.

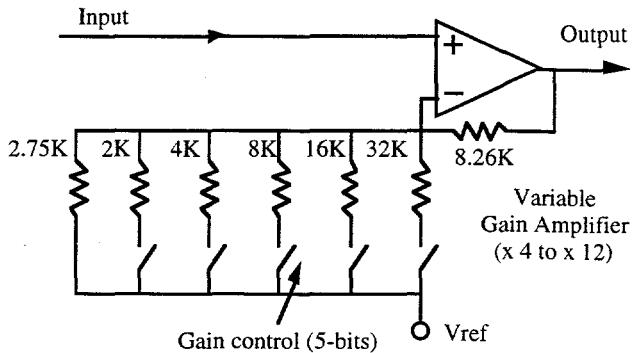


Fig. 2. Variable gain amplifier block diagram.

The Amp11_v4 opamp (Fig. 3) used in the VGA is basically a two-stage design with an additional gain path (M3-M9-M10-M7) that improves the negative slew rate. NMOS input devices are used to allow biasing the input near the positive supply voltage. This is needed for the passive-integrator implementation, where the input to the VGA is basically a negative step and biasing that input near the positive supply allows a large output dynamic range. The nominal bias current is 60 μA which results in a calculated power dissipation of 8.7 mW (at 5V). The opamp is compact and occupies an area of 123 μm by 198 μm . A version of this opamp differing only in having fixed compensation is used in the x16 stage of the passive integrator circuit.

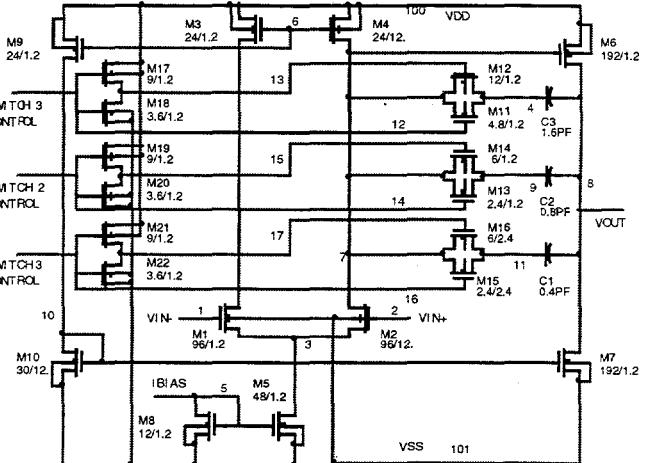


Fig. 3. Amp11_v4 opamp schematic.

In order to maintain the same risetime as the gain is varied, the opamp gain-bandwidth product must be adjusted. This is accomplished by programming the amount of capacitance used for compensation. As shown in Fig. 3, any combination of three compensation capacitors (0.4, 0.8 and 1.6 pF) may be switched in to compensate the opamp. The switches (M11-M12, M13-M14 and M15-M16) also do double duty as series

resistances and were adjusted to improve the opamp's phase margin.

Fig. 4 shows the simulated small-signal risetime for the VGA as a function of the 5-bit gain code and the 3-bit capacitor code. A gain code of 11111 represents all the gain switches closed and produces a nominal gain of 12. A capacitor code of 111 represents all the capacitance switched in and results in the longest risetime for a given gain. From Fig. 4, it can be seen that by choosing the right capacitor code, the risetime can be kept between 10 and 20 ns for all possible gain settings. Lower risetimes are not desirable due to increased noise bandwidth, while the maximum is dictated by the trigger-sum processing requirements.

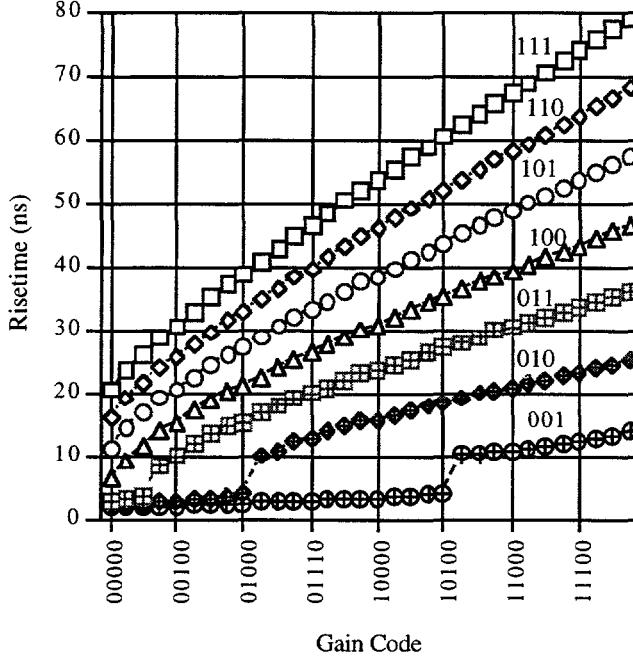


Fig. 4. VGA small-signal risetime as a function of gain and capacitor code.

Fig. 5 is a photograph of the VGA integrated circuit. The resistor network can be seen at the top left with the switches below, while the opamp is at right. The VGA is 507 μm wide and 224 μm high.

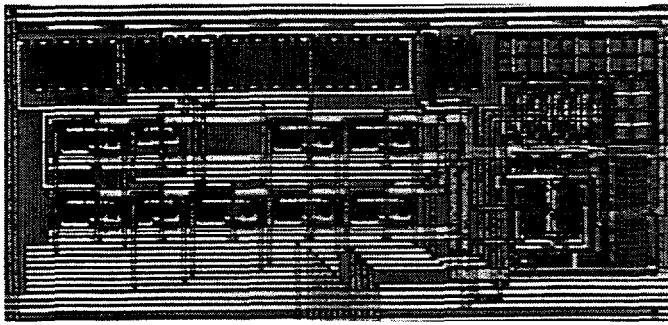


Fig. 5. Photograph of VGA.

For the passive integrating amplifier system shown in Fig. 1(b), the VGA is followed by a $\times 16$ amplifier. This results in

a combined dc gain which can be as much as $12 \times 16 = 192$. Even a 2-mV input offset for the VGA could then result in an unacceptable 0.4-V offset on the high-gain output. As shown in Fig. 6, a gated dc feedback loop is used to reduce the effective input offset voltage. The baseline is restored during scheduled reset times.

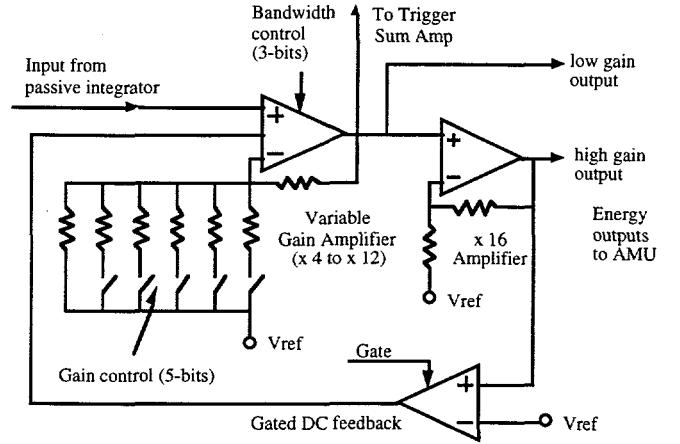


Fig. 6. VGA, $\times 16$ amplifier and dc feedback loop.

The circuit shown in Fig. 7 was used to analyze the noise performance of passive integrator, VGA and high-gain stage. To allow algebraic solution of the problem, a number of simplifying assumptions were made. It was assumed that the noise of the high gain stage would be negligible compared to that of the VGA. It was also assumed that the bandwidth of the high-gain stage would be considerably less than that of the VGA and that the correlator would be noiseless. Also, it was assumed that the $S_n(\omega)$, the equivalent input noise power spectral density of the opamp used in the VGA stage would be white, i.e., there would be no $1/f$ term.

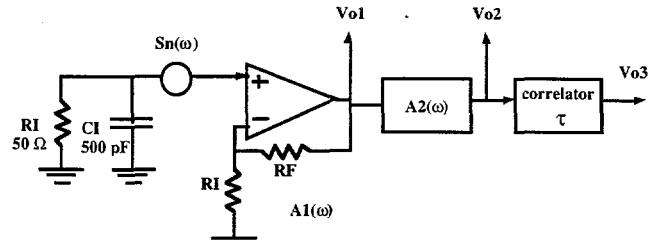


Fig. 7. Passive integrator circuit for noise analysis.

Let

$$\omega_0 = 1 / (R_I C_I), \quad (1)$$

$$A_1 = \frac{R_F + R_I}{R_I}, \quad (2)$$

$$A_2(\omega) = \frac{A_2}{1 + j\omega / \omega_2}, \quad (3)$$

and

$$S_n(\omega) = \overline{e_n^2}. \quad (4)$$

It is also assumed that $\omega_0 \ll \omega_2$. Defining $S_{no2}(\omega)$ as the noise power spectral density at the output of the second amplifier and calculating gives

$$S_{no2}(\omega) = \left[\left(\frac{4kTR_I}{1 + \omega^2/\omega_0^2} \right) A_1^2 + \overline{e_n^2} A_1^2 \right] \left(\frac{A_2^2}{1 + \omega^2/\omega_2^2} \right) + 4kTR_I \left(\frac{R_F^2}{R_1^2} \right) + 4kTR_F. \quad (5)$$

Butler [3] gives the noise transfer function for a double correlated sampler as

$$|H_N(\omega)| = |2\alpha \sin(\omega\tau/2)|, \quad (6)$$

and the signal transfer function as

$$|H_S(\omega)| = |\alpha|. \quad (7)$$

For the case where the baseline is subtracted from the signal, $a=1$. The output noise power spectral density at the output of the correlator is then given by

$$S_{no3}(\omega) = S_{no2}(\omega) H(\omega) H^*(\omega) = S_{no2}(\omega) (4 \sin^2(\omega\tau/2)) \quad (8)$$

Thus

$$S_{no3}(\omega) = 4 \sin^2\left(\frac{\omega\tau}{2}\right) \left\{ \frac{k_1}{1 + \omega^2/\omega_0^2} + \frac{k_2}{1 + \omega^2/\omega_2^2} \right\} \quad (9)$$

where

$$k_1 = 4kTR_I A_1^2 A_2^2, \quad (10)$$

$$k_2 = A_1^2 A_2^2 (\overline{e_n^2} + 4kTR_x) \quad (11)$$

and

$$R_x = R_I R_F / (R_I + R_F). \quad (12)$$

The mean-squared output noise voltage is

$$\overline{e_{no3}^2} = \int_0^\infty S_{no3}(\omega) d\omega. \quad (13)$$

Evaluating the integral gives

$$\overline{e_{no3}^2} = 2 \left\{ k_1 \frac{\pi\omega_0}{2} (1 - e^{-\omega_0\tau}) + k_2 \frac{\pi\omega_2}{2} (1 - e^{-\omega_2\tau}) \right\}. \quad (14)$$

This equation reduces to

$$\overline{e_{no3}^2} = 2 \left\{ k_1 \frac{\pi\omega_0}{2} + k_2 \frac{\pi\omega_2}{2} \right\}, \quad (15)$$

if the correlation time approaches infinity. Thus the noise power is simply twice (due to two samples) the wideband noise due to the various white noise sources. The double correlated sampling process at worst doubles the noise, but can reduce it from that level, depending upon τ .

For the circuit shown in Figs. 1(b) and 2, A_1 is nominally 4, A_2 is 16, $R_I=100 \text{ k}\Omega$ and $C_I=500 \text{ pF}$. The bandwidth of the

high-gain amplifier is approximately 8 MHz. This was chosen to allow the amplifier to respond quickly enough to allow sampling with $\tau = 100 \text{ ns}$; however, the nominal value for τ is 200 ns in order to make certain the pre- and post-samples do not include the transition. To obtain the desired dynamic range (16000:1), the rms noise level of the high-gain channel after correlation should be no more than 3.5 mV rms, based upon a 3.5 V output dynamic range. Eq. 14 can then be used to calculate k_1 and then the term $(\overline{e_n^2} + 4kTR_x)$ equals $12 \times 10^{-16} \text{ V}^2/\text{Hz}$. This requires the opamp to have an input noise spectral density on the order of $10 \text{ nV}/\text{Hz}^{1/2}$ or less, and this result was used as a design aid. Eq. 14 also reveals that the noise due to the passive integrator (k_1 term) is insignificant for the components, sampling times and bandwidths chosen for this application.

III. RESULTS

Fig. 8 shows the measured gain and the percent increase in gain relative to the next lowest gain for every possible gain code. The gain increases monotonically with the code, and the steps are very nearly as calculated. Only one step exceeded the desired 6% level and that step was only 7%.

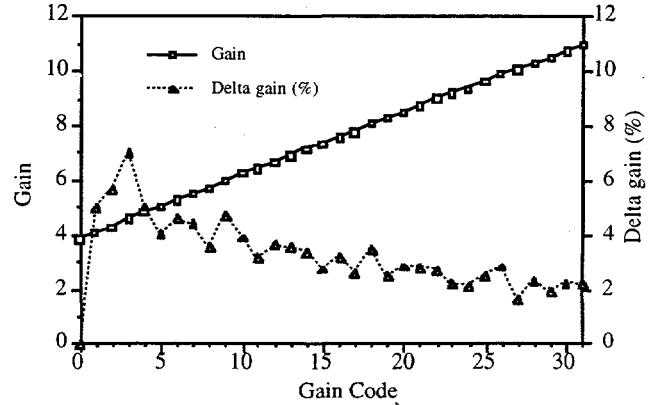


Fig. 8. VGA gain as a function of gain code.

Fig. 9 shows a typical plot of the VGA output as a function of the input for the minimum gain setting. Based on oscilloscope measurements, the integral non-linearity appears to be better than 1% over a 3.5 V range.

Fig. 10 shows the measured VGA small-signal falltime for every possible combination of gain code and capacitor code. Risetimes were very nearly the same as falltimes. Compared to the simulated results of Fig. 4, the actual amplifier was about 20 % faster. The proper choice of capacitor combinations allows the risetime to be kept between 15 and 20 ns over most of the gain range.

The dc feedback circuit was tested and found to be functional. Prototypes without the dc loop had high-gain output offsets as large as 2 V. With the dc restoration circuit gated on continuously, the output offsets of both the high-gain and low-gain cases were typically reduced to less than 25 mV. When operated in a pulsed mode, the dc feedback could return a 0.5 V output level to near zero in 2 μ s.

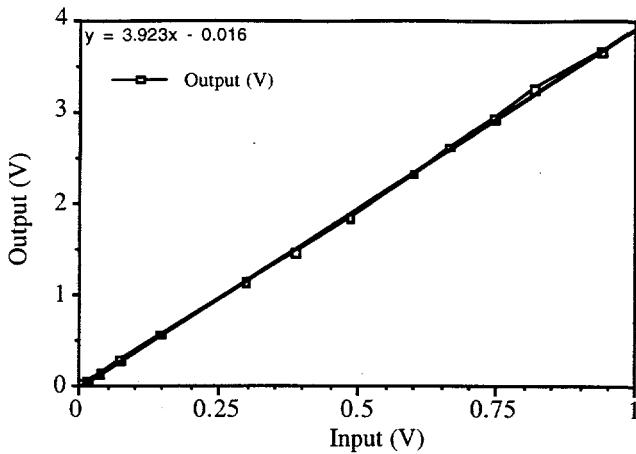


Fig. 9. VGA output as a function of input voltage.

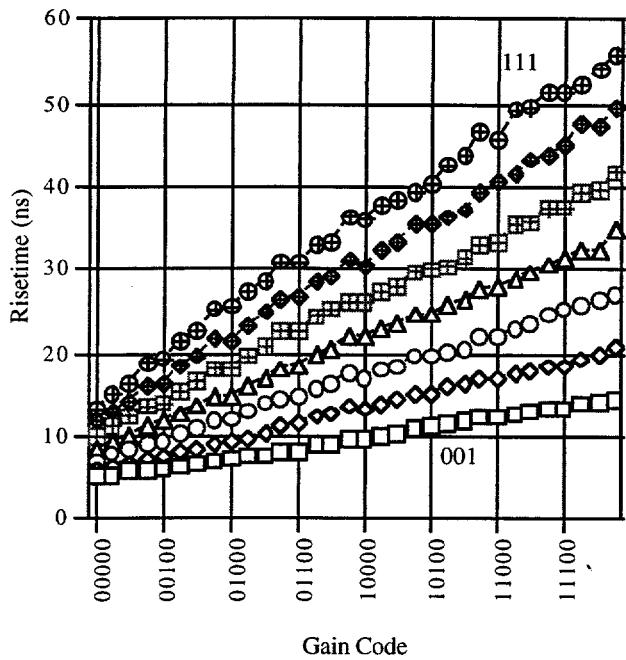


Fig. 10. Measured VGA small signal falltime as a function of gain and capacitor code.

The output noise of the variable gain amplifier was measured using an HP 3589A spectrum analyzer, and the wideband rms noise was computed by numerically integrating the spectrum up to 50 MHz. The test fixture had a noise floor of 0.23 mV rms, which is sufficiently low to allow measuring amplifiers with output noise in the few mV rms range. The capacitor code of the variable gain amplifier under test was adjusted to a give a risetime as near 17 ns as possible for the gain selected. In practice, this meant that the risetime was held between 10 and 20 ns. The VGA output noise (low-gain) was less than 0.63 mV rms for all gains tested. The high-gain output noise measurements were compared to SPICE simulations of the circuit, and these results are given in Table 1. In most cases, the measured noise was about 25% greater than that predicted by the simulation. This is quite reasonable agreement given the uncertainties in the modeling

of the transistor noise characteristics, and the gain and the bandwidth of the circuits.

In PHENIX, the output from the amplifiers will be sampled and double-correlated. Both the simulations and the spectrum analyzer reveal a considerable 1/f component to the output noise spectrum. As shown in Table 1, the simulated noise after correlation ($\tau = 200$ ns) is slightly less than the wideband noise. The mathematical analysis which neglected the 1/f noise did not indicate this reduction.

Table 1
VGA plus high-gain stage output noise.

Gain code	Cap code	Nominal gain	Noise (simulated)	Noise after correlation	Noise (measured)
			mV rms	mV rms	mV rms
00000	111	4	2.4	2.4	3.0
00100	111	5.04	2.8	2.7	3.6
01000	101	6.07	3.3	3.2	4.2
11000	011	10.2	5.2	4.7	6.3
11111	010	12	6.1	5.5	7.4

IV. ONGOING WORK

Several VGA developmental efforts are continuing. A version using an opamp with a PMOS input stage which will allow operation with the input biased near the negative supply voltage is being developed for the RICH detector. Also, prototypes of a fixed-gain amplifier using an opamp with lower noise characteristics have been fabricated and tested for use in the passive integrator circuit. A VGA using this amplifier will also be investigated.

V. CONCLUSIONS

The VGA prototypes designed for the PHENIX calorimeters have exhibited the range of adjustability in gain and bandwidth needed. The output dynamic range of the VGA and the x16 gain stage are sufficient, and the dc loop operates as expected. The output noise levels are sufficiently low if the gain is programmed near 4; however, improvements need to be made for the higher-gain configurations.

V. REFERENCES

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