A MODULAR MULTI-WORD READOUT SYSTEM FOR PROPORTIONAL WIRE CHAMBERS*

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SUMMARY

This paper describes the design features of a data readout system for multi-wire proportional chambers. The electronic circuitry for this "amplifier-per-wire" system has been designed in modular form to provide ease in system assembly, flexibility, and economy. Fast readout of the hit-pattern data is accomplished by using priority encoder integrated circuits for address generation and bit-parallel transfer of the output data words. About 7000 channels have been implemented using this system and an additional 4000 channels have been ordered. An analysis of cost per channel is given, based on the experience gained thus far.

INTRODUCTION

Recently there have been a substantial number of experiments utilizing multi-wire proportional chambers. For those unfamiliar with this type of particle detection, it consists of an array of parallel fine wires suspended in a gas mixture between two negatively charged grids so that a particle passing through the array of wires will cause a signal to be generated on the nearest adjacent wire.[1] This signal is caused by an avalanche of collision electrons drifting to the wire. The signal amplitude is typically of the order of several millivolts across 750 Ω and <100 ns in duration. Two adjacent and perpendicular arrays of these wires will provide means for locating the X,Y coordinates of any particle passing through the chamber. With this scheme, however, there may be four possible X,Y coordinates indicated if, for example, two particles pass through the chamber simultaneously. If it is required to determine the coordinates of more than one particle passing through a chamber at the same time, a common method of eliminating positional ambiguity is to add a third plane, the wires of which are at an angle to the wires of both the first and second planes.

Circuitry must be provided to amplify the low-level signals, discriminate between signal levels and noise levels, provide a time discrimination between desired and undesired signals, convert the signals to digital form, and transmit these data in an efficient manner to a storage device for subsequent processing by a computer.

Basically, the objective of the readout electronics is to identify the wires of a proportional wire chamber that produce electrical pulses following the passage of one or more particles. The logic identifies these wires by generating digital numbers signifying their location. In accordance with common logic parlance, these numbers are called addresses, an address being the digital representation of the location of a group of wires.

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OUTPUT DATA FORMAT

Efficient readout operation is achieved by organizing successive wires of the array into groups of eight. Every group of eight wires is then assigned an address. By combining this N-bit address of a particular group of eight wires with eight bits that represent the hit pattern on these wires, the output word structure shown in Fig. 1 is generated.

Wire groups which are not hit during an event do not generate the N-bit address and are not read during a readout sequence. The number of words is therefore variable, dependent upon the number of hits in each event and their distribution in the chambers.

The format of the output data for an event, then, is a serial set of these words with only as many words in the set as there are eight-wire groups which have had any hit pattern. There are no restrictions imposed by the readout electronics on the pattern or number of hits in an array of wires for each event. By virtue of the fact that all wire groupings having no hits registered are "skipped over," the time required to transfer the data for a given hit pattern from the proportional wire chamber (PWC) array to the receiver depends only on the number of wire groups involved in the event.

The readout operation is controlled by ADVANCE signals from the Receiving Device. (CAMAC, MIDBUS, and buffer memory have been used.) The system can respond to these signals and provide output data at a rate exceeding one word per microsecond.

SYSTEM OPERATION

A general system diagram is shown in Fig. 2. This indicates how a number of physically separated chambers can be linked together in a so-called "daisy chain" arrangement. The details of the box labeled "AMPLIFIERS, STORAGE & OUTPUT WORD GEN." will be described below.

Figure 3 is a more detailed block diagram showing the data flow and functions performed at the first chamber location.

The amplifier/comparators receive signals from the chamber wires and convert those exceeding a preset threshold to levels compatible with the following TTL circuitry. Shapers provide a uniform pulse output which triggers an associated delay one-shot multivibrator and also may be used as a FAST OUT signal to the accept/abort logic. If the event is acceptable, a WINDOW GATE signal occurs in coincidence with the end of the one-shot delay time, and the hit pattern is recorded in the Storage Registers.

The above functional elements are contained on one printed circuit board in an organization similar to

that described by Larsen,[2,3] Dhawan,[4] Lindsay,[5] and others. Design consideration was given to compatibility with hybrid devices providing these same functions.

As indicated earlier, addresses are generated to identify the locations in the wire array of each group of eight wires which has registered any hit pattern. This is accomplished with priority encoder integrated circuits[6] (e.g., Fairchild 9318) which sequentially generate the addresses of eight-wire groups with increasing order from one edge of a chamber to the other and from one chamber to the next. The first level of priority encoders generates the three low-order bits of the address, i.e., the address of an eight-wire group within a "section" of eight groups; there is one such encoder for each section containing eight groups of eight wires. A second level of priority encoders generates the next most significant three bits of the address. These three bits designate the address of the section containing the eight-bit group being transmitted to the receiving device.

Additional bits are generated for the most significant part of the address by encoding a "pointer" bit which advances through the "daisy chain" of interconnected chamber positions as the readout progresses. Look-ahead logic is utilized here to allow the pointer bit to skip over any chamber positions not having stored hits with a minimum of propagation delay. The skipping feature is an inherent property of the priority encoders used for scanning for the lower order bits.

The readout electronics at each chamber location in a system also includes output selection logic and three-state Line Drivers which sequentially transmit as many output data words as are necessary to document the hit pattern. These words are placed on a Data Bus connecting all chambers to the Data Receiver.

The generation of successive output words is under control of the receiving device, which sends an ADVANCE signal to the chain of chamber readout electronics each time it is ready to accept a new word. Typically, these advance pulses can be about 800 ns apart, but this figure may be higher, depending on the experiment layout and the rate at which the receiving device can accept data. When all words have been read, a signal is sent to the WINDOW GATE logic indicating that the chambers are ready to record a new event.

SYSTEM MODULES AND PHYSICAL ORGANIZATION

Circuit boards with active components are removable and interchangeable within a given experiment or from one experiment to another. This feature enhances the flexibility and economy of the system and provides easy trouble-shooting and repair when required.

Modularity within the system is provided on three levels: (1) "daughter" boards which contain amplifier/comparators, delays, registers, and logic serve a group of eight wires; (2) "sections" of eight daughter boards serve 64 wires; (3) "mother" boards holding eight sections of daughter boards serve 512 wires.

Daughter Boards

Figure 4 is a photo of the daughter board. It is designed to plug into two card edge connectors. The first connector (for inputs) is usually mounted on an extension of the proportional wire chamber and carries the wire signals onto the daughter board. This arrangement of two connectors serves two purposes: (1) it provides an efficient means of interconnecting three elements of the system, and (2) it provides a good separation of input and output signals.

Figure 5 shows a simplified diagram of one of the eight channels on the daughter board. Signal detection for each wire is accomplished by the use of 710 comparators. These devices have typical gain of 1000, making them suited to amplifying microampere signals to levels compatible with TTL circuits. Uniformity of thresholds to within ±0.25 mV is obtained in the following manner. The comparators are tested under simulated circuit conditions and sorted into bins, each representing a maximum input offset differential of 0.50 mV. Test data of 4000 units show voltage offsets from -6.5 mV to +6.5 mV with the distribution peak near zero mV. Eight of these graded devices taken from a common bin are loaded onto a daughter board which is then adjusted in a tester (all eight channels) for absolute zero input offset ±0.25 mV. The lower threshold limit of the daughter board input circuitry is approximately 0.75 mV. At this level the 710 comparator is biased slightly into the active region. Caution in regard to electrical grounding must be exercised to utilize the maximum sensitivity.

The comparators sharpen the rise time of the chamber wire signals which are then made available as "FAST OUT" signals to drive "Accept/Abort" logic circuitry used to select only the desired events for storage and subsequent readout. The FAST OUT signals are available as the OR function of all eight channels on a board. They are also available as individual channel signals at a flat ribbon cable connector at the top edge of the board (the latter signals can be utilized as inputs to a coincidence matrix[7] for determining an acceptable particle trajectory). The Accept/Abort logic also receives other signals which the experimenter provides, and if all signals meet the acceptance criteria a "WINDOW GATE" signal 50 to 75 ns wide is generated.

Following each comparator there is a delay one-shot which is triggered by the leading edge of the comparator output signal. This delay allows time for the accept/abort decision to be made. When the trailing edge of the delay one-shot signal occurs within the acceptance time of the WINDOW GATE, a record of the hit is stored in the flip-flop register. Most spurious signals that the comparators may respond to do not pass the external selection criteria and are aborted for lack of WINDOW GATE signal. Adjusting the delay one-shots to a tolerance of ±1% makes it possible to keep the WINDOW GATE signal short. This adjustment is done on an automatic tester[8] which determines the value of a trimming resistor.

Once an event is stored, a data readout cycle ensues. Each daughter board that has stored one or more bits provides a DATA PRESENT signal via an eight-input OR gate from any of the eight storage register flip-flops to a priority encoder circuit. Each of these first-level encoders have one input from each of eight adjacent daughter boards. They are located on the "module address boards" described in the next section.

Other control signals brought onto the daughter board are TEST, RESET, READ, MASTER RESET, AMPLIFIER GATE, and MONO TIMING, which is used as a "vernier" control of all one-shot delays tied to this line.

Groups of eight adjacent daughter boards are called "sections" for organizational purposes.

Module Address Boards

For each section of eight modular daughter boards (64 wires) there is a plug-in address-generating printed circuit board called a Module Address Board. As described earlier a priority encoder integrated circuit is used on each of these boards to generate the least significant three bits of the address part of the output word, i.e., the binary address of one group of eight wires in a section of 64 wires. This board also contains logic which controls the sequence of hit-pattern readout of the successive daughter boards within the section by enabling the open collector output gates of only the daughter board being addressed and by steering a RESET pulse to that board after its data have been received. After the register on one daughter board has been reset, the priority encoder advances to the next daughter board containing stored hits, skipping all empty boards in between.

Output Boards

There is one output board for every eight sections of eight daughter boards (serving a total of 512 wires). This board contains three-state balanced line drivers and line receivers for interfacing with other chambers in the system and with the data receiving device. On this board there is also one more priority encoder for generating the second group of three address bits (2^3, 2^4, 2^5) of the output word. These three bits identify the section from which a hit pattern is being read.

Switches are provided on the output board to set up additional (most significant end) address bits which are asserted when the hit pattern being transmitted is coming from the local chamber daughter boards. The output board contains two bridged cable sockets by which many chambers can be "daisy chained" together and connected to the receiving device. An ENABLE signal sent from the receiving device when it is ready to accept an output data word will enable the three-state line drivers of the first output board in the daisy chain which has hit-pattern data available. While the data is being read from this first-to-be-read output board, the same ENABLE signal that activates this first board also propagates through the daisy chain until it detects the next output board which has data to transmit. The actual enabling of this next set of output line drivers, however, is not done until the completion of readout from the previous output board is signalled by a READY line common to all of the output boards. By means of this "look ahead" technique, cumulative line receiver, line transmitter, and gating delays along the daisy chain are avoided.

Mother Board

All of the above boards, i.e., the daughter boards, module address boards, and output boards, are installed in sockets contained on a large "mother board" which is itself "sub-modular" in that it can be cut between each section of eight daughter board sockets to provide for chamber sizes smaller than the 512 wires which a full mother board will handle. On the other hand, these boards can also be placed end-to-end with no gap in the wire spacing to accomodate larger chambers. The socket spacing for the daughter boards is based on a 2-mm chamber wire spacing. Since each daughter board handles eight chamber wire signals, the center-to-center spacing of the sockets is 16 mm and the full 512-wire mother board length is 1.024 meters. There are no components other than printed circuit board sockets and a few wire jumpers mounted on the mother boards.

Physical Organization

The arrangement of the readout electronics for various experiments will vary considerably from one application to another. However, the general organization is to have one end of the daughter boards plugged into sockets mounted directly on an extension of the wire chamber, i.e., along one edge of each plane of wires. This provides the input signals to the daughter boards. A mother board is then located in juxtaposition with the row of inout sockets and provides the sockets for the outputs of the daughter boards. Figure 6 is a photograph showing the relationship between a chamber, the daughter boards, address boards, output board, and mother board. Figure 7 shows an arrangement of the three planes and readout electronics with respect to each other. In this experiment the mother board has been split into three parts each containing two sections (128 wires). Note that one output board serves all three segmented parts of the mother board.

Chamber wire spacing of 1 mm can be accommodated by placing mother boards on both sides of the chamber and bringing even wires into one mother board array and odd wires into the array on the opposite side. On small chambers, a fan-out of the chamber output leads can also be used to bring the mother board spacing down to a wire spacing tighter than 2 mm.

As mentioned earlier, a number of chambers may be interconnected by a "daisy chain" cabling arrangement as shown diagramatically in Fig. 2. The cable length from the last chamber to the receiving device on current installations ranges from about 50 feet to over 150 feet. The cable used is 25 twisted pairs with the exception of the lines for the FAST OUT and WRITE GATE signals, which are coaxial.

STATUS

Three systems have been built utilizing the modules described. They include two with 1500 channels and one with 4000 channels. Daughter boards for 4000 channels in new systems using some of the techniques here are on order. Results on the present installations have indicated that the design objectives have been met. New installations are requiring progressively less systems engineering time and virtually no electronic design time except where new interfaces to external equipment are required.

AUTOMATED BOARD TESTING

It was realized early in the development of this system that with the volume of daughter boards to be produced and with the stringent requirements on their operation, some form of semi-automatic test stand would be required if costs were to be kept down. A tester has been designed and built[8] which provides the following operations:

1. Performs a go-no-go test of all functions on questionable boards.

2. Performs diagnostic tests to indicate area of failure.

3. Analyzes the delay characteristics of each

channel and indicates the closest trimming resistor value for the required delay time.

The tester is controlled by an IBM 1130 computer but may be used in a manual mode if the computer is not available.

Since we have experienced a new-board rejection rate as high as 30%, we have found this tester to be extremely valuable in analyzing and correcting problems. About 13 minutes per board is allowed for trimming the eight one-shots and performing the go-no-go test. This is an average figure for a run of boards; an individual board can be completed in a shorter time. The cost analysis below includes dollar amounts for testing and trimming all boards as well as for diagnostics and repair of bad boards.

A manual tester is used for the module address boards and the output boards are tested in the final system since there are very few of them.

COSTS

The component parts cost (not including assembly labor) for a 4096-wire readout system amounts to approximately $5.50 per channel. This is for daughter boards, module address boards, output boards, and mother boards (output). Labor costs for the above boards (including testing daughter boards) will vary in different circumstances. For us it comes to about $3.00 per channel. The costs are broken down in the following table.

SYSTEM COMPONENT COST ANALYSIS -- PER CHANNEL

System Component	Labor per Chan.	Material per Chan.	Total per Chan.
1. Daughter board assembly	$1.25*	$4.31	$5.56
2. Daughter board test and trim	.66		.66
3. Daughter board 710 grading	.15		.15
4. Daughter board diagnose and repair	.38		.38
Daughter board total	$2.44	$4.31	$6.75
5. Module address board assembly	.09	.41	.50
6. Module address board test	.02		.02
Module address board total	$ .11	$ .41	$ .52
7. Output board asm.	.22	.26	.48
8. Mother board asm.	.10	.50	.60
Total cost for all of above components	$2.87	$5.48	$8.35

*Outside vendor labor costs.

These costs do not include system assembly and checkout which with these modular components can frequently be handled by people in the experimenters group. Recurring engineering costs on new experiments are minimized through utilization of existing hardware and system designs. The costs do not include the chambers, mounting hardware, inter-chamber cabling, or power supplies, since the requirements for these items can vary greatly from one experiment to another. Power supply costs can be kept low by using central high-current raw supplies with regulators located at each chamber.

SYSTEM VARIATIONS

Several variations to the system as described above have either been built or proposed. As an example, one system has been built which has a 32-word (expandable to 64-word) scratch-pad memory built into the CAMAC computer interface. This reduces dead time of the system between two successive events by allowing fast transfer of data from the PWC to the scratch-pad memory and subsequent transfer at a slower rate to the computer. Another implementation of this technique for reducing readout related dead time between two successive events could be to add a second level of storage flip-flops on the daughter cards at a slight increase in cost per channel.

Front-end dead time between successive events could be minimized by dividing the delay one-shot into two steps.

A 4000-wire system incorporates a variation of the daughter board in which the one-shot delay has been replaced by the transmission delay in 200 ft of flat ribbon cable between the chamber and the storage and readout electronics. This technique[9] avoids the inherent dead time resulting when undesired signals trigger the one-shots on the standard board. The 710 comparators in this case were followed by line drivers which drove signals on the flat cable to the balance of the readout system which, other than the daughter boards, used the same modular components as the basic system. A minor modification on the output board allowed us to accomodate 16 channels per daughter board instead of 8. The output boards (one per mother board) are built with wire-wrap IC sockets and thus can be economically adapted to meet special requirements such as these.

In some cases it is desirable to have the output data words represent simply the address of each wire hit. The eight-bit hit pattern is then converted into one or more binary subaddresses which are scanned with the same skipping techniques used for the other address bits.

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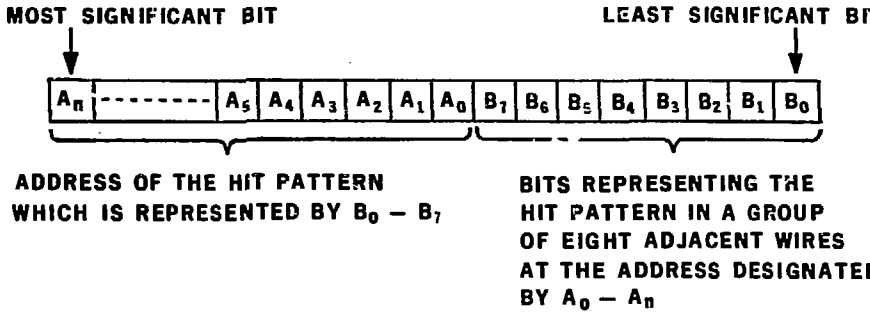

Figure 1. Word Structure For Proportional Wire Chamber Output Data

XBL 7311-1406

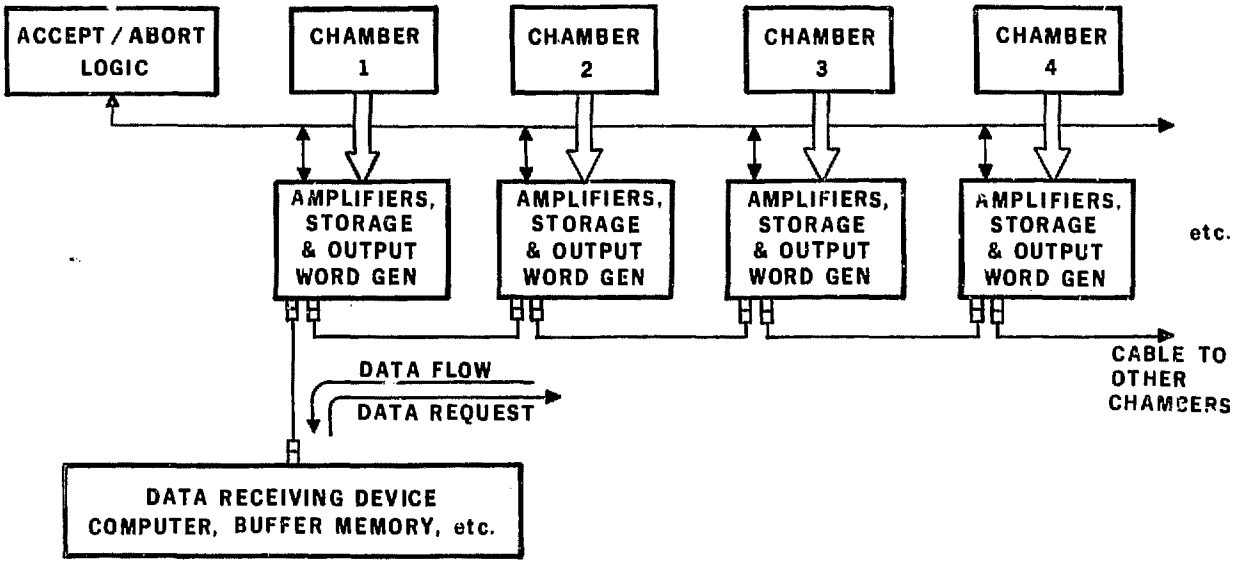

Figure 2. General System Diagram For Proportional Wire Chamber Data Readout

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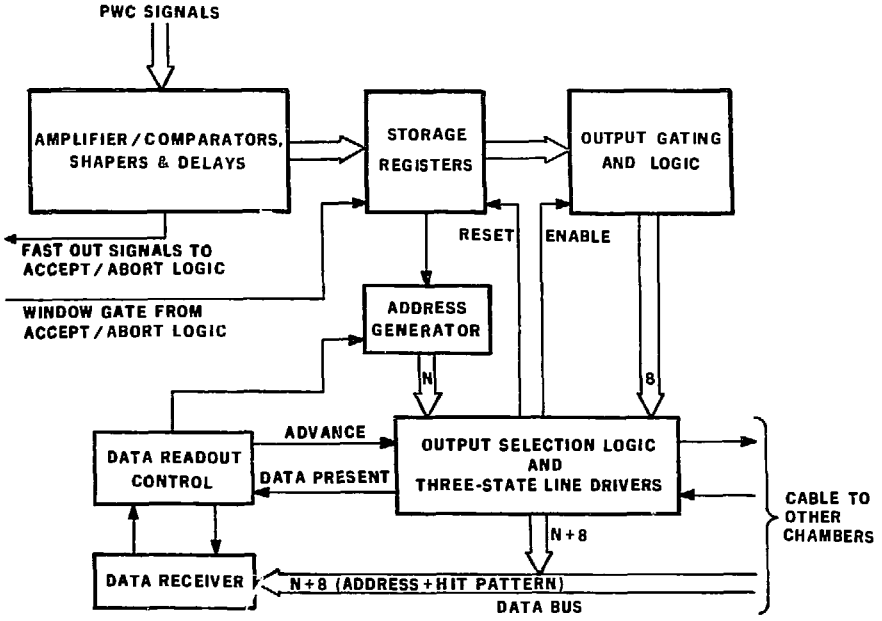

Figure 3. Proportional Wire Chamber Readout System, Functional Block Diagram

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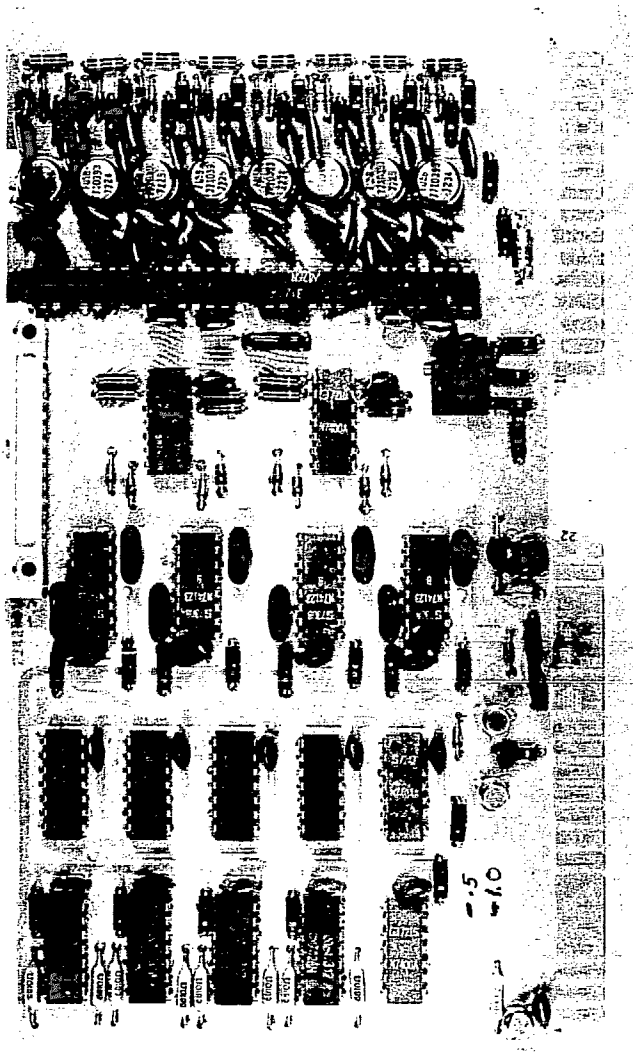

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Figure 4. Daughter Board for Proportional Wire Chamber Readout System

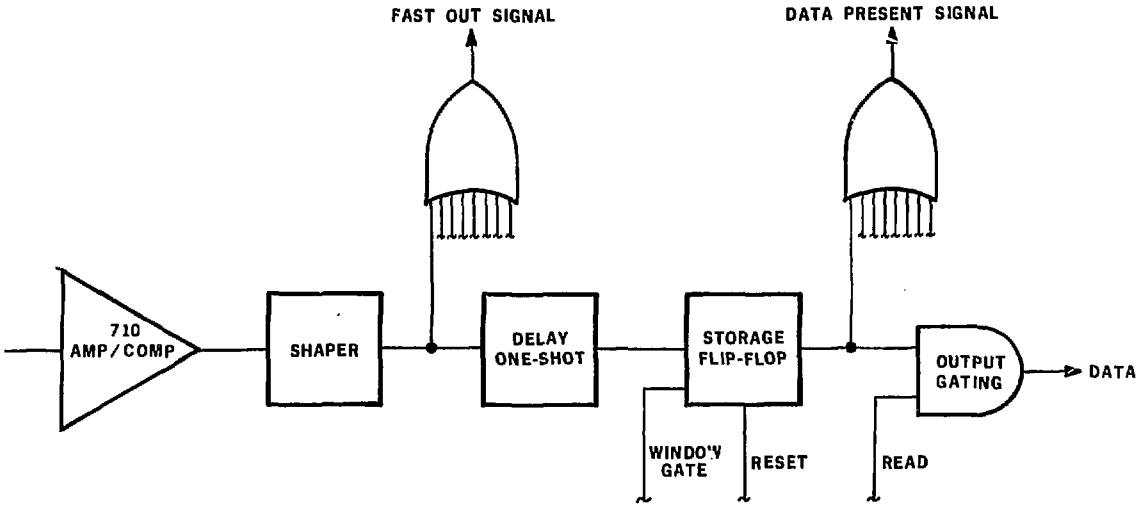

Figure 5. Simplified Diagram Of One Daughter Board Channel

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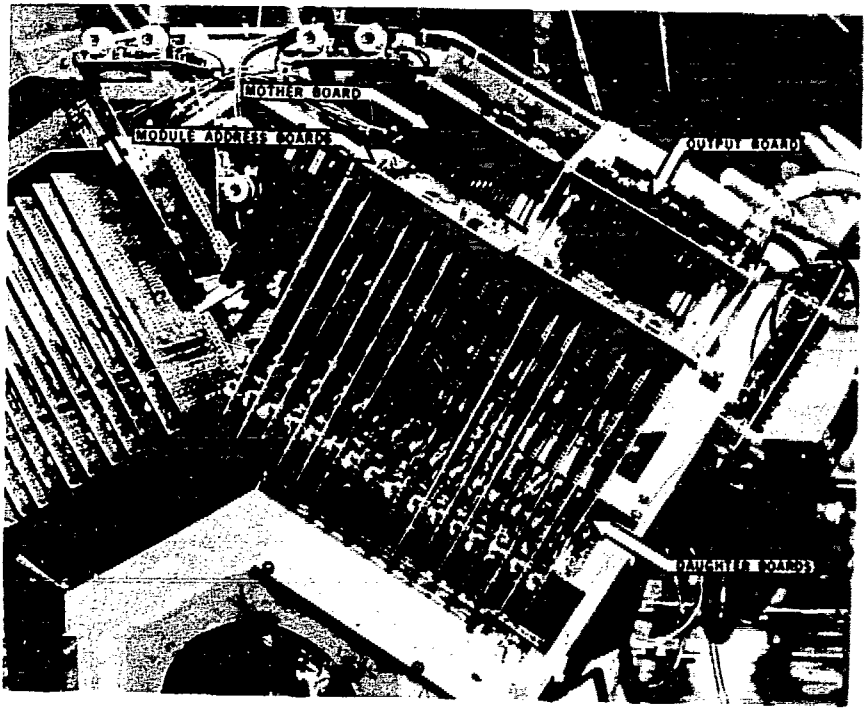

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Figure 6. Physical Organization of Chamber, Daughter Boards, Address Boards, Output Board and Mother Board

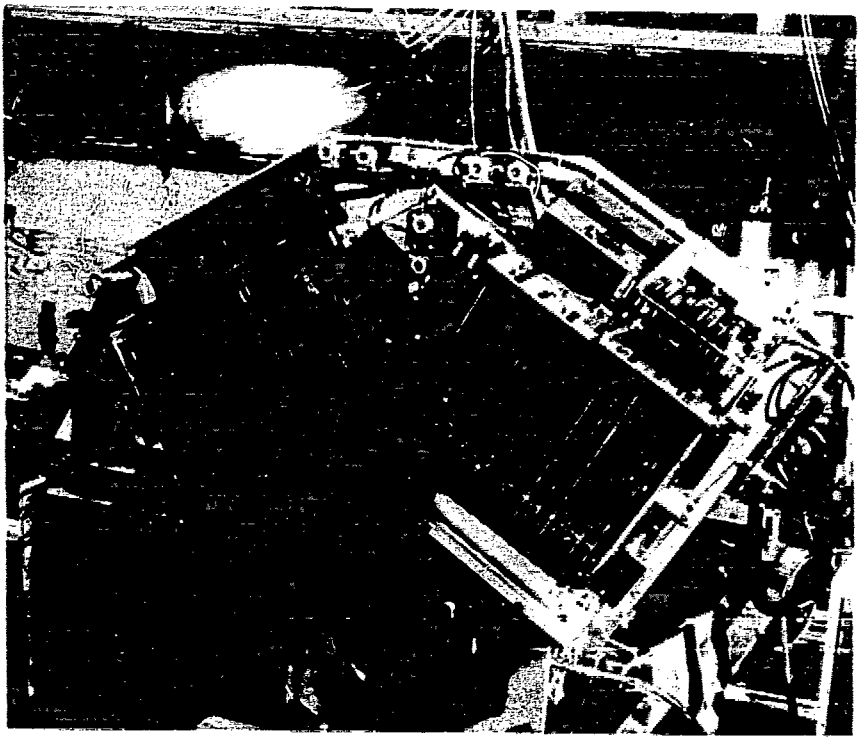

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Figure 7. Proportional Wire Chamber with Readout Electronics for Three Wire Planes