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Bandwidth Utilization Maximization of Scientific RF Communication Systems

Dan Rey, Michael Ross, William Ryan

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Dan Rey
Instrumentation Development Department
Sandia National Laboratories
Albuquerque, NM 87185-0986

Michael Ross
Harris Corporation ESS GCSD
formerly with:
Klipsch Department of Electrical and Computer Engineering
New Mexico State University (through December 1995)
Melbourne, FL 32902

William Ryan
Klipsch Department of Electrical and Computer Engineering
New Mexico State University
Las Cruces, NM 88003

Abstract

A method for more efficiently utilizing the frequency bandwidth allocated for data transmission is presented. Current space and range communication systems use modulation and coding schemes that transmit 0.5 to 1.0 bits per second per Hertz of radio frequency bandwidth. The goal in this LDRD project is to increase the bandwidth utilization by employing advanced digital communications techniques. This is done with little or no increase in the transmit power which is usually very limited on airborne systems.

Teaming with New Mexico State University, an implementation of trellis coded modulation (TCM), a coding and modulation scheme pioneered by Ungerboeck [1], was developed for this application and simulated on a computer. TCM provides a means for reliably transmitting data while simultaneously increasing bandwidth efficiency. The penalty is increased receiver complexity. In particular, the trellis decoder requires high-speed, application-specific digital signal processing (DSP) chips. A system solution based on the QualComm Viterbi decoder and the Graychip DSP receiver chips is presented.

Acknowledgments

Thanks to D. E. Ryerson, and V. P. Salazar, Sandia National Laboratories, for initiating and receiving LDRD funds to perform this work and for all their support throughout the project. Thanks to Dr. William Osborne, formerly New Mexico State University, now University of Texas at Dallas, for the initial conceptual designs. Thanks to Omer Acikel and Ali Ghrayeb, both graduate students at New Mexico State University, Larry Alvarez, New Mexico State University, and David Armistead, Sandia National Laboratories, for their technical support designing, fabricating, and testing the hardware used in the project.

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Bandwidth Utilization Maximization of Scientific RF Communications Systems

1. Introduction

Sandia is presently fielding counter non-proliferation satellites and airborne synthetic aperture radar systems for the DOE and DOD. These systems are a vital player in our national security, and it is imperative that advancement in these technologies continue to be exploited. However, future advances in these technologies will require systems which need to transmit to the ground, via radio frequency (RF) links, scientific data at very high rates (tens to hundreds of megabits per second). At the same time we are witnessing a rapid increase in RF spectrum requests from the private sector from increasing market demands on the communication industry, such as cellular phones and television. It is apparent that the airwaves are becoming a valuable but scarce resource.

The Federal Communications Commission is already reducing the available spectrum reserved for scientific research because of commercial demands for this spectrum. We are seeing a resource, thought to be plentiful, on its way to becoming saturated unless it is used more efficiently, i.e. spectral waste is minimized. Efficient bandwidth utilization would assure that the public continues to benefit from advances in the communications industry and spectrum needed for scientific research and non-proliferation monitoring would continue to be available.

1.1 Technical Proposal

Our current communication systems use modulation and coding schemes that transmit 0.5 to 1.0 bits per second per Hertz of radio frequency bandwidth. This is a direct result of conventional modulation schemes such as frequency-shift-keying (FSK), binary phase shift keying (BPSK), or quadrature phase shift keying (QPSK), combined with forward error correction coding. We want to increase the bandwidth utilization by a factor of 4 to 8, yielding 4 to 8 bits per second per Hz of bandwidth with a minimal increase in transmit power which is usually very limited on airborne systems.

A relatively new modulation and coding scheme, called trellis coded modulation (TCM) provides a means for reliably transmitting data while at the same time maximizing bandwidth utilization. The concept of using trellis soft decoding for forward error correction (FEC) codes has proven to provide dramatic improvements in a communication systems overall bit error rate (BER) performance. Prior to TCM the functions of forward error correction and modulation were treated as two independent operations. TCM, however, combines the principles of forward error correction and modulation. The advantage of this is that we benefit from the error correction process at the demodulation

level without increasing the bandwidth. This removes errors that would normally be contributed by the modulation and demodulation process.

Therefore, TCM can improve the system performance without increasing the bandwidth or power requirements. However, TCM requires a smart demodulator which can make soft decisions using trellis decoding. This increases the complexity of the receiving end of the communications link. To perform soft decision trellis decoding requires large fast memory and high speed digital signal processing (DSP).

TCM has already made an impact on low-data-rate wireline communications, but has yet to be implemented at high data rates on RF channels. We plan on utilizing advances in high speed electronics and digital signal processing to design and build a TCM modulator and demodulator to operate in excess of 10's of megabits per second.

New Mexico State University (NMSU) has been studying the advance of TCM for the past seven years. They have developed extensive simulation models and are actively pursuing the implementation of such systems at the megabit-per-second data rate. Sandia will benefit from the extensive work that NMSU has already completed, and NMSU will be able to improve their models with the test results produced by Sandia.

2. Project Description

The purpose of this project is the development of bandwidth efficient, digital communications suitable for satellite and range applications. Compatibility with efficient high powered amplifiers and applicable (i.e., National Telecommunications and Information Administration, NTIA) bandwidth regulations is of primary importance, in addition to the coding and modulation tradeoffs common to all bandwidth efficiency studies. For the project to be successful, all of the following must be included in the system design:

Bandwidth Efficient Signaling
Error Correction Coding
Pulse Shaping and Matched Filtering
Symbol Synchronization
Carrier Synchronization
Efficient High Powered Amplifier

The goal of this project is to increase the current bandwidth utilization by a factor of 4 for data rates in excess of 20 megabits per second. To accomplish this the project was divided into two phases. Phase I focused on requirements definition, research and selection of a modulation scheme, and computer simulations to verify feasibility of the selected scheme. Phase II of this LDRD focused on the design, development, and implementation of the selected communication system.

Phase I tasks were performed during the first year of this two year LDRD. The modulation scheme selected was the pragmatic Trellis Coded Modulation concept of Viterbi [7] applied using a 32-quadrature amplitude modulation (QAM) signal set. System level design and simulation were performed using the Signal Processing Workshop (SPW) software owned by New Mexico State University.

The pragmatic 32-QAM scheme proposed here offers several advantages. The required Viterbi decoder is already standard technology. A data rate of 40 megabits per second will be obtained by transmitting 10 megasymbols per second, which is well within the range of existing decoders, and will also fit within the 10 MHz bandwidth allowed for the project. The 32-QAM constellation requires a dynamic range no greater than that required for 16-QAM. A standard QAM symbol synchronizer should meet the needs of this system. The most difficult challenge facing this project was a phase tracking loop to track the proposed constellation.

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3. Coding and Modulation Format

The pragmatic TCM concept of Viterbi was applied using a 32-QAM signal set. As shown in figure 3.1, one of 4 bits of source data is fed into a rate 1/2, 64-state Viterbi decoder to generate 2 code bits. The code bits and the three uncoded bits are mapped onto the 32-QAM constellation shown in figure 3.2. Although requiring slightly more energy than the conventional 32-cross constellation (figure 3.3), the proposed constellation presents a stronger pattern to the carrier synchronizer and allows an exceptionally elegant and powerful mapping of the pragmatic code.

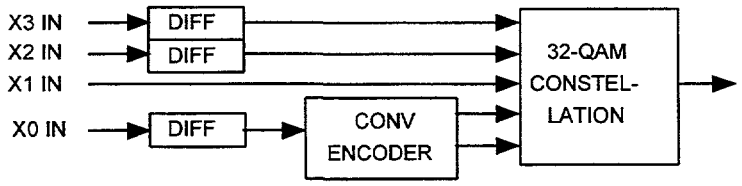

Figure 3.1. *Generation of 32-QAM. X3, X2, and X0 are differentially encoded.*

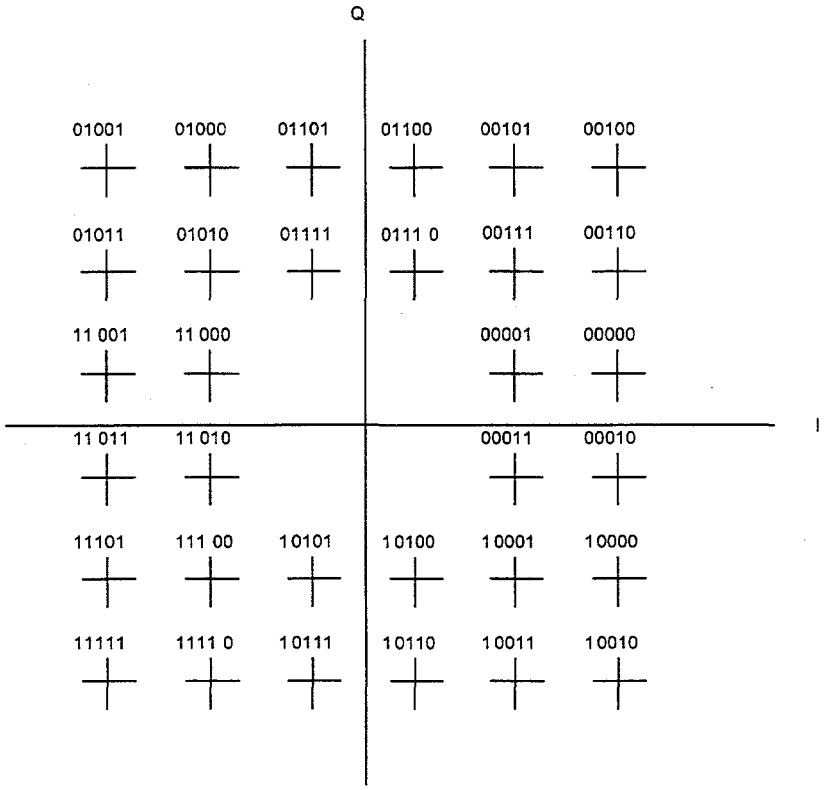

Figure 3.2 *Signal Constellation for the 32-QAM Pragmatic TCM System. The two right-most bits are from the convolutional encoder.*

Single-chip implementations of the Viterbi decoder are readily available and commonly used in the modem industry. This particular code and this particular constellation allow 180-degree phase ambiguities to be corrected by differentially encoding

the source data. Ninety-degree phase ambiguities are corrected by monitoring the Viterbi decoder metrics.

The bit-error-rate performance of this code, determined by simulation is shown in figure 3.4. This result assumes ideal synchronization. The impact of real synchronizers, as well as the details of the decoder are discussed in subsequent sections.

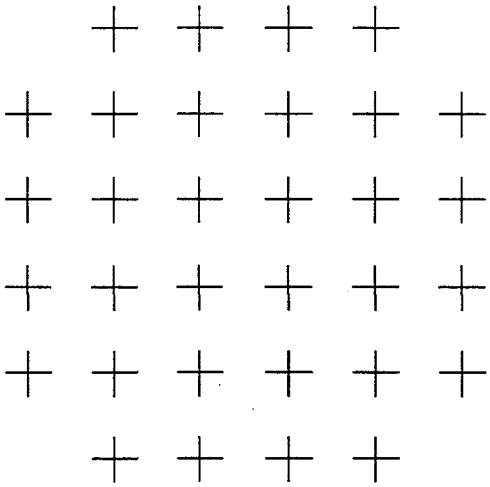

Figure 3.3. *Conventional 32-Cross Constellation.*

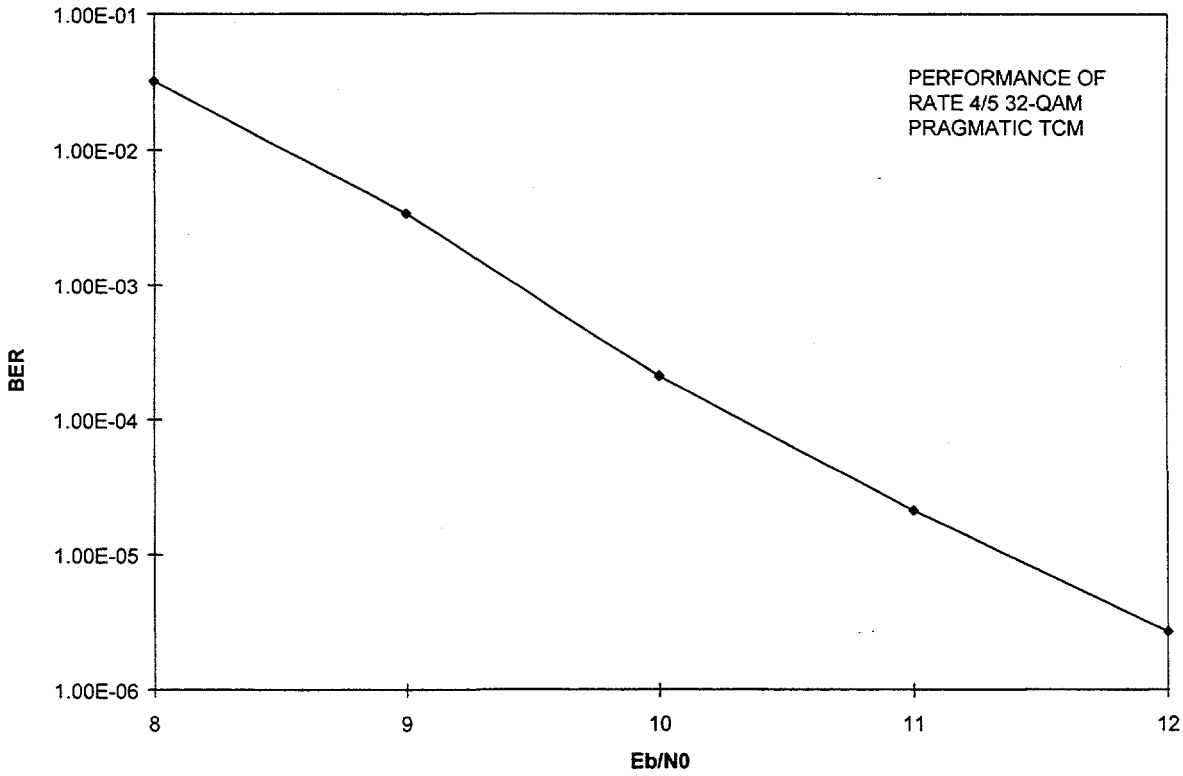

Figure 3.4. *Bit error rate of the 32-QAM TCM code, with ideal synchronization.*

4. Pulse Shaping and Filtering

As stated in the introduction, the purpose of this project, is bandwidth efficiency, as implemented in real hardware. To accomplish this, it is essential that this project include pulse shaping and filtering.

4.1 Applied Definition of Bandwidth

In pure coding studies, bandwidth efficiency is usually stated in terms of bits per two-dimensional symbol, with the assumption that 2-D symbols will be transmitted at the rate of 1 symbol per second per Hz. Thus an uncoded QPSK system and a rate 2/3 encoded 8-PSK system would both be said to have a spectral efficiency of two-bits (of user data) per second per Hz, while the rate 4/5 32-QAM system would be said to have a spectral efficiency of 4-bits per second per Hz. While 1 symbol per second per Hz is the theoretical maximum, it has never been achieved in a practical, truly bandlimited system. This is because the theoretical possibility requires sophisticated pulse shaping, which until recently has been beyond practical electronics, and because severely bandlimited pulses tend to have little or no tolerance for synchronization error.

Because no signal in the physical world has a finite absolute bandwidth (a fundamental theorem proven by Wozencraft and Jacobs in 1965 [33]) bandwidth regulations are often stated in terms of required attenuation as a function of offset from center frequency. Thus bandwidth efficiency of an implemented system must be expressed in terms of an agreed upon definition of bandwidth. As it is the purpose of this project to support telemetry and range applications, spectral efficiency will be stated in terms of user data rates actually achieved through an NTIA allocated bandwidth. The NTIA bandwidth is shown in figure 4.1. As was done for the Multi-Thermal Imaging (MTI) project, this standard is applied using an allocated bandwidth of 10MHz, and a passband edge attenuation of 10dB.

Figure 4.2 shows NTIA specification superimposed on the spectrum of unfiltered QPSK, with symbol rate equal to allocated bandwidth. As can be seen, this configuration does not meet the specification. Figure 4.3 shows that the bandwidth specification can be met using a 3rd order Butterworth filter with a bandwidth of half the symbol rate, but simulations in this configuration resulted in performance degradation of more than 3dB, unacceptable for the purpose of this project. Thus we see that the demands of this project will not likely be met with ordinary filtering, and we must use pulse-shaping techniques.

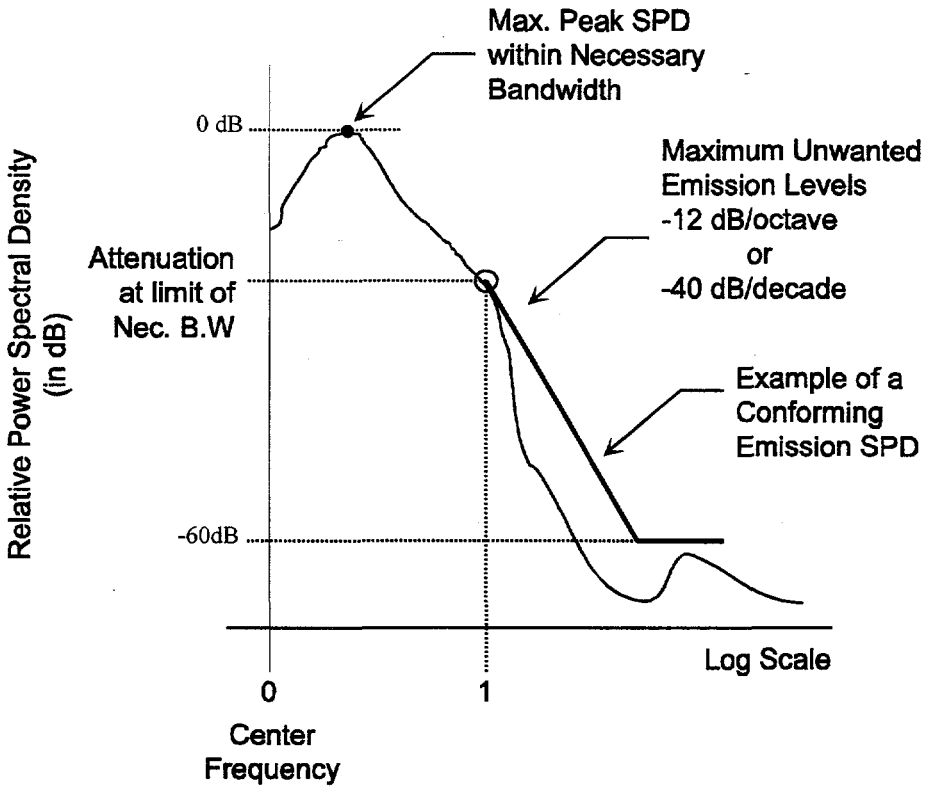

Figure 4.1 *NTIA Bandwidth.*

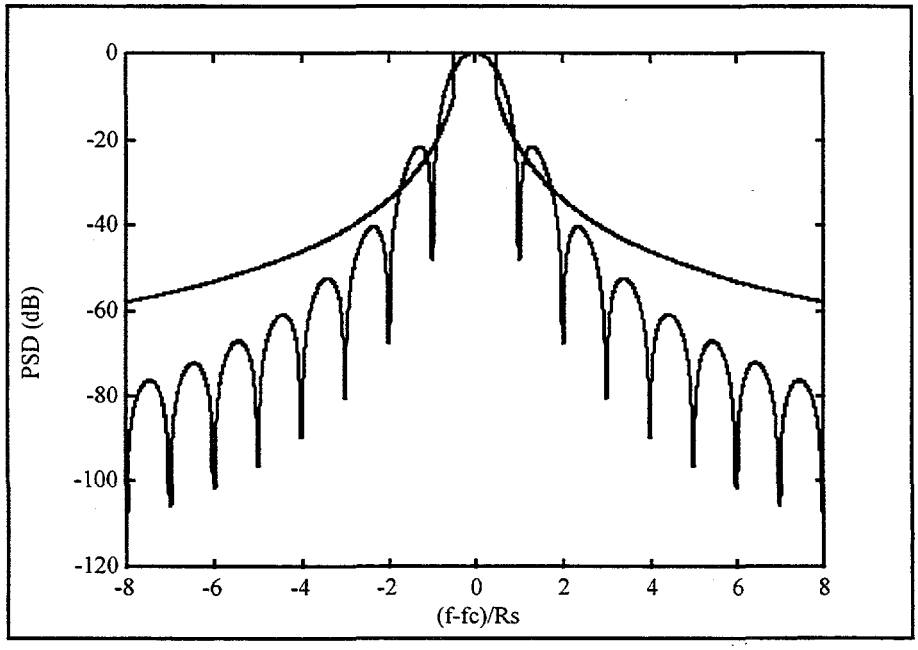

Figure 4.2. *Spectrum of Unfiltered QPSK vs NTIA Mask.*

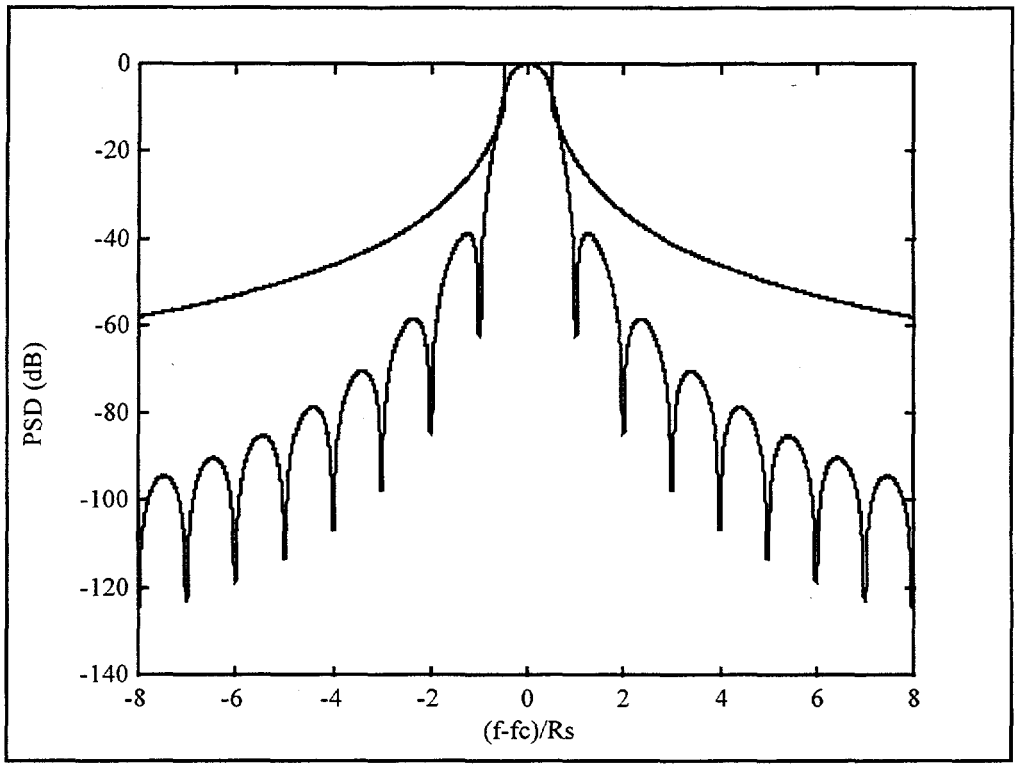

Figure 4.3. *Spectrum of Filtered QPSK vs. NTIA Mask, using a 3rd order Butterworth filter with bandwidth of half the symbol rate.*

4.2. Pulse Shaping and Nyquist Filtering.

A pulsed shaped system is one in which the impulse response of the channel (as observed at the output of the receiver matched filter) is precisely specified to achieve a minimal (or zero) intersymbol interference with minimal bandwidth. This is accomplished by specialized design of the transmitter and receiver filter. Zero intersymbol interference is achieved if the impulse response is non-zero at the sampling time of the current symbol, zero at all other sampling times. The Nyquist theorem states that this is possible if and only if the frequency response satisfies

$$\sum_{\text{all k}} H(f+kR_S) = \text{constant} \qquad |f| < \frac{1}{2} R_S$$

In general, filters meeting the Nyquist criterion attain a 6dB attenuation at a bandwidth equal to the symbol rate. Acquiring more than 6dB attenuation at a frequency offset of $R_S/2$ without insufficient attenuation elsewhere, proves to be difficult or impossible.

Any filter meeting the Nyquist criterion is referred to as a Nyquist filter. The best known Nyquist filter is the raised cosine filter, having frequency response given by:

$$H(f) = \begin{cases} 1 & |f|<f1 \\ \frac{1}{2}\left\{1+\cos\left[\frac{\pi(|f|-f1)}{2f\Delta}\right]\right\} & f1<|f|<B \\ 0 & |f|>B \end{cases}$$

where B is the absolute bandwidth of the filter at baseband, $f_\Delta = B-f_0$, $f_1=f_0-f_\Delta$, and f_0 is $R_S/2$. The magnitude response of the raised cosine filter is shown in figure 4.4. As can be seen, the raised cosine filter is absolutely bandlimited to B at baseband, 2B at transmission frequencies. The rolloff factor r is defined as f_Δ/f_0. This parameter controls the steepness of the transmission band and has a value between 0 and 1. A rolloff factor of 1 corresponds to a filter with no flatband and an absolute bandwidth of $2R_S$ at transmission frequencies. A rolloff factor of 0 corresponds to an abrupt cutoff and an absolute transmission bandwidth of R_S.

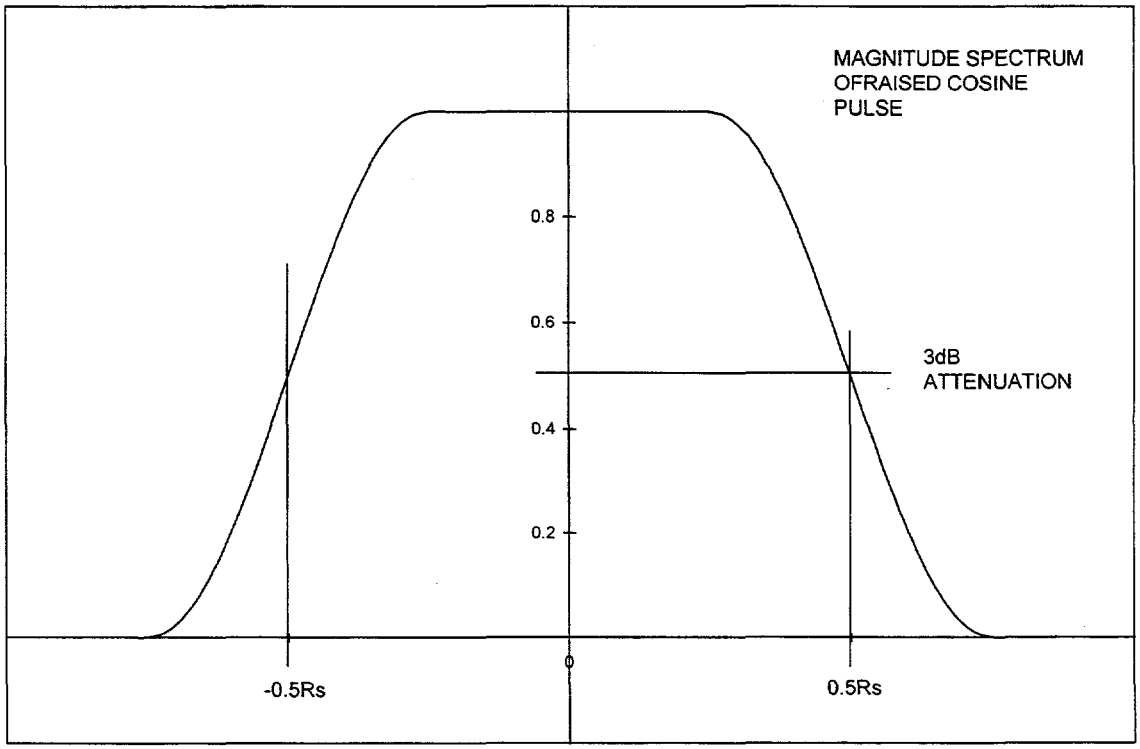

Figure 4.4. *Magnitude Spectrum of Raised Cosine Pulse.*

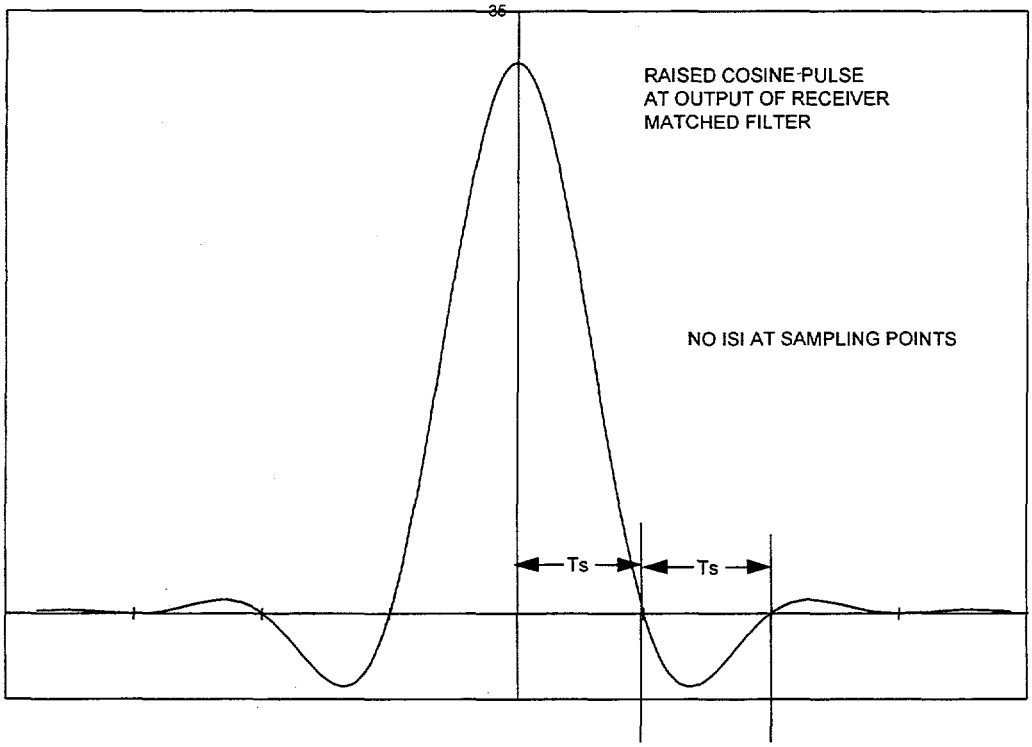

Figure 4.5 *Raised Cosine Impulse Response.*

The difficulty in using a high rolloff factor is twofold: the filter itself is more difficult to build, and symbol synchronization becomes more critical. The impulse response of the raised cosine filter is given by

$$h(t) = 2f0\left(\frac{\sin(2\pi f0t)}{2\pi f0t}\right)\left[\frac{\cos(2\pi f\Delta t)}{1-(4f\Delta t)^2}\right]$$

and is shown in figure 4.5. As can be seen, the zero crossings of the impulse response are separated at intervals equal to the symbol period. A low rolloff factor causes slower attenuation of the impulse response, and greater sensitivity to symbol synchronization error. A rolloff factor of 0 would give an impulse response of $h(t)=2f_0\text{sinc}(2f_0t)$ and a Nyquist minimum bandwidth, but it is impractical to build a symbol synchronizer to operate at this parameter, or to build the filter itself. The 32-QAM system, as presently modeled in SPW, will operate with a rolloff factor as low as 0.2. The performance loss at this parameter is negligible, however the performance completely breaks down at a rolloff factor of less than 0.2.

4.3. Rolloff, Passband Edge Attenuation, and Real Symbol Rate

Because the Nyquist (raised cosine) filter provides a passband edge attenuation of 6dB, whereas the stated specification for the project requires a passband edge attenuation of 10dB, it is necessary to accept a real symbol rate less than the Nyquist maximum. Furthermore, the optimal system (in terms of noise) employs a receiver filter which is

matched to the transmitter filter. Meeting the Nyquist requirement requires that h(t) as defined by equation 4.2 be the impulse response of the complete channel, not simply the transmitter filter. Therefore, optimization for noise requires that square-root raised cosine filters be employed at the transmitter and receiver, hence the passband edge attenuation is only 3dB. Of course, it is also possible to use a raised cosine filter at the transmitter with a non-optimal flatband filter at the receiver.

Using equation 4.1, the implementable spectral efficiency of the system, in symbols per second per Hz, can be calculated as a function of the required attenuation and the rolloff factor. These results are summarized in table 4.1. Using a square-root raised cosine filter with a rolloff of 0.2, and a required passband edge attenuation of 10dB, the implemented spectral efficiency of the system is 0.8944 symbols per second per Hz, or 3.6 bits per second per Hz. It should be noted that the limitations discussed in this section are not unique to the 32-QAM system, but are fundamental to the channel itself. Thus, while the system falls short of the ideal of 4 bits/s/Hz, an uncoded QPSK system, operating under the same rigorous constraints, would achieve a spectral efficiency of 1.8 bits/s/Hz, as opposed to the ideal 2. The required raised cosine filters can be realized using programmable acoustic charge transport (ACT) filters owned by the NMSU telemetry center.

	FILTER/ATTENUATION AT BANDWIDTH EDGE		
rollof factor	RC 10dB	sqrt RC 10dB	sqrt RC 20dB
0.2	0.9543	0.8944	0.8514
0.4	0.9125	0.809	0.7413
0.6	0.8743	0.7384	0.6564
0.8	0.8391	0.6792	0.5889
1	0.8067	0.6288	0.5341

Table 4.1. *Spectral Efficiency, in Symbols per Second, as a function of rolloff factor and required attenuation.*

5. System Design

The system which was simulated by SPW at NMSU consisted of the transmitter, shown in figure 5.1, and the receiver shown in figure 5.2. Between the transmitter and the receiver, phase and frequency error are introduced, as shown in figure 5.3.

5.1 Transmitter Design

In the transmitter, encoding begins with four binary data streams. One of four data bits is input to a rate 1/2 convolutional encoder, so that there are 5-bits to specify a 32 QAM symbol. In the SPW simulation, the 32-QAM symbol is represented as a complex envelope, which is modulated onto a pulse train, and passed through a square root raised cosine filter and an amplifier model.

The signal constellation and the convolutional code allow 180 degree phase ambiguities to be resolved by differentially encoding bits X3, X2, and X0. The differential encoder outputs a one if the current bit is the complement of the previous bit, a zero if the current bit is the same as the previous bit. Thus if 180 degree phase ambiguity consistently inverts certain data bits, the ambiguity may be corrected by differential encoding. Differential encoding does, however, double the bit error rate, since every bit error in the channel results in two bit errors in the decoded data. The 32-QAM constellation has a 90-degree phase ambiguity, which must be resolved by monitoring the Viterbi decoder for an out-of sync condition and taking corrective action. Out of sync indication is a common feature on marketable Viterbi decoders.

In the testbed implementation, to be accomplished during the summer of 1995, the 32-QAM signal will be generated by a Hewlett-Packard vector modulator owned by the NMSU Telemetry center. The vector modulator provides a mode in which 6 bits of data are mapped onto a 64-QAM constellation. The 32-QAM constellation can be implemented as a subset of the 64-QAM constellation, and the logic to map 5-bits of code onto 6-bits required to specify the signal vector is realized in Boolean gates.

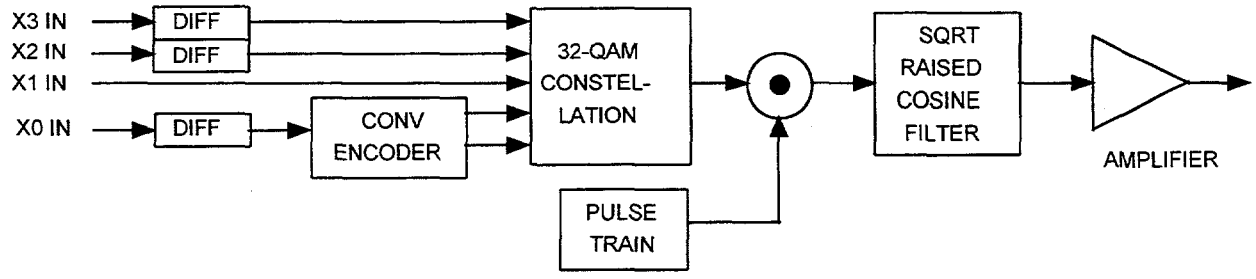

Figure 5.1. *Conceptual Diagram of Transmitter.*

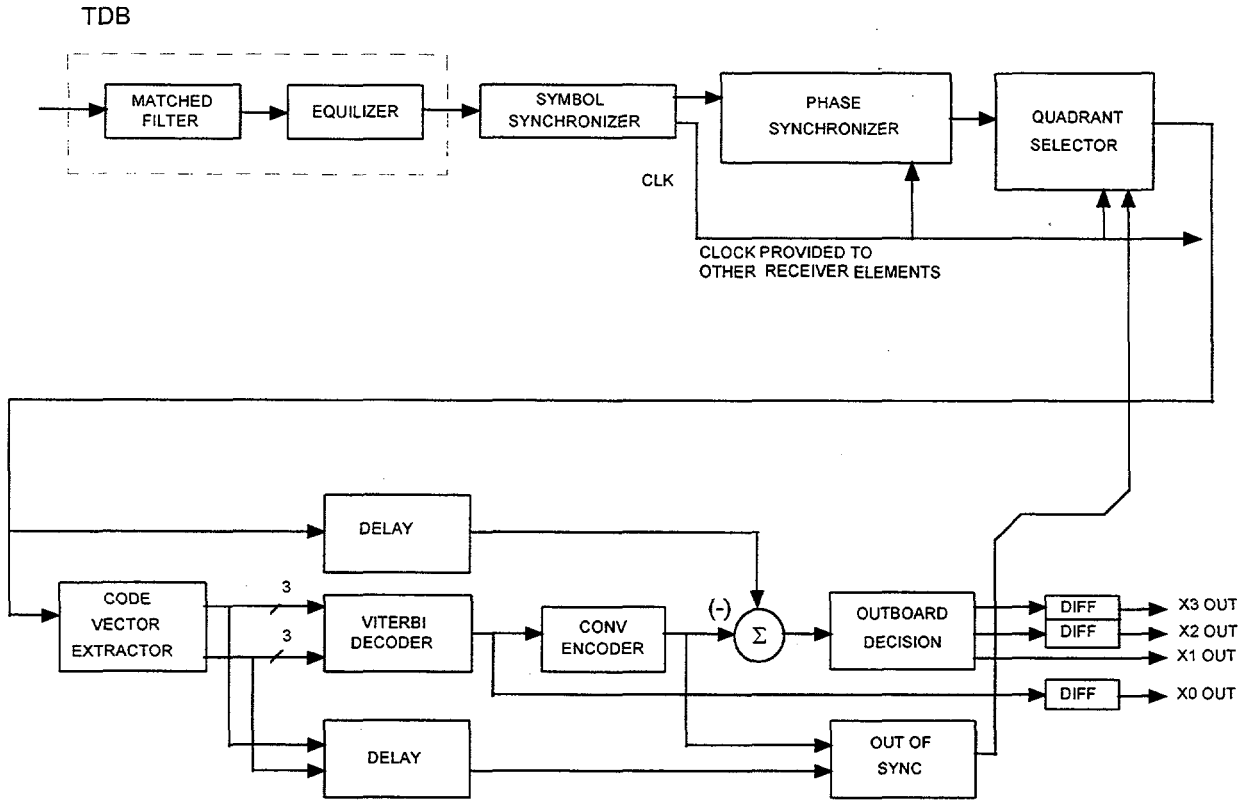

Figure 5.2 *Conceptual View of Receiver Side Logic.*

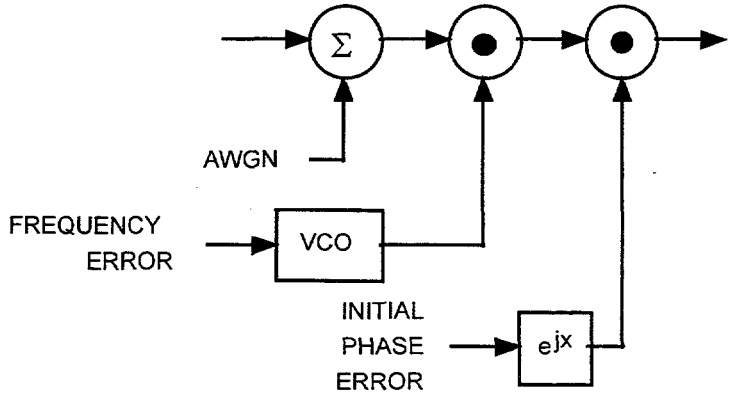

Figure 5.3 *Introduction of frequency and phase errors to the channel model.*

5.2 Receiver Design

The receiver consists of a filter (a matched filter is used in the SPW simulations but hardware may require an equalizer as well), symbol synchronizer, phase synchronizer (carrier tracking loop), a quadrant selector (90-degree phase error corrector) a Viterbi decoder and supporting logic for the Viterbi decoder. The transmit and receive filters are square-root raised cosine filters and have been discussed in the previous section. The symbol synchronizer samples the matched filter output at the optimal time, and provides a symbol clock for the receiver side of the system. The phase synchronizer orients the

receiver I and Q axis with those of the transmitter. The symbol synchronizer and the phase synchronizer are discussed in subsequent sections.

The quadrant selector (figure 5.4) rotates the phase reference of the receiver by 90 degrees in response to an out of sync indication by the Viterbi Decoder. Out of sync indication is accomplished by monitoring state metrics generated internally by the Viterbi decoder. While this is a common feature of off-the-shelf Viterbi decoders, it is absent from the Viterbi Decoder module in the SPW Library. To compensate for this absence, the out-of-sync indicator shown in figure 5.5 was created especially for the 32-QAM project. The output of the Viterbi Decoder is re-encoded to generate a new sequence of code vectors, which is then compared to the sequence of code vectors received from the channel. Small differences between the received sequence and the regenerated sequence are attributed to noise, in which case it is assumed that the Viterbi decoder has corrected errors, and no further action is taken. A large difference in the regenerated sequence is attributed to an out-of-sync condition, in which case the phase reference is rotated by 90-degrees, and time is allowed to determine if this action has corrected the problem. With differential encoding, a 180-degree correction is never necessary, however, the 90-degree correction is generally needed whenever the carrier tracking loop acquires or re-acquires. Comparison of a regenerated code sequence with the received code sequence is also a common out-of-sync indication technique used in commercial Viterbi Decoders.

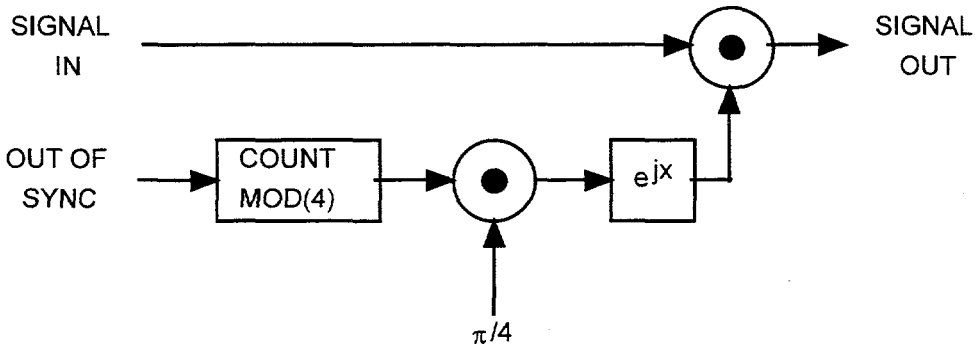

Figure 5.4 *Quadrant Selector, for correction of 90 degree phase ambiguity.*

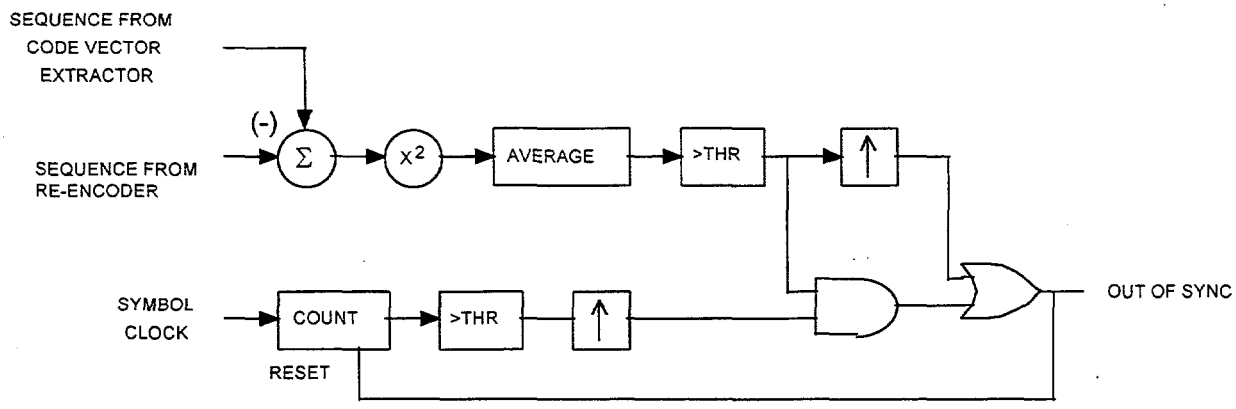

Figure 5.5 *Out of Sync (90 degree phase error) Indicator.*

The Viterbi Decoder is an industry standard for BPSK and QPSK channels. Viterbi's pragmatic concept allows a common Viterbi decoder to be applied to a variety of signal constellations, however the code vector extractor (which provides soft decisions to the Viterbi decoder) and the outboard decision must be unique the chosen signal set mapping.

In the 32-QAM constellation of figure 3.2, the two rightmost bits are generated by the encoder, the three leftmost bits are outboard bits (they arrive at the constellation mapper outboard of the convolutional encoder). In this discussion, a set of eight signal points having the same code bits will be referred to as a partition, whereas a set of four signal points having the same outboard bits are referred to as a cluster. In the encoding logic, the three outboard bits select the center of a cluster, a vector from the convolutional encoder (the code vector) is added to the cluster center to arrive at the signal vector. The purpose of the code vector extractor and the outboard decision logic is to reverse this process. If the received signal vector is within a cluster, then the code-vector is the vector difference between the received signal vector and the ordinary signal vector. If the received vector is vertically between two clusters, the vertical component of the code vector is made opposite; if the received signal vector is horizontally between two code-vectors, the horizontal component of the code-vector is made opposite.

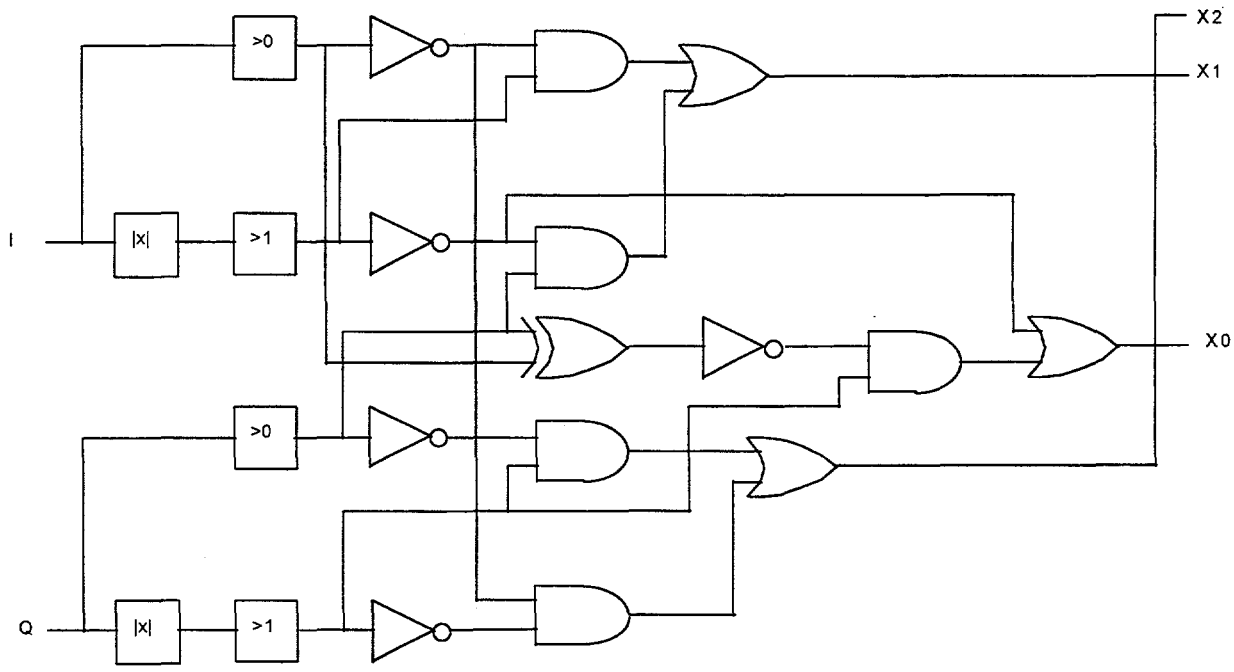

Figure 5.6. *Outboard Decision Logic.*

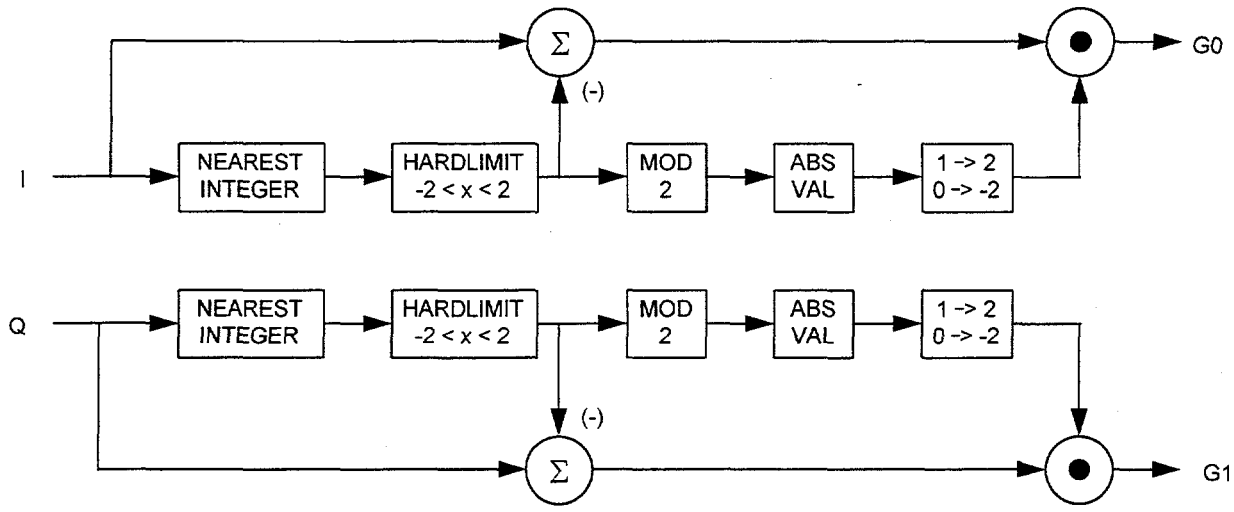

Figure 5.7. *Code Vector Extractor.*

The output of the code vector extractor is actually a pair of soft-decisions. In coding parlance, a soft decision is a number which indicates the likelihood that a logic value is a zero or a one. Usually a zero soft decision value represents the strongest likelihood of a logical zero, whereas a full scale soft decision value represents the strongest likelihood of a logical one. The Viterbi algorithm is able to use this information to obtain performance superior to that of a decoder using hard-decision detection. Most commercial Viterbi Decoders accept 8-level soft decisions, a few accept 16-level soft-decisions. In this system, the horizontal component of the code-vector is the soft-decision associated with one of the two code bits, the vertical component is the soft-decision associated with the other.

The output of the code vector extractor is connected to the soft decision inputs of the Viterbi Decoder, which obtains the decoded data bit. This is one of the four user data bits that was encoded onto the 32-QAM symbol at the transmitter. The decoded bit is also connected to the input of a convolutional encoder, regenerating the code sequence. The reason for doing this is that the regenerated code sequence has had errors corrected, and can thus be used to make optimal soft decisions. Also, the regenerated code sequence is compared to the code sequence extracted from the received signal vectors to provide the out-of-sync indication.

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6. Synchronization

6.1 Symbol Synchronization

Symbol synchronization is accomplished by an early-late gate, a well established technique. The symbol synchronizer is shown in figure 6.1. The signal from the matched filter is sampled by a delayed clock and also by an advanced clock. The energy of the early and late samples is compared and the system clock is adjusted accordingly. The impact of this synchronizer on the bit-error-rate performance of the 32-QAM TCM system is negligible, as shown in figure 6.2.

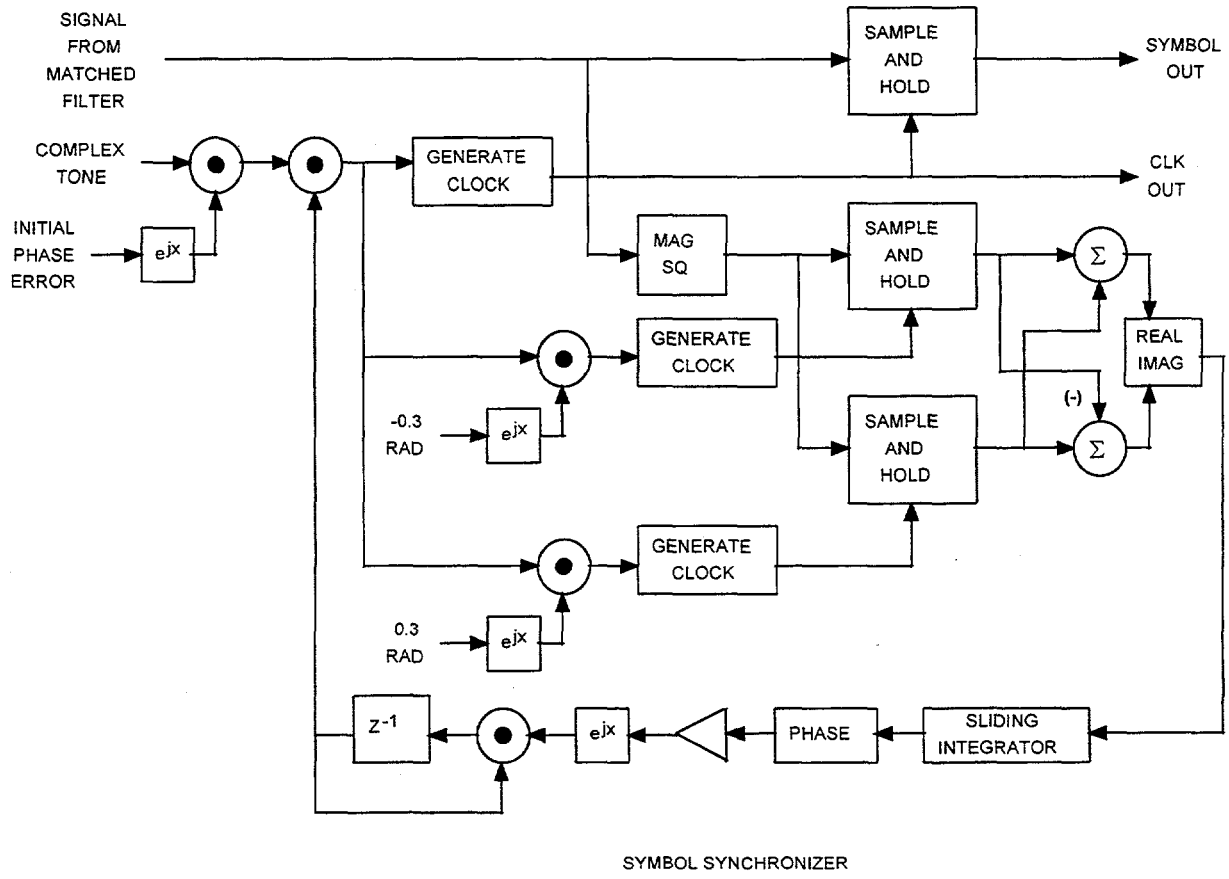


Figure 6.1. *Early-Late Gate Symbol Synchronizer.*

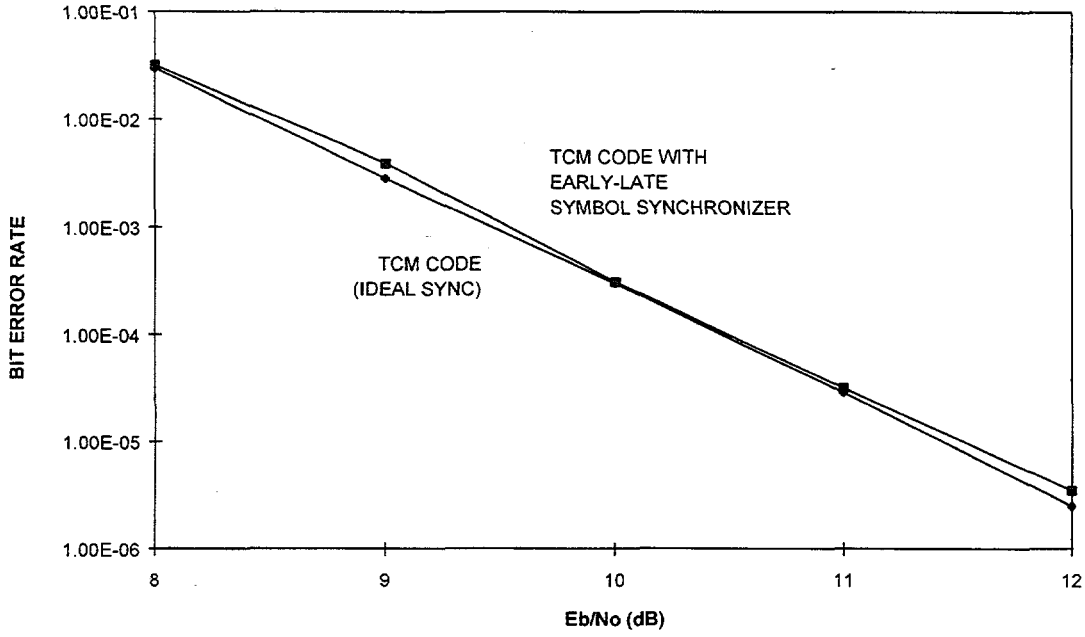


Figure 6.2. *Performance of Early-Late Gate Synchronizer.*

6.2 Carrier Synchronization

In QAM systems, carrier synchronization requires knowledge of the geometry of the QAM constellation. Figure 6.3 shows the main components of a phase locked loop (PLL) that is commonly employed.

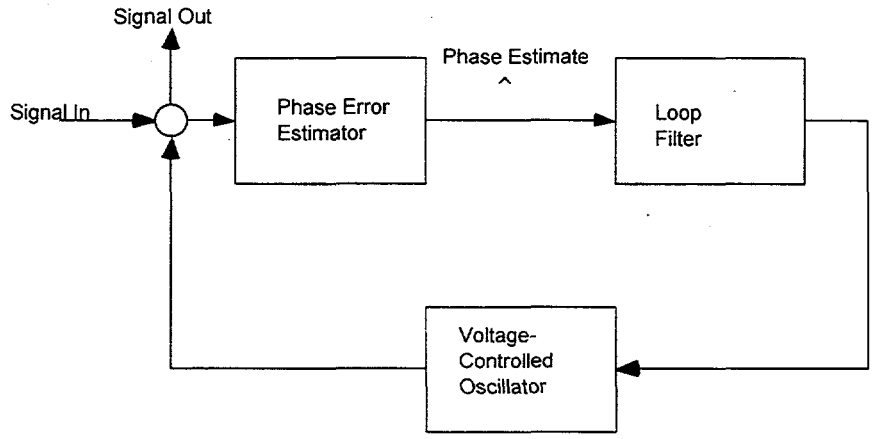


Figure 6.3 *Phase Locked Loop.*

The received symbol is quantized to the nearest constellation point and a phase error estimate is obtained by comparing the phase of the received signal to that of the quantized point. The error estimates drive a voltage controlled oscillator (VCO) that feeds back to the system. The result is that the constellation is rotated, such that the phase error tends to zero. The loop filter controls the response and sensitivity of the PLL to noise.

In describing the action of the PLL the underlying assumption is that the phase error estimates are generally correct. This is not necessarily the case. For symmetrical constellations, like the 4-QAM constellation of figure 6.4, a phase error of 90 degrees is not distinguishable (at the PLL) from the original orientation. For large initial phase errors, the loop may well lock 90 or 180 degrees out of phase, a situation referred to as false lock. The 90 and 180 degree ambiguities resulting from false lock are common in QAM systems and can be resolved using differential encoding and quadrant selectors. With larger, more complex constellations, such as the 32-QAM constellation used in this study, the false lock problem becomes non-trivial.

Additionally, an objective of this study is that the system be self-acquiring. As a result, training sequences, used by other QAM systems to achieve synchronization, are avoided in this case.

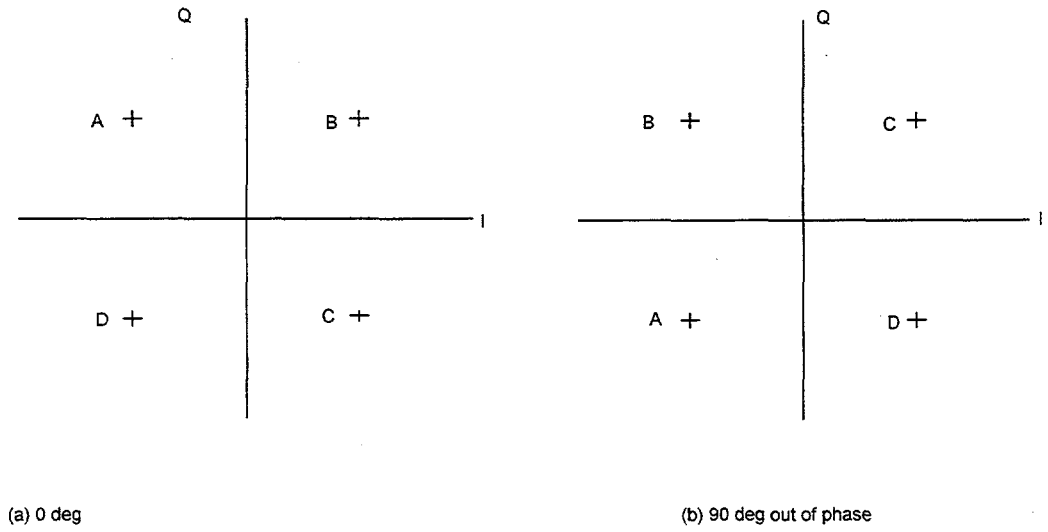


Figure 6.4 *False lock problem.*

The remainder of this section examines the implementation of various devices employed as PLLs for 32-QAM. Some problems unique to this particular constellation are also discussed in arriving at the final (optimal) solution. These include:

* Maximum A Posteriori (MAP) PLL
* Fourth law devices
* Three-Phase sampling device
* Combined MAP and fourth law device

6.2.1 Maximum A Posteriori Device

Figure 6.5 shows a PLL using a Maximum A Posteriori (MAP) device as the phase-error estimator.

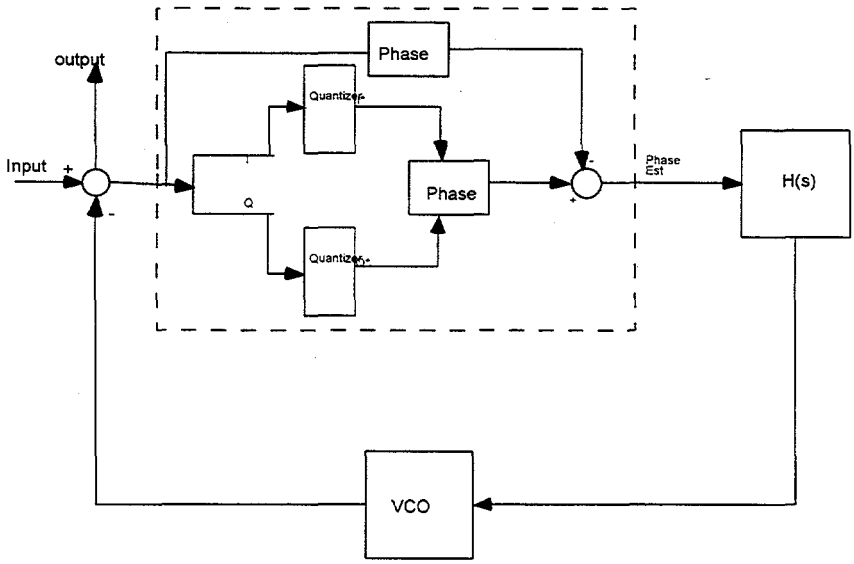
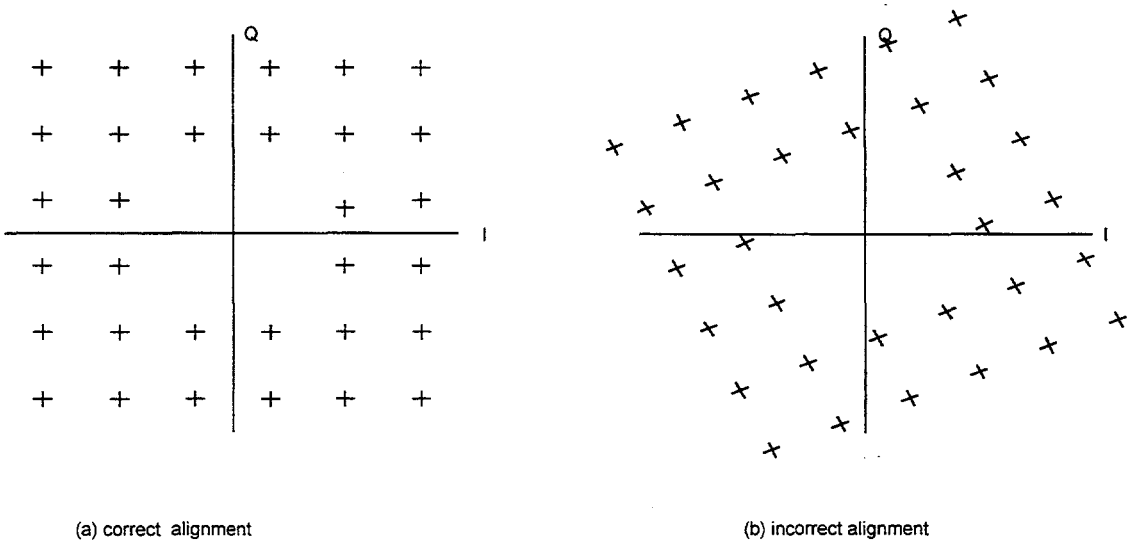


Figure 6.5 *Maximum A Posteriori Device as the Phase-Error Estimator.*

In this device, the received I and Q signals are quantized to the nearest point on the 32-QAM constellation. The phase of this quantized point is compared to the phase of the received signal and a phase error estimate is then obtained. This is used to adjust the VCO frequency. The performance of this device, once lock is achieved, is optimal for QAM systems. With this particular QAM constellation however, a problem exists during acquisition. It is possible for the constellation to become stuck in an incorrect alignment. This can occur, as in shown below (figures 6.6a & 6.6b), when the initial phase difference is large enough, that received signals are quantized to an incorrect constellation point. To resolve this problem is necessary to use a training sequence, or to externally correct the PLL alignment when this condition is detected.



Figures 6.6 *Incorrect Constellation Alignment.*

6.2.2 Fourth Law Device

In this approach the received signal is raised to the fourth power and then averaged over a number of symbols. The phase of all constellation points, except the four corner points, average out to zero. The corner points average to $\pm\pi$ when the loop is locked correctly and $\pm\pi + 4\theta$ if the constellation is out phase by angle θ. The angle θ can be extracted and used to adjust the VCO. This approach is not susceptible to the problems of the MAP device. The performance however degrades considerably (>3 dB) when tracking moderate frequency errors. Figure 6.7 shows the Fourth Law Device.

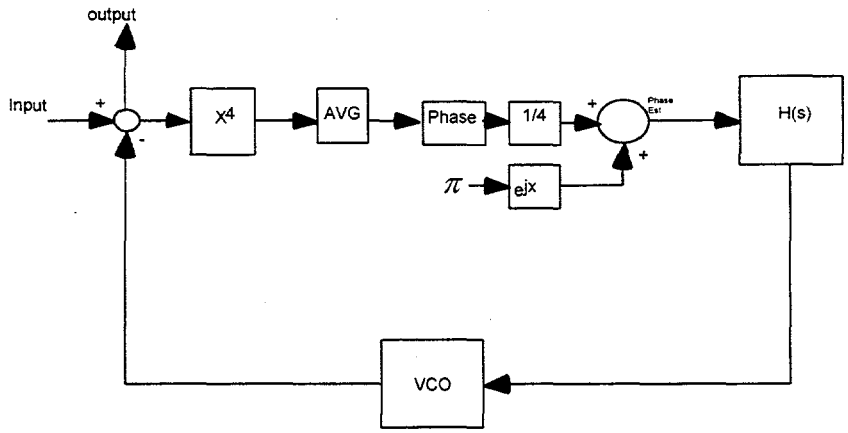


Figure 6.7 *Fourth Law Device.*

6.2.3 Three-Phase Device

Figure 6.8 shows another approach to the PLL. In this device the input signal is branched into three identical metrics. In two of the branches, the signal is rotated slightly in phase prior to input to the metric. The metrics indicate how good is the present phase using the Euclidean distance squared to the nearest signal constellation point. A comparison is made of the output of the three metrics and the loop may be adjusted accordingly.

This method is capable of tracking both phase and frequency errors. The performance is not as good as that of a locked MAP but it does not have the problems of either the MAP or fourth law devices.

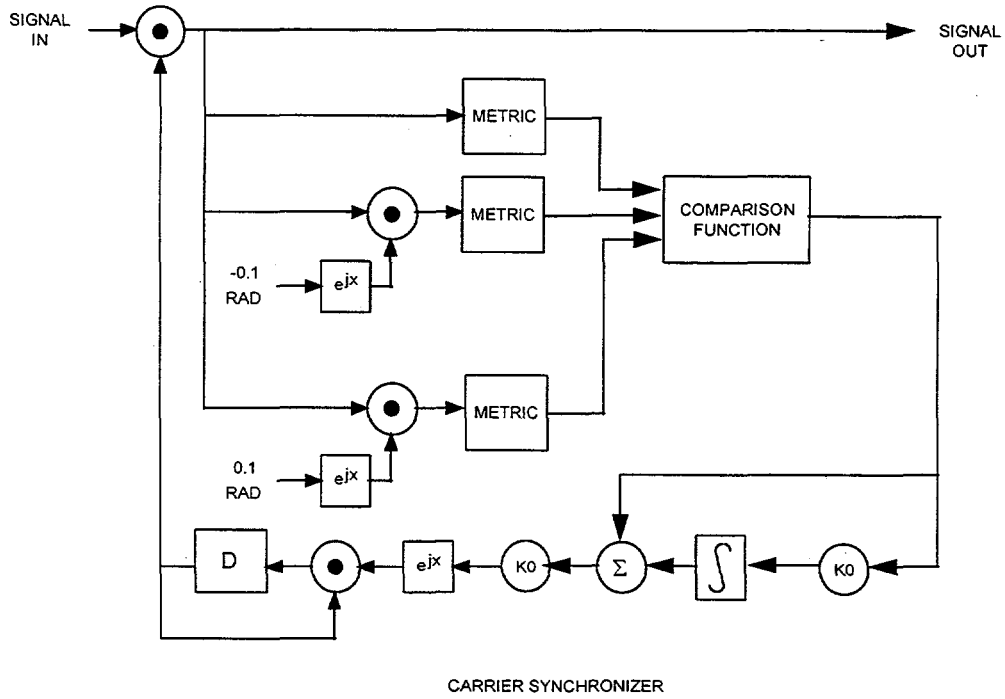


Figure 6.8 *Three-Phase Device.*

6.2.4 Combined MAP and Fourth Law Device

This device, shown in figure 6.9, uses the properties of MAP and fourth law devices to achieve carrier synchronization. The operation of the combined device is as follows. Under locked conditions the MAP PLL is the sole carrier synchronizer. A separate circuit monitors the loop for out-of-lock conditions. Once this condition is detected (e.g. during acquisition) the fourth-law device adds an additional phase estimate to the MAP and effectively knocks the MAP out of any "stuck" alignment. Once lock is established and is detected via a threshold device, the fourth-law device is turned off and the MAP PLL again assumes total control of synchronization. The method thus retains the optimal performance of MAP PLLs while correcting the associated problems with these devices and the constellation. This PLL will acquire and lock within 4000 QAM symbols for a frequency error of 0.002 times the symbol rate at E_b/N_o of 10dB.

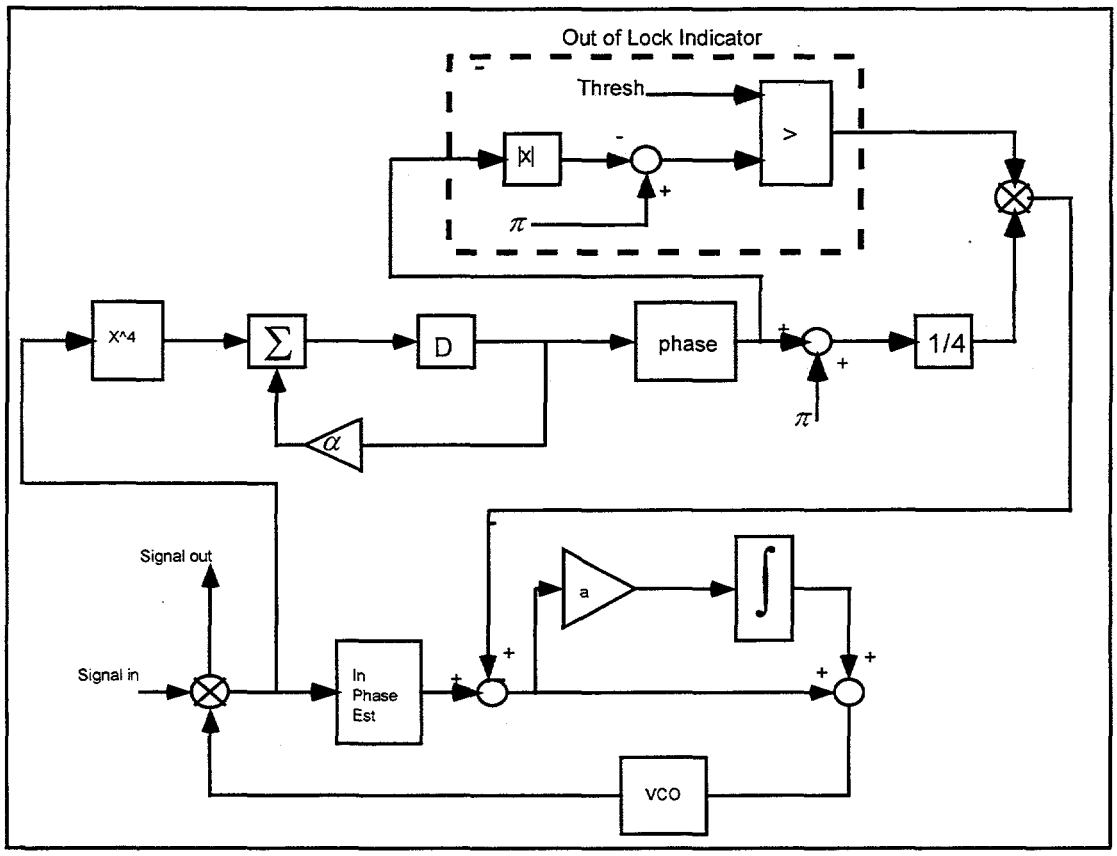


Figure 6.9 *Combined MAP and Fourth Law Device.*

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7. Non-Linear Amplification and Equalization

The effect of non-linear amplification is one of the long-term challenges to the project. This will not be an issue for this LDRD, but it will have to be faced before RF hardware is constructed. The effect of non-linear amplification on bandwidth efficient communication systems is threefold: 1) spectral regrowth occurs in signals that are filtered prior to the amplifier, 2) multilevel signal constellations are distorted, and 3) the precisely controlled pulse shapes discussed in section 4 are also distorted, defeating the non-ISI property of pulse shaping. To determine the impact on system performance, models of non-linear amplifiers must be incorporated into the system.

7.1 Non-linear Amplifier Models

In modeling a non-linear amplifier, it is usually assumed that if the input to of the amplifier is of the form:

$$s(t) = A(t)\cos[2\pi f_C t + \theta(t)]$$

then the response is of the form:

$$x(t) = g[A(t)]\cos(2\pi f_C t + \theta(t) + \phi[A(t)])$$

where $g(x)$ and $\phi(x)$ are respectively the amplitude and phase response characteristics of the amplifier. Usually g(x) and ϕ(x) can be represented as ratios of polynomials, where second degree polynomials are sufficient for most modern amplifiers. For example, figure 7.1 shows the amplitude and phase response of a typical high-powered amplifier (HPA), or traveling wave tube amplifier (TWTA). Although TWT's are being replaced by modern solid state amplifiers, non-linearities are still present, although to a lesser degree, and the mathematical models of the new amplifiers are of similar form. The magnitude response of the TWT is of the form

$$g(x) = \text{maximum output} \cdot \frac{2x}{1+x^2}$$

and the phase response is of the form

$$\phi(x) = \text{maximum phase distortion} \cdot \frac{2x^2}{1+x^2}$$

where x is the input relative to the maximum.

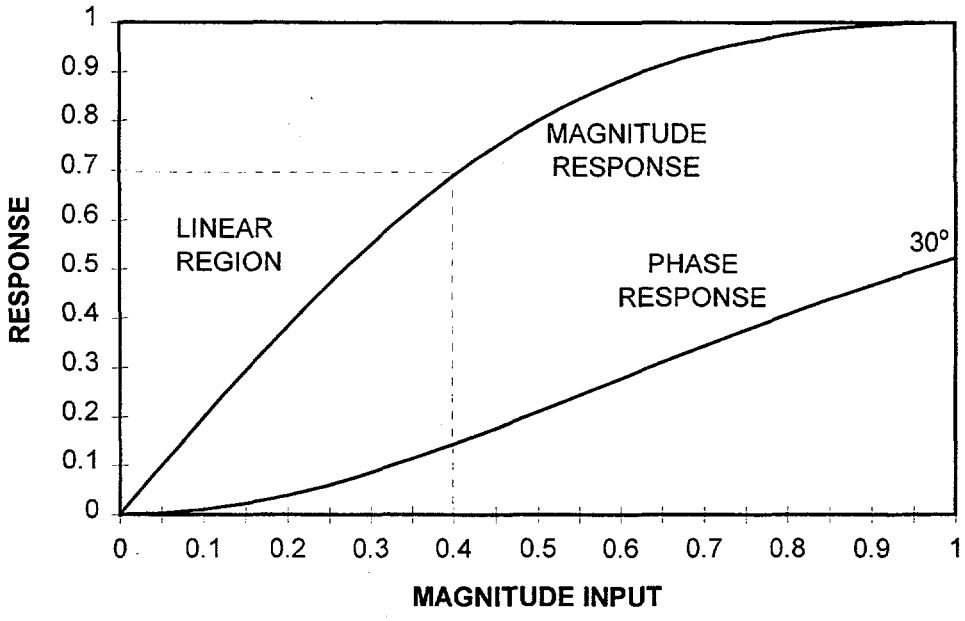

Figure 7.1. *Magnitude and Phase Response of High Powered Amplifier.*

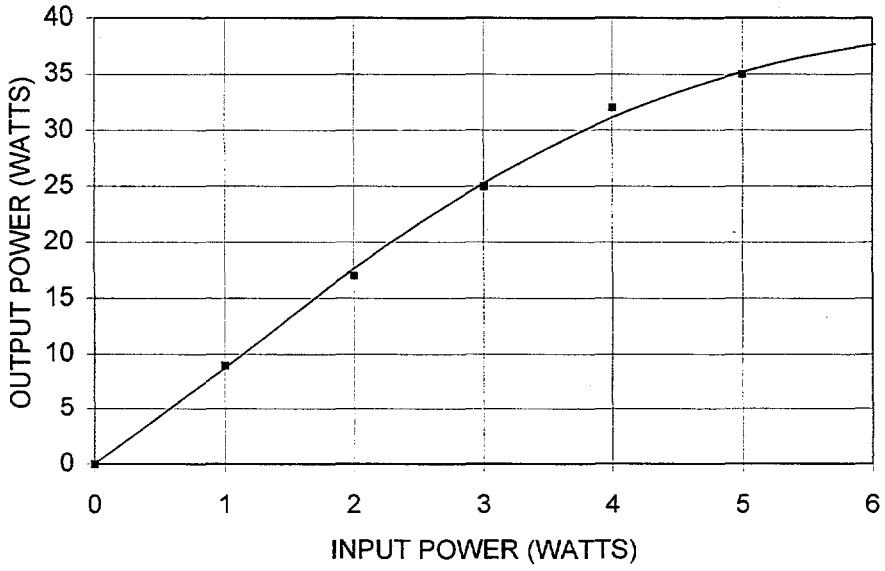

Figure 7.2. *Magnitude Response of typical Modern Electronic Amplifier.*

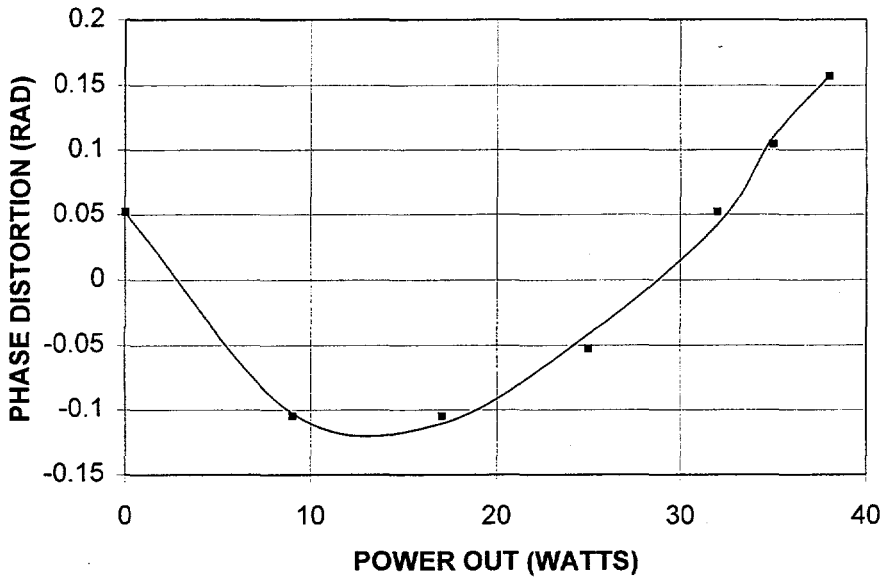

Figure 7.3. *Phase Response of Typical Modern Solid State Amplifier.*

A modern solid state amplifier, as found in the Motorola RF device data book, has amplitude and phase response as shown in figures 7.2 and 7.3 respectively. This response was fit to the curves:

$$g(x) = \frac{-0.2415x^2 + 1.752x + 0.003615}{0.05257x^2 - 0.2148 + 0.6749}$$

and

$$\phi(x) = \frac{0.1111x^2 - 0.2490x + 0.07758}{0.4449x^2 - 1.352 + 1.495}$$

In many cases, AM/AM, or AM/PM curves are not available for a given amplifier, but the data sheet provides a figure for 3rd order intermodulation distortion (IMD). In this case, we must find a set of parameters for the g(x) and ϕ(x) models to match the IMD data given by the manufacturer.

If x is the input to a nonlinear device, then the output, y may be approximated by a polynomial:

$$y = a_0 + a_1x + a_2x^2 + a_3x^3 + \ldots$$

If x is the sum of two pure tones at frequencies f_1 and f_2, then the odd order terms of the response will generate intermodulation products within the bandwidth of the device. Specifically, the third order term will generate tones at frequencies $2f_1$-f_2 and $2f_2$-f_1. IMD

products at other frequencies are assumed to be outside of the system passband or of insignificant magnitude, except in less common cases where 5th order effects are significant.

Third order IMD can be calculated using the g(x) and $\phi(x)$ models described previously. To do this, we define

$$x(t) = s_1(t) + s_2(t)$$

where

$$s_1(t) = A \exp(j2\pi f_1 t) \text{ and } s_2(t) = A \exp(j2\pi f_2 t)$$

Then the output of the non-linear device is given by:

$$y(t) = g(|x(t)|)\exp[\arg(x)+\phi(|x|)]$$

For any choice of f1 and f2 the fundamental period of x(t), and therefore of y(t) will be an integer factor of $\frac{1}{f1\text{-}f2}$. Therefore, the complex Fourier Series coefficient of the output, at frequency f1 is given by:

$$c(f1) = (f1\text{-}f2) \int_0^{\frac{1}{|f1\text{-}f2|}} y(t)\exp(2\pi f1)\, dt$$

Likewise, the intermodulation coefficient at frequency 2f1-f2 is given by

$$c(2f_1\text{-}f_2) = (f1\text{-}f2) \int_0^{\frac{1}{|f1\text{-}f2|}} y(t)\exp(2\pi(2f1\text{-}f2))\, dt$$

The first coefficient represents a desired component in the output, the second coefficient represents an undesired component. Therefore, the figure for third order IMD is given by

$$IMD3 = \frac{|c(2f2\text{-}f1)|^2}{|c(f1)|^2}$$

This calculation was accomplished using MathCAD, and parameters were found to match IMD distortion figures for a typical solid state amplifier suitable for the needs of the

project. A very typical figure was approximately -30dB, essentially flat over an input range of 14dB. This data was matched using a linear amplitude response, and a phase response of:

$$\phi(|x|) = \frac{\frac{50\pi}{3} - \frac{10\pi}{3}|x| + \frac{\pi}{6}|x|^2}{401 + 40|x| + 40|x|^2}$$

This response is illustrated in figure 7.4. Most of the distortion occurs at low power, while the phase offset is flat over most of the useful range of the amplifier. This means that with the amplifier operated at an appropriate drive level, the phase offset will be corrected by the phase synchronizer in the receiver, and no predistortion of the signal constellation is necessary. Only a loss of about 0.5 dB will be experienced due to distortion of the raised cosine pulse.

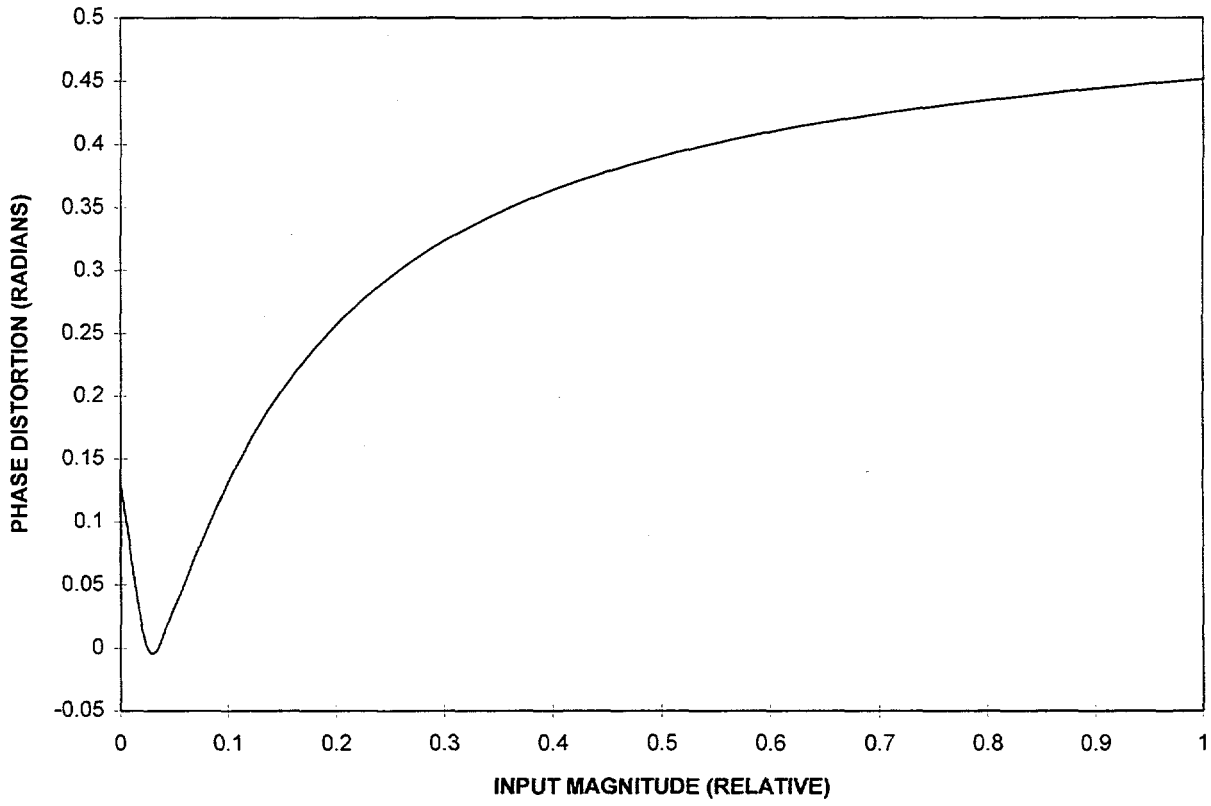

Figure 7.4. *Phase Response derived from IMD data.*

As another example of system performance using a modern solid state amplifier, an SPW model of a high powered amplifier was obtained from JPL. This data was fit to the curves:

$$g(x) = \frac{1.8469x-8.6641x^2+18.7334x^3-25.4113x^4+17.5743x^5}{1-4.0034x+4.5609x^2+4.3601x^3-17.9141x^4+16.0733x^5}$$

and

$$\phi(x) = \frac{1.363e5-2.601e7x+1.299e8x^2-3.673e8x^3+5.369e5x^4-1.177e8x^5}{1+1.342e10x-2.832e10x2+1.913e10x^3}$$

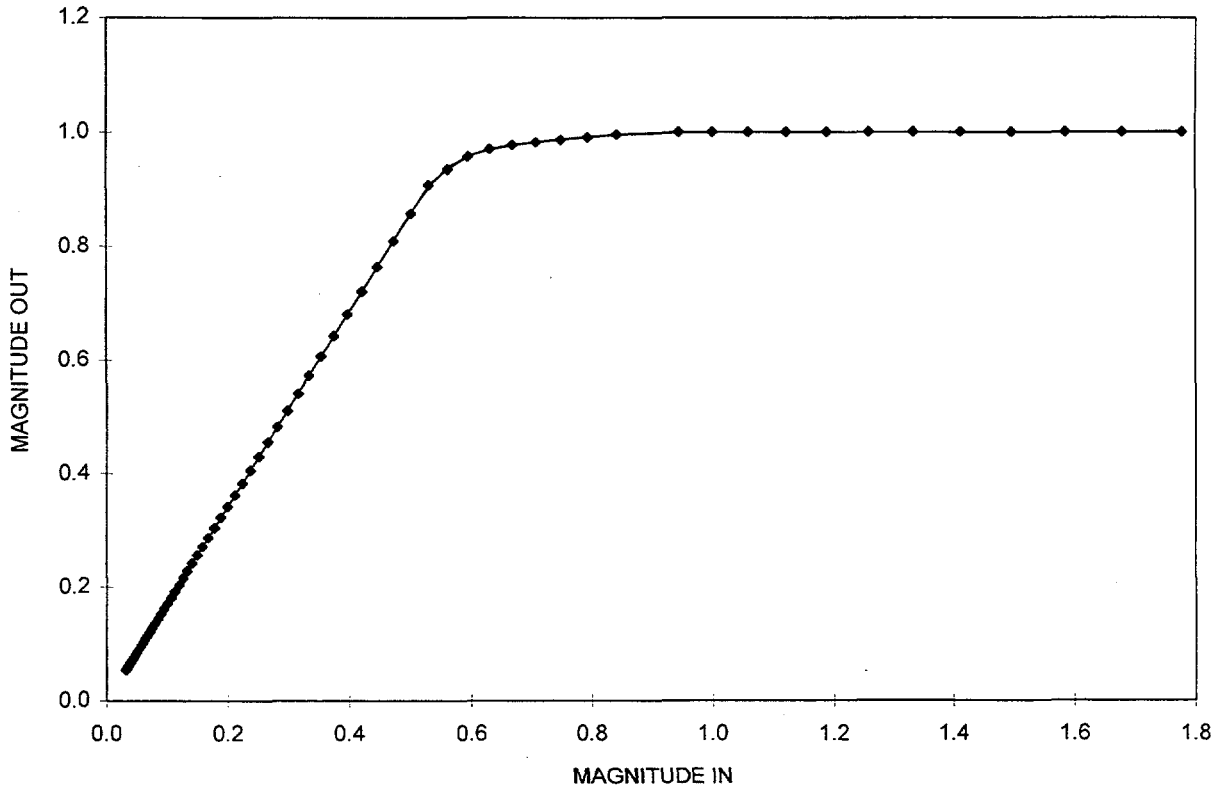

Figure 7.5. *Magnitude response provided by JPL.*

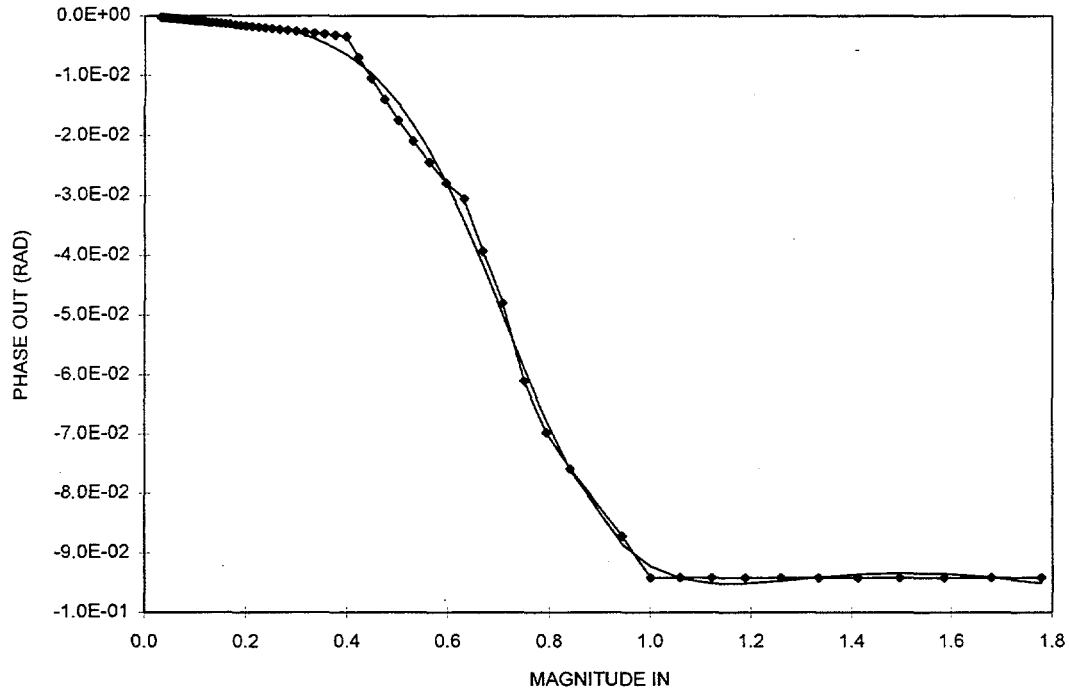

Figure 7.6. *Phase Response Provided by JPL, with fitted curve.*

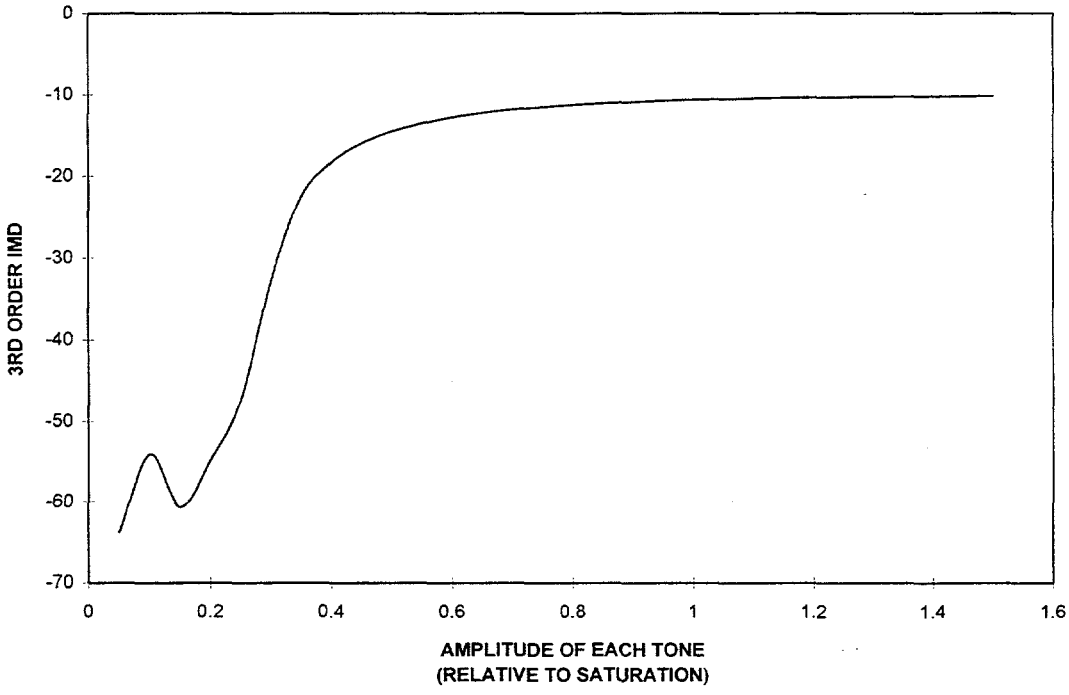

Figure 7.7. *Third order intermodulation distortion calculated from amplitude and phase data provided by JPL.*

7.2 Correction of Phase Distortion

In the case of the TWT, the distortion may be corrected by adding equalizers at baseband as shown in figure 7.8. The equalizer is of the form:

$$IEQ = \sum_{ij} u_{ij} I^i Q^j \qquad QEQ = \sum_{ij} v_{ij} I^i Q^j$$

where $i,j \geq 0$ and $i+j \leq 3$.

In other words, the non-linearity of the equalizer can be corrected by a Volterra equalizer of order 3. The coefficients for the equalizer were found by minimum mean squared error and are given in table 7.1. Because the 3rd order correction is not perfect, it introduces distortion in the response of the raised cosine filter, the effect of which is more significant when a lower rolloff factor is used. The bit error rate performance of the system is shown in figure 7.9. Without any non-linearities, the system will function, with no significant performance loss, with a rolloff factor as low as 0.2. With the high powered amplifier corrected by the equalizer, the system functions with negligible loss at a rolloff factor of 0.4, however, a loss of approximately 0.1 dB occurs at a rolloff factor of 0.2.

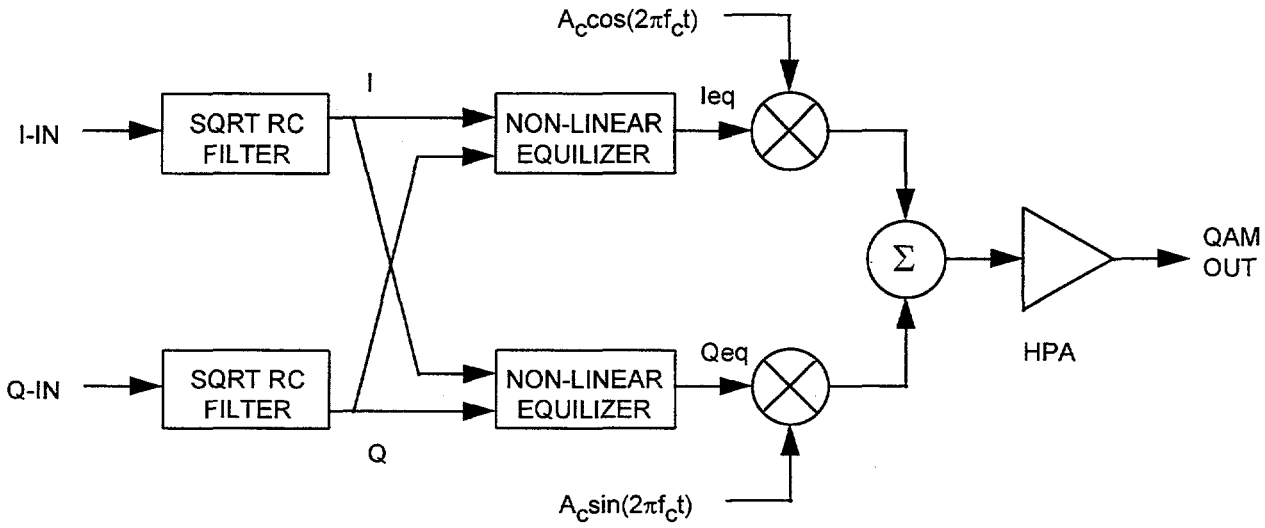

Figure 7.8. *The use of nonlinear equalizers with pulse shaping and non-linear amplification.*

u30	6.954E-02	v30	-8.752E-02
u21	9.976E-02	v21	6.962E-02
u12	6.972E-02	v12	-1.002E-01
u03	8.773E-02	v03	7.089E-02
u20	-7.439E-07	v20	8.260E-07
u11	2.837E-09	v11	-1.024E-06
u02	7.919E-07	v02	3.684E-07
u10	3.440E-01	v10	2.115E-02
u01	-2.112E-02	v01	3.433E-01

Table 7.1 *Coefficients of third order Non-Linear equalizer to invert magnitude and phase response of TWT.*

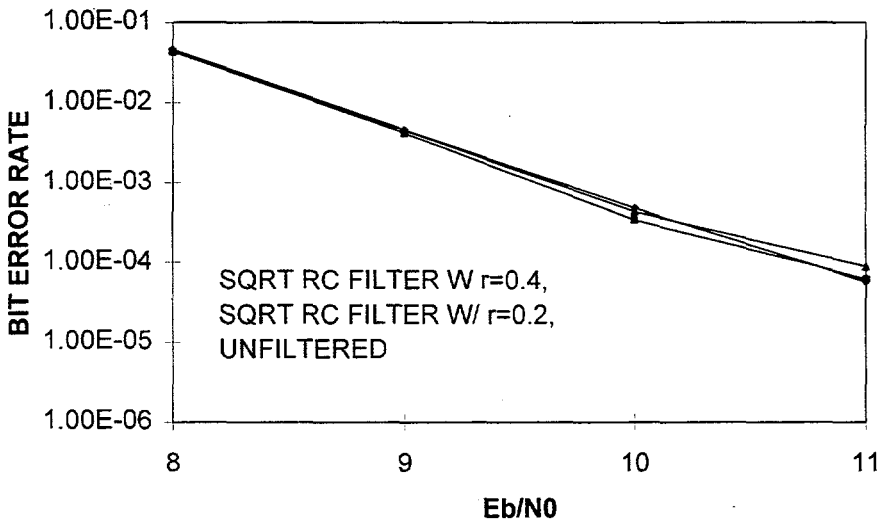

Figure 7.9. *Performance of system using HPA corrected by third order equalizer.*

In the case of the solid-state amplifier, this technique was unsuccessful. For this device, the AM/AM distortion had no significant impact on the bit-error-rate performance of the system when the phase distortion was not included in the system. However, the non-monotonic phase response of figure 7.3 apparently caused problems which the equalizer was not able to correct.

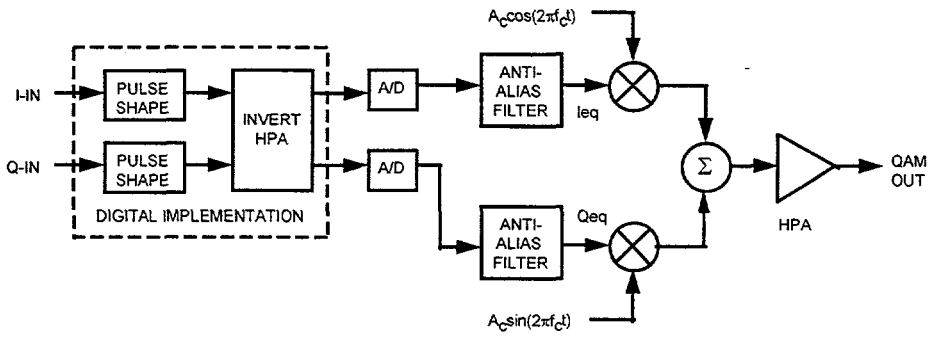

Figure 7.10. *Digital Preconditioning of Pulse for HPA.*

The analog equalizer, though not impossible to build, is not trivial either. Other options include predistortion of the signal constellation, or to accomplish pulse-shaping and equalization digitally, as shown in figure 7.9. Using a sampling rate of four times the symbol rate, this technique achieved performance close to the pulsed shaped system without a non-linearity, as shown in figure 7.10.

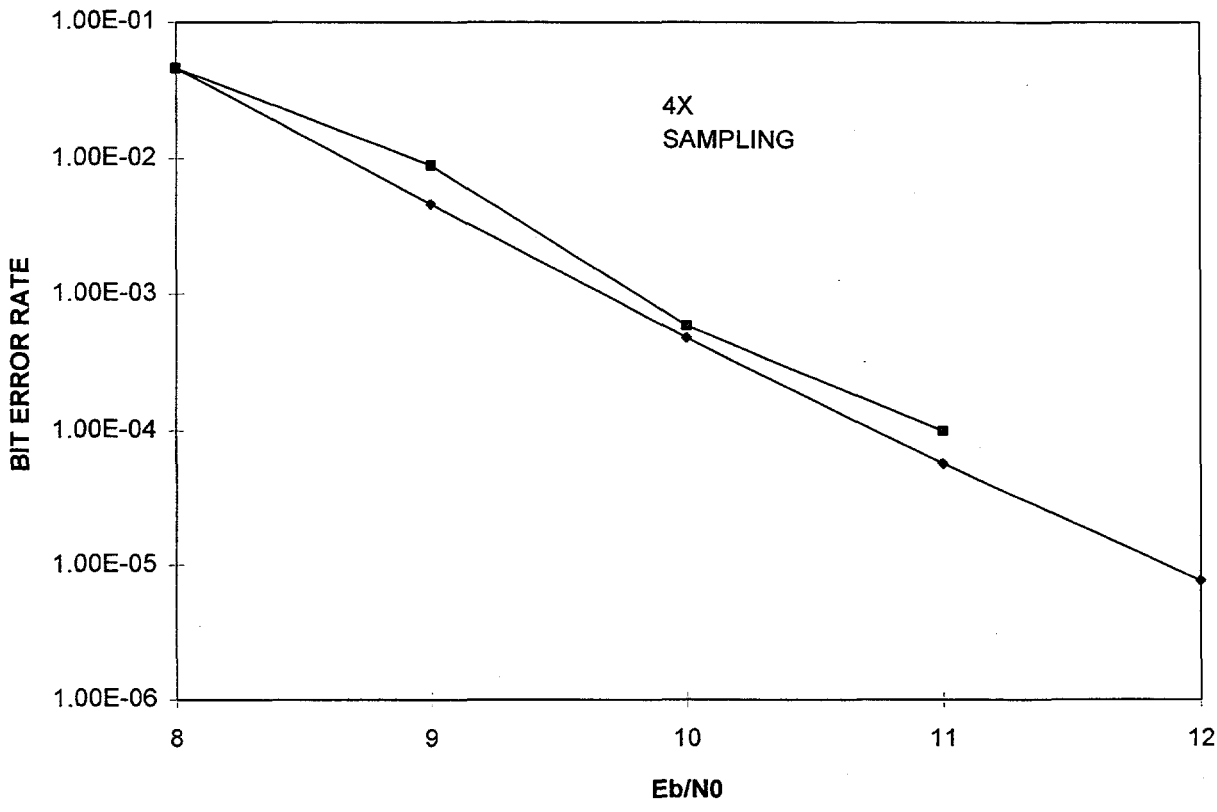

Figure 7.11. *Performance of system with 4 times oversampling digital equalizer.*

The simplest option of dealing with the non-linearity is to predistort the signal constellation. To do this AM/AM and AM/PM curves are obtained for the whole channel, that is, amplitude and phase of the signal vector at the output of the matched filter in the

receiver are compared to the amplitude and phase of the signal vector at the input to the pulse shaping filter in the transmitter. The curve thus generated is similar, but not identical to, the response of the amplifier itself, and can be represented as a ratio of polynomials. The channel response is completely invertable in the dynamic range of interest, that is, it is no problem to predistort the signal constellation in such a way that the desired signal vectors arrive at the output of the matched filter. The problem is that the non-linearity distorts the square-root raised cosine pulses, leading to ISI at the output of the matched filter. With a predistorted constellation, and the receiver scaled so that the distance between nearest signal vectors is unity, the variance of the difference between the transmitted signal and the received signal is 0.07. As the symbol rate was slowed, the variance became arbitrarily close to zero, showing that the predistortion function is accurate, and the difference is indeed due to ISI.

In the case of the modern amplifier, where the phase response was derived from intermodulation distortion data, the non-linearity is less severe, and the problems are less difficult. Here, the system can be operated with no correction of the non-linearity, other than the phase synchronizer in the receiver. The loss in this case will be approximately 0.5dB, as shown in figure 7.12.

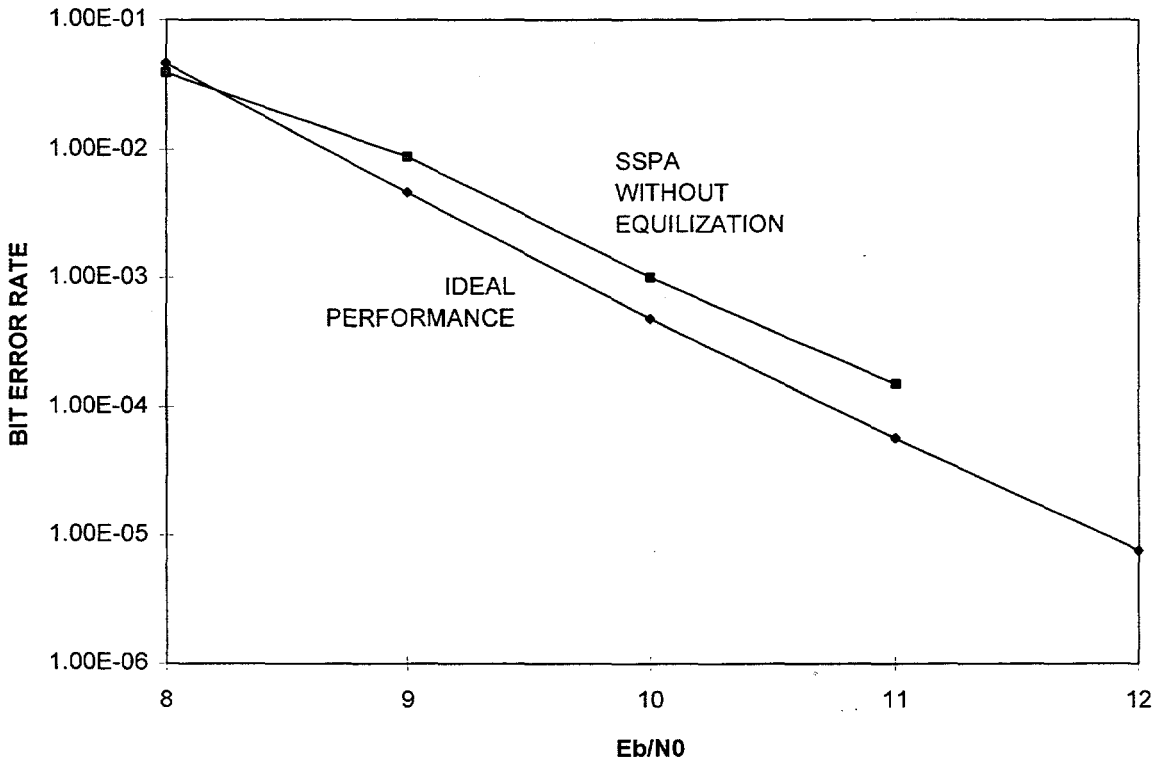

Figure 7.12. *Performance of system with using solid-state amplifier model provided by JPL and no predistortion or equilization.*

7.3 Spectral Regrowth

The spectral regrowth of a square-root raised cosine pulse passed through a severely non-linear amplifier is illustrated in figures 7.13 through 7.15. Here, the spectrum is shown against the NTIA mask. Figure 7.13 shows the spectrum at the output of the TWT when the input is scaled for saturation. The square-root raised-cosine spectrum is essentially coincides with the square lobe in the center, the sidelobes are due to the non-linearity. With the amplifier backed off by 1dB (figure 7.14), the sidelobes clear the NTIA mask, however, as in the linear case, a baud rate slightly less than the NTIA bandwidth is required for an edge attenuation of 10dB. In figure 7.15 it is shown that with the amplifier backed off by 1dB, and a baud rate of 0.9 times the NTIA bandwidth, the spectrum completely fits within the mask.

Looking at the spectrum in terms of 99% bandwidth poses another problem. With no amplifier backoff, the 99% bandwidth is 1.6 times the baud rate. With a 1dB output backoff, the 99% bandwidth is 1.1 times the baud rate. In the case of a severely non-linear amplifier, spectral considerations point in favor of preconditioning the pulse prior to the amplifier, since doing so prevents spectral regrowth, as well as providing the best bit error rate performance.

7.4 Summary of Amplifier Study

If the system is operated with a severely nonlinear amplifier, signal constellation predistortion or equalization may be needed to correct severe losses. In less severe non-linearities, which are typical of modern solid state amplifiers, no predistortion is necessary if an implementation loss of about 0.5dB is acceptable.

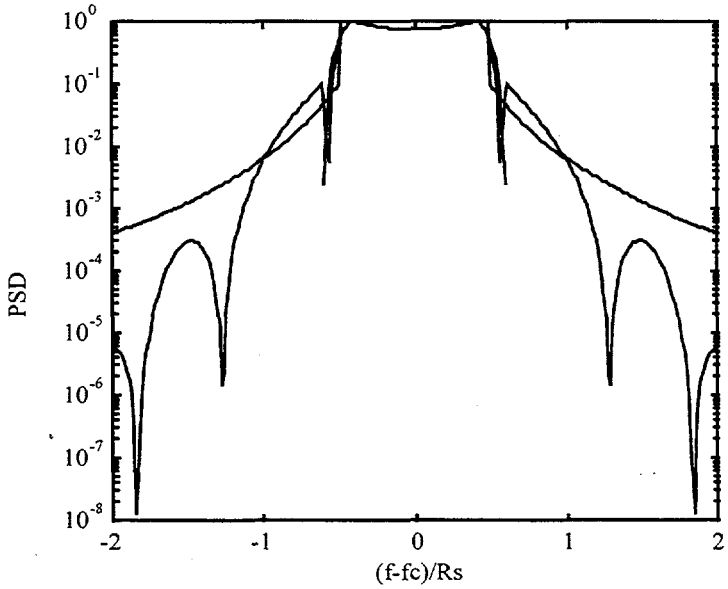

Figure 7.13. *Output of TWT with square-root raised cosine pulse input at saturation.*

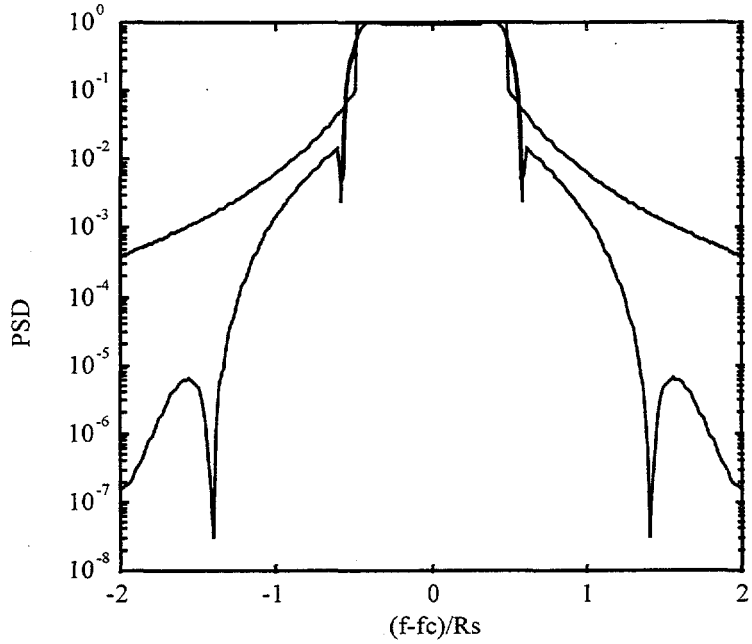

Figure 7.14. *Spectrum of square-root raised cosine filter at output of TWT operated at 1dB output backoff.*

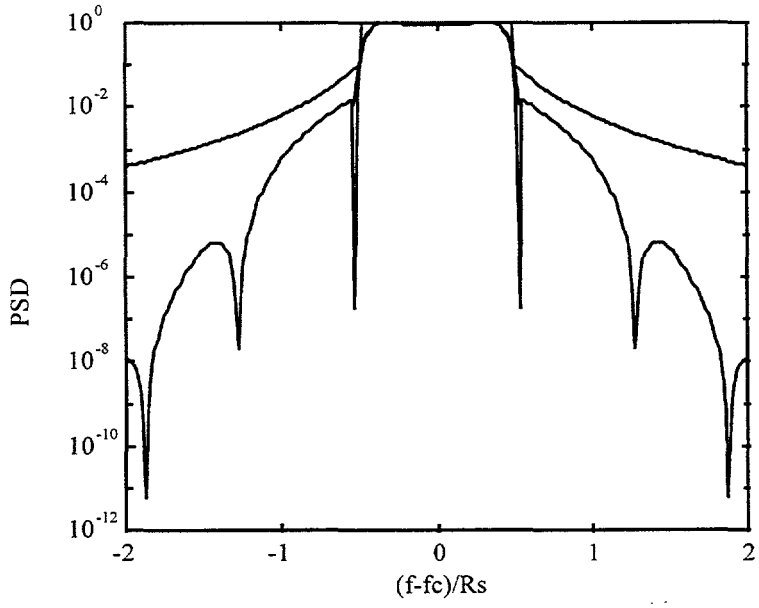

Figure 7.15. *Spectrum of Raised-cosine filter at output of TWT operated at 1dB output backoff and a baud rate of 0.9 times the NTIA bandwidth.*

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8. Implementation

The original goal of the project was to culminate in a proof-of-concept test utilizing existing equipment and off-the-shelf components to implement or emulate system functions. A complete development effort implementing state-of-the-art signal processing devices was beyond the scope of this LDRD project. The testbed constructed did not include equalizers but could be used to evaluate the system concept. A parallel effort included the design of symbol and carrier synchronizers to be added to the testbed later.

The importance of the synchronization circuits became obvious when the global clocks and carrier reference used in the testing were ineffective in providing expected results. This was due to synchronization problems encountered with the global signals themselves. Additionally, without the sophisticated signal processing capabilities, a high signal to noise ratio must be maintained. We believe the testbed which was constructed could not maintain the required signal to noise ratio.

While testbed debugging was ongoing, function specific DSP chips manufactured by Graychip, Inc., were being evaluated for implementing synchronization. These devices were selected along with an architecture suggested by Graychip. During discussions with Graychip representatives it was discovered that Wideband Computers Corp. was developing an identical system. The Wideband effort included full-scale development of QAM modulator and demodulator evaluation boards utilizing state-of-the-art A/D converters and advanced signal processing VLSI components. The design features robust clock and carrier recovery algorithms and block mode equalizer algorithms programmed within an on-board DSP processor.

Because of the problems with the analog testbed implementation and since a design and development effort would be needed in any case, a decision was made to redirect the implementation effort to an all-digital design.

8.1 Analog Testbed Implementation

The diagram for the testbed implementation is shown in figure 8.1. This system operates at 90 MHz IF using programmable transversal filters (PTF), and has global carrier and clock references. Synchronization issues and RF implementation were to be dealt with in future tests. This system utilizes analog components for the modulator and demodulator. Because of the following problems the testbed implementation did not approach the expected performance levels.

- In the testbed setup, the channel was modeled by using a couple of programmable transversal filters as shown in figure 8.1. These filters, manufactured by Comlinear Corp., were not working as expected and are no longer supported by the manufacturer.

- General purpose QAM demodulator outputs, I and Q, were not stable. These outputs were from a subsystem built by a graduate student at NMSU in 1992 and modified for this testbed.

- As a consequence of the demodulator problem, the analog-to-digital converter portion of the decoder did not work properly.

The testbed included commercial equipment as well as equipment designed and fabricated by graduate students at NMSU. Except for the encoder and decoder PC boards all remaining equipment is an analog modulator and demodulator implementation. This testbed did not include the components necessary for symbol and carrier synchronization. These components still needed to be designed and produced. Because of the above problems and because components still needed to be produced to complete the system there was a redirection in the project to an all-digital implementation using DSP chips. The all-digital implementation is discussed in sections 8.4 and 8.5.

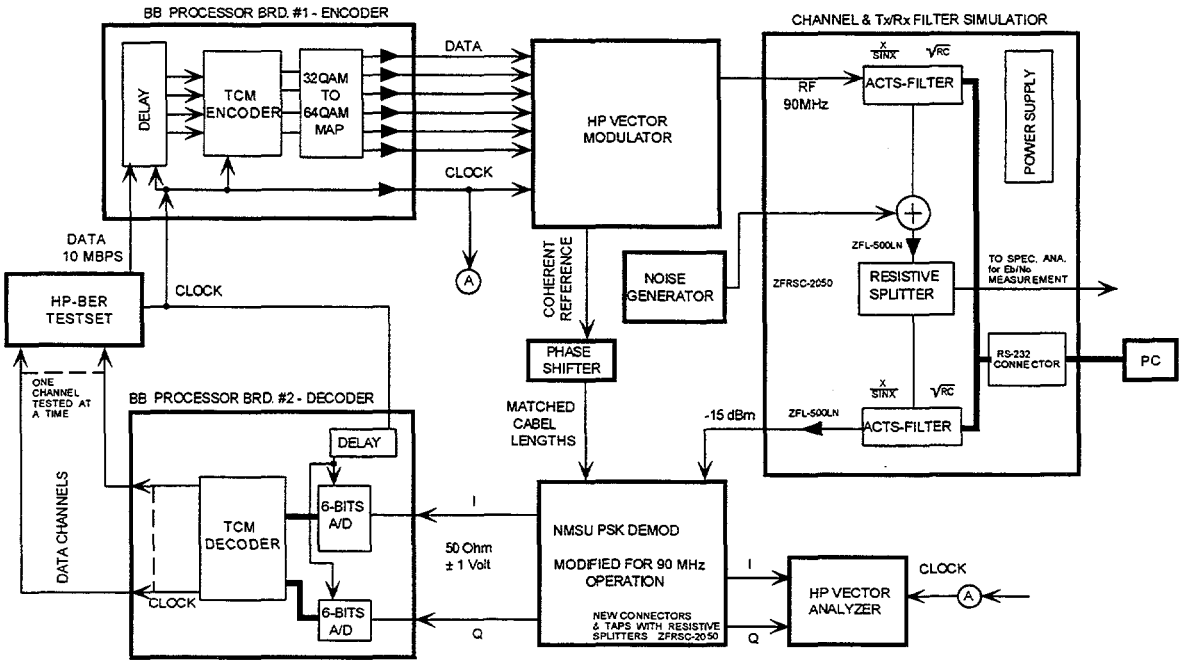

Figure 8.1. *Testbed implementation.*

8.2 Encoder Logic

The baseband encoder logic was developed for the testbed, and implemented in a programmable logic device. However, the encoder logic circuits are still applicable for the all-digital implementation discussed in sections 8.4 and 8.5. The encoder logic is shown in figure 8.2. The data is differentially encoded and mapped onto the 32-QAM constellation, which provides 8-level I and Q for the D/A's. In place of the D/A's, the 64-QAM mode of the Hewlett-Packard vector modulator owned by the NMSU Telemetry Center was used for the testbed. The 32-QAM mapping consists strictly of conventional logic, and generates digital I and Q coordinates to be supplied to the vector modulator or, if necessary (if

predistortion is required), to D/A converters. The convolutional encoder consists of 7-latches and six exclusive-or gates. The most difficult part of the transmitter side is the pulse shaping filter design, given all the trade-offs discussed previously. This filter is discussed later in section 8.4. The encoder modifications necessary for interfacing to the digital modulator required only the reprogramming of the programmable logic device.

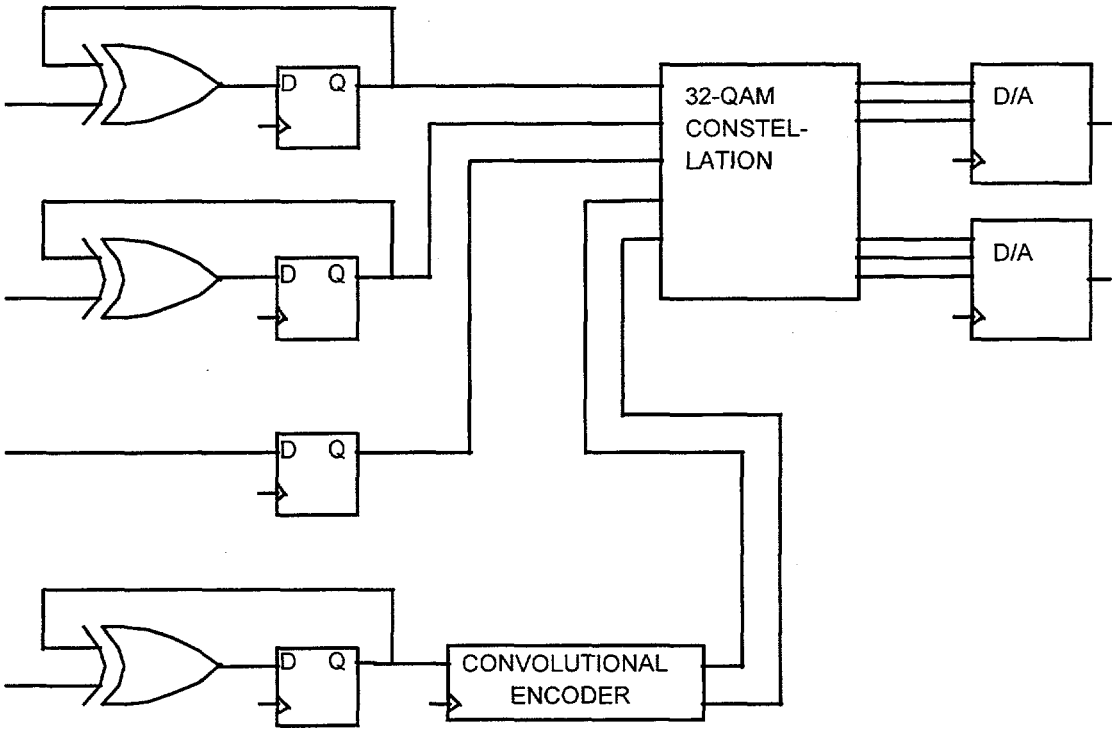

Figure 8.2. *32-QAM Encoder Logic.*

8.3 Decoder Logic

As for the encoder logic the decoder logic required little modification for interfacing to the all-digital receiver. The receiver logic, which is somewhat more complicated than the transmitter logic, is shown in figure 8.3. All of the logic is designed with the assumption that the received I and Q vectors will be represented in six-bit signed magnitude format, although conversion from one binary format to another is not a difficult problem. The A/D converters and the Viterbi decoder chip were purchased, all other logic was implemented in programmable logic devices.

The code-vector-extractor generates a soft decision for the Viterbi decoder. Soft decisions are explained in section 5.2. Because there are two code bits, two soft decisions are needed. In the signal constellation of this system, one of the two soft decisions may be extracted solely from the I component, the other solely from the Q-component. Two code vector extractors are needed for this purpose, but both are identical.

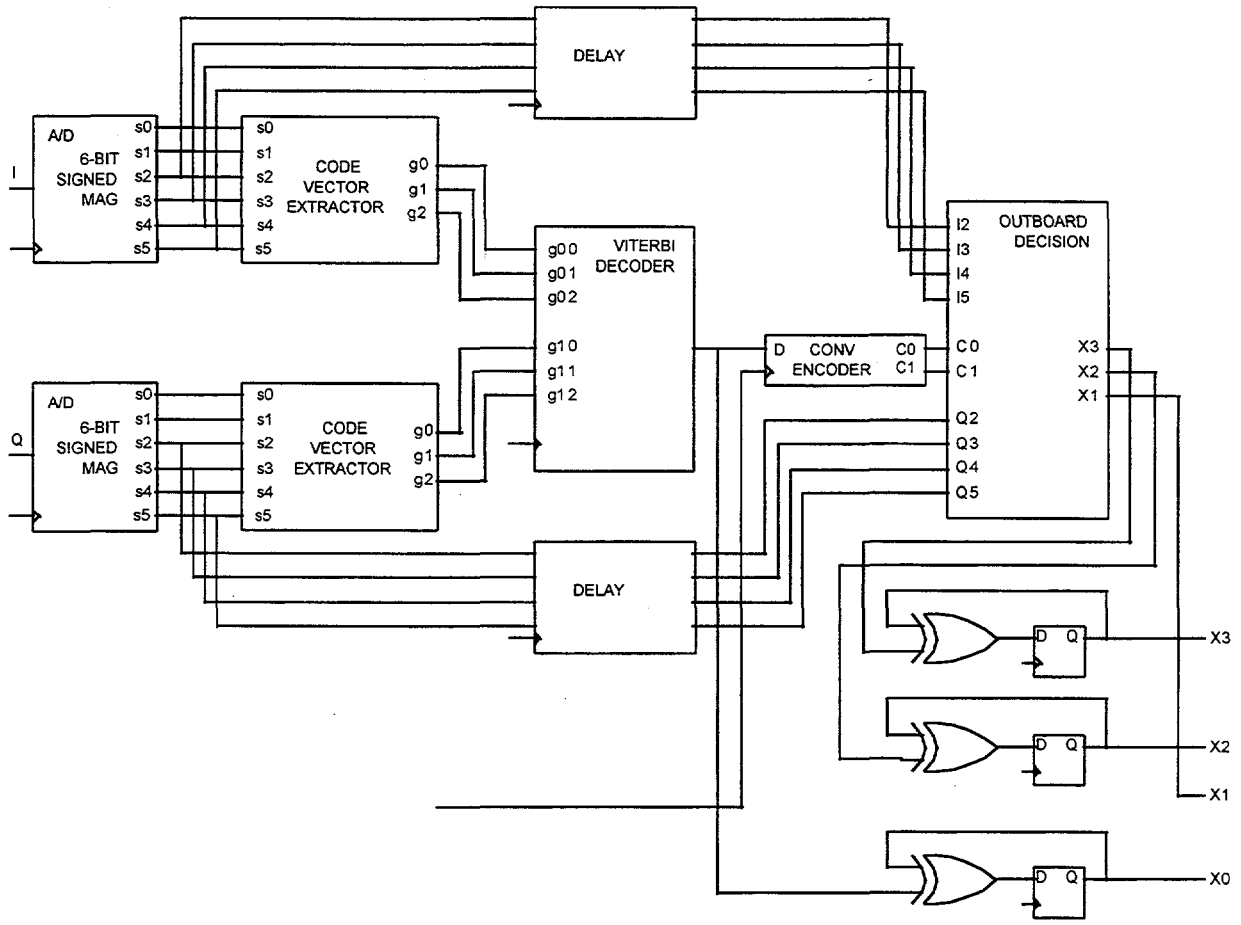

Figure 8.3. *Baseband Receiver Logic.*

The outboard decision logic (figures 8.5, 8.6, 8.7) determines the outboard bits by comparing the incoming signal to a set of thresholds. The optimal thresholds depend up on the code bits, as explained in section 5.2. In the actual boards, this is accomplished by combinational logic. The outboard decision is made using the two code bits and the four most significant bits of each signal vector component. The signal vector components must be delayed to match the end to end delay of the Viterbi decoder.

As can be seen, all of the supporting logic required for the support of the decoder can be implemented without an inordinate volume of gates, or unusual functions. The delay blocks which must account for the delays through the Viterbi decoder required the most real estate on the programmable logic devices. The A/D converters were used during the testbed implementation but later bypassed for the digital demodulator implementation.

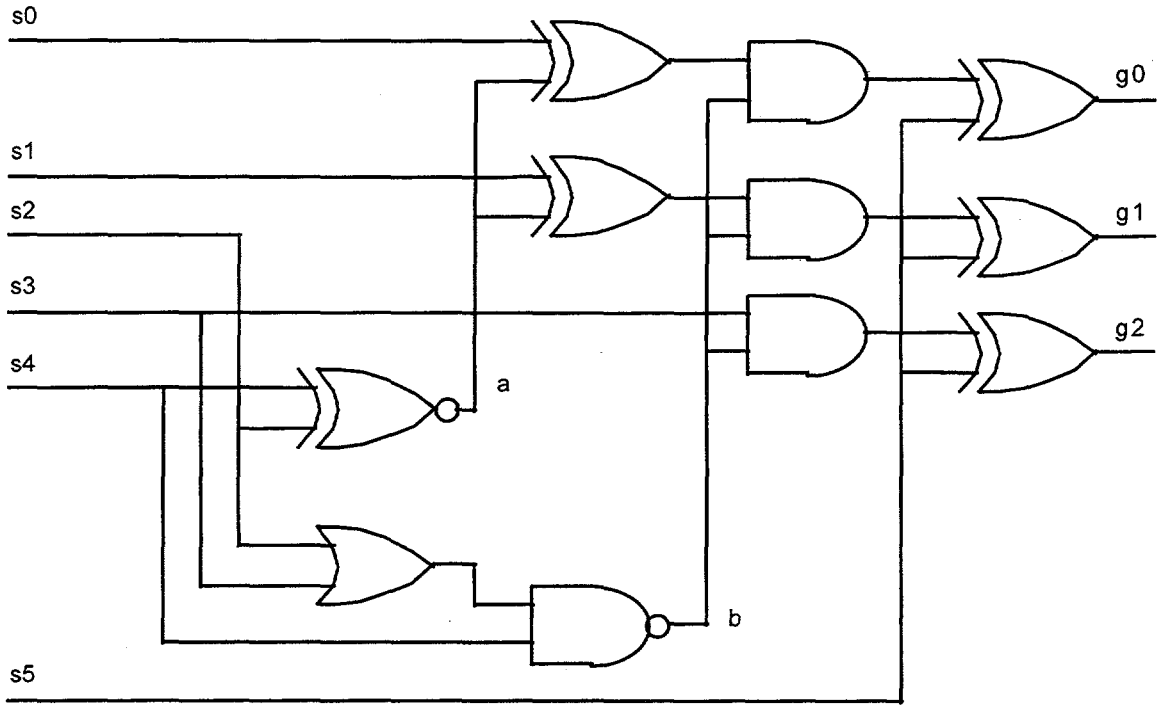

Figure 8.4 *Soft Decision Logic*

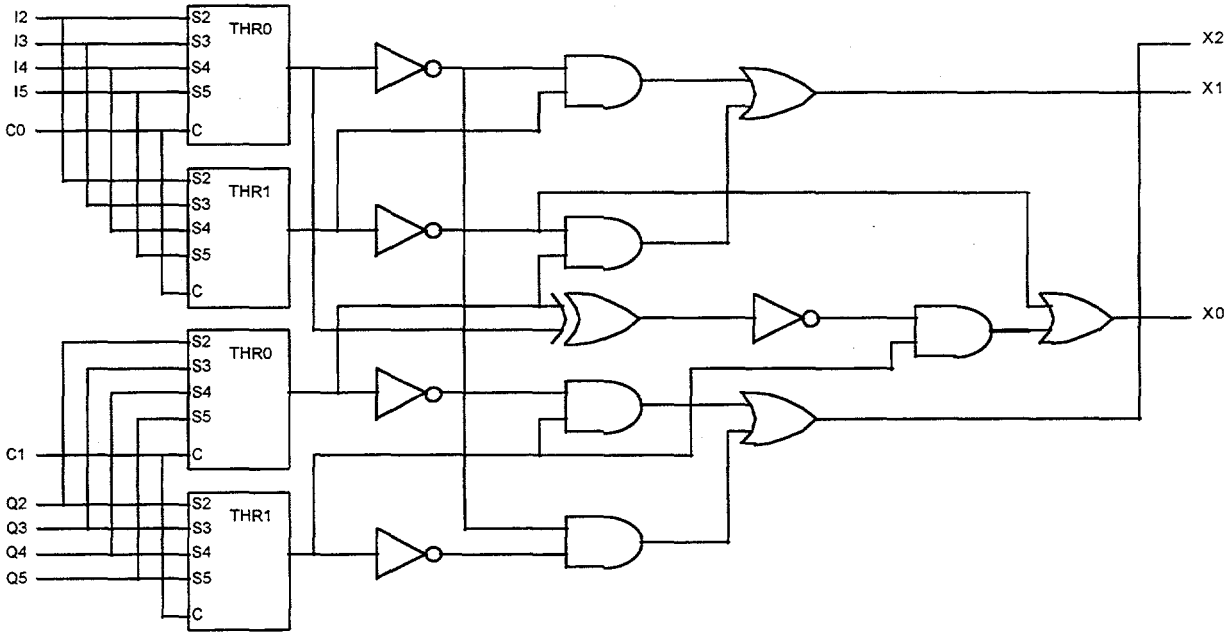

Figure 8.5 *Outboard Decision Logic*

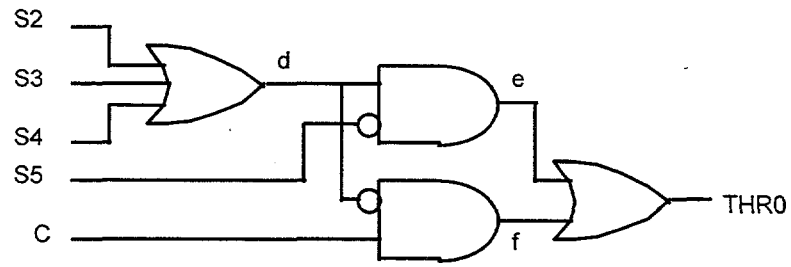

Figure 8.6 *One of two threshold detectors used in the outboard decision logic.*

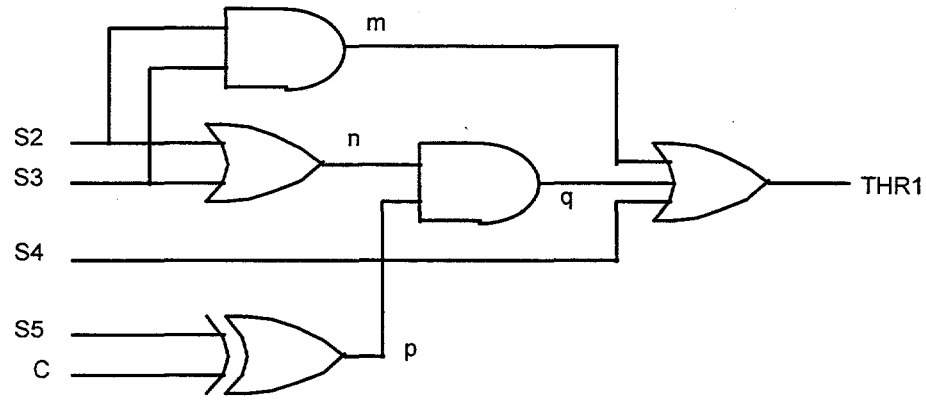

Figure 8.7 *The second of two threshold detectors used in the outboard decision logic.*

8.4 Modulator Implementation using a DSP chip

Once a decision was made to go to an all-digital receiver we decided to implement pulse shaping and Nyquist filtering digitally using a programmable digital filter chip (GC2011). A block diagram of the digital modulator is given in figure 8.8. This modulator evaluation board was developed by Wideband Computers along with the QAM demodulator evaluation board discussed in the next section. The output of the modulator has the signal centered at an IF frequency of 70 MHz. The input to the modulator are the constellation words from the encoder board.

The modulator receives the constellation words from the encoder board and formats the data into I and Q symbols. The I and Q symbols are zero padded to be at a sample rate equal to 2B or 4B. In this case each I and Q baseband symbol is zero padded with three zeroes between each symbol and interpolation filtering raises the sampling rate to 4 times the sampling rate (4B). The GC2011 then receives the zero-padded I and Q symbols to perform Nyquist pulse shaping and Sin(x)/x distortion compensation. In a particular application, predistortion to correct for non-linear amplification could be added.

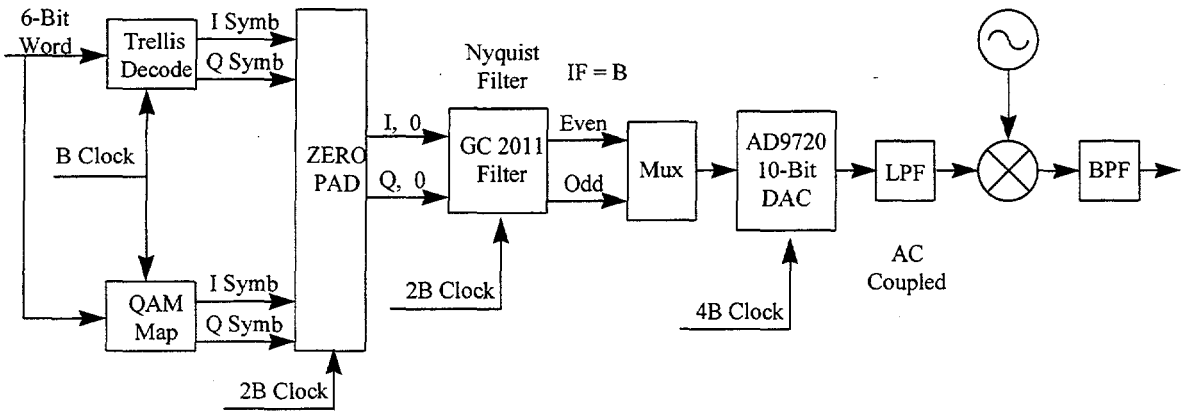

Figure 8.8 *Digital Modulator Block Diagram.*

The filtered and interpolated I and Q samples are converted to real samples. Even and odd time samples are produced at the A and B output ports of the GC2011. These time samples are multiplexed together and sampled by the digital-to-analog converter (DAC) at 4 times the symbol rate. An N-pole analog elliptic filter provides the post DAC anti-image filtering. This signal is frequency upconverted to 70 MHz and bandpass filtered. This IF frequency can be further upconverted to the desired RF frequency.

8.5 Demodulator Implementation using DSP chips

The all-digital receiver block diagram is given in figure 8.9. The portion inside the dotted lines represents the digital demodulator functions performed by the evaluation board developed by Wideband Computers. The demodulator expects a 70 MHz IF signal as an input. This IF frequency was chosen because many RF receivers available commercially will provide a 70 MHz second IF as an output.

In this architecture the analog IF signal is sampled at or above the Nyquist rate. The Nyquist sampled signal is then resampled by a GC3011 chip to a sample rate which is a multiple of the symbol rate, typically 4B for real samples and 2B for complex samples. The baud-synchronous samples are then passed through a fractionally-spaced equalizer (FSE) built using GC2011 filter chips. The FSE performs Nyquist (baud-shaping) matched filtering and removes signal distortion and intersymbol interference (ISI) from the signal. The output sample rate of the equalizer is decimated to be equal to the symbol rate of the signal. The carrier removal chip mixes the signal down to baseband and removes any carrier or phase offset from the sample stream. The I and Q outputs from the demodulator are provided to the decoder circuitry and the Viterbi decoder. The Viterbi decoder provides a signal to the demodulator to rotate the constellation by 90 degrees when out of sync. This rotation resolves the 90 degree phase ambiguity.

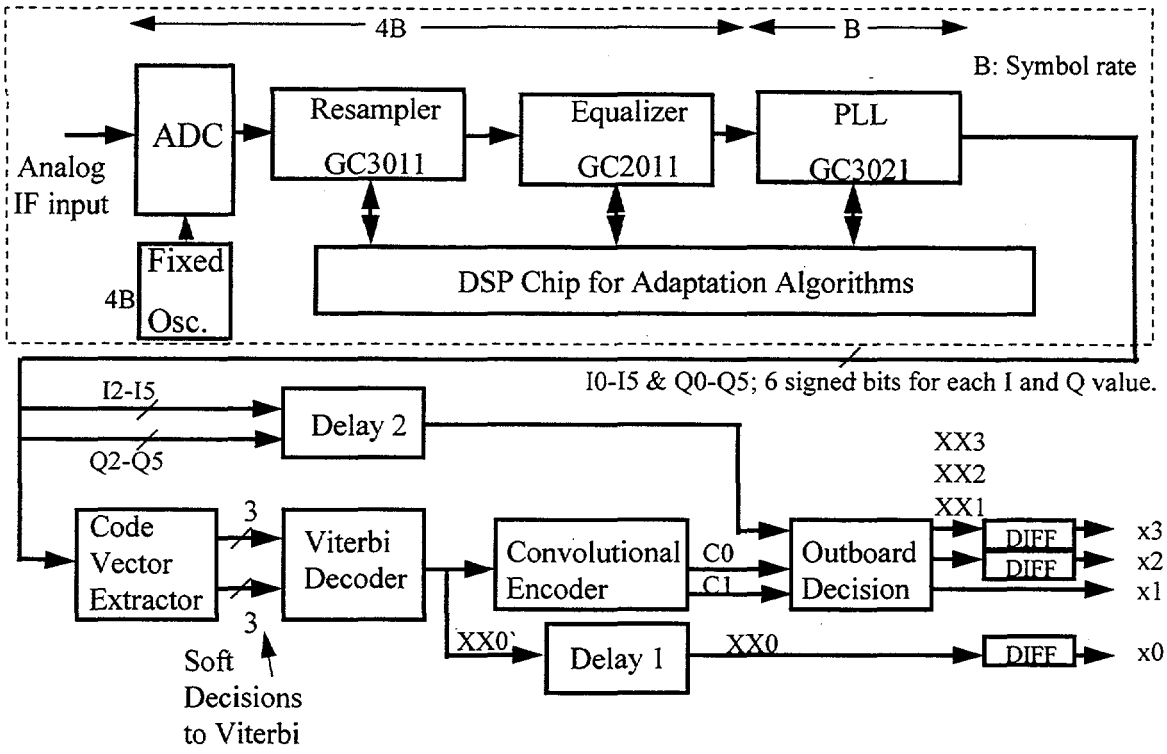

Figure 8.9. *Digital Receiver Block Diagram.*

Three adaptation loops are required to make the demodulator work. First, a baud timing loop adjusts the GC3011's resampling ratio to lock the resampled data rate to a multiple of the symbol rate. Second, a carrier loop removes residual carrier and phase offsets from the equalized signal, and third, the FSE coefficient update loop adjusts the equalizer to remove unwanted signal distortion and ISI.

The analog IF signal is initially sampled by an ADC operating at a fixed clock rate. The sample must exceed the Nyquist requirement for the signal's bandwidth, but does not have to be locked in any way to the signal's symbol rate. This simplifies the analog front end by eliminating the need to synthesize an ADC clock locked to a multiple of the symbol rate. Instead the proposed architecture uses the GC3011 digital resampler chip to lock the signal's sample rate to the symbol rate. Timing recovery is performed by using a simple zero crossing algorithm.

Carrier recovery is performed by using a decision-directed technique. The decision-directed technique uses the phase error between the baseband samples and the symbol decisions to drive the phase offset, and therefore the carrier offset, to zero. The phase errors are used in a PLL which feeds the carrier removal numerically controlled oscillator (NCO). The GC3021 Chip contains the mixer, NCO and phase error loops required to acquire and remove carrier offset. An error lookup table in the GC3021 is programmed with a one bit value for each I and Q error value. This table is 64X64 bits with each location having either a zero or a one. When the bit value is equal to zero the NCO is forced to increase the phase of its oscillator. When the bit value is equal to one the NCO is forced to decrease the phase of its oscillator. Figure 8.10 shows the one bit error values for the upper half of the constellation. This system works when the data has been randomized since any

constellation point not located at a multiple of 45 degrees is considered noise. This forces the constellation to achieve lock in the correct orientation or a multiple of 90 degrees. As discussed earlier, 180 degree phase ambiguity is handled by differential encoding. To correct for ±90 degree phase ambiguity, a signal is supplied to the demodulator from the Viterbi decoder when error metrics exceed a threshold indicating an out of sync condition. When the demodulator receives this signal a 90 degree phase rotation is performed and time is allowed for the Viterbi decoder to achieve sync.

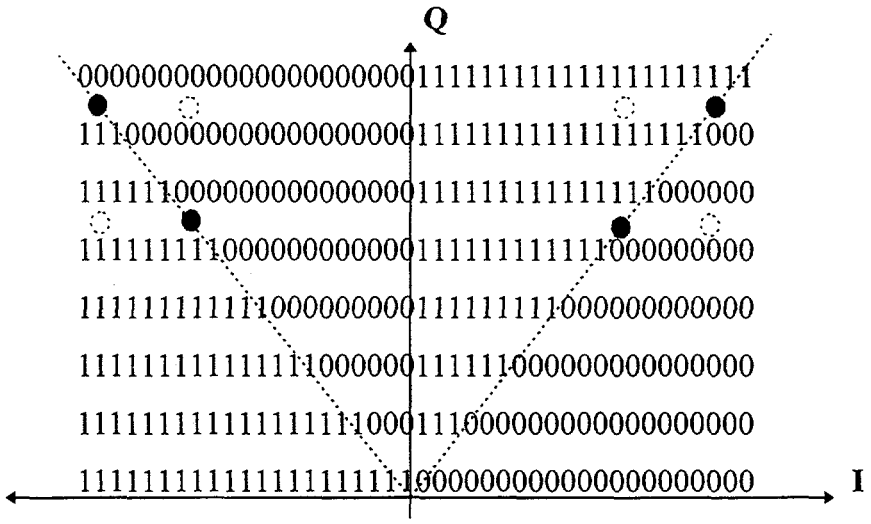

Figure 8.10. *One bit error values of error lookup table RAM for half of the 32-QAM constellation points.*

A baseband equalizer architecture using three GC2011 filter chips, two GC3011 resampler chips and one GC3021 Carrier Removal chip is shown in Figure 8.11. In this architecture the GC2011 and GC3011 chips are clocked at twice the symbol rate allowing symbol rates up to 35 MHz. The GC3021 chip is clocked at the symbol rate. The filter is a 32 tap T/2 spaced FSE which receives coefficient updates from a TMS320C44 DSP processor.

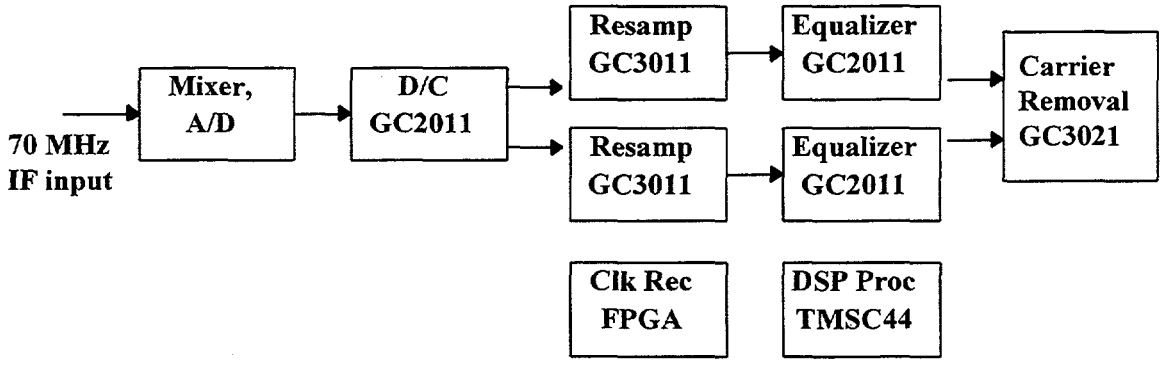

Figure 8.11. *Baseband Equalizer Block Diagram.*

The input signal is initially centered at a frequency equal to $F_S/4$, (or $F_S \pm F_S/4$) where F_S is the ADC's sample rate. The sampled signal will be centered at $F_S/4$. The signal is

then translated down to zero frequency using the GC2011 chip in an $F_S/4$ quadrature down convert mode. In this mode the chip accepts pairs of input samples and outputs down converted complex samples. The complex rate out of the chip is $F_S/2$. The complex samples are then resampled to a rate equal to 2 times the symbol rate by a pair of GC3011 chips, one for the I data and one for the Q data. Figure 8.12 shows the frequency spectra of the signal at different points of the digital modulator. In this case the ADC's sample is 32 MHz.

The complex samples are equalized using two GC2011 filter chips, one producing the I outputs and the other producing the Q outputs. The two chips implement a 32 tap decimate-by-2, complex data by complex coefficient filter. The evaluation board supplied by Wideband uses blind Goddard algorithm during signal acquisition, and switches to a decision-directed least mean squares algorithm after acquisition.

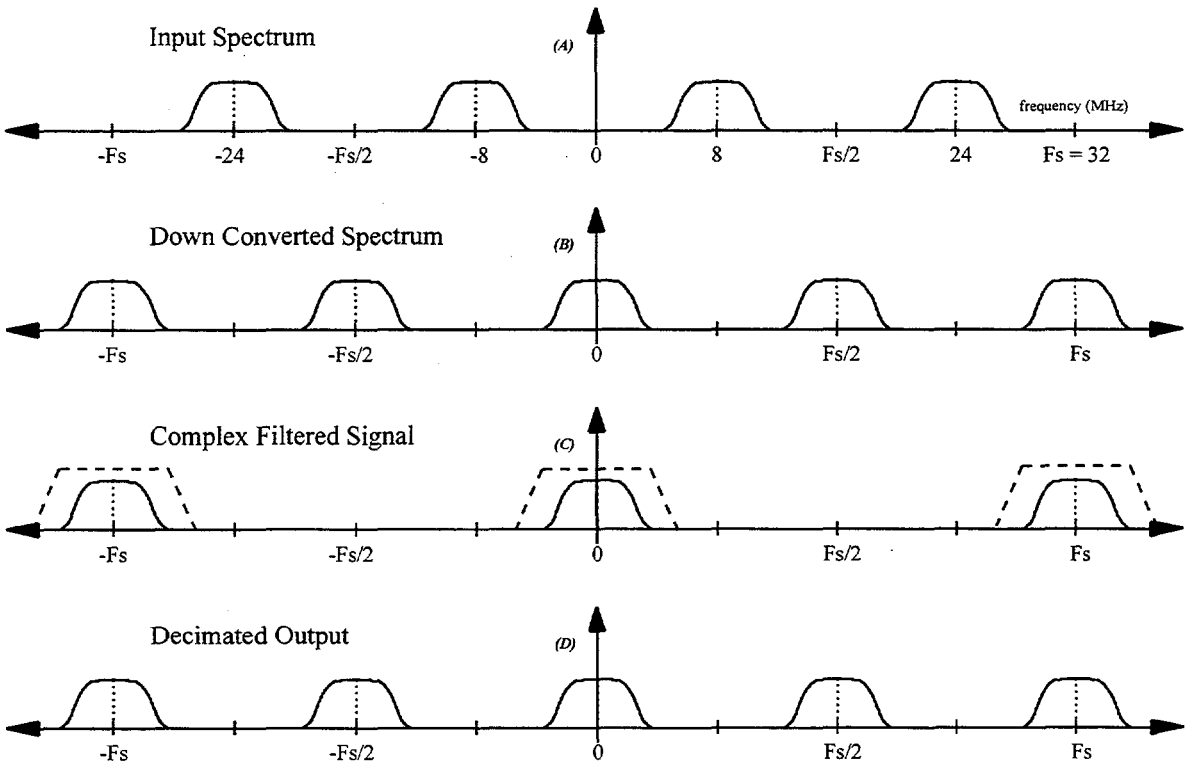

Figure 8.12. *Digital Demodulator Spectral Response.*

9. Conclusions and Recommendations

The analysis and simulations of phase I of the project have shown that the implementation of a 4 bit per symbol system on a bandlimited channel presents significant challenges, but is not infeasible. Accomplishments of the first phase of the project are as follows:

* A suitable trellis-coding scheme has been defined and shown, via computer simulation to have acceptable bit-error-rate performance.

* It was shown that the decoder for the coding scheme can be implemented with an available Viterbi decoder and ordinary logic gates.

* It was shown that symbol synchronizers and phase synchronizers can be designed to operate with the 32-QAM constellation at tolerable loss.

* Pulse shaping was introduced at a negligible loss.

* Non-linear amplification was introduced at tolerable loss. Techniques for correcting the distortion of nonlinear amplifiers were discussed.

The originally proposed system was composed of an analog modulator with a digital encoder for the transmitter and an analog demodulator with a digital decoder. The goal was to emulate the proposed system with test equipment and hardware provided by NMSU along with the Sandia provided encoder and decoder PC boards. Using this equipment a testbed was to be built to allow conceptual testing in the laboratory.

The original goal of using commercial equipment to emulate the proposed system in a conceptual demonstration did not provide the performance levels suggested by computer simulations. This was due to the non-ideal performance of critical components of the systems. The laboratory testing convinced project team members that a different design approach was needed. Advances in digital signal processing technologies allowed for a redirection in the design to use DSP chips for a digital implementation. As a result of this redirection the original goals were exceeded when a state-of-the-art prototype design was completed. Phase II accomplishments are as follows:

* All required logic for encoding and decoding was designed, implemented and tested.

* An all-digital QAM modulator was designed, implemented and tested. This modulator design includes the ability to perform signal pre-distortion to correct for system non-linearity's.

* An all-digital QAM demodulator was designed and implemented. This demodulator is a robust design which included a programmable equalizer, automatic gain

control, and automatic frequency control. These additional features were not originally planned at the beginning of phase II.

The development and fabrication of a modern system prototype exceeded original expectations. This prototype awaits an application to complete application specific tasks such as mechanical packaging, carrier frequencies, etc.

The trellis-coded 32-QAM system developed for this LDRD achieves a spectral efficiency of about 3.33 bits/sec/Hz. This spectral efficiency approximately triples that of the present systems used in Sandia's satellite and airborne applications, albeit with some loss in power efficiency due to the use of the higher-order modulation scheme. We recommend continuation of this work, examining more advanced modulation, coding, and equalization schemes, with the goal of optimizing transmission performance in the environments faced by Sandia.

Except for additive noise and a limited bandwidth, the LDRD study assumes a mostly ideal transmission environment. In practice, the transmitted signal will suffer distortion due to multipath fading and system nonlinearities. In a follow-on study of this trellis-coded QAM project we would examine techniques for mitigating against such channel impairments, including transmitter predistortion methods and receiver nonlinear equalizers. To execute this work properly, characteristics of the channels under study must be measured. Once the channel is properly modeled, methods for combating distortion can be examined. We also believe that it is worthwhile to take a closer look at the trellis-coded 32-QAM scheme to see if further spectral efficiency is achievable (through a higher-order modulation) and if additional coding gain is attainable (through refinements of the encoder and decoder). Of significance is the fact that the QAM constellation is square, a geometric shape that performs poorly through amplifier nonlinearities.

In summary, we recommend the following topics for study in a continuation of the Bandwidth Utilization Maximization project:

- channel characterization
- transmitter predistorter design
- receiver nonlinear equalizer design
- refinement of the trellis-coded QAM scheme

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1 Michael Ross
Harris Corporation ESS GCSD
2130 Forest Knoll Dr. NE #209
Palm Bay, FL 32905

3 William Ryan
Klipsch Department of Electrical and Computer Engineering
New Mexico State University
Las Cruces, NM 88003

1 Roger Bracht
Los Alamos National Laboratory
MS J580
Los Alamos, NM 87545

1 Dave Isaksen
Wideband Computers, Inc.
883 North Shoreline Blvd.
Building B, Suite 100
Mountain View, CA 94043

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