CONF-961123--7

A Multi-Channel ADC for Use in the PHENIX Detector[1]

M. S. Emery, S. S. Frank, C. L. Britton, Jr., A. L. Wintenberg, M. L. Simpson, M. N. Ericson, G. R. Young
Oak Ridge National Laboratory, P.O. Box 2008, Oak Ridge, Tennessee 37831-6006

L. G. Clonts, M. D. Allen
The University of Tennessee, Knoxville, Tennessee 37996

1996 IEEE Nuclear Science Symposium and Medical Imaging Conference
Anaheim, California
Nov. 3-9, 1996.

[1]Research sponsored by the U.S. Department of Energy and performed at Oak Ridge National Laboratory, managed by Lockheed Martin Energy Research Corporation for the U.S. Department of Energy under Contract No. DE-AC05-96OR22464.

DISCLAIMER

A Multi-Channel ADC for Use in the PHENIX Detector[1]

M. S. Emery, S. S. Frank, C. L. Britton, Jr., A. L. Wintenberg, M. L. Simpson, M. N. Ericson, G. R. Young
Oak Ridge National Laboratory, P.O. Box 2008, Oak Ridge, Tennessee 37831-6006

L. G. Clonts, M. D. Allen
The University of Tennessee, Knoxville, Tennessee 37996

Abstract

A custom CMOS analog to digital converter was designed and a prototype 8-channel ADC ASIC was fabricated in a 1.2 μm process. The circuit uses a Wilkinson-type architecture which is suitable for use in multi-channel applications such as the PHENIX detector. The ADC design features include a differential positive-ECL input for the high speed clock and selectable control for 11 or 12-bit conversions making it suitable for use in multiple PHENIX subsystems. Circuit topologies and ASIC layout specifics, including power consumption, maximum clock speed, INL, and DNL are discussed. The ADC performed to 11-bit accuracy.

I. Introduction

The PHENIX detector at the Relativistic Heavy Ion Collider (RHIC) [1] is composed of many detector subsystems each consisting of several thousand individual data channels. The high channel count presented by this detector requires highly integrated front end and signal processing. In order to efficiently handle all this data an analog to digital converter (ADC) is needed that is easily expandable to many channels with a high level of circuit integration. The Wilkinson-type ADC architecture has been shown to be very suitable for multi-channel VLSI applications [2]. An architecturally similar 10-bit ADC was used in the WA98 experiment at CERN [3]. This newly presented design attempts to extend the 10-bit performance of the WA98 version to 12 bits while limiting the conversion time to 10 - 15 μs. The intended application for this ADC is in several front-end subsystems of the PHENIX detector.

II. Description

Figure 1 shows a block diagram of the ADC. The design consists of a 12-bit Gray Code counter and a ramp generator circuit that start simultaneously when a conversion begins. The comparators then latch the current Gray code count into a data latch when the ramp voltage and input voltage are equal. At the end of the 12-bit count the Full Scale Count (FSC) flag is set to indicate a complete conversion. The data is then loaded through a memory register and off the chip through a Gray-to-binary decoder. The ADC design attempts to expand the precision to 12 bits, and offers some additional features such as a differential positive-ECL input for the high speed clock, a data buffer register to allow for simultaneous conversion during data readout, and selectable modes offering 11 or 12 bit conversions.

A. PECL-CMOS

High speed clock signals driving the full 5-V logic levels can cause many noise problems both on the circuit board and on the chip by coupling into sensitive analog circuits. Crosstalk problems can be minimized by using a lower amplitude differential signal. Figure 2 shows the schematic for a circuit that accepts a differential emitter-coupled-logic (ECL) clock signal running between 3.2V and 4.2V. The output from the circuit is standard CMOS level, and operates at frequencies over 230 MHz.

B. Gray Counter

A Gray code counter is used to produce the digital code that is latched to produce the conversion result for each ADC channel. This module (shown in Figure 3) is composed of three primary blocks: a clock/reset generator, a configurable 12-bit synchronous counter, and a 12-bit toggle flip-flop cell.

The clock/reset generator receives the clock and start signals and produces reset and clocking logic for the remaining portions of the ADC. Synchronization of the start signal with the ADC is accomplished using two D flip-flops (DFFs) allowing asynchronous assertion of the ADC start from the acquisition controller. When low, the start signal maintains the ramp generator and entire Gray code generator in a reset state. When the start is asserted, the delayed synchronized output initiates a conversion by releasing the resets and enabling the clock to the Gray code generator.

The synchronous counter is designed to operate as a double-edge clocked counter thus reducing the clock frequency from 409.6 MHz to 204.8 MHz for a 12-bit conversion to be completed in 10 us. One disadvantage of this topology is the sensitivity to clock duty cycle associated with double-edged counting schemes potentially resulting in increased DNL related errors.

The synchronous counter is divided into three nibble counter modules, each having some unique characteristics. The low order nibble COUNT[3:0] implements the double-edge clocking scheme in the least significant bit (LSB). All

[1]Research sponsored by the U.S. Department of Energy and performed at Oak Ridge National Laboratory, managed by Lockheed Martin Energy Research Corporation for the U.S. Department of Energy under Contract No. DE-AC05-96OR22464.

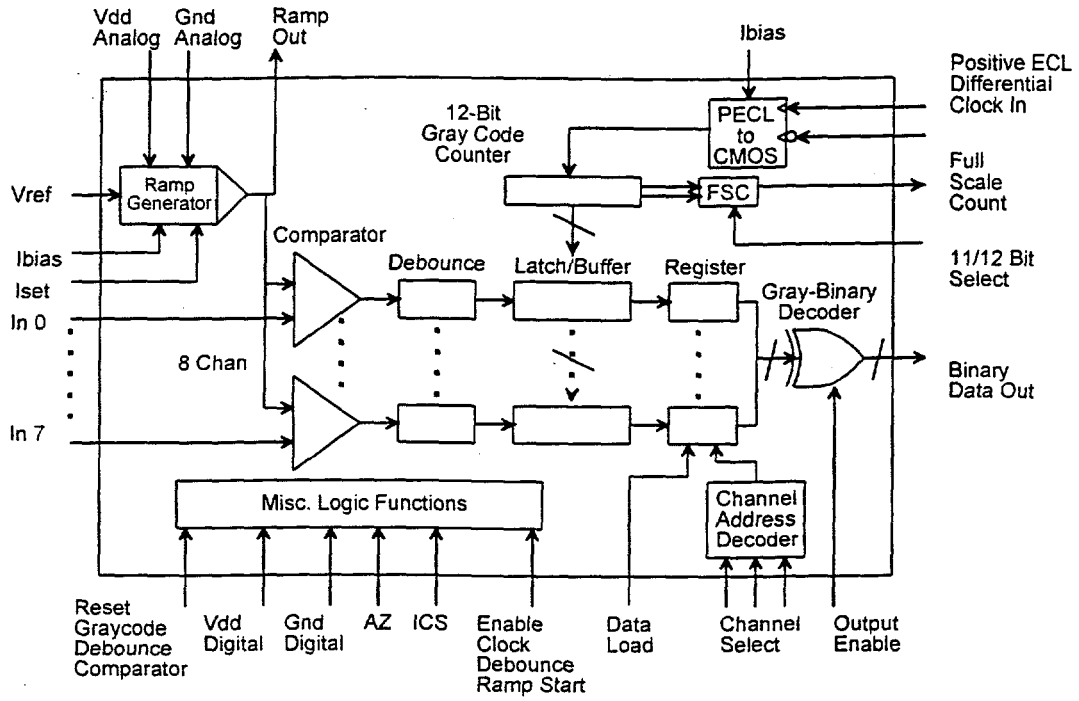

Figure 1: Block diagram of ADC

other bits of the synchronous counter are single edge triggered. A look-ahead carry (LAC) scheme is implemented that reduces the normal rippling associated with synchronous counters. This cell produces a global LAC when COUNT[3:0] is 1110h, one count before the normal roll-over of a 4-bit counter. The middle counter nibble receives a carry-in from the LSB nibble (which is always high), and the global LAC. Use of the global LAC eliminates the delay associated with a 4-input gate required to produce a carry at 1111h. The carry-out from the middle nibble counter is produced by ANDing COUNT[N] to COUNT[N-4] together with the standard carry input. Using this technique allows 16 clock cycles for a carry to be generated before the next global LAC occurs. The most significant nibble of the synchronous counter is a variation of the middle nibble. Modifications have been made to stop the counter at FFFh (12-bit mode) or 7FF (11-bit mode) when a full scale count (FSC) occurs. All generated carry signals are properly buffered and latched to assure proper synchronous operation.

A set of data registers is provided to allow a conversion to be in process at the same time that data from a previous conversion is being read out. When a particular channel is addressed its data passes through a Gray-to-binary decoder. Decoding the data on-chip makes processing easier.

C. *Ramp Generator*

The ramp generator circuit shown in Figure 4 was designed with a low impedance output drive and power supply rejection better than 50dB. The ramp slope is set by an external bias current source. This current is buffered by an op amp and a source follower PMOS transistor to form a very high output impedance current source. This configuration rejects power supply noise that is within the limit of the op amp bandwidth.

The current then drives an op amp integrator. An input voltage (Vref) is used for setting the starting level of the ramp. While the ramp is in reset mode, the capacitor in the integrator is bypassed by a CMOS switch and the output of the ramp generator circuit is at the voltage Vref. The CMOS switch is then opened and the ramp linearly decreases from Vref to the lowest output level of the op amp (about 75mV). The ramp is then reset by discharging the capacitor through the CMOS switch and returning the output of the ramp generator to Vref. This configuration isolates the ramp generating capacitor from the power supply thus reducing power supply noise on the ramp. Also, the output of the ramp generator is an op amp which reduces the effects of loading on the ramp signal, and

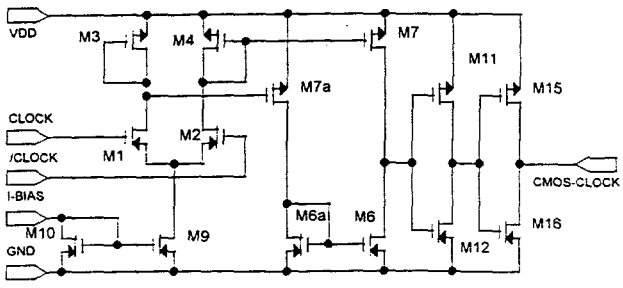

Figure 2: Positive ECL to CMOS logic level converter

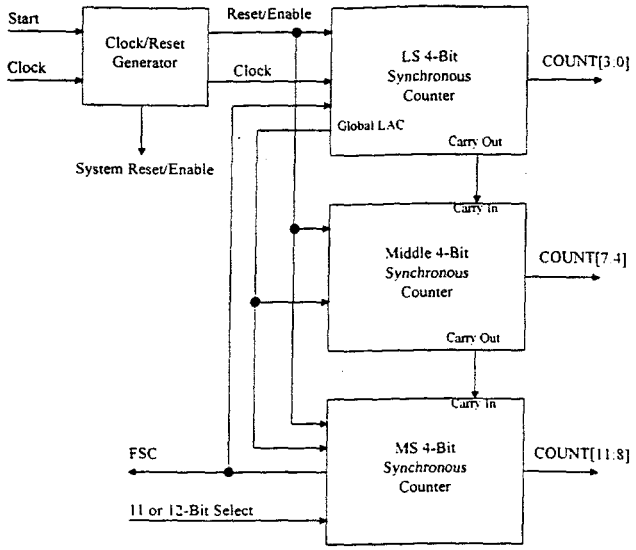

Figure 3: Gray counter block diagram.

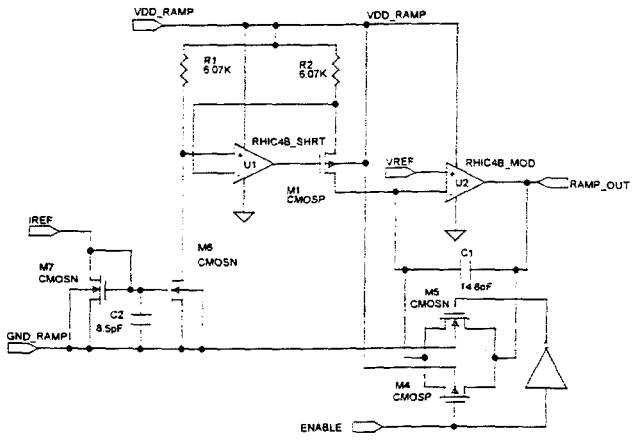

Figure 4: Ramp generator circuit.

the inverting input forms a virtual ground so that the voltage across the current source remains constant throughout the ramp cycle.

D. Comparator

A dynamic autozeroing comparator topology is used here, essentially unchanged from the WA98 circuit [3] where the reference discusses the comparator in more depth. Autozeroing provides an effective method to remove offset errors just before a conversion. The input node is switched to the analog voltage signal to store the appropriate charge on the input capacitor, then switched to the ramp signal when a conversion begins. The comparators are arrayed with a pitch of 85 microns, which is needed for meeting system requirements [4].

III. Results

An 8-channel ADC ASIC was fabricated in the Orbit Semiconductor 1.2 μm n-well process. The chip is shown in Figure 5. The fabricated ADCs were tested on a multi-layer circuit board having ground and power planes that isolate the digital and analog sections. A coaxial connector was provided to supply the clock to an MC10H116 emitter-coupled logic (ECL) chip which generates the clock and clock-bar for the ADC chip.

Precautions were taken in the chip layout to minimize noise and crosstalk as much as possible. Several bypass and decoupling capacitors are included on the layout to filter sensitive nodes. N-well layers are placed under long signal traces to provide shielding. High speed digital sections are placed as far away as possible from analog sections. Separate power and ground lines are provided to further isolate the ramp and comparators from the digital circuitry. The bottom plate of the integrating capacitor in the ramp circuit is connected to the op amp output so substrate-to-bottom plate crosstalk will be smaller due to the low output impedance of the op amp.

A. Operating Frequency

The ADC was tested using both quartz crystal clocks and a LeCroy 9210 Pulse Generator. Although the 9210 had very stable variable frequency, availability was limited. It was used to determine maximum frequency range and to observe the effects of the variation in the duty cycle of the clock. The quartz crystal clocks provided the bulk of the testing at intermediate discrete frequencies, with the majority of the testing done at 80 MHz. The maximum clock frequency was 210 MHz. This is an equivalent counting rate of 420 MHz for the Gray code counter. The intended operating frequency is about 144 MHz which is a binary multiple of the RHIC beam clock (about 9 MHz).

B. Power Consumption

The power consumption for this 8-channel ADC may be broken down as follows: Clock OFF (quiescent) 6.5mW analog + 5.15 mW digital (PECL-CMOS) = 11.65mW. At 100 MHz, the digital circuits increased from 5.15mW to 8.05mW, which gives the following calculation:

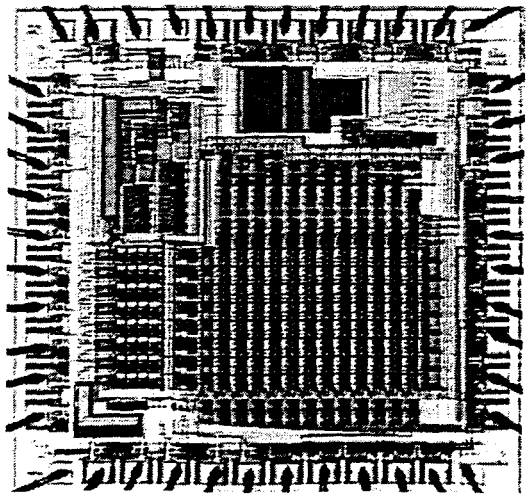

Figure 5: Fabricated ADC chip.

$$\frac{(8.05-5.15)mW}{100\,MHz \bullet 8 channels} = 3.625 \frac{\mu W}{MHz \bullet channel} \quad (1)$$

So for a 32 channel ADC operating at 144 MHz the total power dissipation would be 28.4mW (including the 6.5mW analog and 5.15 mW digital overhead).

C. INL

Precisely known voltages were applied to the input. The results of several ADC conversions were then averaged. A least-squares curve fit would be done on the input voltage versus averaged ADC value. Figure 6 shows the observed Integral Nonlinearity (INL) obtained by looking at the percentage difference of the ADC value from the best-fit line. The INL was less than 0.03% with an 80 MHz clock.

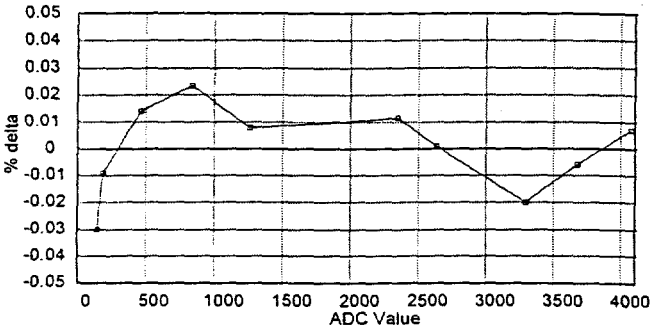

Figure 6: INL measured at 80 MHz.

Another important parameter available from averaged INL statistics is the grouping of multiple conversions at a single voltage, measured here as Full Width Half Maximum (FWHM). An interesting trend can be observed with this ADC in that the FWHM starts out at 6 channels at an ADC average value of 143 and then gradually improves to about 2 channels wide at an ADC average value of 4000. This means that for a single conversion the ADC will not deliver a full 12 bits of accuracy.

D. DNL

The Differential Nonlinearity (DNL) was measured by supplying a very slow triangle waveform to the ADC input with a peak to peak amplitude that just exceeds the conversion range of ADC and allowing conversions to be made at a regular period for a sufficiently long time to collect enough data to be statistically significant. The data consists of a histogram of the number of times each ADC code was hit. DNL is found from the percent difference of the number of times each code was hit and the average value over the entire range of interest. Figure 7 shows the DNL measured with a clock frequency of 80 MHz as 116% of LSB.

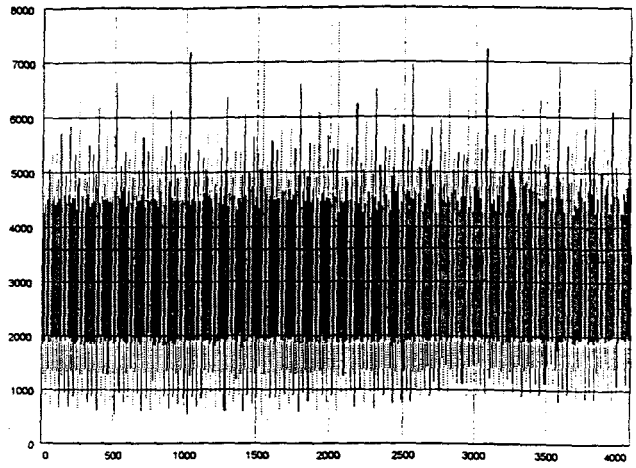

Figure 7: DNL measured at 80 MHz.

IV. Conclusion

A low-power, highly integrated, 8-channel ADC was developed and fabricated in a 1.2 μm CMOS, n-well process. The circuit occupies 4.84 mm^2 and runs at clock speeds exceeding 200 MHz. Measurement results verified proper 11-bit performance with conversion times of 15 μs or less. The ADC cell will be integrated into a 32-channel AMU/ADC ASIC for use in multiple PHENIX subsystems. Future efforts will be directed towards extending the ADC resolution to 12 bits.

V. Acknowledgments

The authors wish to express their appreciation to Jim Walker and John Writt for much assistance in program writing and debugging and data collection.

VI. References

[1] W. L. Kehoe, et al, PHENIX Conceptual Design Report. New York: Brookhaven National Laboratory, 1993.

[2] O. B. Milgrome, et al, "A 12 Bit Analog to Digital Converter for VLSI Applications in Nuclear Science," *IEEE Transactions on Nuclear Science*, Vol. 39, No. 4, pp. 771-5, 1992.

[3] A. L. Wintenberg, et al, "Monolithic Circuits for the WA98 Lead Glass Calorimeter," *1994 IEEE Nuclear Science Symposium Conference Record*, Norfolk, Virginia, Nov. 1994, pp. 493-7.

[4] C. L. Britton, et al, "Design and Performance of Beam Test Electronics for the PHENIX Multiplicity Vertex Detector," presented at the *1996 IEEE Nuclear Science Symposium*.

DIVISION DOCUMENT PEER REVIEW SHEET
(For TM and ORNL reports, CF memos, journal articles, meeting papers, NRC Technical Letter Reports, etc.)

NOTE: ORNL policy requires that documents for publication or presentation, including informal reports such as CF memos, be reviewed by two or more persons familiar with the subject matter. Reviewers may be selected by the author with the concurrence of the author's immediate supervisor, or the supervisor may select the reviewers.

Author(s) _____

Title _____

Proposed Publication or Use _____

To: _____ Date: _____
(Reviewer's Name)

It is requested that you review this document. If you cannot review it by _____, please return it to the author immediately. (Insert deadline)

	Acceptable Yes	Acceptable No		Yes	No
Technical accuracy	✓		I have reviewed my comments with the author	✓	
Effectiveness of organization	✓		I recommend publication of this document		
Adequacy of references, illustrations, tables, etc.	✓		(a) in present form	✓	
Readability	✓		(b) with changes suggested below		
Completeness of information	✓		I recommend editorial review		

I have the following comments or suggestions (use other side for additional comments):

Signed _____ 11/6/86
Reviewer Date

✓ I concur with the reviewer's suggestions and, insofar as practicable, they have been incorporated in this document.

___ I have not incorporated the reviewer's suggestions for the following reasons:

Signed _____ 11/7/86
Author Date

Approved for final processing: _____
Group Leader Date

DIVISION DOCUMENT PEER REVIEW SHEET
(For TM and ORNL reports, CF memos, journal articles, meeting papers, NRC Technical Letter Reports, etc.)

NOTE: ORNL policy requires that documents for publication or presentation, including informal reports such as CF memos, be reviewed by two or more persons familiar with the subject matter. Reviewers may be selected by the author with the concurrence of the author's immediate supervisor, or the supervisor may select the reviewers.

Author(s) M.S. Emery, S.S. Frank, C.L. Britton, A.L. Wintenberg, M.L. Simpson, M.N. Ericson et al

Title A Multi-Channel ADC for Use in the PHENIX Detector

Proposed Publication or Use IEEE 1996 NSS

To: Mike Paulus (Reviewer's Name) Date:

It is requested that you review this document. If you cannot review it by 11/1/96 (Insert deadline), please return it to the author immediately.

	Acceptable Yes	Acceptable No
Technical accuracy	X	
Effectiveness of organization	X	
Adequacy of references, illustrations, tables, etc.	X	
Readability	X	
Completeness of information	X	

	Yes	No
I have reviewed my comments with the author	X	
I recommend publication of this document (a) in present form	X	
(b) with changes suggested below		
I recommend editorial review		X

I have the following comments or suggestions (use other side for additional comments):

- Gray Counter = Fig 3. . .
- Perhaps measured data should be briefly summarized in the Abstract.

Signed [signature] (Reviewer) 11 Nov 96 (Date)

X I concur with the reviewer's suggestions and, insofar as practicable, they have been incorporated in this document.

___ I have not incorporated the reviewer's suggestions for the following reasons:

Signed M. S. Emery (Author) 11/1/96 (Date)

Approved for final processing: (Group Leader) (Date)

DIVISION DOCUMENT PEER REVIEW SHEET
(For TM and ORNL reports, CF memos, journal articles, meeting papers, NRC Technical Letter Reports, etc.)

NOTE: ORNL policy requires that documents for publication or presentation, including informal reports such as CF memos, be reviewed by two or more persons familiar with the subject matter. Reviewers may be selected by the author with the concurrence of the author's immediate supervisor, or the supervisor may select the reviewers.

Author(s) M. S. Emery, S. S. Frank, C. L. Britton, A. L. Wintenberg, M. L. Simpson, M. N. Ericson, et al

Title A Multi-Channel ADC for use in the PHENIX Detector

Proposed Publication or Use 1996 IEEE NSS

To: M. C. Smith (Reviewer's Name) Date: 11/1/96

It is requested that you review this document. If you cannot review it by 11/1/96 (Insert deadline), please return it to the author immediately.

	Acceptable Yes	Acceptable No
Technical accuracy	✓	
Effectiveness of organization	✓	
Adequacy of references, illustrations, tables, etc.	✓	
Readability	✓	
Completeness of information	✓	

	Yes	No
I have reviewed my comments with the author	✓	
I recommend publication of this document (a) in present form	✓ MINOR SUGGESTIONS	
(b) with changes suggested below		
I recommend editorial review		

I have the following comments or suggestions (use other side for additional comments):

Couple of minor "typo's"; see paper

Signed Melissa C. Smith (Reviewer) 11/1/96 (Date)

✓ I concur with the reviewer's suggestions and, insofar as practicable, they have been incorporated in this document.

___ I have not incorporated the reviewer's suggestions for the following reasons:

Signed M. S. Emery (Author) 11/1/96 (Date)

Approved for final processing: _____ (Group Leader) _____ (Date)