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TRANSISTORIZED LINEAR PULSE AMPLIFIERS

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ABSTRACT

The basic investigation of transistor feedback amplifiers has proven mathematically simple and of great practical value. The behavior of single-stage common-emitter amplifiers is described and provides a building block with which cascaded feedback amplifiers can be analyzed and designed. From the results of this analysis the conditions for minimum drift for cascaded single-stages and cascaded loops have been derived.

A transistorized linear amplifier, pulse-height discriminator, scaler, and high-voltage power supply packaged together as a single piece of portable counting gear is under development. The high-gain linear amplifier is the heart of the system and must have good reliability, wide bandwidth, small temperature-drift effects, etc. The amplifier developed has a rise time of 0.5 μ sec and current gain of 7,000, and is designed to drive a current-pulse discriminator so that only a few volts swing at the output are needed.

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I. INTRODUCTION

It is not necessary to discuss the importance of precision high-gain pulse amplifiers. They are perhaps the backbone of nuclear instrumentation. Despite this, little has been written about design for optimum performance, and it is probably due to the nature of the problem. They are used for many different purposes and a specification important to one application may not be important to another. Rise time, gain, overshoot, noise, drift, linearity, and overload are the main problems involved. Clearly not all of these may be optimized in a single design, therefore one must understand the effect of each factor upon the others in order to find an optimum design for a given set of specifications.

The scope of this study is as follows:

1. Description of the drift of the ac gain for local and loop feedback.
2. Analysis of the behavior of the single-stage common emitter amplifier with local feedback.
3. Analysis of the behavior of cascaded amplifiers with loop feedback.
4. Determining a practical method of shaping the feedback network to produce the desired pulse response.
5. Comparison of the types of amplifiers in order to predict which type will give the best performance.

Basically the question is, what benefit will be derived by using different types of simple feedback loops rather than cascaded single stages, and will such benefits be appreciable?

* Work done under the auspices of the U. S. Atomic Energy Commission.

II. DRIFT

The term "drift" here means the change of the ac gain. It is not the change of operating point, as in a dc amplifier. The designation drift is used because these effects are usually slow and rather random owing to their many causes. The greatest effect is due to temperature, but bias-point shifts are also very important. In addition, the transistors may change over long periods of time, or they may have to be replaced, thereby causing some "drift" of the ac gain.

Single Stages

Drift may be described simply for local and loop feedback and for cascaded stages. First, however, the gain equations for the single stage must be discussed. From the equivalent circuits of Fig. 1 and the amplifiers of Fig. 2, one sees that the equations are simply

Case I

$$\text{Current gain} = A_i = \frac{\beta R_S / R'_S}{S} \quad (1)$$

$$\text{Upper 3 db frequency} = \text{BW} = \frac{f_a}{D} S, \quad (2)$$

where

$$S = 1 + (\beta + 1) R'_e / R'_S, \quad (3)$$

$$D = 1 + 2\pi f_a' (R_L + R'_e) C_c, \quad (4)$$

$$R'_S = R_S + r'_b, \quad (5)$$

$$R'_e = R_e + r_e, \quad (6)$$

$$\therefore f_a' = \beta f_\beta. \quad (7)$$

The quantity f_β is therefore the frequency at which A falls 3 db for $R_L = R_e = 0$ and $R_S = \infty$.

$$\text{Gain-Bandwidth product} = \text{GBW}_i = \frac{f_a'}{D} \frac{R_S}{R'_S} \quad (8)$$

Notice that r'_b and C_c are the effects which reduce the GBW "figure of merit." Also, the GBW cannot be considered constant as the gain is changed, because R'_e affects the D factor.

Case II

$$\text{Voltage gain } A_V = \frac{\beta R_L / R'_S}{S} . \quad (9)$$

$$BW = \frac{f_p}{D} S. \quad (10)$$

The same definitions as for Case I hold.

$$GBW_V = \frac{f_p}{D} \frac{R_L}{R'_S} . \quad (11)$$

These formulas are of great practical aid and much easier to use than may be supposed at first glance.

Now for drift analysis:

A_1 = Gain before drift.

A_2 = Gain after drift.

$\Delta A = A_2 - A_1$.

$d_A = \text{Fractional drift of } A = \frac{\Delta A}{A_1}$.

The form of both current and voltage gain is $-A = \frac{\partial H}{S}$, where $H = \frac{R_S}{R'_S}$

for current gain and $H = R_L / R'_S$ for voltage gain.

Remember that these equations are good only for the conditions of Case I and Case II, and the following is limited to small signals

β_1 = β before drift.

β_2 = β after drift.

$\Delta \beta = \beta_2 - \beta_1$

$d_\beta = \text{Fractional drift of } \beta = \Delta \beta / \beta$.

From this one obtains

$$\Delta A = A_2 - A_1 = \frac{\beta_2 H}{S_2} - \frac{\beta_1 H}{S_1}.$$

$$\Delta A = \frac{H[\beta_2 S_1 - \beta_1 S_2]}{S_1 S_2} = \frac{H}{S_1 S_2} [\beta_2 - \beta_1] \left[1 + \frac{R'_e}{R'_S} \right].$$

$$\Delta A = \frac{H \Delta \beta}{S_1 S_2} \left(1 + \frac{R'_e}{R'_S} \right),$$

$$d_A = \frac{\Delta A}{A_1} = \frac{\Delta \beta}{S_2 \beta_1} \left(1 + \frac{R'_e}{R'_S} \right) = \frac{d_\beta \left(1 + \frac{R'_e}{R'_S} \right)}{S_2} \quad (12)$$

The quantity d_β is known upon measurement of β at the limits of operation. The desired d_A and a knowledge of β_2 from measurement of d_β allow a calculation of R'_e/R'_S . For example, if an amplifier is allowed to drift only 5% over a certain temperature range, then $d_A = 0.05$. Suppose d_β is measured to be 0.15 with a β_2 of 60. Then from

$$d_A/d_\beta = [1 + R'_e/R'_S]/S_2 = [1 + R'_e/R'_S]/1 + (\beta_2 + 1) \frac{R'_e}{R'_S}.$$

we have $R'_e/R'_S = 1/29$. The bias scheme must not be changed to achieve this because it determines the drift of operating point which helps determine d_β . There are several references in which one may find discussions of bias-stabilization schemes.

The factor S (local feedback factor) therefore determines the reduction of the percentage drift in a manner which is easily described.

$$d_A = \frac{d_\beta \left(1 + \frac{R'_e}{R'_S} \right)}{S_2} \quad (12)$$

¹For example, R. F. Shea, Ed., Transistor Circuit Engineering (Wiley, New York, 1957).

Loop Feedback

The familiar feedback equation may be used along with a few simple definitions to easily and thoroughly describe the effect of loop feedback upon drift:

A = gain of amplifier without loop,

K = gain of A after loop is applied,

μ = feedback factor (ratio).

$$\text{From } K = \frac{A}{1+\mu A} \quad (13)$$

and defining $I = \mu A$ = loop gain

we have

$$K = \frac{A}{1+I} \quad (14)$$

Subscripts of 1 denote quantity before drift occurs - the reference case.

Subscripts of 2 denote quantities after drift takes place.

The change of gain,

$$\Delta K = K_2 - K_1 = \frac{A_2}{1+\mu A_2} - \frac{A_1}{1+\mu A_1}$$

$$\Delta K = \frac{A_2(1+\mu A_1) - A_1(1+\mu A_2)}{(1+\mu A_1)(1+\mu A_2)} = \frac{A_2 - A_1}{(1+\mu A_1)(1+\mu A_2)}$$

since

$$d_K = \frac{\Delta K}{K_1} = \frac{\Delta A}{A_1(1+\mu A_2)} = \frac{dA}{(1+\mu A_2)}$$

are $A_2 = A_1(1+d_A)$.

$$d_K = \frac{dA}{1+I_1(1+d_A)} \quad (15)$$

where I_1 = loop gain at A_1 and K_1 .

From the graph of Fig. 3 one may quickly see the loop gain required to obtain the desired d_K when d_A has been measured.

Cascaded Drift

Assume two amplifiers of gain A and B cascaded to produce the gain G:

$$\Delta G = G_2 - G_1 = A_2 B_2 - A_1 B_1.$$

$$A_2 = A_1 (1 + d_A).$$

$$B_2 = B_1 (1 + d_B).$$

$$\Delta G = A_1 B_1 (1 + d_A) (1 + d_B) - A_1 B_1.$$

$$\frac{\Delta G}{A_1 B_1} = \frac{\Delta G}{G_1} = d_G = d_A + d_B + d_A d_B + 1 - 1,$$

$$d_G = d_A + d_B + d_A d_B.$$

(16)

The drift is therefore cumulative except for a second-order term ($d_A d_B$) which usually may be ignored. Notice that this effect does not depend upon the magnitudes of A and B -- only on their fractional changes.

Optimum Design for Singles

We now have the necessary tools for optimizing cascaded singles. Suppose gain G is required of n cascaded singles:

$$G = A^n, \quad A = G^{1/n} = \frac{RH}{S},$$

where H is an attenuation factor (R_S/R'_S or R_L/R'_S).

Then

$$S = \frac{RH}{G^{1/n}}.$$

$$d_G \approx n d_A, \quad \text{from Eq. (16)}$$

$$d_A = \frac{d_p (1 + R'_e/R'_S)}{S_2}, \quad \text{from Eq. (12).}$$

Usually $S \gg 1$ for the reduction of drift needed, therefore

$$S = 1 + (\beta + 1) \frac{R'_e}{R'_S} \approx \beta R'_e / R'_S .$$

$$S_2 = \beta_2 R'_e / R'_S = \beta_1 (1 + d_\beta) R'_e / R'_S = S_1 (1 + d_\beta) .$$

$$d_A \approx \frac{d_\beta (1 + R'_e / R'_S)}{S_1 (1 + d_\beta)} .$$

We now limit ourselves to $d_\beta \gg 1$, knowing that the entire analysis is to compare different amplifier types and that when this is done for $d_\beta \ll 1$ it will be sufficient.

$$d_A \approx \frac{d_\beta}{S_1} (1 + R'_e / R'_S) = \frac{d_\beta}{\beta_1 H} G^{1/n} (1 + R'_e / R'_S) .$$

$$d_G = n d_A = \frac{d_\beta}{\beta_1 H} (1 + R'_e / R'_S) n G^{1/n} .$$

This function has a minimum for $n = \ln G$ and $A = G^{1/n} = G^{1/\ln G} = e$. Therefore minimum drift is achieved when each stage has a gain of e .

$$dG_{\min} = \frac{d_\beta}{\beta H} e \ln G (1 + R'_e / R'_S) = \left[\frac{e \ln G d_\beta}{\beta} \right] \frac{(1 + R'_e / R'_S)}{H} . \quad (17)$$

Drift of Two-Stage Loops (Doublets)

The gain of a two-stage amplifier is of the form $A = \beta^2 H$, where H is an attenuation factor determined by the particular design. After the loop is applied one has

$$K = \frac{A}{1 + \mu A} = \frac{\beta^2 H}{1 + \beta} .$$

$$d_K = \frac{d_A}{1 + \beta (1 + d_A)} , \quad \text{from Eq. (15).}$$

$$d_A \approx 2 d_\beta , \quad \text{from Eq. (16).}$$

This is assuming that H does not reduce d_A noticeably. Of course the greatest drift reduction will be realized when it is all done in the loop and none accomplished in local feedback inside the loop. Therefore this is the only case discussed. We have

$$d_K = \frac{2d_\beta}{1 + \frac{1}{T}(1 + 2d_\beta)} \approx \frac{2d_\beta}{T}, \quad (18)$$

because $T \gg 1$ is usually the practical case, and we are limiting ourselves again to very small d_β .

When a total gain G is desired by cascading these doublets what will be the optimum number of loops (n) and what will this minimum drift be?

For n loops cascaded,

$$d_G = nd_K, \text{ from Eq. (16)}$$

$$d_K = \frac{2d_\beta}{T}, \text{ from Eq. (18)}$$

$$d_G = \frac{2d_\beta n}{T}.$$

$$K = \frac{\beta^2 H}{T} = G^{1/n}, \quad T = \frac{\beta^2 H}{G^{1/n}}.$$

$$d_G = \frac{2nd_\beta G^{1/n}}{\beta^2 H} = \left[\frac{2d_\beta}{\beta^2 H} \right] n G^{1/n}.$$

This achieves a minimum when $n = \ln G$, as for singles.

Therefore

$$K = G^{1/n} = G^{1/\ln G} = e.$$

The gain of each unit is again e .

$$d_{G_{\min}} = \frac{2d_\beta}{\beta^2 H} e^{\ln G} = \left[\frac{e \ln G d_\beta}{\beta^2 H} \right] \frac{2}{\beta H}. \quad (19)$$

Notice the comparison to the optimum drift for singles - Eq. (17). If there are two transistors per loop and G is 3,000, then $n = \ln G \approx 8$, which means sixteen transistors. It is very seldom a designer will choose to use this many units even though it is optimum design. For this reason it is good to compare the drift of the optimized singles A with that for doublets using the same number of transistors.

Now $n = \frac{\ln G}{2}$ since n is the number of loops and there are usually two transistors per loop in the doublet.

$$d_G = n d_K = \frac{2nd_\beta}{T}, \text{ from development of Eq. (19),}$$

$$K = G^{1/n} = \frac{\beta^2 H}{T}, \quad T = \frac{\beta^2 H}{G^{1/n}}$$

$$G^{1/n} = G^{2/\ln G} = e^2.$$

$$\therefore T = \frac{\beta^2 H}{e^2}.$$

$$\therefore d_G = \frac{2nd_\beta}{T} = \frac{2 \ln G d_\beta e^2}{2 \beta^2 H}$$

$$d_G = \left[\frac{e \ln G d_\beta}{\beta} \right] \frac{e}{\beta H} \quad (20)$$

Comparing Eq. (20) with Eqs. (19) and (17), we see there is still a distinct advantage in using loops (doublets so far) with negligible local feedback.

Drift of Three-Stage Loops (Triplets)

Three stages with a loop (triplets) have a gain K of the form

$$K = \frac{\beta^3 H}{1 + \mu \beta^3 H} = \frac{\beta^3 H}{1 + \lambda}$$

For the previous approximations,

$$K \approx \frac{\beta^3 H}{T} = G^{1/n},$$

$$d_G \approx n d_K = \frac{n d_A}{T} = \frac{n^3 d_B}{T}.$$

$$l = \frac{\beta^3 H}{G^{1/n}},$$

$$d_G = \left[\frac{3d_B}{\beta^3 H} \right] n G^{1/n}.$$

This function also has a minimum at which $n = \ln G$ and $K = G^{1/n} = G^{1/\ln G} = e$,

$$\therefore d_{G_{\min}} = \frac{3d_B e \ln G}{\beta^3 H} = \left[\frac{e \ln G d_B}{\beta} \right] \frac{3}{\beta^2 H} \quad . \quad (21)$$

Notice the further reduction of $d_{G_{\min}}$.

When there are the same number of transistors as for the optimized singles, n becomes $\frac{\ln G}{3}$, if there are three transistors in a triplet:

$$K = G^{1/n} = G^{3/\ln G} = e^3$$

$$n = \frac{\ln G / 3}{3}.$$

and $d_G = \left[\frac{e \ln G d_B}{\beta} \right] \frac{e^2}{\beta^2 H} \quad . \quad (22)$

It is now shown that the use of triplets offers quite an advantage over both singles and doublets.

The simple drift analysis then states that one does benefit greatly by using feedback loops instead of local feedback, and the more stages in the loop the better.

III. PULSE RESPONSE

The discussion of drift reduction assumed any desired amount of loop gain (β) could be achieved. In every case some shaping of the frequency response of the feedback network is necessary to produce the time response desired. A further comparison must therefore be made between singles, doublets, and triplets to see which is best for rise time and overshoot. The amplifier must be shown in much more detail, and the types discussed here are shown in Figs. 4 and 5. There are other possible configurations of course.

Doublets

The gains spoken of from now on are current gains and apply to Case I of Fig. 1. A denotes the gain without a loop, and K denotes the gain of the same unit after the loop is introduced; $\beta = \mu A$ is still the loop gain. From Fig. 4 we have

$$A_0 = \frac{\beta^2 R_S/R'_S \quad R_L/R'_L}{\left[1 + (\beta+1) \frac{r_e}{R'_S}\right] \left[1 + (\beta+1) \frac{r_e}{R'_L}\right]} = \text{low-frequency gain;}$$

$$A_0 \approx \beta^2 H,$$

$$\text{where } H = R_S/R'_S \quad R_L/R'_L$$

$$\text{and } (\beta+1) \frac{r_e}{R'_S} \ll 1, \quad (\beta+1) \frac{r_e}{R'_L} \ll 1.$$

The local internal feedback is therefore considered negligible.

From here on A is the gain function including frequency

$$A = A(f) = \frac{A_0 \omega_1 \omega_2}{(p+\omega_1)(p+\omega_2)}$$

where $p = j\omega$ and ω_1, ω_2 are the 3-db cutoff frequencies of each stage.

Local feedback (S) is negligible, and good design demands $D \approx 1$:

$$A \approx \frac{A_0 \omega_\beta^2}{(p + \omega_\beta)^2}$$

$$K = \frac{A}{1 + \mu A} \approx \frac{A_0 \omega_\beta^2}{(p + \omega_\beta)^2 + \mu A_0 \omega_\beta^2} \quad (23)$$

$$K = A_0 \omega_\beta^2 / p^2 + 2p\omega_\beta + \omega_\beta^2 + \mu A_0 \omega_\beta^2$$

When μ is constant with frequency one has

$$K = \frac{A_0 \omega_\beta^2}{p^2 + 2p\omega_\beta + \omega_\beta^2 (1 + \mu A_0)}$$

and

$$K_0 = \frac{A_0}{1 + \mu A_0}$$

Here K is of the form

$$K = \frac{A_0 \omega_\beta^2}{(p-a)(p-b)}$$

where the roots a and b cause the step function response to have overshoot and ringing as shown in Fig. 6.

$$a, b = \frac{2\omega_\beta \pm \omega_\beta \sqrt{4 + 4(1 + \mu A_0)}}{2}$$

$$a, b \approx -\omega_\beta [1 \pm j\sqrt{k}]$$

Complex roots always cause overshoot. The angle of the complex roots is $\phi \approx \tan^{-1} \sqrt{k}$, and the overshoot is a function only of this angle, as shown in Fig. 7.

Complex roots may be eliminated by causing μ to be a function of frequency. From the basic definitions and approximations for feedback ratio, we have $\mu = i_f/i_L$ (Fig. 4). This assumes that the input impedance of the first transistor does not affect the feedback ratio. That is a problem many times and must be overcome by inserting an impedance-matching stage in the loop (See Fig. 4):

$$\mu = \frac{i_f}{I_f} \cdot \frac{i_f}{I_e} \cdot \frac{i_e}{I_L} = e \cdot \frac{R_e}{Z_f} \cdot \frac{1}{\alpha} = \frac{R_e}{Z_f};$$

Z_f then must be shaped to eliminate the complex roots for any given μ .

The elimination of complex roots requires that Z_f become a parallel RC combination where

$$R = \frac{R_e}{\mu} \quad (24)$$

and

$$C = \frac{2}{\omega_B \sqrt{I}} R \quad (25)$$

The K equation for this shaping becomes

$$K \approx \frac{A_0 \omega_B^2}{(p + \omega_B \sqrt{I})^2}, \quad A_0 = \beta^2 H.$$

This looks like two identical cascaded singles with gains of $\beta \frac{\sqrt{H}}{\sqrt{I}}$ and bandwidths of $\omega_B \sqrt{I}$.

For $n = \frac{\ln G}{2}$ there is the same number of transistors as for the singles (neglecting buffers):

$$K = G^{1/n} = \frac{\beta^2 H}{I}, \quad \sqrt{I} = \frac{\beta}{G^{1/2n}} \sqrt{H},$$

$$G^{1/2n} = G^{1/\ln G} = e,$$

$$\sqrt{I} = \frac{\beta}{e} \sqrt{H}.$$

The amplifier looks as though there are $\ln G$ single stages in cascade -- each with a bandwidth of

$$f_B \frac{\beta \sqrt{H}}{e} = \frac{f'_a}{e} \sqrt{H}$$

$$BW_{Total} = \frac{f'_a}{e} \sqrt{H} \sqrt{2^{1/\ln G-1}} \quad (26)$$

Triplets

For three stages one has

$$A \approx \frac{\beta^3 H \omega_B^3}{(p+\omega_B)^3} = \frac{A_0 \omega_B^3}{(p+\omega_B)^3}$$

Neglecting local feedback we have also

$$K = \frac{A}{1+\mu A} = \frac{A_0 \omega_B^3}{(p+\omega_B)^3 + \mu A_0 \omega_B^3} \rightarrow \frac{A_0 \omega_B^3}{(p-a)(p-b)(p-c)} \quad (27)$$

When μ is not frequency-sensitive, complex roots appear for $\mu > 0$. In order to eliminate them techniques may be employed which bring about results similar to the doublet analysis. In Fig. 5 Z_L is a series L-R and Z_L is a parallel R-C. It is not possible to completely eliminate the imaginary parts of the roots unless an S factor is introduced in one of the internal stages. This naturally reduces the f achievable, and the drift of G becomes more on the order of that expected for doublets.

There is seldom much reason for using triplets, because in order to get rid of the overshoot the drift is increased and the problem of trimming the feedback network is much more complicated than for doublets.

Singles

For minimum drift,

$$n = \ln G, \quad A = G^{1/n} = e,$$

$$BW = [f_B S] \sqrt{2^{1/n}-1},$$

$$A = \frac{\beta H}{S}, \quad S = \frac{\beta H}{A} = \frac{\beta H}{e},$$

$$BW = \frac{f_B \beta H}{e} \sqrt{2^{1/n}-1} = \frac{f'_a H}{e} \sqrt{2^{1/\ln G-1}} \quad (28)$$

The rise time for the singles is the same as for doublets. It is possible to peak the singles response with coils, and also possible to peak the doublets response by adjustment of the feedback capacitor.

IV. DESIGN PROBLEMS

Buffers

It is sometimes necessary to put in an impedance-matching stage (buffer) in the loop or in the output. Figures 4 and 5 show the use of such buffers. For the doublets the feedback resistor usually is made low enough so it is of the same order of magnitude as the input impedance of the first transistor. As the input impedance drifts, the feedback ratio is affected and the gain drifts much more than predicted from Eq. (19). The grounded-base stage is chosen because its input impedance is very small and its current gain is close to unity and very stable.

For triplets the load usually may not be taken off the third collector because it would upset the feedback ratio. It is seldom the load is a pure resistance.

Linearity

For small-signal stages, the linearity is not a very big problem. The output stages, however, may have large voltage or current swings and the gain may change as the pulse height is changed. This is of course due to β 's being dependent upon voltage and current. The voltage effect can be reduced greatly by inserting a grounded-base buffer stage between output and load, but the current effect is still important in most cases. The answer lies in knowing over what operating region β varies least as current is changed. From a curve of collector current as a function of base current for different values of collector voltage, the most linear region can be easily found. Linearity and drift may be analyzed in the same manner, and feedback has the same effect upon both.

Overload Effects

When pulses are present which drive the transistors beyond cutoff or saturation, care must be exercised so that dead time between pulses does not result. Dead time results when coupling capacitors charge through a small impedance and discharge through a large impedance. It is possible to cascade PNP and NPN units alternately so that each is being driven on by the pulse, but if there is undershoot at the end of the pulse it may cause dead time owing

to some of the units' being cut off. It may seem better to design such an arrangement that each unit will be driven toward cutoff normally and undershoot at the end of a pulse will not cause any dead time. This, however, could require more stand-by current than can be tolerated.

Dead time may usually be eliminated by careful biasing. The output stage should be made to be driven further into conduction by the pulse, but it must be biased into conduction enough to absorb the undershoot without causing dead time. Of course, stages that are normally driven toward cutoff need only be biased on enough for the normal pulse to be passed.

V. CONCLUSIONS

The design for high-gain linear pulse amplifiers is obviously complicated, and to optimize its performance is almost hopeless because of conflicting requirements.

Let us piece together some sort of consistent guiding statements by which the problem may be approached.

1. Drift of the ac Gain. There is a great advantage in using doublets rather than singles. The triplets have a much better drift performance than doublets, but most of this is lost when the pulse overshoot has to be eliminated. The optimum design for doublets has three times as many units as the optimum design for singles because a buffer must be used in the loop. There is still a large advantage when half as many loops are used. There must be no local feedback (S factors) within the loops, and the use of buffers is essential if the drift is to be minimized.

2. Biasing. Bias stability is of primary concern because β is very sensitive to operating point as well as to temperature. The bias point must be carefully selected so that the most linear (distortionless) operation may be obtained. Since the S factor of each stage depends upon r_e , $r_e \propto \frac{1}{I_e}$, the emitter bias current I_e must be high enough to insure that local feedback is negligible. Bias will also determine the response under overload conditions. A stage must not be allowed to be cut off while the coupling capacitor is recovering from the pulse.

3. Pulse Response. Singles, doublets, or triplets may be designed so that the ringing of the pulse response is eliminated for any specified gain. For singles this ringing cannot occur unless there are peaking coils, of course; for doublets it is a small problem; for triplets an S factor must be used in

one of the latter two stages, and this results in a loss of the triplets' drift-response advantage. The rise times are about the same for each type for a given over-all gain G . The rise times are equal when the number of transistors (not counting buffers) is kept the same for each type in accomplishing the over-all gain G .

From these three considerations it becomes apparent that the best practical amplifier should usually be composed of doublets. The number of stages depends upon the gain needed, the drift that may be tolerated, and sometimes the number of transistors that can be tolerated. The rise time will be determined entirely by the frequency response of the transistors used if the D factor mentioned in Section II is kept very close to unity for each stage. It would not be good to cascade identical loops because the bias plays such an important role in the operation of each loop, and each loop plays a somewhat different part in the operation of the over-all amplifier.

VI. RESULTS (EXPERIMENTAL)

The descriptions of single-stage and loop drift behavior in Section II are in good agreement with experiment. Since the whole mathematical development is built upon Eqs. (1), (9), and (13) and a knowledge of d_B , the drift formulas should be accurate. That is, once Eqs. (1), (9), and (13) are substantiated all the rest is simple, rigid algebra and differential calculus. These equations have also been substantiated easily by simple experiment.

During the course of this study an amplifier has been built with the following characteristics. It consists of three doublets and one single-stage inverter.

Current Gain - 7,000.

Rise time - 0.5 μ sec

Overshoot - Negligible on a 'scope. This may be adjusted, resulting in about 0.3 μ sec rise times for 20% overshoots.

Input Impedance - Series resistor of 1K.

Input Pulse - Negative

Output - Up to 8 or 10 ma positive. Voltage swings less than 2 v.

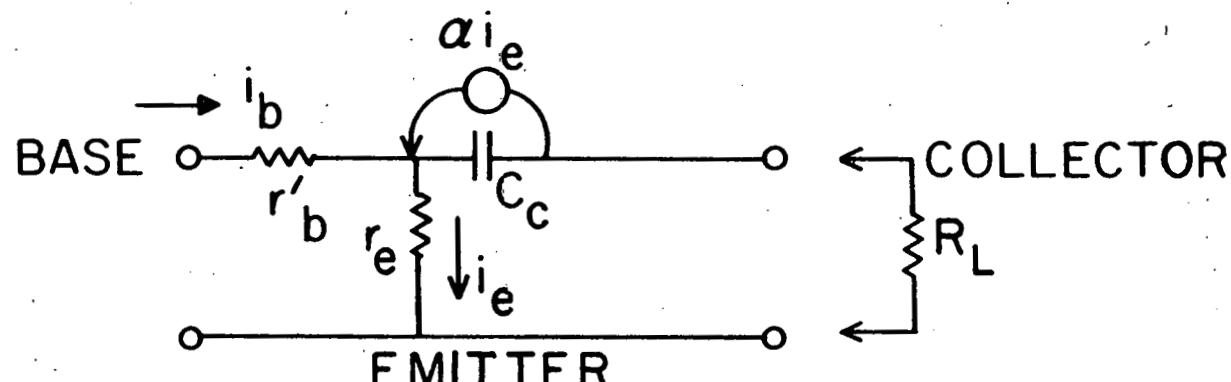
Drift of Gain - 4.5% per 10°C rise.

These doublets did not have buffers and it is expected the drift would go down by about an order of magnitude if they were used. The output works into a forward-biased diode subtractor, therefore only very small voltages are required to drive this circuit.

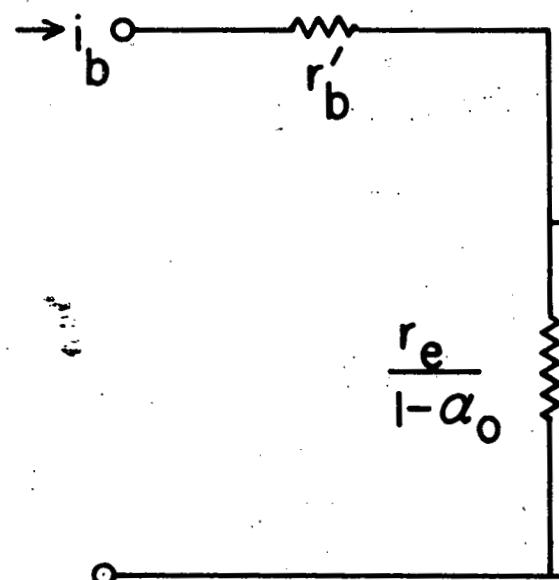
This amplifier is not an optimum design for drift response, but it gives a good idea of the results that may be achieved.

FIGURE CAPTIONS

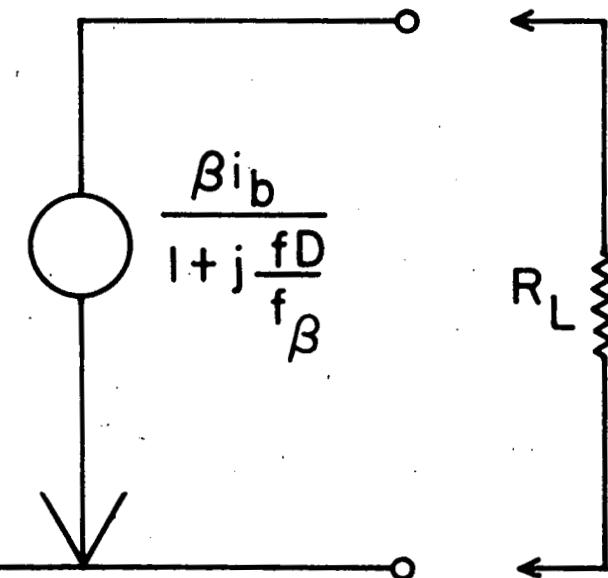
- Fig. 1. Familiar "T" circuit and the very useful "w" circuit.
- Fig. 2. Basic common-emitter amplifier circuits.
- Fig. 3. Effect of loop gain (β) upon the drift (d_A) of an amplifier.
- Fig. 4. The doublet.
- Fig. 5. The triplet.
- Fig. 6. Step-function response with complex roots.
- Fig. 7. Percent overshoot as a function of the angle of the complex root.



"T"-EQUIVALENT



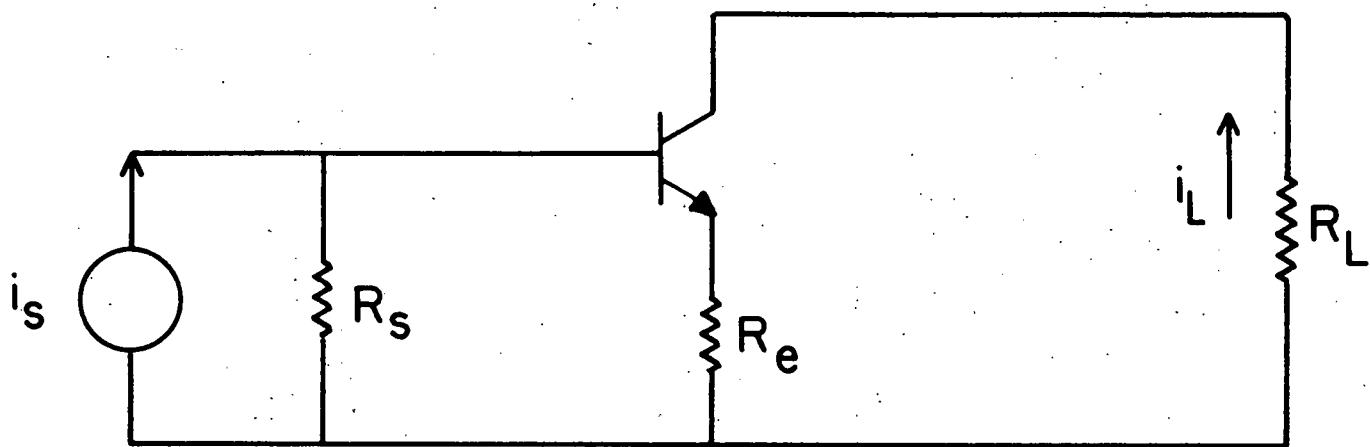
$$C = \frac{D}{r_e \omega'_a}$$



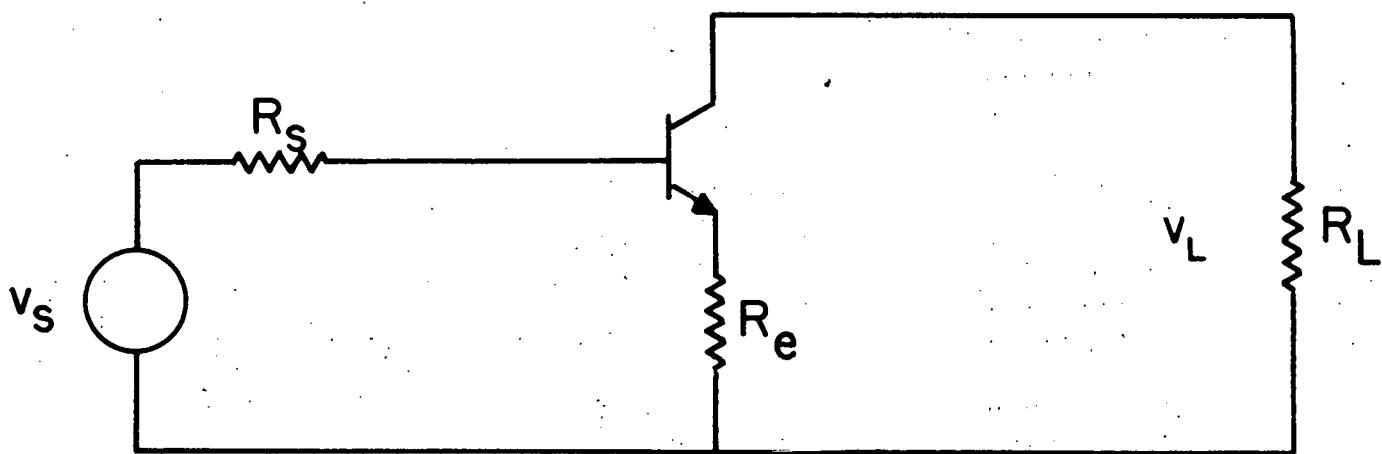
"π"-EQUIVALENT

F-1

51,320-1



CASE ONE

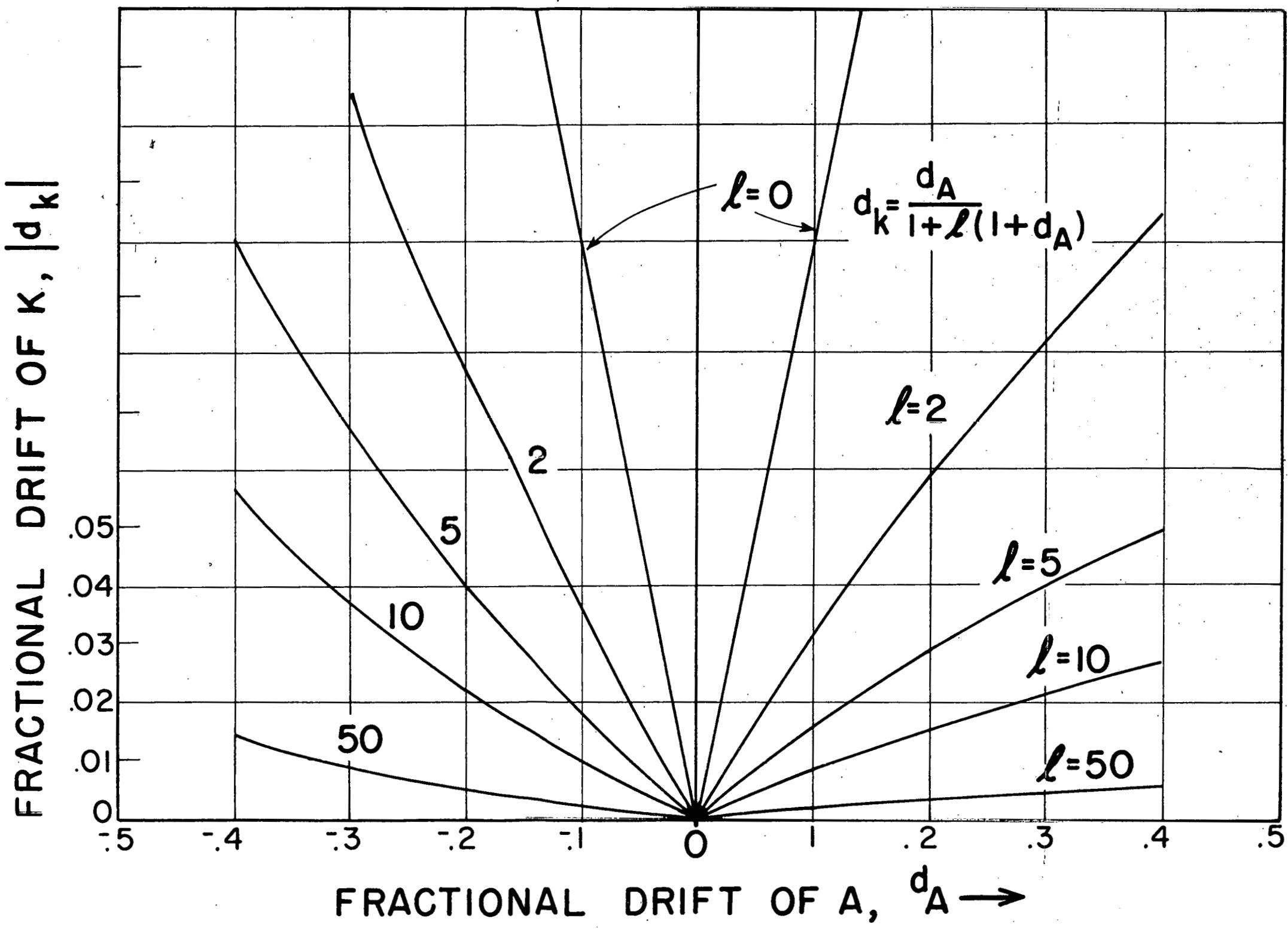


CASE TWO

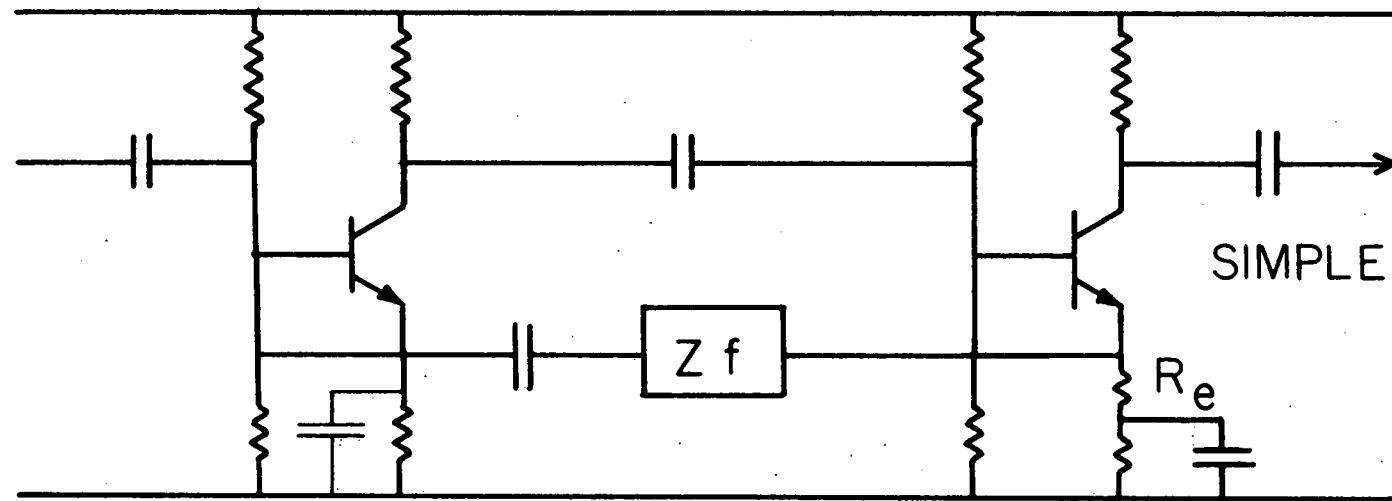
243 023

1-2 17

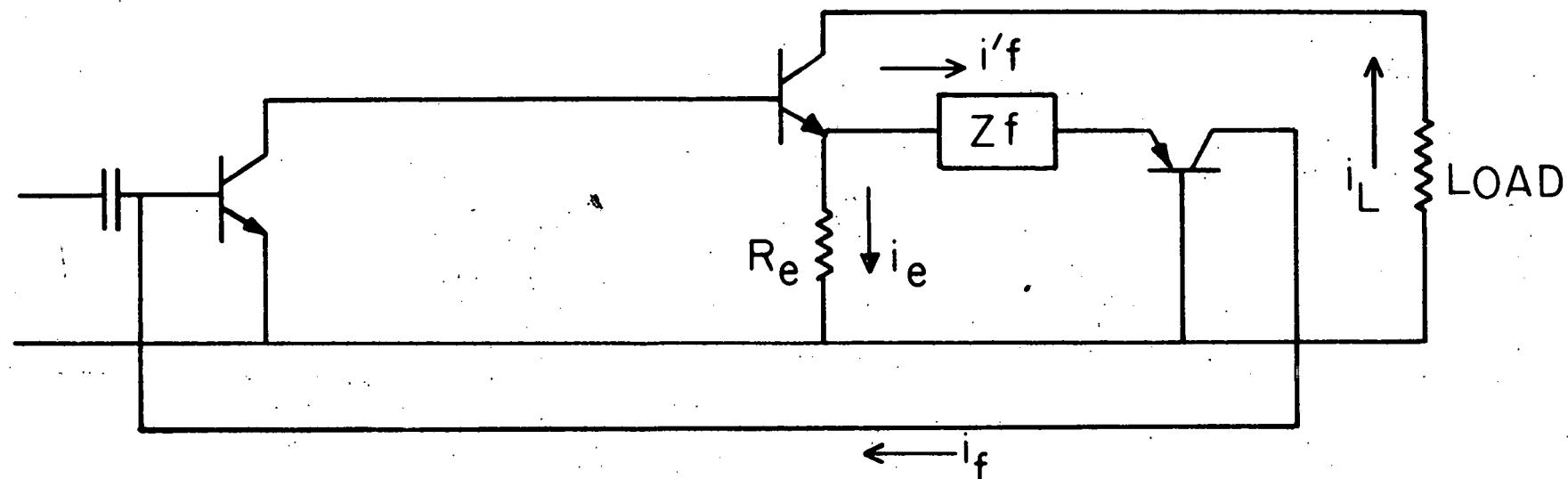
51321-1



F-3



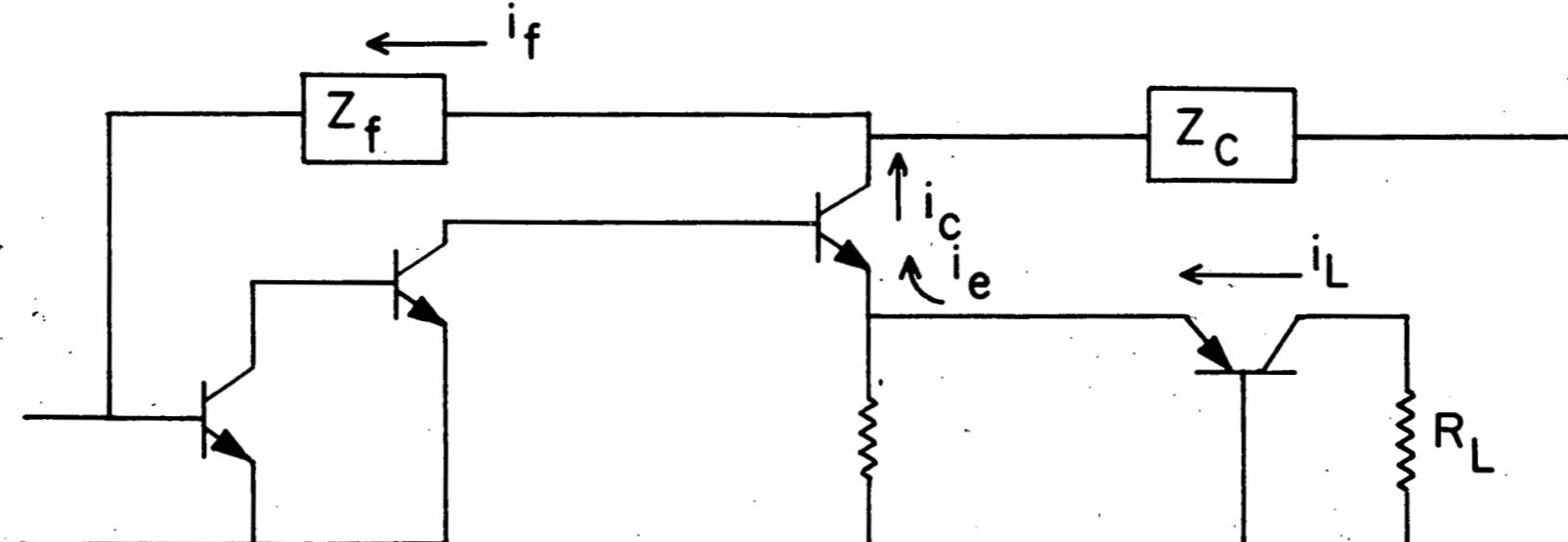
SIMPLE DOUBLET



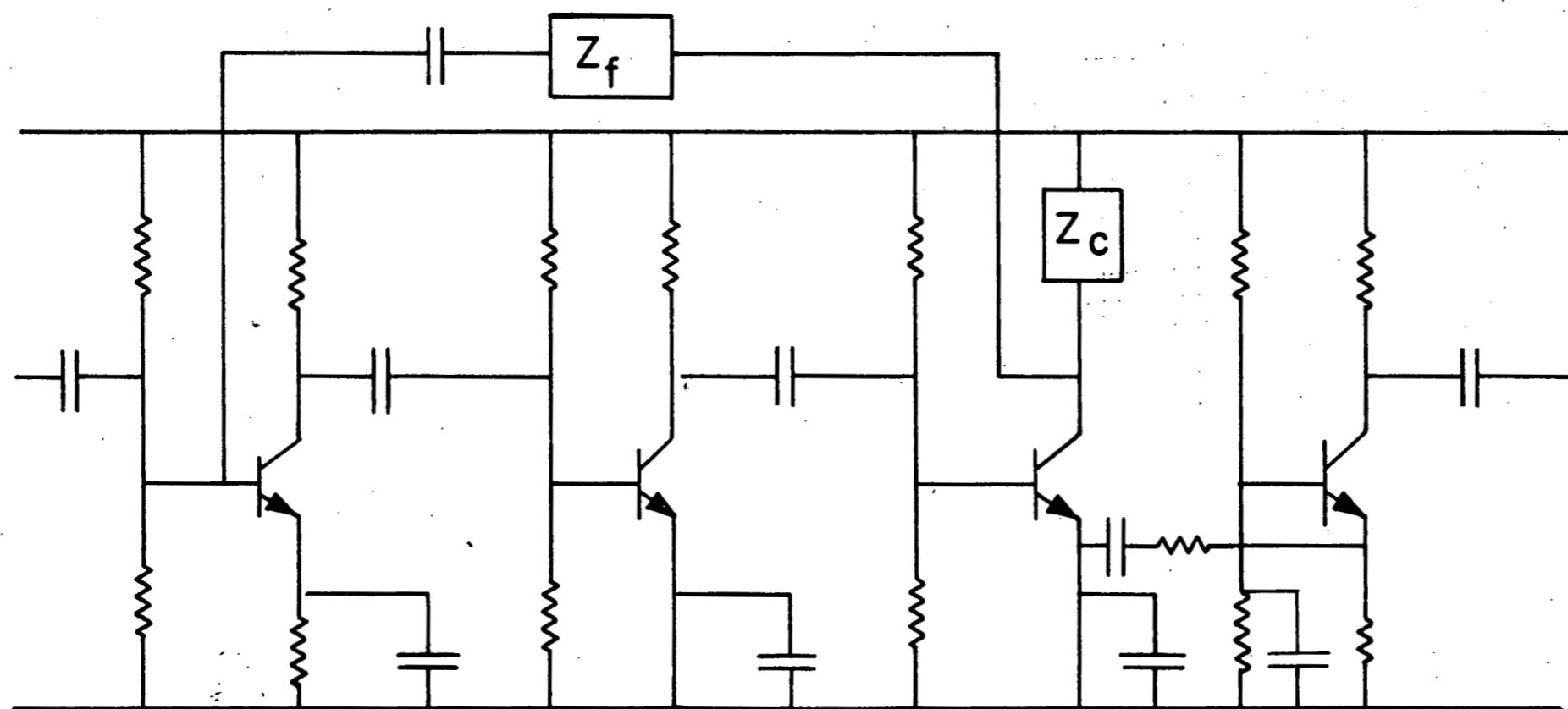
DOUBLET WITH FEEDBACK BUFFER

51.319-1

TRIPLET WITH LOAD BUFFER



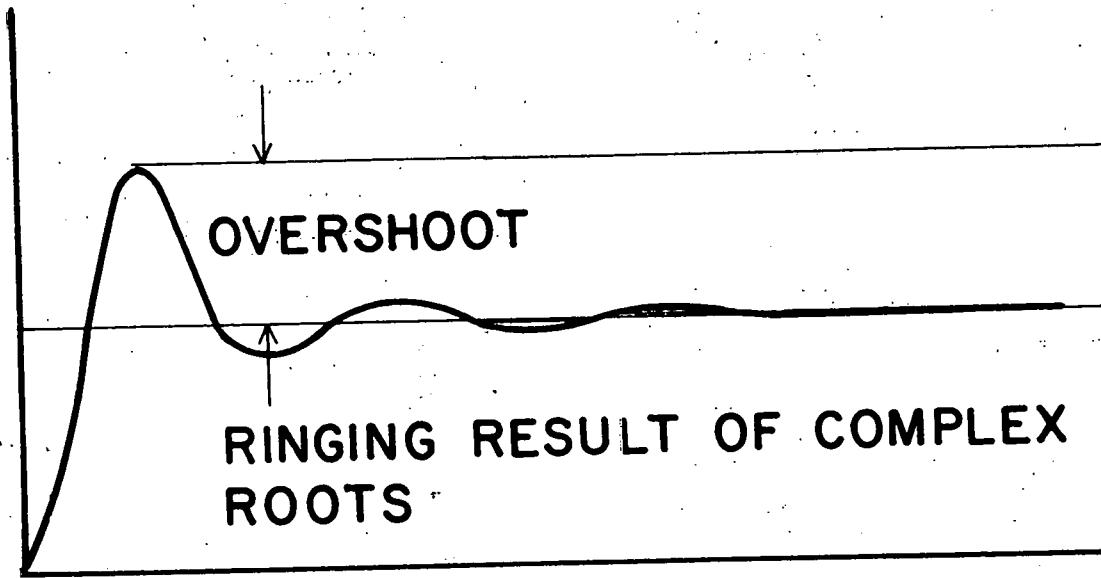
TRIPLET BIAS CIRCUIT AND BUFFER



243 026

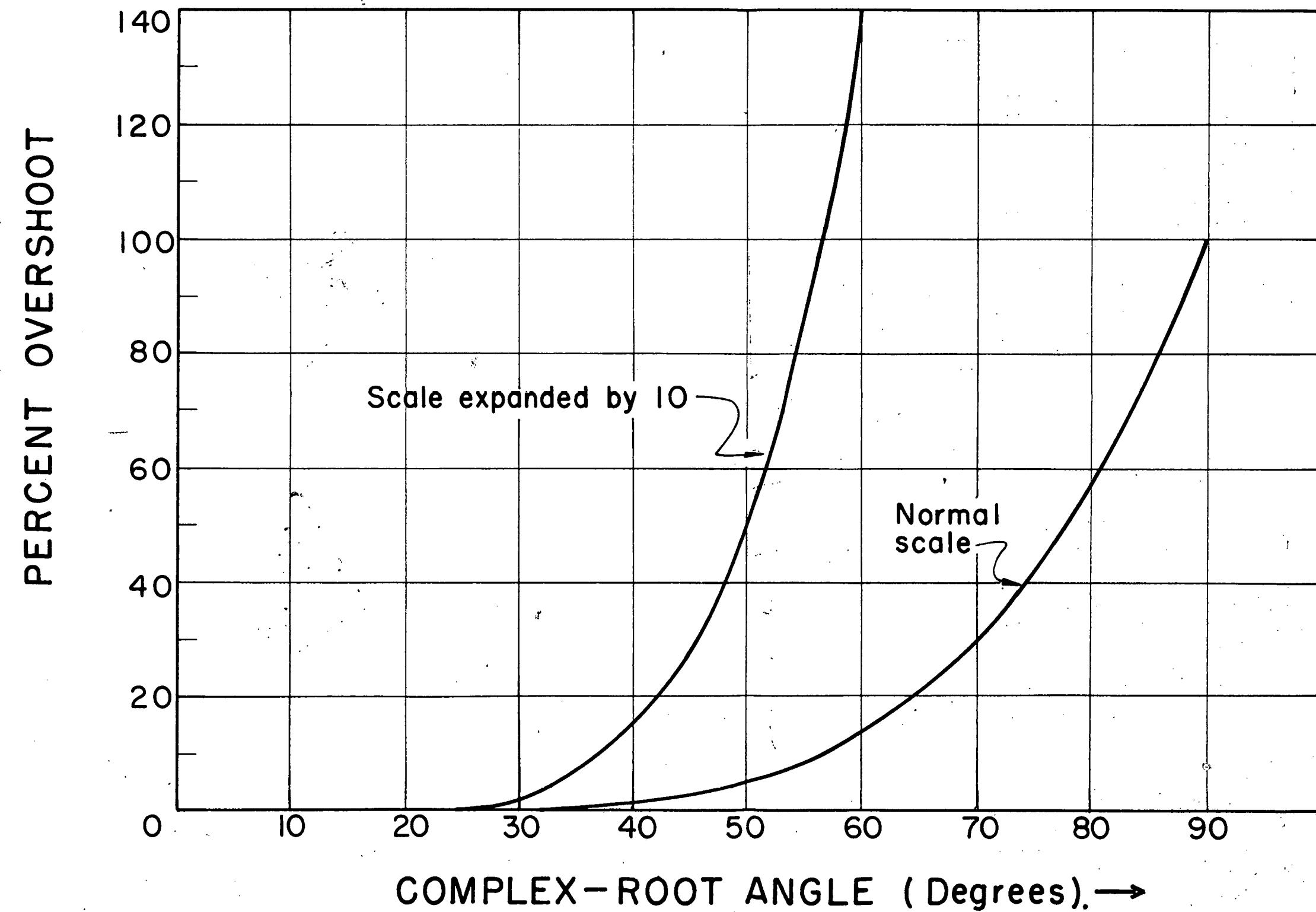
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1-5



843 227

166
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F-1