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Finite Element Modeling of a Microhotplate for Microfluidic Applications

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ABSTRACT

A hand-held chemical laboratory (μChemLab) is being developed that utilizes a silicon- nitride-supported microhotplate in the front-end, gas sampling and preconcentration stage. Device constraints include low-power (<200mW at 5V), rapid heating (<20msec), and a relatively uniform temperature distribution throughout the heated area (~3mm^2). To optimize for these criteria, the electro-thermal behavior of the microhotplate was modeled using Thermal Analysis System (TAS). Predicted steady-state and transient behavior agree well with infrared (IR) microscope data and measured transient response for a low-stress silicon nitride thermal conductivity of $k_n = 6.4 \cdot 10^{-2}$ W·(cm·°C)$^{-1}$ and a convection coefficient of $h_{cv} = 3.5 \cdot 10^{-3}$ W·(cm^2·°C)$^{-1}$. The magnitude of h_{cv} is framed in the context of vacuum measurements and empirical data. Details and limitations of the IR measurement are discussed. Finally, the efficacy of methods for reducing thermal gradients in the microhotplate's active area is presented.

Keywords: Microhotplate, preconcentrator, IR microscope, chemical analysis, TAS

INTRODUCTION

An autonomous, portable, hand-held chemical laboratory (μChemLab) is being developed for the detection of selected target analytes, such as chemical warfare (CW) agents and explosives in environments that may contain more than 1000-fold higher concentrations of interferents. Thus, rapid, sensitive (1-10 ppb) and selective response, using small, low-power components is crucial, and to this end, all critical components are microfabricated. Sensitivity and selectivity are enhanced via parallel analysis channels; each gas analysis channel contains a microhotplate-based sample collector/preconcentrator, a gas chromatographic (GC) separator, and a chemically selective surface acoustic wave (SAW) array detector [1].

The microhotplate-based preconcentrator (Figure 1) is required, based on system-level restrictions, to operate with less than 200 mW at 5V in the steady state. After selectively concentrating the desired analyte in a coating deposited on its surface, the microhotplate must attain 200 °C in less than 20 msec to thermally desorb the analyte in a pulse of temporal width sufficiently narrow for GC separation. To effect ample collection/desorption, the microhotplate must, furthermore, have a large, uniformly heated active area.

The coupled electro-thermal response of the microhotplate was simulated using Thermal Analysis System (TAS), an affordable, Windows-based thermal analysis package. Though sometimes neglected in modeling of microsystems [2], natural convection was found to be an important heat loss mechanism for this device, accounting for nearly 25% of the total heat lost. Moreover, a silicon nitride thermal conductivity, k_n, roughly twice published values [3] was required. Explanations for the magnitudes of k_n and h_{cv} will be offered. Because IR microscopy is important to the thermal analysis of microsystems, the details and limitations of this technique will be discussed.

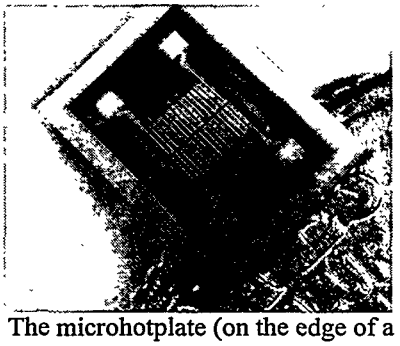

Figure 1: The microhotplate (on the edge of a quarter). "Bosch etching", stopping on the SiN membrane, was used to produce the free-standing structure.

IR MICROSCOPY

Steady-state measurements of microhotplate temperature distribution were used for model validation, and to tune the relatively unknown values of k_n and h_{cv}. A Barnes Infrascope™ was utilized for these measurements. This system employs a liquid-nitrogen-cooled array of 5 x 5 μm InSb pixels with spectral sensitivity from 1.5- 5.5 μm. Radiative emission from the sample is focused on the array by a system of IR optics. Objective lenses up to 10x are available; for the data presented here, a 5x lens with a specified spatial resolution of 8 μm and a depth of field (DOF) of 25 μm was applied.

The microscope obtains the temperature distribution, $T(x,y)$, of a sample by measuring its self-emitted radiance, $R(x,y)$, and correcting for the emissivity, ε, of the surface. A global value of ε would be quite useless for a microhotplate, given the variety of materials present. Instead, this system makes use of a two-temperature

DISCLAIMER

Design Guidelines for Use of COTS Technology in Military and Space Systems[1]

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Abstract

This paper provides a set of guidelines for the cost-effective use of COTS microelectronics in radiation environments that enables the circuit or system designer to manage risk and ensure mission success. Clearly, COTS with low radiation tolerance should not be used when it degrades mission critical functions or leads to premature system failure. These guidelines review the many factors and tradeoffs affecting the successful application of COTS including (1) definition of the radiation environment and setting component requirements, (2) hardness assurance and qualification techniques, (3) evaluation of life-cycle costs, and (4) system hardening techniques. The paper also describes several experimental studies that evaluate trends in radiation hardness as COTS technology scales to smaller feature sizes. As an example, the level at which dose rate upset occurs in Samsung SRAMs increases from 1.4×10^8 rads(Si)/s for a 256K to 7.7×10^9 rads(Si)/s for a 4M, perhaps symptomatic of design rules for reduced noise and increased switching speed. In another study, we report 10-15% variations in upset and latchup thresholds for SRAMS from three different date codes. The paper attempts to carefully define terms and clear up misunderstandings about the definitions of "COTS" and "radiation tolerant" technology.

I. INTRODUCTION

The commercial electronics market is driving the electronics industry. While defense electronics was once 60 to 70% of the electronics industry in the early 1960's, it is now about 0.5% of a $150B market! Designers of military systems, which often must operate in radiation environments ranging from natural space to a hostile nuclear threat, will no doubt strive to use the latest semiconductor microelectronics technologies for enhanced processing capability, autonomous control, and low power operation. However, state-of-the-art commercially available microelectronics (i.e., COTS) is often susceptible to radiation damage. This document provides a set of guidelines for the cost-effective use of COTS microelectronics in radiation environments that enables the designer to manage risk and ensure mission success. The paper provides the results of several experimental studies intended to provide a technical basis for hardness assurance approaches and techniques.

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I. DEFINITION OF TERMS

A. *What is COTS?*

"COTS" means that the product is Commercially available Off The Shelf. It means that you are buying what the supplier offers as their standard product, which can be found in supplier databooks or Standard Military Drawings (SMDs). A diode from Radio Shack is COTS. A radiation-hardened R6000 microprocessor from Lockheed Martin Federal Systems Manassas, VA (LMFS) is also COTS, although it doesn't meet the high volume and low cost attributes usually associated with commercial offerings. In addition, ASICs with standard cell libraries and Gate Arrays that allow for user unique specifications are still characterized as COTS.

Although suppliers of radiation-hardened COTS technology like LMFS and Honeywell Solid State Electronics Division (HSSED) carefully control and qualify their technology (through QML) to meet high levels of radiation, most commercial COTS parts suppliers do not identify or control technology parameters that affect radiation hardness. Consequently, radiation hardness of COTS microelectronics is often low and highly variable. For example, state-of-the-art CMOS ICs, e.g., an Intel Pentium II chip, will fail at total-dose levels as low as a few kilorads and suffer latchup if exposed to high-energy particles in space. *It is important to note that >99% of COTS microelectronics is radiation soft and, consequently, the focus of the guidelines is to address the challenges of using COTS in radiation environments.*

We define product that is not commercially available in supplier databooks as **"Custom."** Custom parts are sometimes "special order" from a COTS supplier. For example, a customer may require a change in layout or a different type of packaging. The customer must pay for these changes. Custom products are often defined in a Source Control Drawing (SCD).

B. *What is radiation-soft, -tolerant-, and –hardened technology?*

It has become popular to characterize technology based on its susceptibility to radiation damage as either radiation soft (RS), radiation tolerant (RT), or radiation hardened (RH). *Note that*

the radiation hardness level of a technology has nothing to do with whether or not it is "COTS" or "custom." Typically, RS technology is susceptible to latchup (LU) and fails at total-ionizing-dose (TID) levels less than 50 krads(Si). RH technology is LU immune and can survive TID levels in excess of 100 krads(Si). RT technology fills the gap between RS and RH. Although the concept of RT technology is intuitively appealing, the authors believe it can be potentially confusing and difficult to quantify. Where does one draw the line between RS, RT, and RH? *From the designer's prospective, one important and distinguishing feature of RH technology is that radiation hardness is qualified and guaranteed by the manufacturer.* RH technology would include QML-qualified product from LMMS and HSSED capable of operation at 1 Mrad(Si), as well as RT product from UTMC/AMI or National capable of operation at 100 krads(Si). *When purchasing parts from non-RH vendors for use in radiation environments, please note that the customer is responsible for assuring the level of radiation hardness.* Once again, the vast majority of COTS is RS.

III. EXPERIMENTAL STUDIES

A. *Technology Trends*

Table 1, provided by DTRA [1], summarizes the expected effects of increased integration density and reduced operating voltage on radiation sensitivity. The chart indicates that single-event upset, single-event latchup, dose-rate upset (transient), and total-ionizing dose hardness will degrade as MOS and bipolar technologies scale down to smaller feature sizes and reduced operating voltages. More specifically, SEL and SEU will degrade due to a reduction in nodal capacitance and voltage (i.e., notionally a reduction in "critical charge") [2]. But eventually, single-event latch-up will go away as V_{DD} approaches 1 V. If the effective junction area on the chip in which photocurrents are generated increases, then dose rate upset levels may degrade. In addition, complex metal routing schemes may contribute to rail span collapse and failure in the transient environment. There is a suggestion that total ionizing dose will get worse, but this is a hard one to call. The LOCOS isolation scheme should scale down to 0.35-μm, so one might think things would remain the same or improve slightly as isolation oxides get thinner. However, most manufacturers are migrating to "shallow trench" which is likely to be softer [3]. The important point is that right now at 0.5-micron, some circuits fail at doses as low as a few kilorads!

Table 1. Effects of Increased Integration Density and Reduced Operating Voltage on Radiation Sensitivity

Technology	SEL*	SEU*	Total Ionizing Dose	Displace-ment Damage	Dose Rate Upset
MOS	X	XX	X	O	XX
Bipolar	X	XX	X	✓	X

* SEL = Single Event Latchup
SEU = Single Event Upset

Legend	
XX	Significantly worse
X	Worse
O	No Change
✓	Better

There is a slight improvement in the hardness of bipolar technologies with respect to displacement damage as active device "base" regions are reduced in depth (i.e., higher f_T) and doping levels increase. There is no change in CMOS with respect to displacement damage because CMOS is a majority carrier device that is not sensitive to bulk lattice or displacement damage.

Overall, technology trends are poor for radiation hardness. Consequently, use of commercial technologies in space applications will become increasingly difficult. In some cases, the spacecraft designer may choose to raise the operating voltage, trading off low-power requirements (and perhaps reliability) for improved radiation hardness. *In addition, new physics and failure modes occur as technologies scale - some examples are multi-bit upset, microdose, and microlatch.*

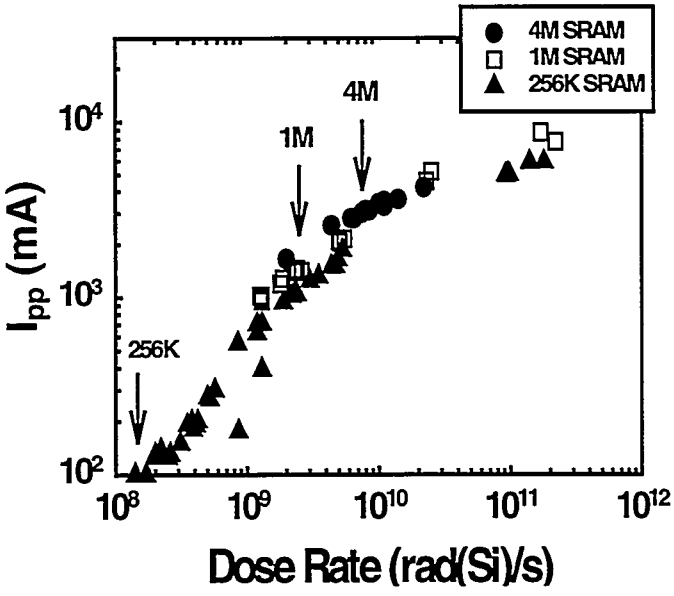

Figure 1. Radiation-induced photocurrent for SAMSUNG SRAMs following LINAC irradiation at room temperature and 5 V. Vertical arrows indicate upset levels.

This design guideline contains experimental studies aimed at providing a technical basis for decisions concerning the use of COTS in radiation environments [1-6]. For example, to better understand the impact of technology trends on the radiation susceptibility of COTS, and experiment was performed to examine effect of scaling on dose-rate susceptibility. Figure 1 shows photocurrents for 256K, 1M, and 4M COTS SRAMs from Samsung irradiated at room temperature and 5 V with ~20-ns FWHM pulses of 40-MeV electrons at the NSWC LINAC. The photocurrent increases with increasing dose rate, but is independent of the level of integration. In addition, the upset level is seen to increase at higher levels of integration.

Specifically, the level at which dose rate upset occurs in Samsung SRAMs increases from 1.4×10^8 rad(Si)/s for a 256K to 7.7×10^9 rad(Si)/s for a 4M, perhaps symptomatic of design rules for improved noise immunity. Improved dose rate immunity may also result from use of an epi layer or improved metal routing that mitgated the effects of rail-span collapse. This study clearly disagrees with the technology trend of Table 1 and further suggests that upscreening may be a viable approach to identify SRAMs with improved performance in dose-rate environments.

SEE tests of the Samsung SRAMs were performed at the BNL tandem Van de Graaff accelerator using 141-MeV Fl, 210-MeV Cl, 265-MeV Ni, and 312-MeV Au ions. All parts were tested with a logical checkerboard pattern while exposing the parts at a bias of 4.5 V. No difference was observed using a pattern of all ones or all zeros. Three parts each of the 256K and 1M SRAM and 7 parts from three different date codes of the 4M SRAM were tested. Comparing the error cross section curves in Fig. 2, we observed no significant difference in upset threshold for these three designs. The upset threshold for all three designs was approximately 3-5 MeV-cm^2/mg and clearly indicates that state-of-the-art non-hardened COTS is highly susceptible to SEU. The saturation cross section increased by more than the factor of 4x increase in number of cells between the 256K and 1M SRAM, while the saturation cross section for the 4M appears to be much lower than expected compared to the 1 Mb. A destructive physical analysis of these parts is in progress to explore the underlying design differences that may explain these data. These parts would readily upset in proton environments. Surprisingly, testing showed no SEL to an LET of 120 MeV-cm^2/mg. However, these tests were at nominal conditions, with bias at 4.5 V and room temperature not at worst case. The data suggests that state-of-the-art SRAMs are highly susceptible to proton-induced SEU and cannot be used in systems without EDAC or redundancy.

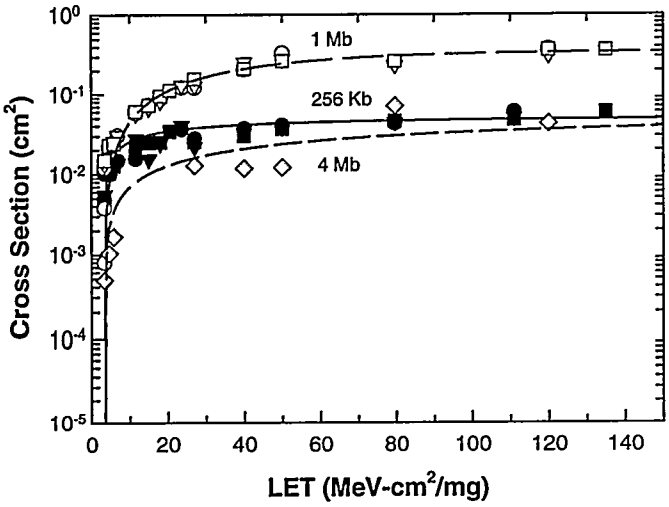

Figure 2. SEU response of Samsung SRAMs tested at Brrokhaven National Laboratories Tandem Van de Graaff. Solid symbols show 256K data, open symbols 1M data, and the half-tone symbols 4M data.

B. Variability & Date Codes

Except for RH COTS vendors (which is <0.1% of the market), technology parameters that determine radiation hardness are not intentionally controlled during the manufacture of COTS. Consequently, one expects a wide variability in the radiation hardness of COTS. This claim is supported by several studies that have appeared in the literature in recent years. In one study [6], the failure level for commercial SEEQ FG 256K E^{2}PROMs measured across thirteen wafers from the same diffusion lot varied between 5 and 25 krad(Si). In addition, there was a factor of 3 variation for a single wafer! In an investigation of the effects of packaging and burn-in on the radiation response of National Semiconductor 54AC02 Quad 2-input NOR gates [7], leakage currents varied from 10^{-7} to 10^{-2} A following a 50 krad(Si) irradiation. *Clearly, variability in the total-dose response of COTS is a major obstacle to upscreening, and perhaps the most serious hardness assurance challenge.*

Diffusion lot traceability may be important for ensuring radiation hardness of ICs, since total dose hardness can vary significantly from lot to lot (or even from wafer to wafer within a lot). The implied assumption is that all material from a single date code is also from a single diffusion lot. In a study [8] of fourteen COTS vendors, it was found that date codes do not necessarily relate to the assembly date, but to the test date. This is because parts can only be binned and marked for performance after test, and full AC tests are not usually performed until after assembly. Also, there can be delays between assembly and test and test to mark depending on workload, priorities, and the location of facilities. In some cases, this delay can be as long as a month due to priorities and loads. In addition, COTS vendors use contract assemblers depending on the volume of their fabrication and assembly. Where contract assembly houses are used it is nearly impossible to get diffusion lot traceability, because all traceability is lost at the assembly level. In a study of the total-dose and SEU response of memories [9], a post-test destructive analysis revealed that in some cases supposedly identical parts contained a different die revision in the package, and indeed had different radiation characteristics! *The bottom line is that we need to be careful in qualification of COTS components by acknowledging that parts from a given date code don't represent a single diffusion lot.*

In another experiment, the dependence of dose rate upset and latchup as a function of lot date code was examined for parts from three different date codes of the Samsung 4M-bit SRAM exposed to 40-MeV electrons at the NSWC LINAC. An "upset" was defined as a change in the data pattern read into the memory prior to exposure. The data shown in Table 2 indicate <10% variation in the average minimum dose-rate upset threshold. This is expected, since dose rate upset is normally determined by factors that do not vary from lot-to-lot, such as the memory design and layout, and doping profiles in the silicon. Similarly, the variation in latchup sensitivity was <15% for these parts over these date codes, indicating that

the parasitic bipolar transistors that control latchup are not varying from lot-to-lot. Unlike total-dose, dose-rate upset and latchup threshold may be somewhat independent of date code as long as basic technology/design parameters remain constant.

Table 2. Dose rate upset and latchup threshold

Date Code	Average upset threshold [rad(Si)/s]	Average latchup threshold [rad(Si)/s]
749	5.78E9	4.21E10
817	5.86E9	4.87E10
743	6.19E9	4.02E10

IV. SYSTEM HARDENING TECHNIQUES

In light of defense cutbacks, attrition, reduction in the number of hardened foundries, reduction in Above Ground Test facilities, and elimination of Under Ground Testing, we find ourselves with the biggest challenge of designing hardened systems in the future at lower cost. Past designs found radiation-hardened parts readily available and cost was seldom an issue. Since parts were quite robust, system designs generally provided plenty of margin and hardening techniques were not overly emphasized. However, when we find ourselves considering the potential performance benefits of COTS, we are finding that a lot more emphasis is now placed on system hardening techniques. Some of the impetus for system hardening techniques is a result of the following concerns:

- Variability in radiation hardness of a COTS component
- Rapid obsolescence of a component
- Increased sensitivity to radiation as technologies advance
- Minimal DC and AC parametric tests
- Processes and designs can change without notification
- Absence of traceability
- Hardness assurance is the customer's responsibility
- Manufacturer not familiar with radiation-hardening techniques and approaches
- Radiation data not available, mistakes in the database, or data is limited
- Test and Certification without UGT
- Reliability

There are a number of techniques for mitigating potential degradations and impacts on system performance. Several of these techniques are outlined below. In addition to applying these techniques, it is important that these techniques be integrated into a design as early as possible prior to the development stage of a program. Many projects have faltered by designing a package without the consideration of radiation until the design has been completed. This has resulted in slippage in schedules, costly redesigns and limited flexibility in hardening techniques. Radiation must be integrated prior to the predevelopment phase.

System hardening methods include:

1. parts selection
2. designing in degradation using degraded parameters
3. current limiting
4. shielding
5. conformal coating of boards
6. software and hardware error detection and correction
7. terminal protection devices at entry ports (TPDs)
8. fast circumvention or power strobe
9. watchdog timers
10. redundancy
11. minimize the number of selected suppliers and part count
12. minimize the number of active components
13. constant refreshing
14. use hardened parts in critical circuits in a system
15. use hardened nonvolatile memory for storing critical data.

Several of these methods will be discussed in the paper.

CONCLUSIONS

The use of COTS in radiation environments presents a significant challenge to system designers. Since most (>99%) COTS is very susceptible to radiation damage, the designer must make wise choices to carefully manage risk and ensure mission success. This paper outlines a set of design guidelines that evaluates many of the factors and tradeoffs affecting the successful application of COTS. In some cases, the designer may be able to upscreen parts (perhaps for dose-rate) or employ shielding (for total-ionizing dose). The use of radiation-hardened parts is highly encouraged – if you've got a radiation-hardened part that performs a mission critical function, then use it! As technology scales to smaller feature sizes and reduced operating voltages, the use of COTS in radiation environments will become increasingly difficult.

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