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Analysis of Interlayer Shorts in a 0.5 μm CMOS IC Technology

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Introduction

Sandia is manufacturing CMOS ICs with 0.5 μm LOCOS and shallow trench isolation (STI) technologies and is developing a 0.35 μm SOI technology. A program based on burn-in and life tests is being used to qualify the 0.5 μm technologies for delivery of high reliability ICs to customers for military and space applications. Representative ICs from baseline wafer lots are assembled using a high reliability process with multilayer hermetic, ceramic packages. These ICs are electrically tested before, during, and after burn-in and subsequent 1000 hour dynamic and static life tests. Two types of ICs are being used for this qualification, a 256K bit SRAM and a Microcontroller Core (MCC). Over 600 ICs have successfully completed these qualification tests, resulting in a failure rate estimate of less than 4 FITS for satellite applications. Recently, a group of SRAMs from a development wafer lot incorporating nonqualified processes of the 0.5 μm LOCOS technology had an unusually high number of failures during the initial electrical test after packaging. The investigation of these failures is described.

Sandia's 0.5 μm CMOS6 LOCOS Technology

Sandia's CMOS6 0.5 μm technology uses 150 mm (6 inch) diameter silicon wafers with (100) orientation. These wafers have a 3 μm thick p^- epitaxial layer grown on a p^+ substrate. A semi-recessed, 450 nm LOCOS oxide isolation is used. The gate oxide thickness is 12.5 nm and the minimum drawn transistor gate length is 0.6 μm (0.5 L_{eff}). An LDD (lightly doped source/drain) process is used for both the *n*- and *p*-channel MOS transistors with a 180 nm silicon nitride spacer for the LDD implant. The polysilicon gates and the n^+ and p^+ source and drain regions have $TiSi_2$ for low sheet and contact resistance. Chemical-mechanical polishing (CMP) is used for planarization of the PETEOS interlevel dielectric. CVD tungsten followed by CMP is used for contacts and vias. A sputtered Ti-AlCu-TiN metallization layer is deposited and RIE etched to complete the first interconnect layer. The other two metal interconnect layers are processed in a similar manner. Finally, a 2% CVD phosphosilicate glass (PSG) passivation of 1200 nm thickness is deposited followed by a H_2/N_2 forming gas anneal at 450 °C.

The 256K SRAMs are used as test vehicles for process development, yield and reliability enhancement, and qualification. The SRAMs have an *n*-well CMOS design with six-transistor memory cells.

Qualification Group Failures

The SRAM qualification group had 89 packaged ICs from a recent wafer lot. During the initial electrical tests, nine SRAMs (~10% of the group) failed all functional tests at all temperatures (-55 C, 125 C, and 25 C) and all voltages (3.3, 4.5, 5.0, and 5.5 V).

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These ICs also had high I_{DDQ} (about 20 to 50 mA at 5 V). The functional tests consist of writing and reading data with three patterns: topological checkerboard, complementary topological checkerboard, and unique address. The standard functional test provides only pass/fail information for the three functional patterns.

A diagnostic test provided information on the failing blocks, pages, and data. The diagnostic test data indicated that all nine SRAMs had the same failure mode. Data bits were failing at page increments of 256, corresponding to memory cells on the same word line. Further examination of the diagnostic data revealed that all data bits downstream (away from the word line driver) from a certain location on a word line were failing (the data bits from this location back toward the word line driver were working properly). The failure mode therefore appeared to be a word line that was defective (stuck) at a certain location along the word line (note: the particular word line that was defective and the location where the word line appeared to be stuck was different for each of the nine failing SRAMs).

Dynamic voltage contrast analysis was performed on one of the failures using a Cambridge S-200 SEM. The word line identified with the diagnostic test data did not switch properly in the region corresponding to the failing bits. However the specific failure site was difficult to identify because the 256K SRAM, like many commercial SRAMs, has self-timed logic circuitry. The self-timing logic completes its cycle in about 20 ns and then all row decoders and their associated word lines are off until the next address transition and read/write initiation. The fast on-off transition of the word line made it difficult to obtain a good quality voltage contrast image.

Thermally-Induced Voltage Alteration (TIVA) analysis was performed using a scanning optical microscope (Zeiss Laser Scan Microscope) [1]. A 1340 nm, Nd:YVO_4 laser illumination source was used to generate the TIVA signal and a Ge diode photo-detector provided reflected light imaging. A TIVA signal was found in the failing word line. Fig. 1 shows this signal for one of the failing SRAMs. The TIVA signal corresponds to the M3 interconnect from the word line driver to the location where the word line was logically stuck.

The TIVA site was examined optically and an abnormal feature was found at this site (Fig. 2). These unusual features were the same for all failures. These dark features appeared to be several microns long, on top of the M3 word line, and above an M2 power bus that ran perpendicular to the word lines. (Note: M3 is used to route global word lines across the entire memory array. At each block, the global word line signal is decoded and drives the polysilicon word line for that particular block.)

A failure site was cross sectioned using a FIB (focused ion beam) system. A short was found between M2 and M3, due to metallization in an ILD crack (Fig. 3). Metal also partially filled a crack in the PSG passivation. The passivation crack and metal partially filling it caused the dark feature observed optically. Fig. 4 is an FESEM image of the short (at a slightly different location due to additional FIB polish mills to obtain a better quality FESEM image).

Discussion and Conclusion

The ILD (and passivation) cracks and the associated metal shorts occurred either during the final wafer fabrication process steps or during packaging. It is considered

unlikely that they occurred during wafer fabrication because (1) over 600 SRAMs from eight different wafer lots with the same baseline process have successfully completed the qualification process with no indication of this failure mode, (2) the nine failures are nearly equally distributed among the four wafers used for the packaged SRAMs (two failures from each of three wafers and three failures from the other wafer), and (3) all nine failures would have to have been "near shorts" at the time of completion of wafer fab and wafer probe electrical testing (all nine passed all wafer probe tests prior to packaging). Therefore it is reasonable to conclude that the shorts occurred during packaging. The high reliability packaging of these SRAMs is performed by a service company. There are several elevated temperature steps during packaging: die attach (a silver glass material), pre-seal bake, lid solder seal (gold-tin eutectic), ink marking cure, stabilization bake, temperature cycling (10 cycles), and gross leak bubble test.

The evidence indicates that the shorts were due to misprocessing during packaging. However it is possible that something unusual occurred during the wafer processing of this development lot that made these SRAMs susceptible to failure during packaging. The only known unusual event during wafer fab was a delay (about nine days) between M3 patterning and PSG deposition (normally these steps are completed within one to two days). It has been suggested that moisture could have been absorbed during this process delay, resulting in high mechanical stress during the packaging thermal processes. The investigation of the root cause of the SRAM failures is continuing.

Acknowledgment

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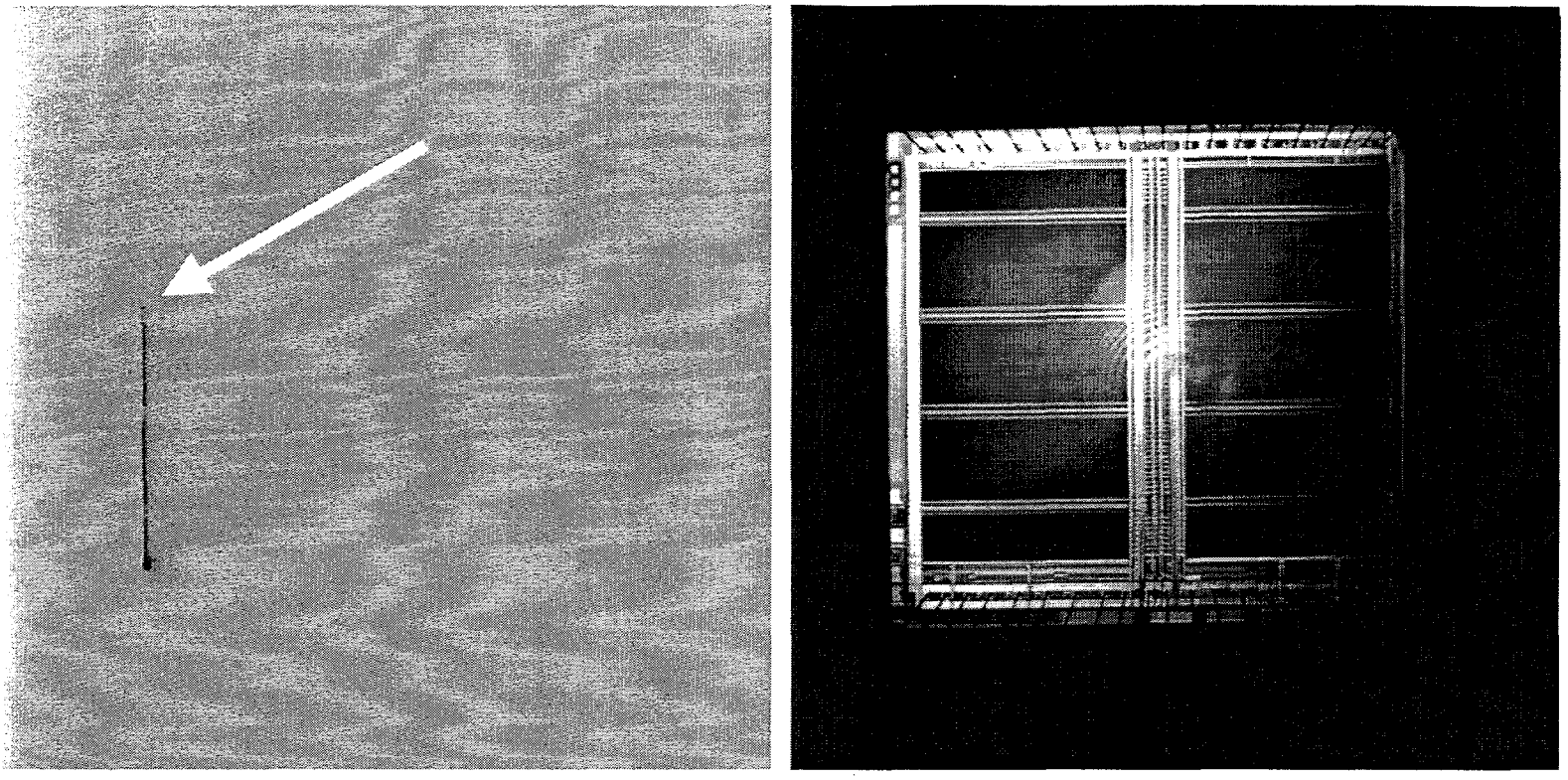
[1] E.I. Cole Jr, P. Tangyunyong, and D.L. Barton, "Backside Localization of Open and Shorted IC Interconnections," Int. Reliability Physics Symp., pp. 129-136, 1998.



A. B.

Fig 1.
A.TIVA signal of the word line short (arrow points to the end of the signal that correlates with the location of the first failing bit).
B. Reflected light image at same field of view as A.

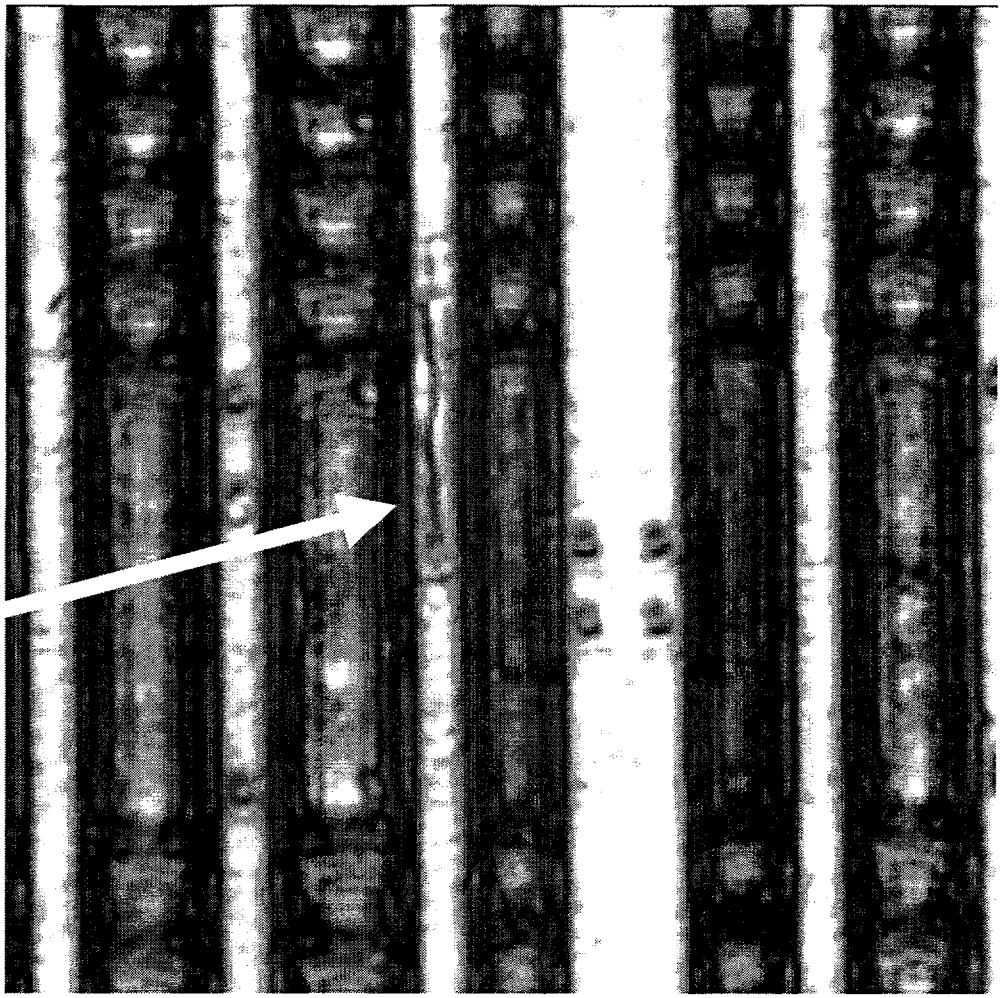


Fig 2. Optical image of word line short site.

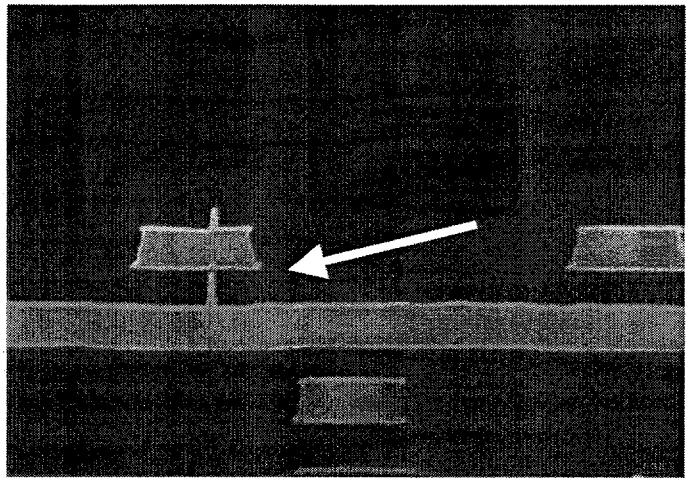


Fig 3. FIB cross section of the word line short (arrow points to short location).

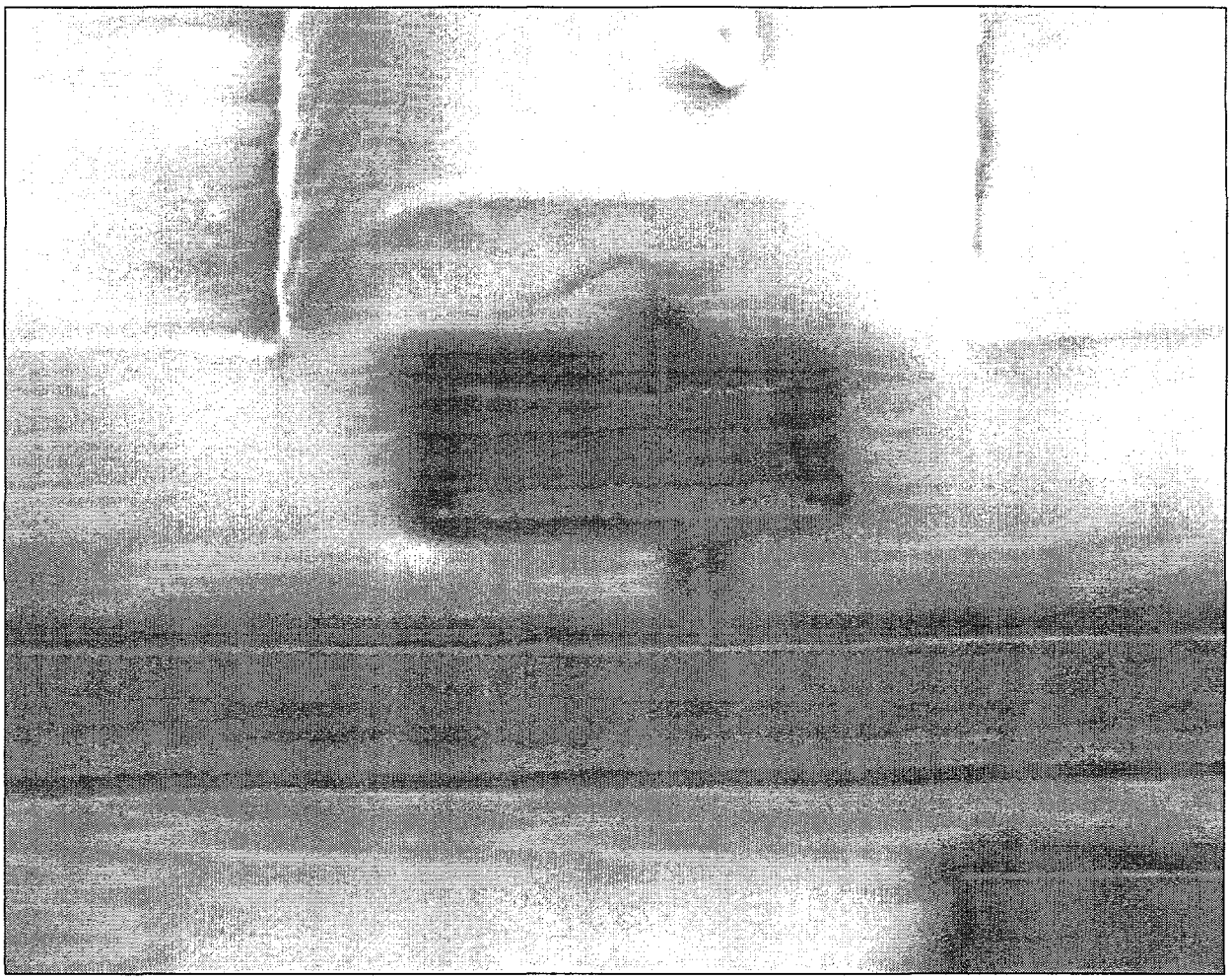


Fig 4. FESEM image of the FIB cross section of the word line short.