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Highly Focused Ion Beams in Integrated Circuit Testing

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Abstract

The nuclear microprobe has proven to be a useful tool in radiation testing of integrated circuits. This paper reviews single event upset (SEU) and ion beam induced charge collection (IBICC) imaging techniques, with special attention to damage-dependent effects. Comparisons of IBICC measurements with three-dimensional charge transport simulations of charge collection are then presented for isolated p-channel field effect transistors under conducting and non-conducting bias conditions.

1. Introduction

Single event upset is the disruption of a circuit's normal operation, caused by the passage of an ionizing particle through an integrated circuit (IC). In space-based systems, the sources of ionizing radiation can be galactic cosmic rays, particles emitted by solar activity, or protons trapped in the earth's magnetic fields. Terrestrially, energetic ions arise from naturally occurring, alpha-emitting transuranic impurities in IC manufacturing materials, products of cosmic ray showers and neutron-induced Si-recoils. When such particles lose energy transiting an IC, electron-hole pairs are created. The magnitude of this electrical charge is referred to as the particle's linear energy transfer (LET); it is the electronic portion of the stopping power (dE/dx) measured in units of MeV/mg/cm^2. High electric field gradients present in a circuit can enhance separation and collection of this electrical charge before recombination occurs. If the magnitude and duration of the charge collection transient is greater than a critical value for the circuit, upset may occur.

In order to probe circuits with higher resolution than is possible with apertured ion beams ($\cong$2μm), nuclear microprobes, which utilize magnetic and/or electrostatic lenses to focus high-energy ion beams, were applied to SEU testing and charge collection imaging of integrated circuits in 1992 [1,2]. Using this means of controlled, highly localized ion delivery, the upset susceptibility and charge collection characteristics of individual transistor components within a circuit can be directly measured. Additionally, calibrated charge collection spectra from isolated circuit structures can be compared with charge transport simulation results in order to test the predictive capability of simulation codes for future IC designs.

2. Nuclear Microprobe System

The Sandia Nuclear Microprobe is installed on a 6 MV Pelletron-upgraded EN Tandem Van de Graaff accelerator. The microprobe system is described in detail in reference [1]; it routinely produces beam spot sizes of 1.0 micron diameter. The scanning of the incident microbeam, and therefore the impact point of the ions on the circuit, is controlled by the data acquisition computer. Registry is thereby maintained between the position of the incident ion beam on the target and the signals arising from that exposure. The rastered scan of the normally incident beam consists of a 512x512 position grid. Owing to the highly damage-dependent effects on charge collection within ICs, event-by-event recording of the pulses arising from the ion exposures has been implemented. The resulting data file consists of a sequence of (x,y,z,t) entries which record the x and y position of the microbeam at the time the event occurred, the digitized height, z, of the event pulse, and the time, t, at which the event occurred (as derived from the computer's system clock).

The occurrence of SEU is detected by an external computer which is programmed to repetitively exercise the target circuit and issue a +5V pulse to the data acquisition computer if a malfunction is detected.

Measurement of the charge collected from the passage of an energetic ion through the circuit (IBICC) is accomplished by directly recording the charge pulse height resulting from each ion strike. In direct analogy to the configuring of a surface barrier detector, a charge-sensitive pre-amp is connected to the bias pin (V_{dd}) of the IC package; normal operating bias is applied to the IC through the pre-amplifier.

The duration of the ion beam exposure at each point in the scan is controlled by the data acquisition computer. All pixels in the scan are exposed for an equal period of time, and therefore to an equal average

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incident dose. The practical lower limit for exposure of a single pixel is dictated by the data conversion and storage time needed by the data acquisition system to process a single event; this value is 20 microseconds. Therefore, the average ion arrival rate must be less than 50,000 ions/sec, if single ion resolution is expected. Typically beam currents of only 500 to 2000 ions per second ($\cong$ 0.1 femtoamp) are used, providing on average a 500 microsecond period between ion arrivals. To improve display statistics, the data is normally binned to a resolution of 64x64x64 pixels, though the original data file retains the original 512x512x4096 resolution.

The SEU, IBICC and circuit simulation results presented here are all based on the Sandia-designed TA670 16K SRAM. The TA670 was designed in 1987 as a total dose and SEU rad-hard test chip using 2 μm design rules and fabricated on a 1 μm process line. Since we have access to the complete circuit design masks, vertical layout, doping concentrations, and other circuit parameters, the TA670 has been a valuable test-bed for evaluating microbeam radiation testing techniques.

3. Damage Effects in Single Event Upset (SEU) Imaging

Using a small number of TA670s which had been specially fabricated with reduced feedback resistance in order to increase their otherwise low upset susceptibility, SEU-images were recorded using 33 MeV Cu ions which have an LET of 27 MeV/mg/cm^2. The circuit layout of an individual memory cell being scanned in this measurement is shown in figure 1a. The dimensions of the memory cell are 30μm x 37μm. Alignment of the circuit design mask with the accompanying upset images is done through comparison to subsequently measured IBICC images. For the upset measurements in figures 1b and 1c, the memory cell contains a '1' logic state. In figure 1b, with no accumulated damage, upsets are produced only in the p-drain region; no upsets are observed in the n-drain. After a dose of approximately 500 ions/μm^2 [20Mrad(Si)], the n-drain begins to exhibit upset. After a dose of roughly 1200 ions/μm^2 [52 Mrad(Si)], both the n- and p-drain upset cross-sections saturate, as shown in figure 1c. A full description of this dose-dependence is given in reference [3], where it is proposed that the effect of the accumulated ion-induced damage is to decrease the restoring drive in the "on" transistors, and thereby slow charge dissipation and effectively reduce the LET-threshold of the n-drain to below the ~27 MeV/mg/cm^2 LET of the Cu beam.

When the measurement is repeated on a new, unexposed memory cell containing the opposite logic state, the same dose-dependence is observed, but with upsets occurring in the complementary pair of p- and n-

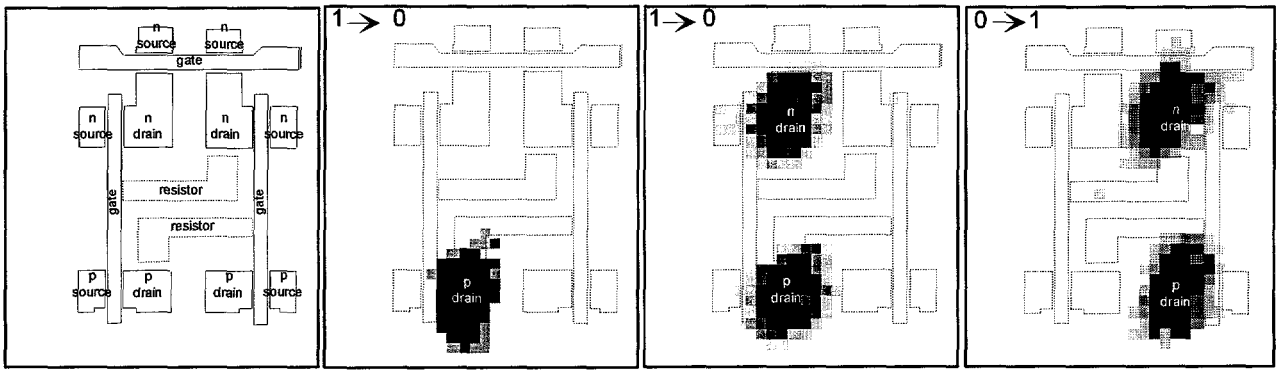

Figure 1. Dose and logic state dependence of SEU-Imaging. (a) Circuit layout of a single TA670 memory cell, scaled and oriented to the accompanying upset images; the cell size is 30 x 37 μm^2. (b) Initial upset image measured with 33 MeV Cu ions. (c) Upset image recorded after a dose of 1200 ions/μm^2. (d) Upset image for the opposite logic state after a dose of 1200 ions/μm ^{2}. Darker pixels reflect higher numbers of upsets.

drains. The resulting SEU-image, after an exposure of 1200 ions/micron^2, is shown in figure 1d.

The fact that such high doses (Mrad) were necessary to change the upset susceptibility of this part is a consequence of this device's initial radiation hardness. In 'softer' commercial devices, which often have upset thresholds of 2 to 4 MeV/mg/cm^2, we have observed changes in device response with dose much

more quickly. Thus, damage effects play a dominant role in microbeam-based radiation testing, even at beam intensities of less than a thousand ions/second. Unlike analytical applications of the nuclear microprobe, in which samples are routinely exposed to picoamp beam currents for many minutes during ion beam analysis, both the SEU and IBICC response of a device can degrade after only hundreds of ions per exposure location. This has been a prime motivation for implementing event-by-event recording and optical targeting of the ion beam using a front-viewing microscope.

4. Upset Effects in Ion Beam Induced Charge Collection (IBICC) Imaging

An SEU-image displays only those device structures which cause circuit malfunction under irradiation. Alternatively, the continuum of ion-induced charge collection within the integrated circuit can be measured, thus producing a detailed picture of the circuit layout, as shown in figure 2.

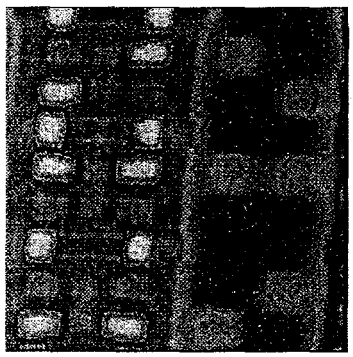

Figure 2. IBICC image of TA670.

Since the generation of charge within an IC is the underlying physical process which causes SEU, the amount of charge generated and collected at specific circuit nodes is an important point of comparison between experiment and computer simulations of circuit response to ionizing radiation. The complementary nature of the IBICC- and SEU-images also allows the two related phenomena to be examined independently. This is especially important since not all structures exhibiting high charge collection are necessarily sources of upset. Simulation results, in fact, have indicated that some regions that exhibit lower charge collection can in some circumstances induce upset [4].

The effect of accumulated dose on the pulse height of IBICC signals has previously been examined and been shown to play a significant role in IBICC measurements [3, 5]. We will comment on the effects of dose on the lateral collection of charge in section 6. In this section, the effect of the circuit's normal operation on the resulting IBICC image will be examined. This will require a slightly more detailed description of the circuit's operation and especially the conduction paths existing in the circuit for a given logic state.

The six transistor memory cell shown in figure 3a can be thought of as consisting of two cross-coupled inverters. Each inverter is formed by the serial connection of one n-channel and one p-channel field effect transistor. The overall logic state held in each inverter can be accessed through a transistor (either #5 or #6) which controls access to the "bit" or "not-bit" outputs of the memory cell. One inverter in figure 3a is composed of transistors #1 and #2; these two transistors share a common gate as well as an electrically conducting path between their drains. The second inverter is similarly formed out of transistors #3 and #4. Owing to the complementary nature of the memory cell's operation, when n-channel transistor #1 is "on", p-channel transistor #2 is "off", and vice versa. Additionally, when n-channel transistor #1 is "on", n-channel

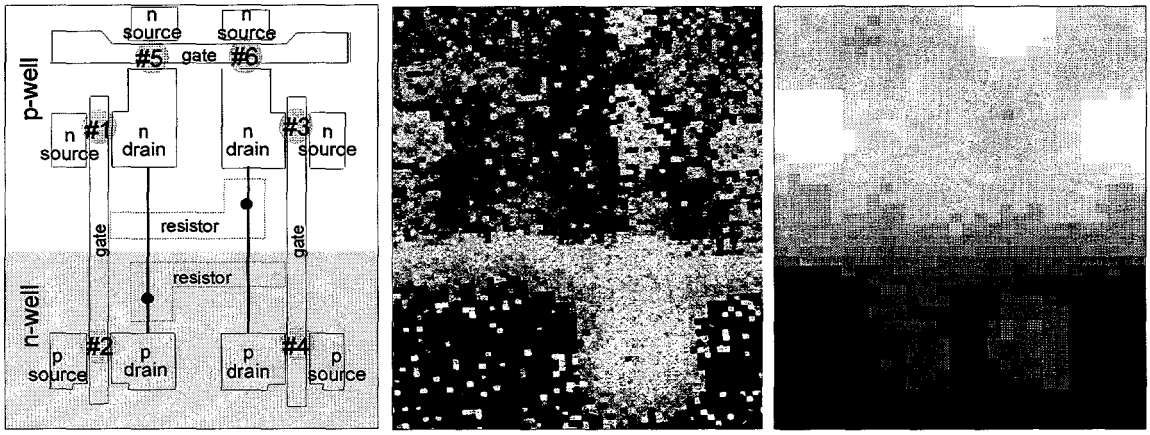

Figure 3. Upset effects in IBICC Images. (a) Circuit layout of TA670 memory cell. (b) IBICC-image of SRAM cell using 2.5 MeV He, (c) IBICC-image of SRAM cell using 12 MeV C while softened TA670 is biased at 2.5V. Greater charge collection is indicated by greater brightness in the IBICC images

transistor #3 is "off". Thus, for this condition, (i.e. #1-on, #2-off, #3-off, and #4-on), charge collected from the p-drain of transistor #4 and n-drain of transistor #3 can be measured with a pre-amp connected to the IC bias line, V_{dd}; charge collected into the n-off and p-on drains of transistors #1 and #2 cannot be measured since they have no conducting path to V_{dd} in this logic state. Conversely, when the memory cell contains the opposite logic state, the state of each transistor is likewise reversed, (i.e. #1-off, #2-on, #3-on, and #4-off) and charge collected into the n-off and p-on drains of transistors #1 and #2 can be measured, but not the n-on and p-off drains of transistors #3 and #4. Thus, as corresponding pairs of transistors turn on or off, two separate charge collection paths become connected to the V_{dd} bias line from which the IBICC measurement is being made. Since not all regions of the memory cell can, by definition, be measured and imaged simultaneously for a given logic state, any IBICC image of a static device will display only those circuit structures with a conducting path to the external charge-sensitive pre-amp. This is the condition displayed in figure 3b, in which a 2.5 MeV He ion beam has been used to image a single memory cell in the TA670. If, however, a higher LET beam is used, such that the memory cell is caused to upset by the beam's exposure, BOTH available conduction paths to the pre-amp will alternately become available as the memory cell successively 'flips' from one logic state to another. Thus in figure 3c, an IBICC image measured with a 12 MeV carbon beam, with 2.5V biasing of the device, depicts both p-drains in the memory cell, whereas in the 2.5 MeV He IBICC image of figure 3b, only one p-drain can be seen.

Charge collection measurements made from a transistor imbedded in surrounding circuitry can be quite different from the results obtained when the same transistor is irradiated in isolation. Differences arise from the introduction of external loading, capacitive coupling, and additional charge conduction paths or biasing conditions enforced by neighboring circuit structures. Without explicit control or measurement of this chorus of external influences, the conditions of the measurement can differ significantly from those assumed in the simulation. Therefore, as a first step toward validation of the simulation code for the entire circuit, we have begun by comparing the charge collection predicted by simulation, and measured by experiment, for an isolated, p-channel field effect transistor (FET) fabricated on the same die as the TA670 SRAM. A cross-sectional view of this p-channel FET is shown in figure 4, along with biasing conditions for the conducting ('on') and non-conducting ('off') states.

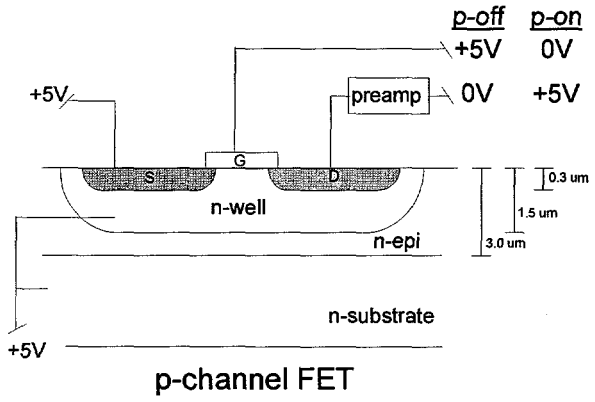

Figure 4. Biasing and vertical structure of the isolated p-channel FET.

5. Numerical Simulation of Charge Collection

The charge-collection characteristics of Si junction diodes and transistors in response to an ion strike are often computed using semiconductor device simulation codes [6]. Such codes solve Poisson's equation and the current continuity equations in one, two, or three dimensions, using finite element techniques. These equations describe the physics of carrier transport under potential and carrier concentration gradients, giving detailed microscopic information such as transient electron and hole densities throughout the simulated device. In this work, we have used DAVINCI, a commercially-available three-dimensional device simulator [7]. The simulations reported here typically require 6-8 CPU hours to execute on a Hewlett-Packard J210 workstation.

Inputs required for the simulations include structural information and doping profiles for the TA670. For the p-channel transistors simulated here, we have modeled only the drain junction diode. Simulations of the entire transistor produce identical results, because the charge collection is dominated by the drain junction. Doping profiles were taken from process simulations and spreading resistance measurements of the TA670 fabrication technology. A normally-incident 14 MeV C strike to the center of the drain was simulated using the charge generation profile (LET vs. depth) computed by TRIM [8], and a uniform track radius of 0.1 μm.

Following electron-hole-pair generation in the device, 3D drift and diffusion of the free carriers is computed by DAVINCI. The resulting terminal currents, (lower curve in figure 5), are integrated to give the simulated circuit node's charge collection characteristics, (upper curve). The transition from drift-dominated charge transport to diffusion-dominated transport is visible in the charge collection curve as the region of inflection occurring approximately 0.5 nanosecond after the ion strike.

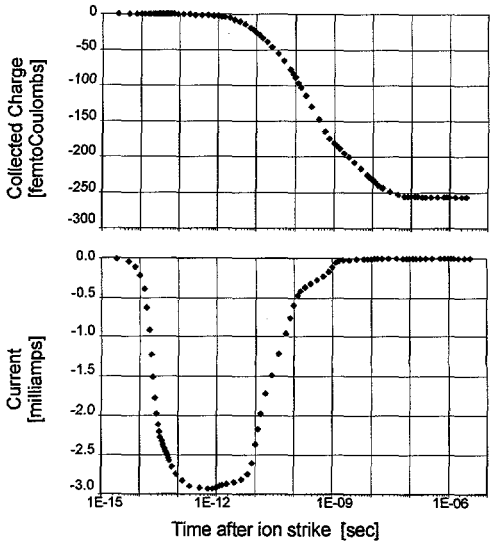

Figure 5. The DAVINCI simulation calculates the collected charge during the first microsecond after a 14 MeV C ion strikes the 'off' p-channel FET drain.

6. Comparison of 3-D Simulations and IBICC Experiment

Calibrated IBICC measurements were performed on a series of isolated p-channel FETs. Since degradation of IBICC pulses can occur after exposures of only hundreds of ions/μm^2, the target IC was replaced with an unexposed part upon exceeding ion exposures of 200 ions/μm^2. Furthermore, the data files were examined after the measurement for evidence of any signal degradation during the irradiation. The laboratory IBICC measurements were performed using a 14 MeV carbon beam, focused to 1 μm diameter as determined from STIM (scanned transmission ion microscopy) images of a 1000 mesh grid. The size of the beam scan was calibrated using the pitch of the 1000 mesh grid in the STIM image; the IBICC images shown in figure 6 are 40 x 40 μm.

The dwell time used in the calibrated IBICC measurements was 50 microseconds per exposed pixel. The original 512 x 512 resolution of the scanned beam has been binned to produce a 64 x 64 pixel image; thus each image pixel has a cumulative dwell time of 3.2 milliseconds, (64 exposure pixels * 50 microseconds/exposure pixel). The ion arrival rate was measured in a PIN diode four times during the IBICC measurements, yielding an average of 775 ±144 ions/sec. This results in an average ion exposure per image pixel per scan of 2.5 ±0.5 ions.

The range of 14 MeV carbon in silicon is 14 μm, with an LET of 4.2 MeV/mg/cm^2 at the surface, a maximum LET of 5.5 MeV/mg/cm^2 at a depth of 10 μm, and dropping below 4.2 MeV/mg/cm^2 at a depth of 11.5 μm. The vertical structure of the FET is shown in figure 4; the distance from the top of the encapsulation layer (not shown) to the underlying silicon substrate is 7.3 μm. Thus the 14 MeV carbon beam has an LET in excess of 4.2 MeV/mg/cm^2 throughout the entire active device and 4 μm into the underlying substrate. The data collection electronics were calibrated by measuring charge collection spectra of this ion in a previously unexposed PIN diode, biased to form a depletion depth of 30 μm (twice the calculated range of the beam). The full charge collection peak of the resulting spectrum, shown in figure 6, was equated to the calculated maximum charge production of this ion in silicon, 622 femtoCoulombs

In order to avoid damage effects such as discussed in section 3 and 4, the p-drain structures were optically targeted using a front-viewing microscope and only then exposed to the scanned 14 MeV carbon beam. In this way, the effects of any initial beam-induced damage on the IBICC pulse height could be detected if present. From examination of the time-evolution of the IBICC pulse heights measured from different regions of the scanned image, it was seen that the collection of diffusive charge from outside of the p-drain was quickly suppressed, (presumably by the introduction of defect sites acting as recombination centers), but that for doses up to 200 ions/image pixel, charge collection pulses from the drain itself did not show any measurable degradation. The images and charge collection spectra shown in figure 6 were generated using events collected in the first 20 scans of the beam across the test structure, or an equivalent ion exposure of 50 ions/image pixel. The charge collection from the p-drain is therefore taken to be unaffected by damage for the ion exposures used, and therefore representative of the p-drain charge collection under 14 MeV C irradiation. The boundaries of the p-drain, as specified in the design mask, are outlined in white dashed lines in the IBICC-images inset in figure 6.

The charge collection spectra recorded from the outlined region of the p-on and p-off drains are shown in figure 6. Charge collection measurements from the p-on drain display a peak at 245 femtoCoulombs (fC), while the DAVINCI simulation predicts a charge collection magnitude of 242 fC. Charge collection from the p-off drain is measured to be 262 fC, while the simulation again predicts a slightly smaller value of 257 fC. Thus, the magnitudes of the charge collection determined from simulation and experiment for both biasing conditions are found to agree to within 2%. Additionally, the roughly 15 fC difference in charge collection from the p-on and p-off drains is clearly resolved experimentally and predicted from simulation. In both biasing conditions, the simulation predicts charge collection which is slightly lower than the experimentally measured result. Though this is quite good agreement, we note that the simulation results can be extremely sensitive to inaccuracies in the device parameters supplied to it. In performing these simulations, device design parameters such as the dopant concentrations and thicknesses have, where possible, been subjected to independent verification using techniques such as spreading resistance measurements.

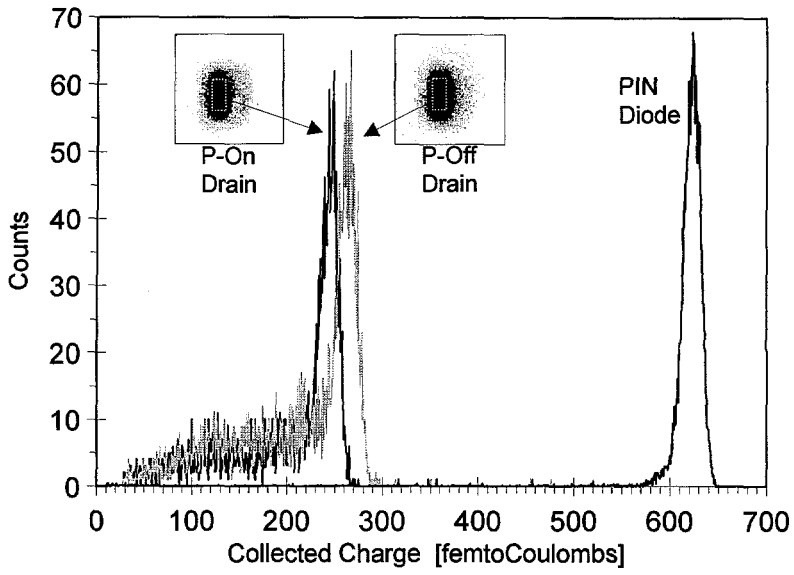

Figure 6. Charge collection spectra and IBICC images (inset) of isolated p-on and p-off drains for TA670 test FETs. The full charge generation of the 12 MeV carbon ions is indicated by the PIN diode measurement.

7. Conclusions

One of the most beneficial applications of microbeam-based radiation testing may lie in the verification of charge transport results from three-dimensional device simulations. However, unlike many analytical applications of ion microbeams, in which sub-picoamp beam currents cause little degradation of most samples, great care must be taken to measure and control ion dose when performing charge collection measurements from circuit structures that are susceptible to ion dose damage effects. This has been shown with explicit examples from both SEU- and IBICC-imaging measurements. Calibrated charge collection measurements from p-drains of isolated field effect transistors have been compared to DAVINCI device simulations. With measurements made under very controlled dose conditions, and inspected for the presence of any damage effects, microbeam-based calibrated charge collection measurements are found to agree with computer modeling to within 2%. The relative differences in charge collection from the p-off and p-on drains also conform to simulation predictions. Validation of device simulation codes is a necessary first step in establishing the capacity of such codes to predict the radiation tolerance of future circuit designs.

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