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Fifth Workshop on the Role of Impurities and Defects in Silicon Device Processing

Extended Abstracts

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Fifth Workshop On The Role of Impurities and Defects In Silicon Device Processing

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Defect Engineering in Solar Cell Manufacturing and Thin Film Solar Cell Development

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During the last few years many defect engineering concepts were successfully applied to fabricate higher efficiency laboratory (small-area) silicon solar cells on low-cost substrates. This achievement was made possible by many advances that include: (i) use of new characterization tools that can rapidly acquire information on material properties and collect sufficient data to have statistically meaningful information on commercial Si wafers/cells, and interpretation of the data, and (ii) new understanding of mechanism of impurity diffusion, gettering, and passivation. There are now attempts to incorporate these results into commercial processes for production of solar cells. Some of the research results responsible for these advances are described below for different areas of material growth and processing:

MATERIAL GROWTH AND PROPERTIES

• Dislocations appear to have the dominant effect on the cell performance. Dislocations are caused by thermal stresses during crystal growth. Low thermal stresses result in a preponderance of coherent twins. These regions of low or zero dislocation density are indicators of the quality of the material.

• Regions of zero-D appear to have some (undermined) type of defects that act as precipitation centers for interstitial metallic impurities.

• The concentrations of metallic impurities like Fe and Cr in as-grown commercial PV silicon materials can exceed $10^{12}/cm^3$. A high fraction of these impurities is gettered during the solar cell fabrication. Thus, in spite of the fact that high concentrations of impurities may be present in the starting material, it is possible to getter many of these impurities by post-growth processing.

IMPURITY GETTERING

- Several gettering methods such as Cl, Al, and P gettering can be very effective in improving the minority carrier diffusion length in the substrates
- Certain synergistic effects of impurity diffusion and segregation result in enhanced gettering efficiencies of some impurities; this feature can be exploited for improved gettering by simultaneous phosphorus and Al treatments.
- A difficulty in the gettering arises due to the fact that heavily dislocated regions cannot be gettered well because such regions "trap" impurities and precipitates making them immobile.
- A theoretical model was developed that agrees well with the experimental results. This model can provide valuable help towards optimizing gettering procedures.
- In most cases Al and P gettering have additive effects.

IMPURITY DEFECT PASSIVATION

• New insight into the defect passivation mechanisms was gained. It was determined that hydrogen can diffuse via formation of a vacancy-hydrogen complex, and that the presence of vacancies can enhance hydrogen diffusion at low temperatures.
• Variations in the degree of passivation due to hydrogen in different PV silicon substrates was determined to be related to concentrations of oxygen and carbon in the substrate. Further understanding of the passivation mechanism is needed.

OTHER RESULTS

• It has been determined that unlike IC quality material, low-cost substrates and cells degrade when process temperatures are increased above 950 °C.

• Modeling of nonuniformities in solar cells has shown that low-performing regions have a disproportionately strong influence on the cell performance. This result, coupled with the fact that gettering does not significantly improve high dislocation regions, suggests that the improvements in the performance of large-area cells by gettering will only be modest unless methods for effective gettering in highly dislocated regions are developed.

DISCUSSION OF SOME PROCESS RELATED EFFECTS IN MULTICRYSTALLINE SILICON

Many observed results of gettering, passivation, and thermal processing on the solar cell performance can be explained by considering various interactions between defects and impurities that take place during a gettering or a thermal process. A model that illustrates these interactions is shown in Figure 1. This figure depicts a multi-crystalline silicon sample containing grain boundaries, dislocations, impurities, and point defects as interstitials and vacancies. The impurities are shown to be in two states — dissolved, and precipitated at grain boundaries and dislocations. This model can be used to explain qualitatively why gettering does not improve the regions of high dislocations, and why processing at temperatures higher than about 950 °C result in degradation of the material quality. The former is related to the fact that impurities precipitation at the defect sites takes place at high temperatures during the cool down of the crystal. Experimental results suggest that during the crystal growth impurities precipitate on dislocations and grain boundaries with the formation of silicides. Since precipitated impurities cannot migrate, a typical gettering process does not effectively remove impurities from heavily dislocated regions. On the other hand processes, point defect injection that can take place during a gettering process can enhance impurity dissolution. If the impurity dissolution rate is greater than the gettering rate, gettering step can result in an increase in the concentration of dissolved impurities, accompanied by degradation in the cell performance. This process is likely to occur at higher temperatures.

MANUFACTURING ISSUES

Although application of these concepts have led to 17.8% small area solar cells, there are several basic obstacles that must be overcome before such high efficiency cells can be commercially manufactured by low-cost processes. These are:

• Need to remove surface regions following P or Al gettering. The need to remove the surface regions is due to several factors. (i) high concentrations of impurities can accumulate at the surfaces causing their properties to deviate from the optimum. For example, extensive phosphorus gettering may not produce good emitter properties. (ii) Gettered impurities may diffuse back into the bulk of the substrate during subsequent processing. However, etching the gettering region can be an expensive process step.

• Improving the spatial uniformity of the cell. As pointed out above, low performing (high dislocation density) regions can act as internal "sinks" and lower the cell efficiency.

• Effective means for hydrogen passivation

• Low-temperature gettering

THIN FILM CRYSTALLINE SILICON SOLAR CELLS

Another area of rapid advances is the development of thin film silicon solar cells. It is clear that a significant reduction in the cell costs can take place if lower quality silicon thin films, on low-cost substrates like glass, can yield reasonably high efficiencies. However, many problems need to be solved before such structures can be realized. Some of the critical areas of these cells are:

- Development of suitable method of deposition /formation of large-grain films
- Impurity diffusion (inter diffusion) during thin layer growth and subsequent cell processing
- Degree of light trapping that can be achieved on thin cells
- Optical losses arising from local field (intensity) enhancements in thin film cells
- Interface recombination effects

This workshop is oriented to address two major issues:

1. Applications of defect engineering concepts for commercial production of high efficiency solar cells on low-cost substrates that are being developed in laboratory, to commercially produce high efficiency cells, approaching 18%, on low-cost substrates

2. Identify critical areas of thin film silicon solar cells for further research and development

The program for this workshop is somewhat different from previous workshops. The program committee has come up with a schedule that will provide plenty of time for discussion (this was a general request from the participants of previous workshops). Three major features of this workshop are: (i) review talks on selected topics that will emphasize the basics of certain critical issues in achieving high efficiencies. (ii) Panel discussions that will discuss issues of timely importance, and (iii) Poster sessions that will present most recent results from industry as well as research laboratories. Because of the importance of the recent results from poster session, there are two poster committees that will summarize highlights of the poster presentation on the following mornings.

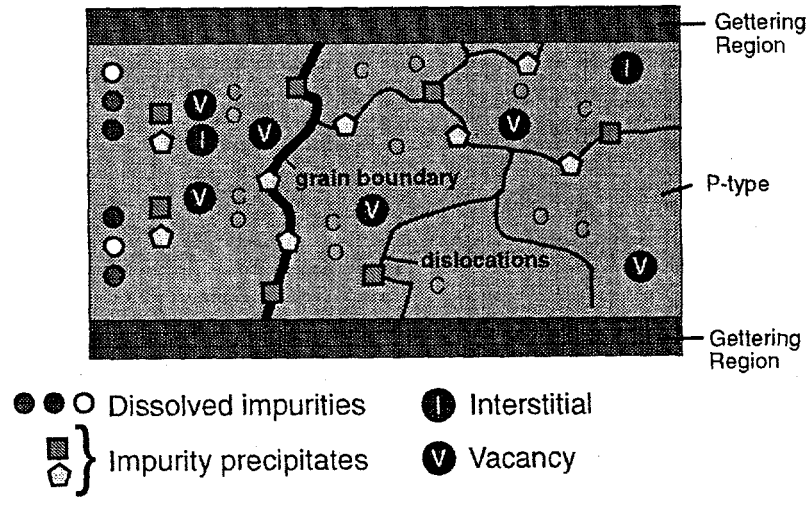

Figure 1
A schematic illustrating various processes that can take palce in a multi-crystalline silicon solar cell during processing

ELECTRONIC PROPERTIES OF IMPURITIES AND DEFECTS IN SILICON/HIGHLIGHTS OF ICDS18

Kim Kimerling

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BEHAVIOR OF DISLOCATIONS IN SILICON

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Abstract : A review is given of dynamic behavior of dislocations in silicon on the basis of works of the author's group. Topics taken up are generation, motion and multiplication of dislocations as affected by oxygen impurities and immobilization of dislocations due to impurity reaction.

1. Introduction

Various kinds of structural defects are generated in semiconductor crystals due to energetic stimulation given during device production processing. Generation of defects can be controlled and, as a consequence, high performance of devices can be achieved if one understands the mechanism of generation of any type of defect and the roles of various factors in such a process. This paper gives a review on the mechanisms of generation and multiplication of dislocations in Si together with the effects of temperature, stress and impurities on such dislocation processes.

Those who are interested in more detailed description of dislocation-related phenomena in semiconductors and their application to the device production technology may refer author's review articles given at the end of this paper.

2. Dislocation Generation in Si

2.1. Mechanism of dislocation generation in real Si crystals

When a Si crystal initially free from dislocations is stressed at a high temperature, dislocations are generated heterogeneously under a stress lower than the ideal strength for dislocation nucleation by orders of magnitude (Sumino and Harada, 1981). The ideal strength is the stress necessary to cause slip or to generate a dislocation in a perfect crystal and has theoretically been evaluated to be about 0.24 G for a diamond-type crystal, where G is the shear modulus of the crystal. Usually, dislocations are observed to be preferentially generated at the surface region of the crystal and to penetrate into the bulk if the crystal contains no structural irregularities inside which facilitate dislocation generation.

Such a observation naturally leads to the idea that any real crystal has some irregularities on the surface that act as the preferential generation centers of dislocations under stress at an elevated temperature. The irregularities are thought to be microscopic regions with strongly disturbed atomic structure which may be formed by some energetic stimulation such

as mechanical shock or chemical reaction at the surface which is inevitably or accidentally involved during the surface preparation.

Recent TEM observations have revealed that an extremely tiny region of amorphous silicon surrounded by a dislocated crystalline region is formed locally due to mechanical stimulation, such as scratching, abrasion or indentation under a very small load on silicon surface at room temperature (Clarke et al., 1988, Minowa and Sumino, 1992). The amorphous region seems to be formed not as a result of heavy plastic deformation of the Si crystal but by means of phase transformation of crystalline Si under a highly localized stress. Dislocations developed around the amorphous region are on the {111} planes and have Burgers vectors parallel to the <110> directions. The magnitude of the shear stress realized in the region under the above type of mechanical stimulation is estimated to be close to the ideal strength of the crystal. Thus, these dislocations are thought to be generated by spontaneous nucleation under such a high stress. The amorphous region is observed to transform to a heavily dislocated crystalline Si when the crystal is brought to a temperature higher than about 500 ℃ (Minowa and Sumino, 1992).

The mechanically stimulated region on the surface of a Si crystal accompanies a strained region around it which is extended over a macroscopic scale observable with X-ray topography. Such strained region shrinks in size when the amorphous micro-region transforms to the dislocated micro-region due to annealing. When the crystal is under stress, some of dislocations which have the maximum Schmid factor come out of the micro-region and penetrate into the matrix and expand on a macroscopic scale (Sumino and Harada, 1981). At this stage dislocations are usually recognized to be generated.

2.2. Impurity effect on dislocation generation

Dislocations are easily generated from a flaw formed by local mechanical stimulation in high purity silicon crystals even under extremely low stresses at high temperature. However, in a crystal doped with a certain kind of impurities no dislocations come out of the flaw until the applied stress exceeds a critical stress even though the flaw accompanies a dislocated micro-region. Light element impurities such as oxygen and nitrogen in Si have been observed to be effective in suppressing dislocation generation. The impurity effect on the generation of dislocations in CZ-Si has been investigated making use of intentionally introduced surface flaws such as indentations

Figure 1 shows the critical stress for dislocation generation from a Knoop indentation made at room temperature in a FZ-Si and a CZ-Si crystal as a function of the temperature (Sumino and Harada, 1981). In high purity FZ-Si dislocations are generated under a stress lower than 1 MPa over the whole temperature range tested. On the other hand, in CZ-Si fairly high magnitudes of the critical stress are measured. The critical stress increases with an increase in the temperature. It is not related to the

resistance against the dislocation motion due to oxygen atoms dissolved in the crystal.

The suppression of dislocation generation in impurity-doped Si has been found to be caused by the immobilization of dislocations due to gettering of impurities atoms at the dislocation core, which will be discussed in section 4. The critical stress for dislocation generation is related to the release stress of immobilized dislocations in the flaw region.

When stress is low enough to allow the development of clusters or complexes of oxygen atoms along dislocations in recrystallized dislocated region at a flaw, the dislocations are immobilized and do not come out of the flaw region until the applied stress exceeds the release stress. This is thought to be the mechanism of suppression of dislocation generation in the CZ-Si crystal.

3. Dislocations in Motion and Multiplication of Dislocations

3.1. Velocity of dislocations in Si

The most reliable experimental technique for the measurements of dislocation velocity in Si, especially in the presence of pinning impurities, is that by means of *in situ* X-ray topography developed by the Sumino group (Sumino and Harada, 1981, Imai and Sumino, 1983) utilizing a high-power X-ray source, a high temperature tensile stage, and a highly sensitive T.V. system. Motion of isolated dislocations in a crystal introduced from some sources can be followed by real time observation as functions of the temperature and the applied stress with this technique. The technique is free from the ambiguity related to pinning effect of impurities in determining the dislocation velocity. Kinetic behavior of dislocations in Si as clarified with such in situ X-ray topographic technique is described in this section.

The velocities of isolated 60 ° and screw types of dislocations in high purity FZ-Si have been measured to be linear with respect to the shear stress in the stress range 1 − 40 MPa and the activation energies to be independent of the shear stress in the temperature range 600 − 800 ℃ . The dislocation velocity v is expressed well with the following equation:

$$v = v_0 (\tau / \tau_0) \exp (- Q / k_B T). \qquad (1)$$

The magnitudes of v_0 are 1.0×10^4 and 3.5×10^4 m/s and those of Q are 2.20 and 2.35 eV for 60 ° and screw dislocations, respectively (Imai and Sumino, 1983).

3.2. Effect of oxygen impurities on dislocation velocity

As will be discussed in the next section, oxygen impurities are effective in immobilizing dislocations upon segregating on the dislocations. We mention here the effect of such kind of impurities on the

velocity of dislocations in motion.

Figure 2 shows the relations between the velocity of a 60 ° dislocation and the shear stress at various temperatures in CZ-Si crystal containing oxygen impurity at a concentration of 7.4×10^{17} atoms/cm^3 (Imai and Sumino, 1983). Data for high purity FZ-Si are also shown in the figure. Dislocations in the crystal containing oxygen impurity move at velocities which are equal to those in the high purity FZ-Si crystals in a high stress range. However, dislocations originally in motion under a high stress cease to move when the stress is reduced lower than the stress shown by vertical broken lines in the CZ-Si crystal. The velocity of dislocations in the crystal containing oxygen decreases more rapidly than in the high purity FZ-Si as the stress is decreased toward the critical stress for the cease of dislocation motion shown by vertical broken lines in the figure.

Figure 3 shows the velocity versus stress relations for 60 ° dislocations at 647 ℃ in Si with dissolved oxygen impurities at various concentrations (Imai and Sumino, 1983). Again, the dislocation velocities in the crystals containing oxygen impurity at any concentration are almost the same as those in high purity FZ-Si under high stresses. Both the deviation of the velocity from that in the high purity FZ-Si with decreasing stress in the low stress range and the critical stress for the cease of dislocation motion increase with an increase in the concentration of dissolved oxygen impurities.

Essentially the same effect of dissolved oxygen impurities on the dislocation velocity is observed also for screw dislocations.

The shape of moving dislocations in high purity FZ-Si crystals is observed always to be a regular hexagon or half-hexagon of which segments are straight along <110> directions over the wide stress range investigated. This is true also in Si crystals containing oxygen impurity when dislocations are moving at the velocities equal to those in the high purity FZ-Si in the high stress range. However, whenever the velocities of dislocations deviate from those in the high purity FZ-Si under relatively low stresses, the shape of the moving dislocations is observed to be perturbed from the <110> straight lines and to become irregular. Namely, the retardation of dislocation motion due to impurities is accompanied by the perturbation in shape of the dislocation in motion. The perturbation in shape of dislocation means per se that the obstacles against dislocation motion developed not uniformly along the dislocation line on a macroscopic scale.

We have now the following picture. In Si crystals containing oxygen impurity oxygen atoms catch up to a slowly moving dislocation and develop clusters on the dislocation line which have a high interaction energy with the dislocation. This results in both the perturbation of the line shape and retardation of the dislocation. A dislocations ceases to move when such clusters or complexes of impurities are developed closely along the dislocation line.

3.3. Multiplication of dislocations

Once dislocations are generated in a crystal, they multiply themselves during motion and increase their density (dislocation length in the unit volume of crystal).

In situ observations of dislocation multiplication processes by means of X-ray topography (Sumino and Harada, 1981) and transmission electron microscopy (Sato and Sumino, 1977, Sumino and Sato, 1979) have revealed that dislocation multiplication takes place by two basically different mechanisms in Si crystals; one is spontaneous multiplication of gliding dislocations, for example, by means of double cross slip, and the other multiplication through interaction of dislocations belonging to different slip systems.

In the former case a simple model leads to the following multiplication rate of dislocations (Peissker et al., 1961):

$$\mathrm{d}N/\mathrm{d}t = K \tau_{\mathrm{eff}} N \bar{v}, \tag{2}$$

where N is the dislocation density and K is a constant. τ_{eff} is the so-called effective stress and is given by

$$\tau_{\mathrm{eff}} = \tau_{\mathrm{a}} + \tau_{\mathrm{i}}, \tag{3}$$

and

$$\tau_{\mathrm{i}} = G b N^{1/2} / \beta, \tag{4}$$

where G is the shear modulus, b is the magnitude of the Burgers vector of dislocations and β is a constant of about 3 — 4. $\bar{v}$ in Eq.(2)is obtained by substituting τ_{eff} in Eq.(3)in the place of τ in Eq.(1).

In the case in which the two multiplication mechanisms work simultaneously, the multiplication rates of dislocations of the two different slip systems labeled by suffixes 1 and 2 are given by

$$\mathrm{d}N_1/\mathrm{d}t = K N_1 v_1 \tau_{\mathrm{eff},1} + K^* N_1 N_2 v_1 \tau_{\mathrm{eff},1}, \tag{5a}$$

$$\mathrm{d}N_2/\mathrm{d}t = K N_2 v_2 \tau_{\mathrm{eff},2} + K^* N_2 N_1 v_2 \tau_{\mathrm{eff},2}, \tag{5b}$$

respectively (Sumino and Yonenaga 1991), where K and K^* are constants which characterize the two multiplication processes. $\tau_{\mathrm{eff},1}$ and $\tau_{\mathrm{eff},2}$ are given by

$$\tau_{\mathrm{eff},1} = \tau_{\mathrm{a},1} - G b N_1^{1/2} / \beta - G b N_2^{1/2} / \beta^*, \tag{6a}$$

$$\tau_{\mathrm{eff},2} = \tau_{\mathrm{a},2} - G b N_1^{1/2} / \beta^* - G b N_2^{1/2} / \beta, \tag{6b}$$

where $\tau_{\mathrm{a},1}$ and $\tau_{\mathrm{a},2}$ are the resolved shear stresses of the applied stress with respect to the two slip systems and β and β^* are constants characterizing the interaction between dislocations of the same slip system and that between dislocations belonging to different slip systems, respectively ($\beta > \beta^*$).

The validity of Eqs.(5a)and(5b)has been confirmed from the calculation of stress-strain curves of Si crystals using these equations (Sumino and Yonenaga, 1991).

4. Immobilization of Dislocations due to Reaction with Impurities

When a dislocation originally moving under a high stress is halted under no applied stress in a Si crystal containing some kind of impurities at a high temperature where diffusion of the impurities is appreciable, it is immobilized due to the development of impurity agglomerations on it. An extra stress is necessary to start such a dislocation moving. It increases with an increase in halting duration. Such stress is termed the release stress or unlocking stress of the dislocation and is interpreted to be the stress to release the dislocation from impurity atoms segregated on the former.

Figure 4 shows the variation of the release stress for originally fresh 60 ° dislocations at 647 ℃ in CZ-Si containing oxygen impurities at various concentrations against the duration of halting at the same temperature (Sumino and Imai, 1983). No appreciable release stress is detected for dislocations in a high purity FZ-Si crystal even after a prolonged halting at high temperature. The increasing rate of the release stress increases with an increase in the concentration of oxygen impurities.

The release stress of a dislocation which is immobilized by any given heat treatment decreases as the stressing temperature is raised, reflecting the fact that the release of the immobilized dislocation is a thermally activated process.

A theoretical analysis of impurity distribution around a dislocations in thermal equilibrium has shown that an oxygen-rich or lean region (the Cottrell atmosphere) never develops around a dislocation at the typical oxygen concentration in CZ-Si is concerned. Thus, we are led to the conclusion that the immobilization of dislocations due to oxygen segregation in Si is not related to the development of the Cottrell atmosphere around dislocations. Oxygen atoms or, more generally, impurity atoms are gettered by dislocations at high temperatures by the following two mechanisms (Sumino, 1989b): (1) Impurity is supersaturated and dislocations act as preferential nucleation sites of precipitates of the impurity. (2) Some special reaction which incorporates impurity atoms from the matrix region takes place at the dislocation core. Special reaction which never takes place in the matrix region may occur at the dislocation core because of the peculiarity of atomic arrangement there. The reaction product may have a high interaction energy with the dislocation. Occurrence of such special reaction incorporating oxygen impurity at the dislocation core has indeed been observed in CZ-Si (Koguchi et al., 1982, Yonenaga and Sumino, 1985).

TEM observations have revealed that oxygen atoms gettered by a dislocation are usually not distributed uniformly in the atomic state but

discretely along the dislocation line in the form of particles. The size and separation of the particles depend on the temperature and duration of thermal treatment which the crystal experienced. The analysis of the temperature dependence of the release stress for immobilized dislocations also leads to the same picture (Sato and Sumino, 1985).

5. Conclusion

The development in semiconductor device processing technology is achieved most successfully on the basis of correct knowledge on a variety of defect properties in semiconductors.

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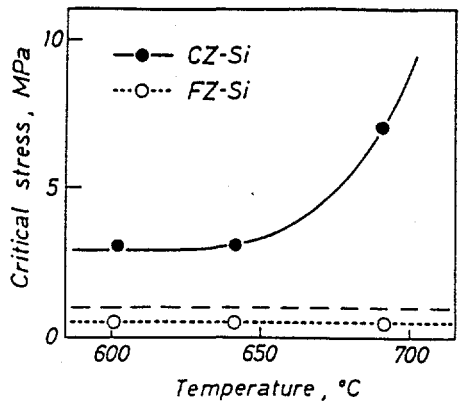

Fig. 1. Critical stress for dislocation generation from a Knoop indentation plotted against temperature in FZ-Si and CZ-Si (Sumino and Harada, 1981).

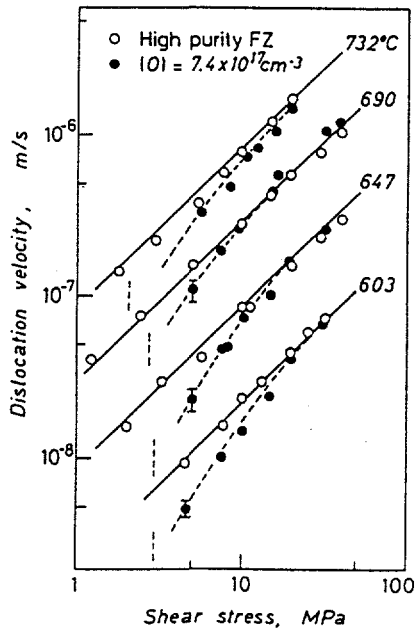

Fig. 2. Velocity versus shear stress relations of 60 ° dislocations at various temperatures in a Si crystal containing oxygen impurities at a concentration of 7.4×10^{17} atoms/cm^3. Open circles indicate the data for high purity FZ-Si (Imai and Sumino, 1983).

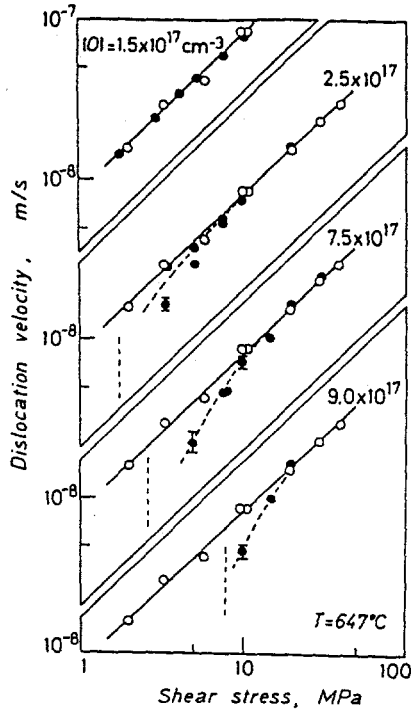

Fig. 3. Velocity versus shear stress relations at 647 ℃ of 60 ° dislocations in Si crystals containing oxygen impurities at concentrations shown in the figure. Open circles indicate the data for high purity FZ-Si (Imai and Sumino, 1983).

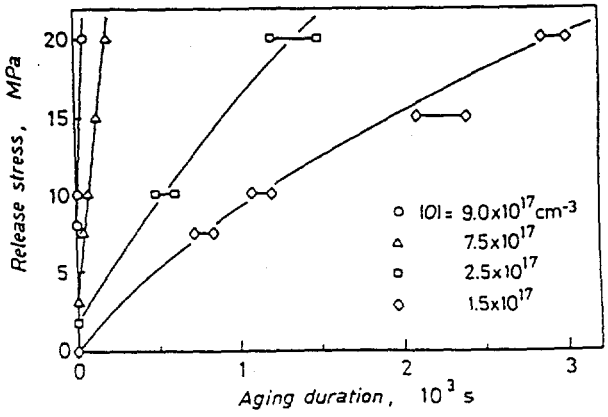

Fig. 4. Variation of the release stress at 647 ℃ for initially fresh 60 ° dislocations against the duration of aging at 647 ℃ in Si crystals containing oxygen impurities at concentrations shown in the figure (Sumino and Imai, 1983).

FUNDAMENTAL ASPECTS OF METALLIC IMPURITIES AND IMPURITY INTERACTIONS IN SILICON DURING DEVICE PROCESSING

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A review on the behavior of metallic impurities in silicon can be considerably simplified by a restriction on pure, dislocation-free, monocrystalline silicon. In this case interactions between different impurities and between impurities and grown-in lattice defects can be reduced. This restriction is observed in Chap. 1 for discussing the general behavior of metallic impurities in silicon.

The main impurities in Czochralski-grown monocrystalline silicon in the sequence of decreasing concentrations are: oxygen: 6-9 10^{17} cm^{-3}, carbon: <2 10^{15} cm^{-3}, iron, nickel, copper: <2 10^{12} cm^{-3} each, other metals: <$10^{10}$$cm^{-3}$, and low densities of precipitated oxygen. Multicrystalline and low-cost solar material exhibit more impurities and higher concentrations as well as dislocations and grain boundaries where impurities may be accumulated.

1. BEHAVIOR OF METALLIC IMPURITIES

1.1 Contamination

The first step of introducing metal impurities into silicon single crystals is the contamination taking place during the manufacturing of wafers or the subsequent processing for device production. The possibilities for metal contaminations are manifold. They can be subdivided in solid-phase, liquid-phase and vapor-phase contaminations [1].

A solid-phase contamination takes place by mechanical contacts of metals to uncoated silicon surfaces, e.g., by handling wafers, by carriers, and control measurements. The small quantity of material remaining on the silicon surface after a weak friction acts often as an inexhaustible diffusion source during subsequent high temperature processes. As a consequence the solid-phase contaminated area exhibits typically the form of streaks. The finger-prints may help to identify the contamination source.

A liquid-phase contamination takes place during any processing of uncoated wafers in liquid chemicals such as cleaning, wet etching, lapping, and polishing. After a heat treatment and a subsequent haze test the wafer exhibits typically a more or less uniform contamination on the whole

surface. For the strength of the contamination the electronegativity of the metal with respect to that of silicon (1.8) plays a major role. Especially noble metals (Cu, Ag, Au..) predominate in replating processes.

A vapor-phase contamination takes place during heat treatments, and chemical vapor deposition where metals evaporate, as well as ion implantation, and plasma etching, where impurity metals are sputtered simultaneously. After diffusion processes the marks of the boat are often contaminated, other processes exhibit, in general, less characteristic features.

1.2 Diffusivities

The second step of introducing metal impurities into silicon is a diffusion process at high temperatures. The diffusivities of metals in silicon depend strongly on the temperature applied. For different metals and a definite temperature the diffusivities vary by many orders of magnitude. The diffusivities of slowly diffusing metals (W,Ta) are comparable to those of boron and phosphorus, the diffusivities of fast diffusing metals (Ni,Cu) amount to about 10 orders of magnitude higher values [1] and enable even a minor diffusion at room temperature. The differences in the diffusivities are important for a sample preparation to detect and distinguish different impurities. Fast diffusion takes place via an interstitial mechanism whereas a substitutional diffusion via vacancies (Frank-Turnbull) or self-interstitials (kick-out mechanism) is slowlier. Several metals which form interstitial and substitutional defects diffuse via both mechanisms exhibiting different diffusivities (Ni,Cu,Pd,Pt,Au). Diffusivities can be enhanced by the presence of lattice defects which can be important for solar material.

1.3 Solubilities

The solubility is the highest concentration of an impurity in a matrix when the in-diffusion equals the out-diffusion at the boundaries of the sample after reaching thermal equilibrium. This requires an inexhaustible, unchanged diffusion source. However, at elevated temperatures metals form silicides when coming in contact with uncoated silicon. The common high temperature modification is $MeSi_2$ (Me=metal) which then acts as a diffusion source. The solubilities published in the literature were measured with the respective stable silice at the sample surface which is, in general, not mentioned. The concentration of metallic iron after a short diffusion time exceeds by far its solubility as long as the iron has not completely changed to silicide.

The solubilities exhibit a strong temperature depen-

dence with increasing values for increasing temperatures as reported for the diffusivities. In contrast to the diffusivities all solubilities almost vanish at room temperature. As a consequence, dissolved metals are unstable at room temperature, although they often can be detected. In these cases the dissolved metals are supersaturated frozen-in. The respective diffusivity was not high enough to reach thermal equilibrium during the fast cooling process.

There are several possibilities to overcome the instability due to the supersaturation in the sequence of increasing diffusivities with respect to the cooling rate:

(i) the metals remain dissolved and form deep energy levels in the band gap of silicon. They tend to change their state if possible

(ii) the metals diffuse to the next surface, precipitate as silicides and form denuded zones beneath the surfaces. The precipitates are revealed as haze by etching

(iii) the metals precipitate in the bulk of the sample by a homogeneous nucleation mechanism.

Different kinds of defects can be present in one sample. The precipitation of metallic impurities is favoured by foreign nucleation points since a heterogeneous nucleation mechanism is favoured compared to a homogeneous nucleation mechanism, which is the principle of "precipitation" [1] or "relaxation gettering" [2].

2. IMPURITY INTERACTIONS

The dissolved metallic impurities can cause several chemical reactions even at room temperature. The main compounds observed in contaminated silicon are pairs.

2.1 Donor-Acceptor Pairs

The donor-acceptor pairs are the most famous compounds between two different impurities observed after a moderately fast cooling of the sample from high temperatures. Since iron belongs to the main impurities in silicon FeB pairs are common in p-type silicon. All interstitial defects of the transition metals form at least one deep donor state in the band gap of silicon. In general, the Fermi-level at room temperature is situated between the deep donor state of the impurity and the shallow acceptor state of the dopant. Therefore, the donor will be positively charged and the acceptor negatively. If the interstitial iron atom diffuses to the almost immobile substitutional boron a pair is formed by an electrostatic attraction. The iron atom in FeB pairs occupies an interstitial place next to the boron atom

and the pair is oriented in [111]-direction. For pairing with Al, Ga, and In two different structures are formed in [111]- and in [100]-direction. All pairs are electrically active and the donor state is situated between the donor of the metal and the acceptor of the dopant. The donor state of the metal can also be situated in the upper half of the silicon band gap (Cr).

Besides the shallow acceptors of the dopants also deep acceptor states of substitutional metallic impurities (Zn, Au) can form donor-acceptor pairs. The most common is FeAu since gold can be easily introduced by a cross contamination. This pair forms a donor state in the upper half of the silicon band gap and an acceptor state in the lower half and acts as a strong lifetime killer. Consequently, the wide-spread iron impurity can be found in different defects in p-type silicon such as interstitial iron, FeB pairs, FeAl pairs, and FeAu pairs. In order to determine the total iron content the concentrations of all defects must be summed up.

2.2 Other Impurity Compounds

There are still many other unidentified compounds observed after an intentional contamination of silicon with metals. In general, their composition and structures are unknown and their energy levels are only correlated to the respective metal introduced intentionally.

Besides compounds of impurities those of impurities and lattice defects have been investigated, especially radiation-induced defects exhibiting various combinations with vacancies and selfinterstitials. In general, radiation-induced defects are formed by impurities of high concentrations such as oxygen, carbon, and dopants, metals are rarely found because of their low concentrations.

3. IMPACT ON DEVICE PERFORMANCE

The impact on device performance of dissolved and precipitated metallic impurities must be discussed separately because of their different electrical properties.

3.1 Dissolved Metal Impurities

After applying common temperature processes for device production with low cooling rates only substitutional defects (Au) and few interstitial defects of slowly diffusing metals (Ti) can be observed in processed silicon. After applying at least moderately fast cooling processes interstitial iron can be kept dissolved.

Dissolved metals can affect the carrier concentration due to their electrical activity if their concentration is sufficiently high. However, they mainly reduce the minority carrier lifetime, which is a function of the defect concentration and the minority-carrier capture cross-section of the respective defect for low injection level measurements. The injection level is the concentration of excess carriers generated during sample illumination in relation to the dark carrier concentration. The carrier lifetime at higher injection levels depends on the relation between the capture cross-sections for electrons and holes. The capture cross-sections of different defects vary by many orders of magnitude and they also differ for electrons and holes, in general. Therefore, the injection dependence of the minority carrier lifetime of different defects vary considerably, showing a more or less steep increase of the lifetime with increasing injection level.

Interstitial iron in p-type silicon causes a strong increase of the lifetime with increasing injection. FeB pairs, on the other hand, exhibit only a weak injection dependence. Both cross at medium high injections. A degradation of the low-level carrier lifetime can be observed after a strong illumination of the sample since the FeB pairs can be splitted by an intense illumination [3]. The degradation is reversible because the pairs regenerate with the time elapsed after switching off the illumination.

3.2 Precipitated Metal Impurities

In contrast to the dissolved metals the precipitates exhibit a vanishing electrical activity due to their much lower concentration. Nevertheless, they reduce the carrier lifetime if their density is sufficiently high. A quantitative relationship between the minority-carrier diffusion length L and the density N of $NiSi_2$ precipitates was deduced recently from experiments [4]:

$$L = 0.7 / N^{1/3}$$

The reduction in carrier lifetime is almost independent of the chemical nature of the precipitates as could be shown recently by a simultaneous diffusion of various metals in one sample. Because of the dependence on the density of precipitates the cooling rate after the last temperature process is important for the lifetime reduction: low cooling rates yield higher lifetimes.

Furthermore, precipitates in the space charge region of a pn-junction cause enhanced reverse currents and soft reverse current-voltage characteristics, which is a typical indication for the presence of precipitates.

4. ANALYSIS AND CONTROL OF METAL CONTAMINATION

For the detection and analysis of metal impurities particular problems arise due to low concentrations and different kinds of defects combined with strong inhomogeneities in lateral and depth distribution. An universal method is not available therefore several different techniques must be applied to detect the various kinds of contaminations: surface contamination, total metal content, dissolved metals, and precipitated metals.

4.1 Surface Contamination

Total Reflection X-Ray Fluorescence Analysis (TXRF) has proved as the best modern technique so far. Its sensitivity can be considerably enhanced by the Vapor Phase Decomposition (VPD) which concentrates the impurities of the whole sample surface in a droplet at the expense of a lateral resolution.

4.2 Total Contamination

Neutron Activation Analysis (NAA) and Atomic Absorption Spectroscopy (AAS) have been widely used in the past. Both methods require a sophisticated sample preparation. Their sensitivities vary considerably for different metals. Both techniques are time consuming, expensive, and therefore not suitable to accomplish the requirements of modern analysis technology.

4.3 Dissolved Metals

Deep Level Transient Spectroscopy (DLTS) offers a high sensitivity for electrically active impurities. Together with the sample preparation a temperature scan requires one hour and yields results only on few mm^2 of the sample surface. Therefore the technique is not suitable for routine measurements.

Carrier Lifetime and Diffusion Length measurements are most suited for routine control due to their extremely short measurement times of ms. They also allow to record mappings of the whole wafer surface. However, the carrier lifetime is a cumulative parameter and the chemical nature of the impurities and their concentrations cannot be directly determined. Reciprocal partial lifetimes of different impurities sum up and even precipitates can reduce lifetimes if present in high densities.

In spite of these disadvantages lifetime measurements can be applied to determine the iron content in monocrystalline silicon due to the limited number of impurities:

Fe, Ni, and Cu. A suitable sample preparation keeps iron dissolved whereas Ni and Cu impurities precipitate quantitatively. In general, the densities of the precipitates are too low to be detected by lifetime measurements at least in p-type silicon where iron and FeB pairs are strong lifetime killers and hence predominate. In this case the carrier lifetime can be calibrated versus the iron content measured by DLTS in the same area. Samples of different iron content are used for calibration, pairing of iron should be completed, and equal injection levels should be applied in order to obtain reproduceable results. After calibration the iron concentration of a sample can be deduced from measured lifetimes.

A final problem arises from the Surface Recombination Velocity (SRV) which strongly affects the lifetime measured in thin samples. It must be reduced as far as possible to achieve real bulk lifetimes. Common but insufficient techniques for its reduction is an immersion of the sample during measurement in liquids such as HF or a iodine solution in ethanol. Widely used is a preceding thermal oxidation of the wafer which is especially effective on (100)-oriented silicon wafers. However, an oxidation in a contaminated furnace tube yields an additional contamination of the wafer, and an oxidation in a pure tube reduces the iron content in the bulk due to gettering of iron in oxide layers. The sample preparation should not change the parameter to be measured.

Two improved techniques to reduce the SRV have been developed recently:

(1) the first is based on a thermal oxidation and the results are improved by applying an additional corona charging of both oxidised surfaces. Best results (SRV<1 cm/s) were obtained by using a polarity which rejects the minority carriers from the surface [5].

(2) the other is based on chemical passivation of the surfaces. Instead of liquids a varnish composed of colophony dissolved in 2-propanol with an addition of 10% of iodine is used. The coating is obtained by painting, spraying, or dipping in the liquid varnish. Lifetimes are measured after a short drying period. This technique yields best results compared to the alternatives. Due to a room temperature preparation the lifetime is not effected. A deficiency is the degradation with extended storing times which avoids sequent recordings of many lifetime mappings [6].

4.4 Precipitated Metals

The Haze Test seems to be the only technique which enables a sensitive detection of precipitates at the sample surface and their lateral distribution. It requires a sample preparation as needed for lifetime measurements. There-

fore it can be performed on the same sample by adding a preferential etching process. Its sensitivity is sufficient to accomplish the requirements of modern technology if an improved etch solution is applied which has been published recently [7]. The new etch, free of dangerous CrO_3, is based on selected mixtures of nitric, hydrofluoric, and acetic acid. It was developed for improving the sensitivity in revealing haze on (111) and (100)-oriented silicon wafers. Applying two different mixtures the etch distinguishes copper from nickel haze. After etching the strength of haze can be determined quantitatively by measuring optically the scattering of light or by measuring light point densities by means of modern laser scanning methods.

5. CONCLUSION

The paper presents a brief review on the fundamental aspects of metal impurities in monocrystalline silicon combined with selected techniques for analysis and control required for a successful defect engineering. For multicrystalline silicon the behavior of metallic impurities and their detection becomes still more complicated. Several solubilities and diffusivities may change due to high dislocation densities. More impurities and higher concentrations are expected. The distribution of the impurities and the minority carrier diffusion lengths are considerably affected by the presence of grain boundaries. Gettering to reduce dissolved metallic impurities is still more important. But problems arise even here since internal gettering cannot be applied for solar cells which require high lifetimes in the whole volume of the device.

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Basic research challenges in crystalline silicon photovoltaics

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Silicon is abundant, non-toxic and has an ideal band gap for photovoltaic energy conversion. Experimental world record cells of 24 % conversion efficiency with around 300 μm thickness are only 4 % (absolute) efficiency points [1] below the theoretical Auger recombination- limit of around 28 %. Compared with other photovoltaic materials, crystalline silicon has only very few disadvantages. The handicap of weak light absorbance may be mastered by clever optical designs. Single crystalline cells of only 48 μm thickness showed 17.3 % efficiency even without backside reflectors [2]. A technology of solar cells from polycrystalline Si films on foreign substrates arises at the horizon [3]. However, the disadvantageous, strong activity of grain boundaries in Si could be an insurmountable hurdle for a cost-effective, terrestrial photovoltaics based on polycrystalline Si on foreign substrates. This talk discusses some basic research challenges related to a Si based photovoltaics.

Grain Boundaries in Si: The best solar cells from coarse-grained polycrystalline Si are about 6 % lower in efficiency than cells from float zone Si, and about 3 % lower than devices from Czochralski-grown Si. This efficiency reduction stems from recombination at inter- and intra-grain defects in the (usually cast) polycrystalline Si. Despite long lasting research efforts on the microscopic origin of the electrical activity of dislocations and grain boundaries in Si, there is still no complete understanding. Clear correlations between crystallography and electronic activity have not been revealed. As a consequence, only rules of thumb such as to use large-grained material, to avoid oxygen and carbon, transition metal contamination, and to use hydrogen passivation can be given to processing technologists. Here, the lower activity of grain boundaries in epitaxially grown material [3] promises further understanding the origin of grain boundary charges. The concept of 'intrinsic physical passivation' needs detailed investigations.

Auger Generation: For ultra violet light, crystalline Si cells show internal carrier multiplication by optically induced impact ionization [4]. Effective use of this effect would allow for a drastic efficiency increase of solar cells [5]. However, the onset of Auger generation must be shifted into the wavelength regime of the visible light. The compound $Si_{1-x}Ge_x$ seems promising, but experimental data are not available yet. Here, not only experimentalists but also theorists are challenged in order to tailor an optimal band structure for new photovoltaic materials that make use of the combined effects of strong light absorption and subsequent internal carrier multiplication.

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DOPANT AND CARRIER CONCENTRATION IN SILICON, IN EQUILIBRIUM WITH SiP PRECIPITATES

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The methods recently reported to study the equilibria in the Si-As system (1), were extended to the Si-P. On this line the behaviour of Silicon slices very heavily implanted with 1.5×10^{17} P^+/cm^2, was followed by transmission electron microscopy (TEM) and secondary neutral mass spectrometry (SNMS) after annealing at 800, 850, 900 and 1000 C.

Precipitation of large monoclinic, and partially orthorhombic, SiP takes place in the most heavily doped region. From the shape of the SNMS profiles in the dissolution stage of these precipitates, we determined for the first time, the concentration C_e of P in equilibrium with the conjugate phase: $C_e = 2.45 \times 10^{23} \exp(-0.62/kT)$ cm^{-3}, were kT is in eV.

This concentration has to be compared with the saturation concentration n_e of electrically active dopant after equilibration annealing. To this end new and more accurate determinations of n_e were performed on heavily doped silicon films. It was found that: $n_e = 1.3 \times 10^{22} \exp(-0.37/kT)$ cm^{-3}. Hence, for T > 750 C, C_e exceeds n_e and the concentration of inactive mobile P increases with temperature. The profiles in Fig, 1 are representative of the equilibria at 1000 C.

In the regions downstream of the large precipitates, i.e. for dopant concentrations below C_e, TEM provides evidence of particles, whose diameter can attain 10 nm. They are shown in Fig. 2, a cross sectional weak beam dark field micrograph taken in a sample annealed 3 hours at 900 C, and are similar to the ones which we reported in previous papers.

To account for the diffusion behaviour of the inactive mobile dopant these particles, in spite of their size, must be in a mass action equilibrium with the ionized P. This equilibrium should strongly depend on the concentration of P ions; in fact we reported evidence that, as it is also shown in Fig. l, n_e is fairly insensitive to the excess dopant.

These findings, which underline the similarities between the inactive As and P, put in a new perspective the results of our previous analysis and lead to conclude that the inactive mobile dopant results from an aggregation phenomenon which closely precedes the phase transition, i.e. a preprecipitation process. Unusual features of this phenomenon are its amplitude and the size of the aggregates as shown in Fig. 2.

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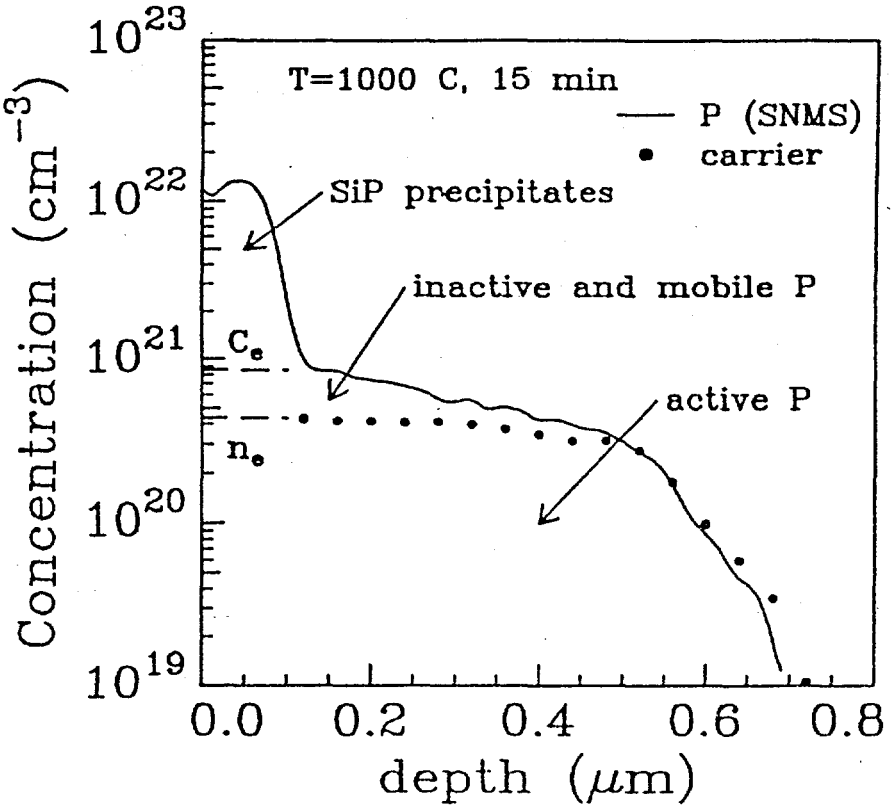

Fig. 1.

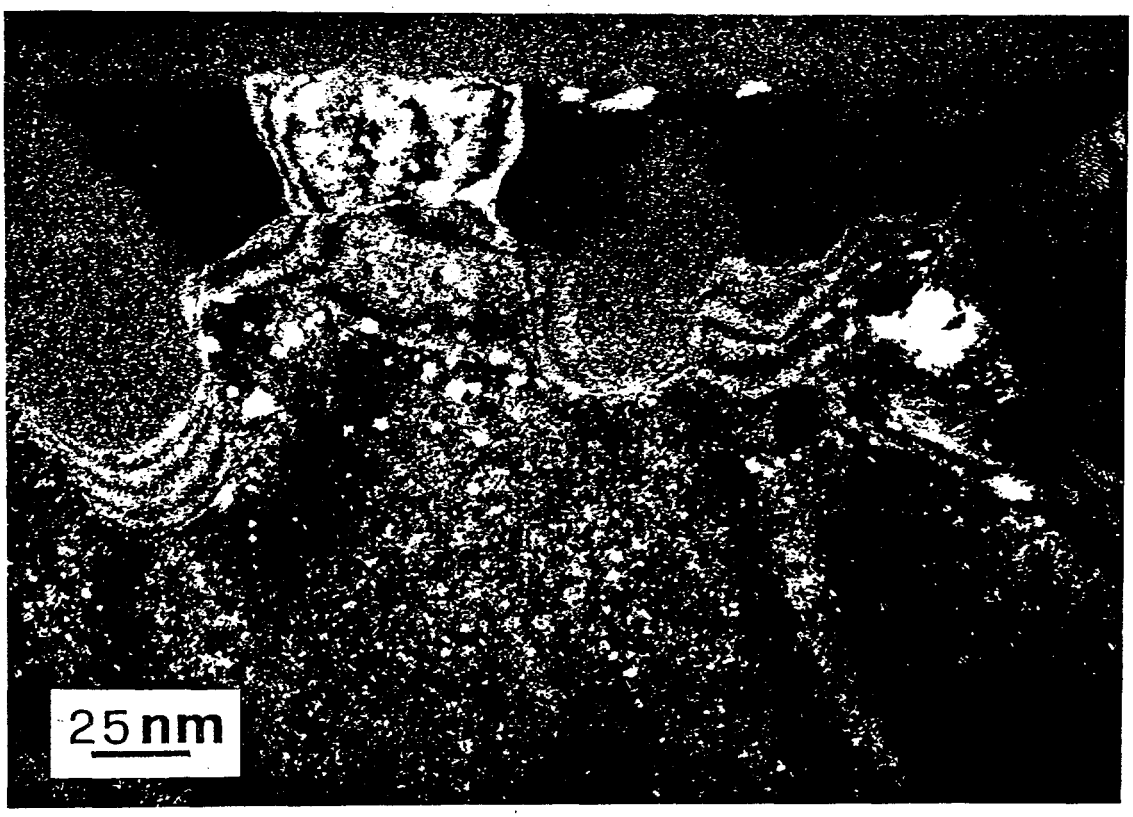

Fig. 2. Small particles showing Moiré fringes between large, out of contrast, SiP precipitates.

The Structure and Bonding of Iron-Acceptor Pairs in Silicon

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Key words: transition metal, iron-acceptor pairs, ionic model, polarization

ABSTRACT

The highly mobile interstitial iron and Group III impurities (B, Al, Ga, In) form iron-acceptor pairs in silicon. Based on the migration kinetics and taking host silicon as a dielectric medium, we have simulated the pairing process in a static silicon lattice. Different from the conventional point charge ionic model, our phenomenological calculations include (i) a correction that takes into account valence electron cloud polarization which adds a short range, attractive interaction in the iron-acceptor pair bonding; and (ii) silicon lattice relaxation due to the atomic size difference which causes a local strain field. Our model explains qualitatively (i) trends among the iron-acceptor pairs revealing an increase of the electronic state hole emission energy with increasing principal quantum number of acceptor and decreasing pair separation distance; and (ii) the stable and metastable sites and configurational symmetries of the iron-acceptor pairs. The iron-acceptor pairing and bonding mechanism is also discussed.

INTRODUCTION

Contamination by transition metal (TM-3d) impurities is a major concern in the processing of silicon photovoltaic (PV) devices. It has been found that the highly mobile interstitial TM-3d forms complex pairs with both shallow and deep acceptors[1]. In particular, iron and Group III impurities (B, Al, Ga, In) form electrically active iron-acceptor pairs in silicon which bring a detrimental effect on PV device performance. The iron-acceptor pairs in silicon have been extensively studied by the electron paramagnetic resonance (EPR)[1-5] and deep level transient spectroscopy (DLTS)[6-15] experiments, showing that the pairs have both the ⟨111⟩ (Fe-B,-Al,-Ga,-In) and ⟨100⟩ (Fe-Al,-Ga,-In) configurational symmetries with different deep levels in the

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bandgap. It is assumed that the pairs may consist of a substitutional acceptor with an iron either placed at the nearest-neighbor ($\langle 111 \rangle$) or next-nearest-neighbor interstitial site ($\langle 100 \rangle$). An ionic microscopic model for iron-acceptor pairs was also suggested by the EPR experiment[1]. According to the ionic model the pairs are formed by an interstitial positively charged iron and a substitutional negatively charged acceptor. The DLTS experiments[11, 13] show that electrostatic interaction plays a fundamental role in the iron-acceptor pairing. However, the bonding mechanism of a stable pair is still unclear. Theoretical electronic structure calculations show the importance of covalency in pair bonding[16]. The trend among the iron-acceptor pair deep levels have also been investigated[12, 13] and reveal a deeper location in the bandgap with increasing acceptor size.

Following the previous work[17], and considering the effects due to valence electron cloud polarization and lattice relaxation due to atomic size difference, we study the structure and bonding of iron-acceptor pairs. Different from the point charge ionic model, a short range attractive component is added to point charge Coulomb interaction in order to take into account valence electron cloud polarization. Comparing to silicon atom size, larger acceptor relax outward and smaller acceptor relax inward their neighbors. This lattice relaxation effect is approximated by adjusting the four silicon atom sites, adjacent to the acceptor, leading the silicon-acceptor bond length to $r_{\rm cov}({\rm A}) + r_{\rm cov}({\rm Si})$. The repulsive interaction for iron-acceptor and iron-silicon is still approximated by the softened repulsive Lennard-Jones type potential[17], and silicon crystal is treated as a dielectric medium.

RESULTS AND DISCUSSION

The potential contours in a (100)-plane for Fe_i^+ are shown in Fig.1. Figs.1(a) and 1(c) show that Fe_iB_s and Fe_iIn_s pairs display $\langle 111 \rangle$ and $\langle 100 \rangle$ symmetries, respectively, in their stable configurations as observed by EPR. The potential curves along $\langle 111 \rangle$ and $\langle 100 \rangle$ directions for Fe_i^0, Fe_i^+ and Fe_i^{++} are shown in Fig.2. Our calculations predict $\langle 111 \rangle$ symmetry for stable $Fe_i^+Al_s^-$, $Fe_i^+Ga_s^-$, and metastable $Fe_i^+In_s^-$ pairs. In addition, our results show that $\langle 100 \rangle$ symmetry can be assigned to metastable Fe_iB_s, Fe_iAl_s and Fe_iGa_s pairs. Our predictions for the configurational structures and bistability are in good agreement with the EPR and DLTS observations, except for Fe_iB_s pair in $\langle 100 \rangle$ symmetry which has not been detected in the experiments. The structure and bistability behaviors of Fe_i^0 and Fe_i^{++} related pairs remain the same as that of Fe_i^+, except that stable $(Fe_i^0Ga_s^-)^-$ pair shows $\langle 100 \rangle$ symmetry. The different structural behavior displayed by the Fe_iIn_s pair is mainly attributed to the large repulsive potential between In_s and Fe_i.

We evaluated energy positions of iron-acceptor pairs from Eq.(4) and list the results in Table 1, where the experimental data and calculated results from the point charge ionic model are also shown. The polarization model with lattice relaxation gives the correct trends of the energy positions for the first neighbor ($E_T(1)$) and the second neighbor ($E_T(2)$) pairs with increasing acceptor size and decreasing pair separation distance as observed in the experiments, while the point charge ionic model gives an opposite trend with increasing acceptor size. According to our model, repulsive energy from the acceptor should give a maximum contribution at the first neighbor site (T1) and yield the greatest variation in defect energy levels. This is consistent with the experimental observations that $E_T(1)$ displays the greatest sensitivity to acceptor atom identity and $E_T(2)$ shows relative uniformity. The binding energy reflects the energy variation of the interstitial iron in a pair from remote sites to the stable configuration. The binding

energy data are shown in Table 2. The point charge model predicts a trend of monotonical decreasing with increasing acceptor size for both charge states of iron. The increase in binding energy due to valence electron cloud polarization compete with the repulsive potential so that the polarization model gives near constant binding energies for both charge states of iron.

The success of the polarization model in predicting pair structures and donor charge transition energy positions seems to confirm the existence of a short range attractive component in the iron-acceptor interaction at near neighbors. However, the deviations at $E_T(1)$ between the measured and calculated data, especially for Fe_iB_s pair, imply that other interaction mechanism may also exist in the pair bonding. The reasons for these deviations could come from the limitations of the ionic models (point charge and polarization) at near neighbors. First, the bulk host medium dielectric screening assumption at near neighbors is handwaving. The bulk dielectric constant may still be a valid description for the space between the second neighbor site (T2) and substitutional acceptor, since T2 has four silicon neighbors which do not include the acceptor. However, at T1, the screening, if any, can hardly be effectively described by the bulk dielectric constant, since one of the iron first neighbors is an acceptor atom. Second, charge transfer concept is ambiguous for the nearest neighbor pairs, sharing of common electrons between atoms (interstitial iron, substitutional acceptor and silicon atoms), especially between iron and acceptor, occurs. Therefore, covalency involving iron, acceptor and surrounding silicon atoms may also play an important role in the bonding of stable iron-acceptor pairs. The evaluation on covalency has not been included in our classical model.

CONCLUSIONS

The long range electrostatic interaction between interstitial iron and acceptor is the driving force for the iron-acceptor pairing. Based on the migration kinetics, taking host silicon as a dielectric medium, considering valence electron cloud polarization and lattice relaxation due to atomic size difference, we have qualitatively explained: (i) trends among the iron-acceptor pairs revealing an increase of the electronic state hole emission energy with increasing principal quantum number of acceptor and decreasing pair separation distance; and (ii) the stable and metastable sites and configurational symmetries of the iron-acceptor pairs. According to our phenomenological model, the iron-acceptor pairing and bonding mechanism can be characterized as: the point charge interaction for remote sites; the point charge interaction plus valence electron cloud polarization correction for near neighbors; and the covalent interaction for the nearest neighbors. One should keep it in mind that our calculations in this work are from classical discussion, the complete understanding of electronic state energy levels and covalency in pair bonding, especially at the nearest neighbors, should be given by the first-principles dynamic simulations.

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(a) Si:B_s:Fe_i (b) Si:Fe_i (c) Si:In_s:Fe_i

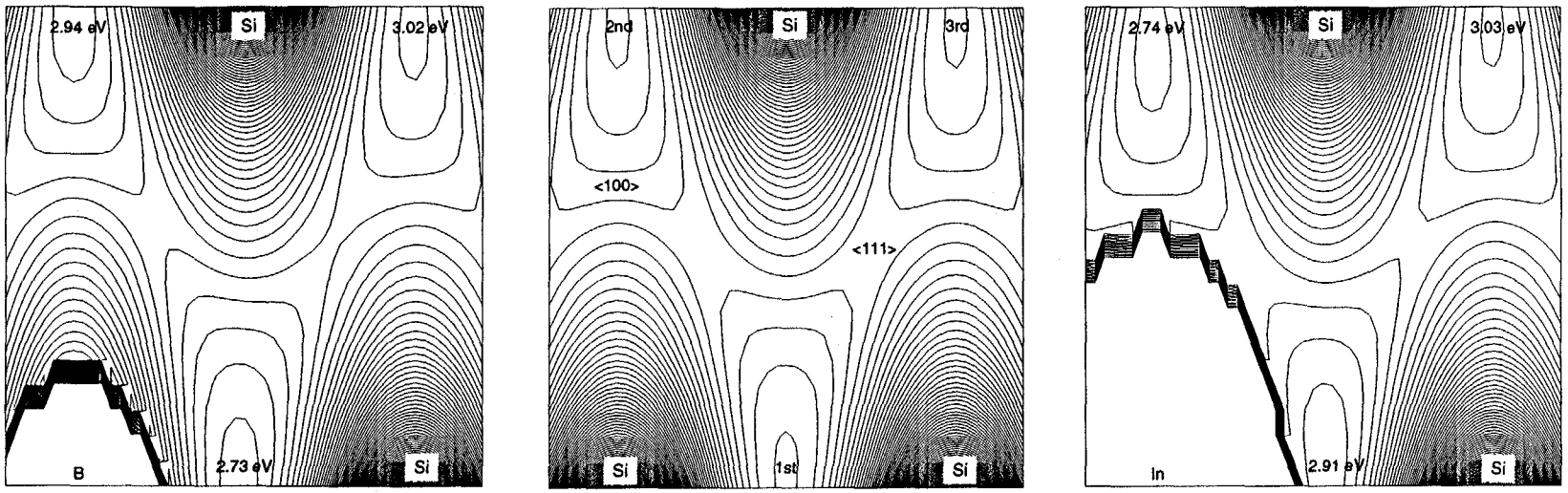

Fig. 1 The potential contours in a (100)-plane for Fe_i in silicon lattice. B_s, Si and In_s are placed on the lattice site at the lower left corner of (a), (b) and (c), respectively. (a) The Fe_iB_s pair has the lowest potential at the first neighbor interstitial site, shows <111> symmetry; (c) The Fe_iIn_s pair has the lowest potential at the second neighbor interstitial site, shows <100> symmetry.

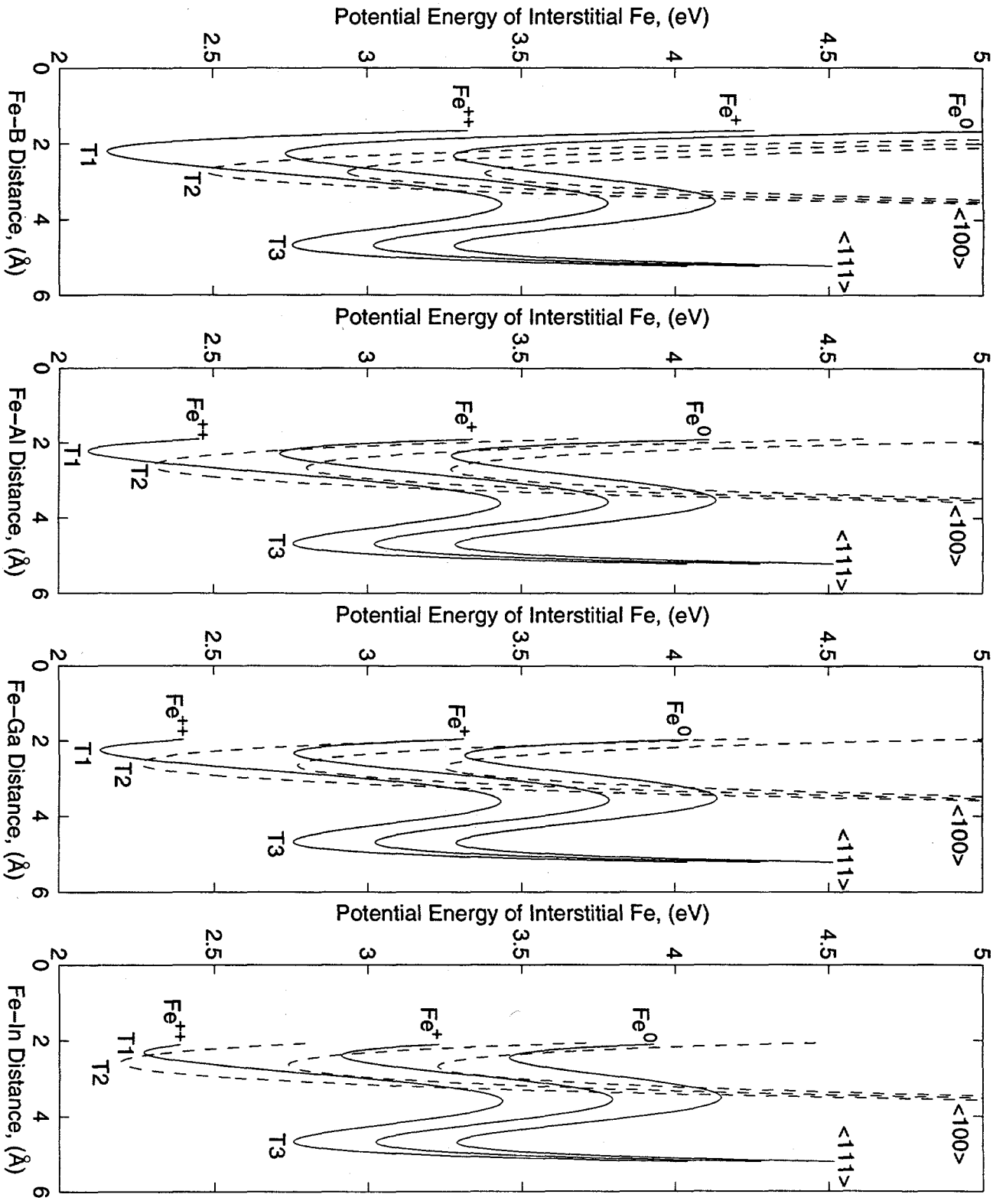

Fig.2 The role of Fe charge state on the pair configurational symmetry and stability

Table 1 Energy Positions for the First, $E_T(1)$, and Second, $E_T(2)$, Neighbors

Acceptor	$\frac{R_{cov}(A)}{R_{cov}(Si)}$	(I) Energy Positions of $[(Fe_i^+A_s^-)^0/(Fe_i^{++}A_s^-)^+]$					
		Measured [eV] [11, 12, 13]		Point Charge Model [eV] (no lattice relaxation)		Polarization Model [eV] (with lattice relaxation)	
		$E_T(1)$	$E_T(2)$	$E_T(1)$	$E_T(2)$	$E_T(1)$	$E_T(2)$
B	0.74	0.10	–	0.25	0.14	0.21	0.09
Al	1.01	0.20	0.13	0.20	0.13	0.25	0.13
Ga	1.08	0.23	0.14	0.19	0.125	0.26	0.14
In	1.23	0.27	0.15	0.17	0.12	0.27	0.17

Acceptor	$\frac{R_{cov}(A)}{R_{cov}(Si)}$	(II) Energy Positions of $[(Fe_i^0A_s^-)^-/(Fe_i^+A_s^-)^0]$					
		Measured [eV] [8, 9]		Point Charge Model [eV] (no lattice relaxation)		Polarization Model [eV] (with lattice relaxation)	
		$E_T(1)$	$E_T(2)$	$E_T(1)$	$E_T(2)$	$E_T(1)$	$E_T(2)$
B	0.74	0.83	–	0.82	0.61	0.75	0.54
Al	1.01	–	–	0.73	0.59	0.81	0.60
Ga	1.08	–	–	0.71	0.58	0.81	0.62
In	1.23	–	–	0.66	0.56	0.82	0.66

Table 2 Binding Energies for Stable Donor-Acceptor Pairs in Silicon

$(D_i^{+/++}A_s^-)$ Pairs	Measured E_b [eV]	Point Charge Model (no lattice relaxation) E_b [eV]	Polarization Model (with lattice relaxation) E_b [eV]
$(Fe_i^+B_s^-)$	0.65 ± 0.02 [11]	0.89	0.56
$(Fe_i^{++}B_s^-)$	–	1.47	1.13
$(Fe_i^+Al_s^-)$	0.47 [12]	0.52	0.58
$(Fe_i^{++}Al_s^-)$	0.99 [12]	1.05	1.19
$(Fe_i^+Ga_s^-)$	–	0.41	0.53
$(Fe_i^{++}Ga_s^-)$	–	0.93	1.16
$(Fe_i^+In_s^-)$	–	0.29	0.55
$(Fe_i^{++}In_s^-)$	–	0.74	1.09
$(Li_i^+B_s^-)$	0.43 [18, 19]	–	–
$(Li_i^+Al_s^-)$	0.51 [19]	–	–

MICRODEFECTS IN CAST MULTICRYSTALLINE SILICON

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Abstract

The microdefect etching behaviour of cast multicrystalline BAYSIX and SILSO samples is mainly the same as that of EFG silicon, in spite of the very different growth parameters applied to these two techniques and the different carbon contents of the investigated materials. Intentional decorating of mc silicon with copper, iron and gold did not influence the results of etching and with help of infrared transmission microscopy no metal precipitates at the assumed microdefects could be established. There are many open questions concerning the origin of the assumed, not yet doubtless proved microdefects.

Introduction

Recently some investigations about the presence of microdefects in EFG silicon were published. Shallow saucer-like etch pits were found which could be clearly distinguished from the dislocation etch pits by pit size and shape [1,2]. These etch pits, attributed to microdefects, are inhomogeneously distributed and may attain densities in excess of 10^8 cm^{-2}. A decrease of the pit density may be visible within a region of 5...10 µm of the grain boundaries. A model for the microdefect generation is proposed which considers the formation of carbon-related and vacancy-based microdefects in the as-grown EFG silicon lattice, comparable with the B- and D- (swirl-) defects in FZ silicon.

An indirect evidence of the existence of microdefects was obtained by the intentional contamination of EFG ribbon material with iron at high temperature [3]. The precipitation rate of the iron is much greater than can be explained by the dislocation densities in different grains. The results of the experiments indicate that a high concentration of hitherto unidentified defects exists in EFG material, which act as nucleation sites for iron precipitation. This fact and the presence of shallow saucer-like etch pits within dislocation-free grains led to the conclusion that the iron precipitation in EFG silicon is dominated by the presence of intragrain defects or microdefects. Because of the high carbon concentration in EFG silicon the defects are believed to be (similar to FZ silicon) B-swirl-like defects, but no evidence of such defects was found.

Impurity decoration of defects in FZ silicon containing swirl defects and EFG polycrystalline silicon via the chemomechanical polishing was investigated by [4]. With help of EBIC it was found that swirl defects are electrically inactive without chemomechanical polishing. In polycrystalline silicon a homogeneous precipitation of the polishing impurity (copper) was observed in a thin surface region which only occurs with a low temperature copper injection process such as chemomechanical polishing. "Clean" polishing was accomplished with diamond/Al_2O_3 mechanical polishing. Swirl defects in intentioinally copper decorated FZ samples showed the same behaviour as with chemomechanical polishing, in

contrast with EFG samples, where the precipitation of electrically active points did not occur. This fact suggests that there is no indication of a microdefect acting as a preferable nucleation site for inpurities in the EFG polysilicon.

The techniques of edge-defined film-fed growth (EFG) and and ingot casting are quite different in growth speed, interface temperature gradient, interface cooling rate and carbon content. There is to be expected that the recommended mechanisms of (swirl-like) microdefect formation [5,6] will act in a different manner which may result in the generation of different microdefects with different sizes and concentrations. Cast multicrystalline samples of Wacker-SILSO and Bayer-BAYSIX were investigated to draw comparisons between the materials grown by the two growth techniques mentioned above.

Experimental

50 x 50 mm^2 wafers of SILSO and BAYSIX, cut from variable ingot positions, were investigated in different ways:

1. In order to find an etching method which reveals both dislocation and microdefect etch pits with little dependence from the crystallite orientation, SECCO-, SIRTL- and WRIGHT-etchants were applied to chemomechanical polished wafers. The best results were obtained with the solution after WRIGHT.
2. Prior to the polishing a fraction of the samples were intentionally decorated with copper, iron and gold, either to find influences of these metals on the etching behaviour or to subject them to infrared transmission microscopy after optical polishing on both sides.
3. Another fraction of the samples, as grown or decorated, were polished by means of a "clean" mechanical polishing with diamond and Al_2O_3.
4. Instead of mechanical polishing, chemomechanical polished wafers, as grown and decorated, were additionally chemically polished with $HF:HNO_3$ = 1:4. In this way the surface layer was removed by 10 to 50 µm. After this procedure the defect etching was carried out in the same way as mentioned above (1.).

The optical investigation of the etched samples was done with a modern optical microscope by using the Nomarski interference and the infrared transmission modes. For counting etch pits a digital image analyser was applied.

Because of the fact, that the grains within the wafers show a different etching behaviour, more than 200 single grains of two wafers as grown were crystallographically oriented after the ECP/SACP method with a scanning electron microscope. These wafers were etched with WRIGHT in the same way after chemomechanical polishing.

Results and discussion

Chemomechanically polished samples of BAYSIX and SILSO as grown show the same etching behaviour as EFG silicon: A high percentage of the crystallites contains saucer-like shallow etch pits with concentrations up to $>10^7$ cm^{-2}. The sizes of the pits after 4 min WRIGHT-etching amount to 1 µm on average. Grains with dislocations and saucer-like pits are existing close to grains containing dislocations or saucer-like pits exclusively or grains being completely free of any etch pits. Denuded zones of saucer-like pit densities, expected near grain boundaries and extended defects such as dislocations, dislocation agglomerates and small angle

grain boundaries, may be observed in isolated cases, preferably near some grain boundaries. The width of these zones amounts to 5...20 µm. In the vast mayority of the crystallites the etch pits are distributed nearly homogeneously within the grains inclusive of the areas close to the extended defects.

Intentional copper or iron diffusion (decoration) improves the etching with WRIGHT in such a manner that the microdefect etch pits become more markedly. Another difference in the etching behaviour between decorated samples and wafers as grown was not established. But: An unintentional decoration (or defect activation in a not yet known manner) of the material as grown during the chemomechanical polishing process can not be excluded [4], that means, that chemomechanically polished samples are decorated or "activated" on principle.

Quite different results were obtained with multicrystalline silicon as grown, mechanically polished with diamond and Al_2O_3. On this samples no saucer-like etch pits could be observed after the same etching treatment.

On chemomechanically polished wafers, as grown or decorated with copper or iron, the number of saucer-like etch pits dcreases after an additional chemical polishing with HF/HNO_3 mixtures and becomes zero after reduction of more than 25 µm from the starting chemomechanically polished surface.

The fact, that grains absolutely free of saucer-like etch pits are situated close to crystallites with high defect concentrations gives rise to the assumption that there is a dependence of the microdefect etching on the crystallite orientation. Comparisons of the defect presence with the results of SACP-orientation did not show a correlation between the two parameters. Further works have to be done in this field.

In FZ silicon microdefects such as A-, B-defects and D-defects in pedestal grown crystals may easily be decorated with copper and gold. The decoration via the metal precipitation enlarges or widens the grown-in defects, forming starlike precipitates of e.g. copper or copper silicide which become visible with infrared transmission microscopy or Lang X-ray topography. In this way also very small "latent" B-defects down to a not known size can be proved, which were not detectable before decoration with help of etching or any other methods. In mc silicon the metals precipitate very effectively to extended defects and grain boundaries. Starlike mikrodefect-related metal precipitates could not even be proved in dislocation free crystallites. That means, that the microdefects in mc silicon, if they are present, must be much smaller than the "latent" B-defects in FZ silicon.

All these results obtained with etching and decoration agree in a remarkable manner with the results reported in [1-4], in spite of the very different growth parameters between the EFG and ingot casting methods. The growth speed in the EFG technique amounts to 2 cm min^{-2} [1,2], that is the 40...200 fold growth speed used in modern casting methods (0.01...0.05 cm min^{-1}). The carbon content in mc silicon is 5- to 10-times smaller than in EFG silicon. The application of the models proposed in [5 and 6] to the microdefect formation in mc silicon suggests that in this material carbon-related and interstitial-based mikrodefects are mainly formed, and these are B-swirl-like defects. The origin of B-defects with a growth rate below 0.05 cm min^{-1} leads to a B-swirl concentration of less than 10 defects / cm^3 without regarding the defect sizes [6]. These results were derived from the pedestal pulling of dislocation free crystals and must not be relevant to ingot casting.

In a proposed model of swirl formation in dislocation free FZ crystals [5] a detection limit for swirl defects with etching was introduced, and this was estimated to be in the order of 1000 silicon self interstitials (Si_I), precipitated to very small carbon clusters. That means, that B-defects smaller than 1000 Si_I may be present in high conzentrations but they are not detectable with any analytical methods. In this model is also included that swirl defects shrink

or disappear near dislocations and other extended defects because the self disorder (interstitials and vacancies) is gettered by these defects. This effect was stated in the growth of dislocation free FZ crystals without of restrictions.

In the casting process the multicrystalline silicon crystallizes extremely slowly. On the one hand the carbon and the self disorder have a lot of time to form precipitates which are thaught to be the microdefects discussed here, peferably insides of large grains nearly free of dislocations. On the other hand the mentioned time is long enough to allow the self disorder and also the carbon near dislocations and grain boundaries, to diffuse to the extended defects, creating microdefect free areas close to grain boundaries and dislocation agglomerates. But, if the saucer-like shallow etch pits belong to microdefects, what is rejected by [4], the latter condition is only fulfilled in the mentioned exceptions.

The fact that there is not one direct proof for the existence of microdefects in polycrystalline silicon up to now and the assumption that lifetime limiting intragranular defects are present in this material, give rise to some open questions, e.g.: In which way become latent microdefects activated by the chemomechanical polishing, in contrast to the intentional decoration? Are there correlations between the saucer-like shallow etch pits and the assumed micro defects? If no: Which kind of defect is represented by the saucer-like etch pits? To answer these and other questions further works will be done within the German project DIXSI in cooperation with the Department of Materials Science, University of California, Berkeley.

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Reduced Cu Concentration in CuAl-LPE-grown Thin Si Layers

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Cu-Al has been found to be a good solvent system to grow macroscopically smooth Si layers with thicknesses in tens of microns on cast MG-Si substrates by liquid phase epitaxy (LPE) at temperatures near 900°C [1]. This solvent system utilizes Al to ensure good wetting between the solution and substrate by removing silicon native oxides, and employs Cu to control Al doping into the layers. Isotropic growth is achieved because of a high concentration of solute silicon in the solution and the resulting microscopically rough interface.

The incorporation of Cu in the Si layers, however, was a concern since Cu is a major solution component and is generally regarded as a bad impurity for silicon devices due to its fast diffusivity and deep energy levels in the band gap. A study by Davis [2] shows that Cu will nonetheless not degrade solar cell performance until above a level of 10^{17} cm^{-3}. This threshold is expected to be even higher for thin layer silicon solar cells owing to the less stringent requirement on minority carrier diffusion length. But to ensure long term stability of solar cells, lower Cu concentrations in the thin layers are still preferred.

When grown under near equilibrium conditions from a Cu-Si melt, the silicon crystal is expected to be saturated with Cu to its solid solubility limit at the growth temperature (1.2×10^{17} cm^{-3} for 900°C). More components in the melt will somewhat change Cu incorporation about this level because of the change in free energy in the melt. During post-growth cool down, the Cu will become supersaturated and segregate to the surface or precipitate out at the defect sites.

1. Reduction of Cu Incorporation due to Presence of Al in the Liquid

With the assumption of a regular solution for the multicomponent Cu-Al-Si melt, the interaction parameters between the components have been determined [3]:

$\Omega^{l}_{SiAl}=2.430RTe, \Omega^{l}_{SiCu}=2.469RTe, \Omega^{l}_{AlCu}=-0.103RTe$

where the superscript l denotes liquid mixture, R is the gas constant, Te is the growth temperature of 1173K, and the subscripts denotes the interacting elements.

Both Ω^{l}_{SiAl} and Ω^{l}_{SiCu} are large positive numbers, so Si-Al and Si-Cu are of repulsive nature. Ω^{l}_{AlCu} is negative, however, implying an attractive interaction between Al and Cu. Therefore, Al in the melt will not only dilute Cu, but also will retain Cu in the liquid, reducing Cu incorporation as compared to Si growth from Cu-Si melt. Cu incorporation in the Si layer as a function of liquid compositions can be expressed as:

$$x^{s}_{Cu} = \left(\gamma^{s}_{Cu}\right)^{-1} \exp\left[2.469\left(x^{l}_{Si}\right)^{2} - 0.103\left(x^{l}_{Al}\right)^{2} - 0.064x^{l}_{Si}x^{l}_{Al}\right]$$

where the constant, γ^{s}_{Cu}, is the activity coefficient for Cu in solid silicon. Using 0.67Cu-0.33Si binary solution and a reported solubility of 1.2×10^{17} cm^{-3}, we found $\gamma^{s}_{Cu}\approx1.12\times10^{5}$.

This Al retaining effect on Cu is difficult to measure experimentally, since the measurable Cu concentration in the Si layer after growth is not the as-grown quantity as we will discuss next, but the same effect of Cu on Al incorporation has been confirmed.

2. Surface Segregation of Cu

Surface segregation is a redistribution of solute atoms (e.g., Cu) between the surface and bulk of a (Si) crystal from the as-grown uniform distribution until the total energy of the crystal becomes a minimum. The equilibrium surface coverage (mole fraction in the surface monolayer) x^{ϕ}_{Cu} of Cu as a function of temperature is described by the Bragg-Williams equation:

$$\frac{x^{\phi}_{Cu}}{1-x^{\phi}_{Cu}} = \frac{x^{B}_{Cu}}{1-x^{B}_{Cu}} \exp[\frac{\Delta G + 2\Omega^{s}_{SiCu}(x^{\phi}_{Cu} - x^{B}_{Cu})}{RT}]$$

where $\Delta G = (\mu^{0\phi}_{Si} - \mu^{0B}_{Si}) - (\mu^{0\phi}_{Cu} - \mu^{0B}_{Cu})$, μ's are the surface and bulk chemical potential of pure Si and pure Cu, x^{B}_{Cu} is the bulk mole fraction of Cu, and Ω^{s}_{SiCu} is the interaction parameter between Si and Cu in the solid. For the grown Si crystal, a binary Si-Cu consideration (excluding Al) leads to $\Omega^{s}_{SiCu}=12.81RTe$. Fig.1 shows x^{ϕ}_{Cu} as a function of temperature and ΔG, which clearly displays ΔG as the driving force for the surface segregation.

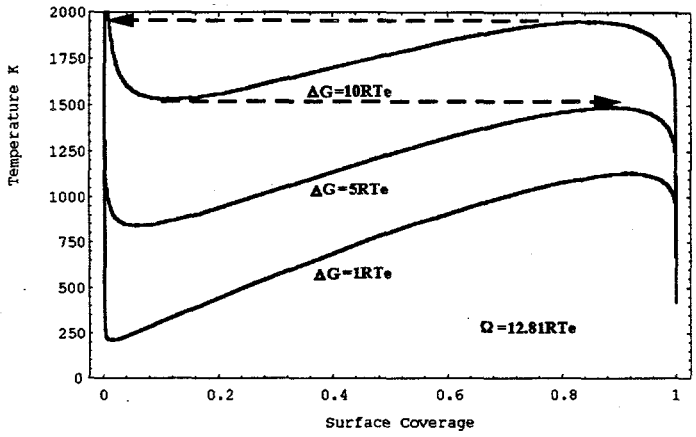

Fig. 1. Surface coverage vs. temperature as a function of ΔG. Te =1173K. The real physical paths are indicated by the arrows as an example for rising (left arrow) and falling (right arrow) temperatures.

This means that it is because the chemical potential difference between the surface and bulk is larger for pure Si than for pure Cu that Cu atoms are driven toward the surface in a Si-Cu solid. Since Cu has a high diffusivity in Si (7×10^{-9} m^2 sec^{-1} at 900°C), the characteristic diffusion length of Cu is ~3.5 mm in 30 minutes of growth time, hence this surface segregation phenomenon will have a significant reduction effect on Cu concentration in the bulk of Si layers.

3. Experimental Results

Depth profiling of impurities including Cu was obtained with secondary ion mass spectroscopy (SIMS) analysis in thin layer silicon grown on high-purity single crystal silicon substrates (Fig. 2 and 3). Due to the dynamic nature of SIMS measurements, the signal in the first 100 Å is not accurate. But both samples show Cu enrichment in the 0.3~0.4 μm surface region. One can easily notice the difference in the bulk Cu concentrations between the two

samples. A logical explanation for this is the difference in substrate thicknesses since the layer in Fig. 3 should have lower starting Cu concentration as we have discussed in section 1. The sample shown in Fig. 3 is thicker, and would gather more Cu during growth from in-diffusion of Cu than the sample shown in Fig. 2. During the sample cool-down period after growth, Cu out-diffuses to the surface and results in different levels of reduction in bulk Cu concentrations.

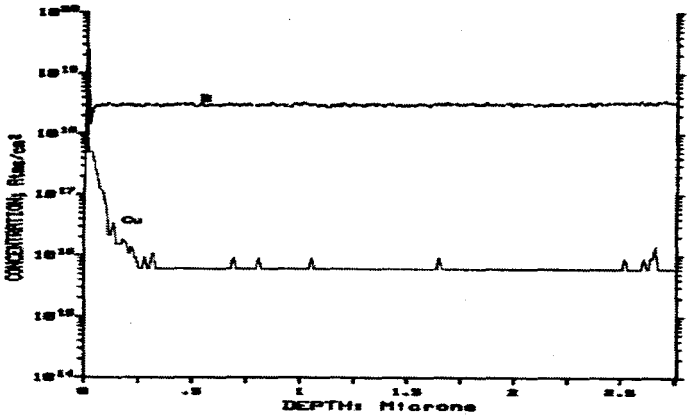

Fig. 2. SIMS depth profile of impurities in a thin (~10 μm) layer grown on a ~150-μm-thick single crystal substrate from a 0.35Si-0.65Cu solution after the substrate was partially dissolved.

The slow diffusers, B and Al, also exhibit surface segregation but the effects were limited to much smaller regions, indicating that surface segregation for slow diffusing impurities is farther away from reaching the equilibrium state during the sample cooling period.

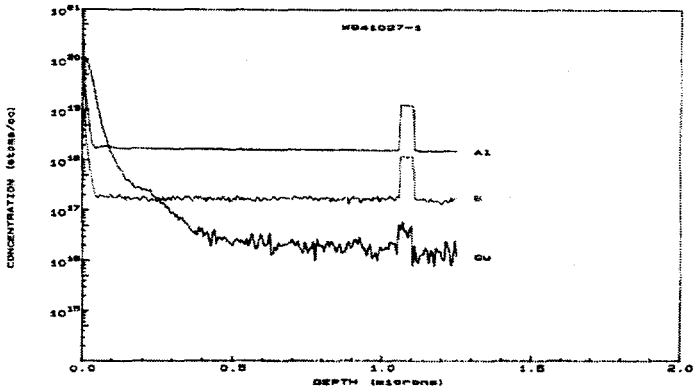

Fig. 3. SIMS depth profile of impurities in a thin (~10 μm) layer grown on a 300-μm-thick single crystal substrate from a 0.28Al-0.49Cu-0.23Si solution. The upward steps around 1.1 μm are test signals that indicate real signals instead of background noises.

The supply of Cu for surface segregation comes from the bulk of the layers and the underlying substrates. The Bragg-Williams equation only deals with ideal monolayer surface segregation. In reality, the free energy difference ΔG, and thus the surface enrichment, can extend deep into the sub-surface region as we have seen in Fig. 2 and Fig. 3.

In order to fully utilize this Cu sink near the surface, a slower cooling after layer growth can be done to speed up the segregation process (Fig. 4).

Although it is difficult to compare the bulk Cu between the two procedures due to varying SIMS background, the enhancement in surface segregation after slow cooling is obvious. We can take the Cu depth profile in Fig. 4 as nearly equilibrium in addition to a full surface coverage of a monolayer, to roughly calculate the gettering capability by numerical integration.

[surface area density of Cu] = $(5\times10^{22})^{2/3}$ + 1/2 × $(10^{20}-10^{18})$ ×(0.15×10^{-4}) + 1/2×$(10^{18}-2\times10^{17})$ ×$((0.55-0.15)\times10^{-4})$ + 1/2×$(2\times10^{17}-3\times10^{16})$ ×$((0.6-0.55)\times10^{-4})$ ≈ 1.357×10^{15} + 0.743×10^{15} + 1.6×10^{13} + 4.25×10^{11} ≈ 2.12×10^{15} (cm^{-2})

The total area density of Cu in the layer before surface segregation can be estimated at the uniform concentration of 1.2×10^{17} for the total thickness of the layer and the substrate, 30 μm and 200 μm, for example:

[total area density of Cu] = $1.2\times10^{17}\times230\times10^{-4} = 2.76\times10^{15}$ (cm^{-2})

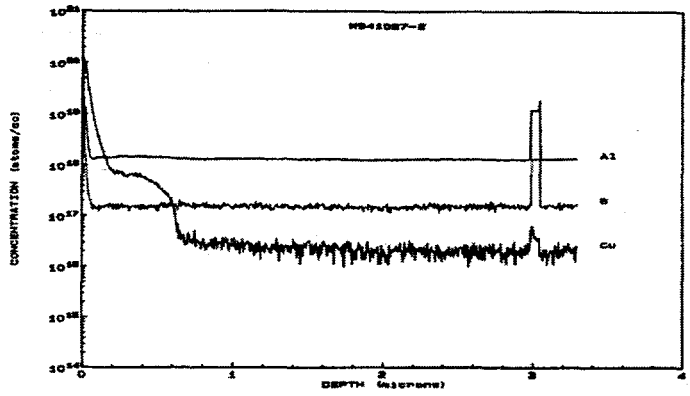

Fig. 4. Slow cooling to room temperature in 10 minutes after growth (as compared to 2 minutes in Fig. 3)

Therefore, the bulk Cu concentration after surface segregation is only 2.8×10^{16} cm^{-3}. After we remove the top Cu-enriched surface region by wet chemical etch, the total Cu remaining in the layer and the substrate will only be able to provide 0.5% of a surface monolayer and thus will be of no concern to long term device stability.

It is worthy to note that this surface segregation will have the same effect in gettering other fast diffusing impurities like Ni or Fe. Due to their overall lower solubility in silicon (5×10^{16} cm^{-3} for Ni, 2.5×10^{15} cm^{-3} for Fe at 900°C), the bulk concentrations of these impurities after surface segregation should be low enough to not cause any device performance degradation even if a low purity MG-Si substrate is used. For grain boundaries, the chemical potential of Si atoms is likely to be lower than that of a free surface since no significant impurity enrichment at grain boundaries in thin Si layers was observed with SIMS.

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Controlled Samples for Silicon Defect and Impurity Studies

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Introduction

Because of the diverse defects and impurities that are present in any given sample of silicon material, it can be extremely difficult to conduct a controlled experiment to study the influence of any particular defect or impurity on photovoltaic properties such as minority charge carrier lifetime τ or solar cell efficiency η. For example, the influence of iron may be different if boron is present, or the influence of silicon self interstitial clusters may be different if oxygen is present. It thus becomes important to conduct such studies on controlled samples where the influence of secondary effects is minimized.

At NREL, over the past several years, we have focused on using the high-purity float-zone (FZ) growth method to obtain controlled samples. Because the silicon melt is not in contact with a container, and no heated components are in the growth region, very high purities and low defect levels can be achieved in baseline material. The baseline can be controllably perturbed by introduction of specific defects or impurities. The chart shown below lists some of the types of defect and impurity combinations that can be studied in this way. The boxes marked with an "x" represent combinations we have studied to some extent.

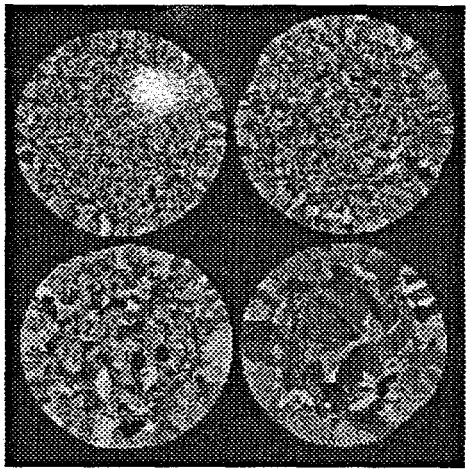
	IMPURITIES							
DEFECTS	none	O	C	N	H	Fe	Cr	others
vacancies, D defects				x	x			
Si self interstitials (I)				x	x			
Type B swirl defects	x			x	x			
Type A swirl defects	x			x	x			
Twins								
dislocations	x							
slip								
lineage								
grains-low defect	x			x				
grains-high defect	x							
others								

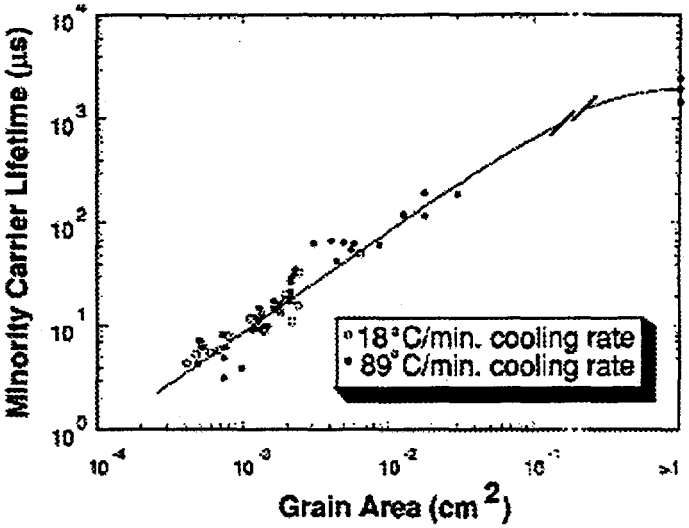
There are an exhaustive number of combinations that could be studied, particularly if multiple combinations are considered (e.g. slip with oxygen plus carbon plus iron). In this paper, we present some examples of controlled studies that have been carried out, but the main purpose is to poll the silicon defect and impurity research community concerning the types of controlled samples that are most needed for ongoing and planned new studies.

Examples

Grain Size Effects on τ and η

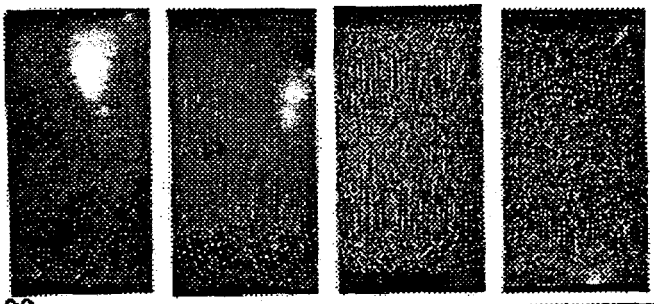
Float zoning with a large diameter and very fine-grained polycrystalline seed was used to generate a set of high-purity samples with increasing grain size. Wafer lifetimes were measured and correlated with grain size and the results are shown below. Grids of 2-mm-square diagnostic mesa solar cells were also fabricated and correlated with grain size.

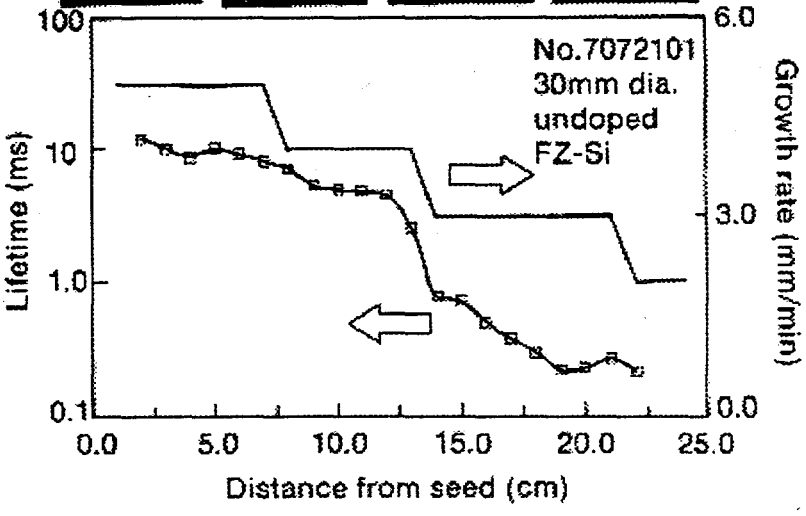




Type A and B Swirl Effects on τ

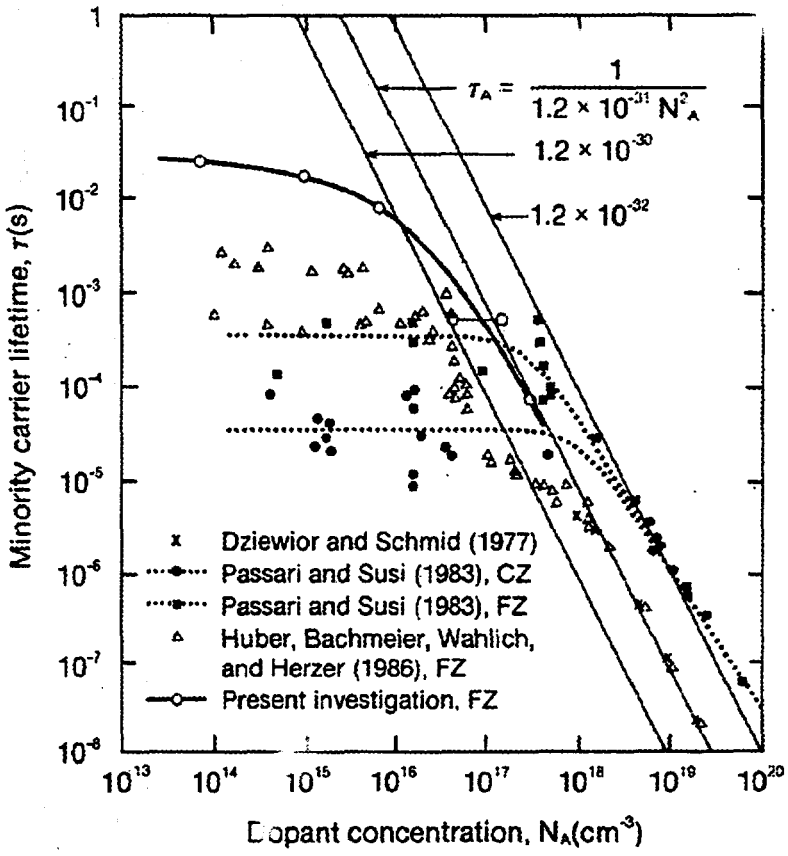
As the growth rate of FZ dislocation-free (DF) crystals increases, the incidence of grown-in type A and type B swirl defects decreases and at a threshold rate (~ 4mm/min for the 30-mm-dia. example shown here) swirl defects are eliminated leaving only type D or type I microdefects. The elimination of swirl defects has a remarkable effect on τ – more than an order of magnitude increase. Besides growth rate, the crystal cooling rate (involving growth rate and thermal gradient) also has an effect on τ.





Dopant Effects on τ (Auger Recombination)

High-purity FZ crystals were grown with varying dopant concentrations and under conditions that precluded microdefect swirl formation and fast-cooling defects. Lifetimes as high as 20,000 μsec resulted, and the sample set was used to obtain τ vs. dopant (in this case, Ga) density in this high-τ regime. In the course of the study, we also gained insight on growth parameters that affect the value of τ – in particular growth rate and thermal gradient.



Summary

A few examples of the types of defect and impurity studies that can be done with controlled silicon samples generated by the FZ method have been given. Many other types of controlled samples could be generated this way (e.g. Fe in Si with or without dislocations, highly defected vs normal grains in multicrystalline Si material, effects of O or C in Si on τ, etc.). What types of Si samples should have high priority, and what types would be of most assistance to other researchers? Your views on this are valued. If you would like to comment, please do so by returning the last sheet of this abstract with the appropriate boxes marked and/or with your written suggestions. If there is a clear trend, we will attempt to consider this in our future research.

Suggested high-priority controlled, high-purity Si sample sets:

Mark the appropriate box(es) and or comment below

	IMPURITIES							
DEFECTS	none	O	C	N	H	Fe	Cr	others
vacancies, D defects								
Si self interstitials (I)								
type B swirl defects								
type A swirl defects								
twins								
dislocations								
slip								
lineage								
grains-low defect								
grains-high defect								
others								

Comments:

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Organization:
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Nitrogen Effects on Silicon Growth, Defects, and Carrier Lifetime

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Introduction

Silicon crystal or multicrystal growth in N_2 or partial-N_2 atmospheres can provide mechanical strengthening, lower purge-gas costs (nitrogen from liquid sources is about a factor of 4 less expensive than argon from liquid sources), and reduce swirl-type microdefect formation in dislocation-free (DF) crystals. There is not much literature on electrical effects of N in Si, including lifetime effects. We studied the effects of Si growth in atmospheres containing N_2 on minority charge carrier lifetime τ using the float-zone (FZ) crystal growth method. Ingots were grown with purge gases that ranged from pure argon (99.9995%) to pure N_2 (99.999%). We found that multicrystalline silicon ingot growth in a partial or total nitrogen ambient has a negligible effect on τ. Values of 40 μs < τ < 100 μs were typical regardless of ambient. For DF growth, the degradation of τ is minimal and τ values above 1000 μs are obtained if the amount of N_2 in the purge gas is below the level at which nitride compounds form in the melt and disrupt DF growth.

Experimental

We used a high-purity, induction-heated, FZ crystal growth method to produce DF, single-crystalline and multicrystalline ingots of Si in a growth ambient that was changed by varying the purge gas source in increments from pure argon at the beginning of the growth process, to various compositions from the group 95% Ar/5% N_2, 75% Ar/25% N_2, 50% Ar/50% N_2, and 100% N_2. The flow rate was typically 5-6 standard liters$\cdot$min^{-1}, with a chamber volume of 150 liters and a chamber pressure of 1.2 bar. Under these conditions, a step change in purge gas source composition results in a slowly changing ambient (about 25 minutes for a complete change even if there was no mixing).

FZ growth effectively precludes large-scale introduction of other impurities such as O or C which can be incorporated when the Czochralski (CZ) method is used. It also allows the effects of N to be studied in isolation from other impurity effects. The ingots were zoned once in vacuum or pure argon and then (in some cases) doped p-type during the final FZ pass, with 99.99999%-pure Ga. The low segregation coefficient of Ga (k_o = 0.008) provides very uniform p-type doping in small experimental FZ crystals like those used in this study. Some ingots were grown DF; others were started from thin or thick multicrystalline seeds. The ingot diameter was typically 33 mm.

After growth, τ was measured as a function of position along the ingots using the ASTM F28-75 photoconductive decay (PCD) method, and by masking off all but a 1-cm-wide window which was repositioned for each data point. Microdefect examination was conducted by copper decoration and acid etching, and FTIR measurements of N contents were made using the 963 cm^{-1} wavenumber absorption peak with a calibration factor:

$$N \text{ (in atoms}\cdot\text{cm}^{-3}) = (1.83 \pm 0.24) \times 10^{17} \cdot \text{(absorption coefficient)} \quad [1].$$

Results and Discussion

Multicrystalline Ingots

Ingot 941031 was grown at 3 mm•min^{-1} with 35 Ω-cm Ga doping and a diameter of 33 mm, using a 22-mm-thick seed from a previously grown multicrystalline ingot. A purge gas of 100% Ar at a flow rate of 6 standard liters•min^{-1} and a pressure of 1.2 bar was used for the first 65 mm of growth and 100% N_2 under the same flow and pressure conditions for the last 90 mm of growth. The observed lifetimes were ~85 μs for the portion grown in 100% Ar and ~75 μs for the segment grown after the purge gas was changed to 100% N_2 (see Fig. 1). The observed values of τ for the corresponding grain sizes correlate well with our previously published data for τ vs. grain size in similarly doped, pure silicon [2], implying that the grain structure rather than the N_2 ambient is the dominant factor in establishing the measured τ values. The lifetime degradation effect due to the 100% N_2 purge gas is at most 12%. After a short time of growth with 100% N_2 purge gas, island-like clumps of a thin nitride skin are seen to form on the melt surface, but growth is able to proceed anyway. We have grown entire ingots (start to finish) using a 100% N_2 ambient. A 33-mm-dia. crystal growing by the FZ method with clumps of a nitride skin on the floating zone surface is shown in Fig. 2.

Four samples were cut from ingot 941031 and polished for FTIR measurements. The segment grown in Ar was used as the reference for determining the N content (see Table I) at the other positions marked in Fig. 1. The thickness of the FTIR samples was approximately 10 mm.

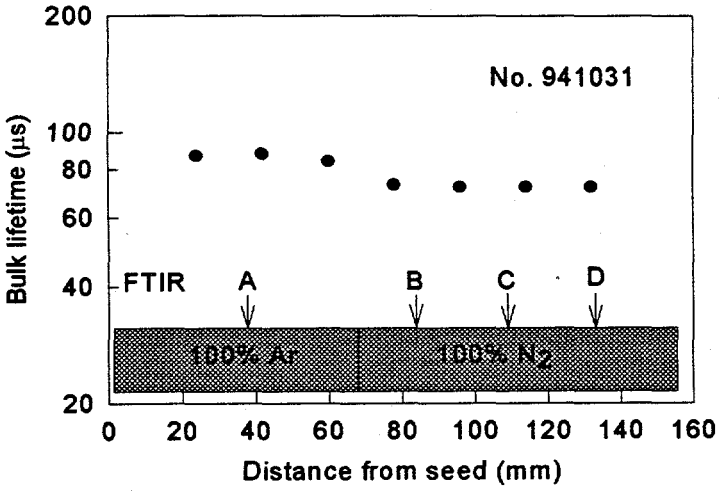

Fig.1. τ vs. position for multicrystalline Si growth using two purge gas compositions: 100% Ar and 100% N_2.

Table I. FTIR values for nitrogen concentrations in sample positions A-D of ingot 941031, as marked in Fig. 1

Sample	Position (mm)	N (atoms•cm^{-3})
A	40	Reference
B	84	4.2.x 10^{14}
C	110	2.3 x 10^{15}
D	134	7.8 x 10^{15}

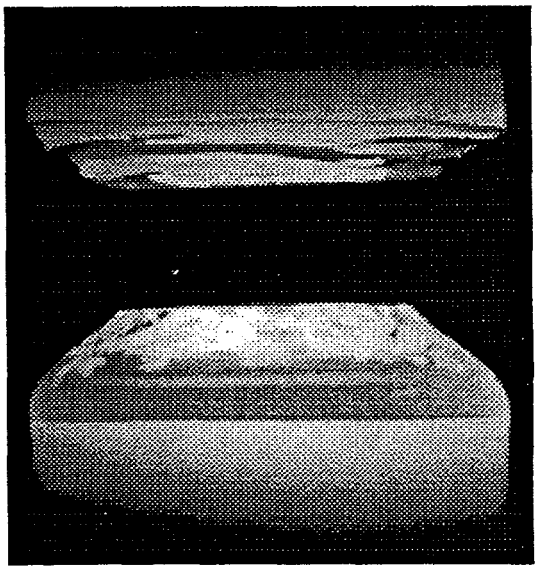

Fig. 2. Photograph of a 33-mm-dia. Si floating zone in a 100% N_2 ambient. Nitride clusters are present on the molten zone's surface. ⟶

Dislocation-Free Crystals

Several DF crystals were grown. Crystal 941024 grew at 3 mm•min^{-1} with no doping and a diameter of 33 mm. The first 60 mm grew in 100% Ar at a flow rate of 6 standard liters•min^{-1} and a pressure of 1.2 bar. The purge gas was switched to 75% Ar/25% N_2 under the same flow and pressure conditions for the next 75 mm of growth, and to 50% Ar/50% N_2 for the last 105 mm. The end resistivity for this crystal was 51 kΩ-cm, indicating that N does not dope silicon. The segment grown in 100% Ar was measured to have τ = 2,000-3,000 μs (see Fig. 3). τ rose to ~4,000 μs for the portion grown with 75% Ar/25% N_2 purge gas, as well as for the initial growth in 50% Ar/50% N_2 purge gas. However, dislocations nucleated about 50 mm beyond the start of the 50% Ar/50% N_2 purge (at position ⊗ in Fig. 3) and slipped back into about 30 mm of the previously DF region. The cross hatched region is dislocated. This caused τ to drop to about 400 μs as shown in Fig. 3. The levels of N in crystal 941024 are given in Table II. Dislocations nucleated shortly after N reached 9.9 x 10^{15} atoms•cm^{-3}.

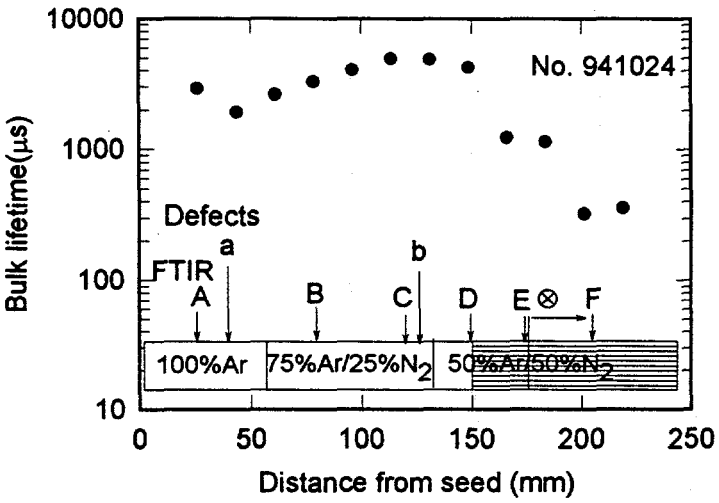

Table II. FTIR values for N concentrations in sample positions A-F of Fig. 3.

Sample	Position (mm)	N (atoms•cm^{-3})
A	25	Reference
B	85	5.0x 10^{14}
C	120	2.2 x10^{15}
D	154	5.3x 10^{15}
E	169	9.9 x 10^{15}
F	214	3.2 x 10^{16}

Fig. 3 Lifetime vs. position for an undoped, DF crystal grown at 3 mm•min^{-1} in purge compositions 100% Ar, 75% Ar/25% N_2, and 50% Ar/50% N_2.

Samples from positions a and b of crystal 941024 were Cu decorated and etched to reveal microdefects. As shown in Fig. 4, swirl-type defects were seen in sample a (which is normal for this ingot diameter and growth rate). Sample b shows only homogeneous D- or I-type defects. The increase of τ for the crystal region grown in 75%Ar/ 25% N_2 purge gas arises because the partial N_2 ambient prevented swirl defect formation. Swirl defects have been shown to decrease τ much more than D- or I-type defects [3].

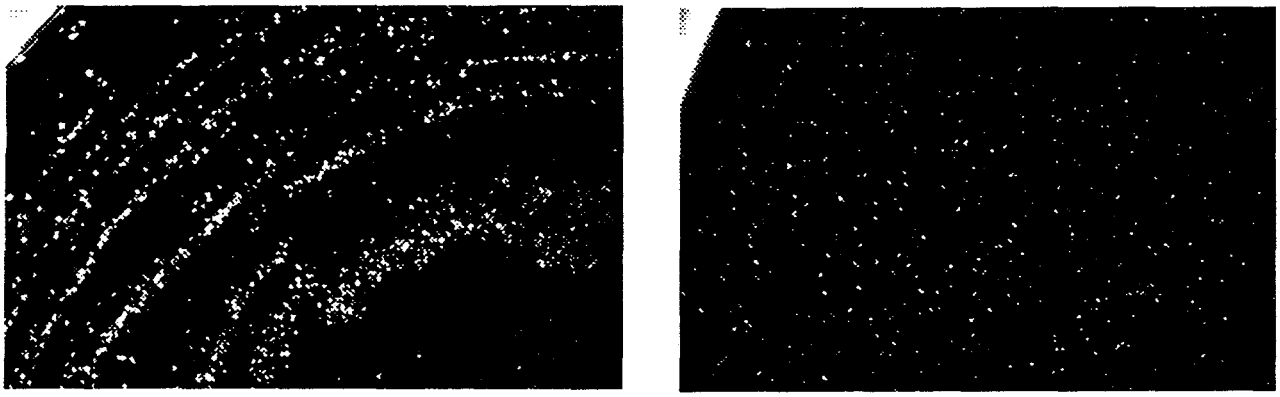

Fig. 4. Microdefects in DF crystal 941024: (left, a) region grown in Ar; (right, b) region grown in 25% N_2/75% Ar. (Photo diagonal is approximately the crystal radius).

Summary

Ga-doped multicrystalline silicon ingot growth in a partial or total nitrogen ambient has a minimal degradation effect on τ. Rather, τ is determined predominantly by the ingot grain size and values are near 80 μs. However, nitride compounds will form on the melt surface and on the hot feed rod and crystal surfaces. Growth can be conducted despite the nitride formation and should be easier in casting or directional solidification where the top of the melt is far from the ingot interface. The concentration of N in multicrystalline ingots grown in N_2 purge gas approaches 1×10^{16} atoms$\cdot$cm^{-3}.

For DF, single-crystal growth, the effect of N_2 on τ is minimal and can even be beneficial (values around 4,000 μs were observed), provided that the amount of N_2 in the purge gas is kept below the level at which nitride compounds form in the melt and nucleate dislocations. A beneficial effect of N_2 is the elimination of swirl-type defects. We have not established the upper limit of N_2 content in the purge gas for steady-state "start-to-finish" DF growth, but it is <10% N_2. At this level nitride compounds eventually form on the melt .

It should be possible to conduct Si growth in a partial N_2 ambient, within the limits discussed above, to take advantage of mechanical strengthening effects, lower purge gas costs, and other process advantages without significant reductions in τ.

Acknowledgment

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CASTING LARGER POLYCRYSTALLINE SILICON INGOTS

BY

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Introduction

Solarex has developed and patented a directional solidification casting process specifically designed for photovoltaics[1]. In this process, silicon feedstock is melted in a ceramic crucible and solidified into a large grained semicrystalline silicon ingot. In-house manufacture of low cost, high purity ceramics is a key to the low cost fabrication of Solarex polycrystalline wafers[2].

The casting process is performed in Solarex designed casting stations. The casting operation is computer controlled. There are no moving parts (except for the loading and unloading) so the growth process proceeds with virtually no operator intervention.

Today Solarex casting stations are used to produce ingots from which 4 bricks, each 11.4 cm by 11.4 cm in cross section, are cut. The stations themselves are physically capable of holding larger ingots, that would yield either: 4 bricks, 15 cm by 15 cm; or 9 bricks, 11.4 cm by 11.4 cm in cross-section. One of the tasks in the Solarex Cast Polycrystalline Silicon PVMaT Program[3] is to design and modify one of the castings stations to cast these larger ingots. If successful, this effort will increase the production capacity of Solarex's casting stations by 73% and reduce the labor content for casting by an equivalent percentage.

Equipment Modifications

Solarex manufactures its own ceramic vessels. Casting of larger ingots requires larger pour vessels and larger receivers. The size and shape of the receivers into which the silicon pours are dictated by the shape of the ingot desired. For the PVMaT program the ingot cross-section increases from approximately 25.5 cm by 25.5 cm to 32.7 cm by 32.7 cm, so the receiver must increase in size accordingly. Patterns for the molds were designed, built and used to produce the molds. Receivers have been produced and used to cast ingots.

The largest ceramic piece is the crucible, in which the silicon feedstock is melted. A potential problem was the ability to fire larger pieces of ceramic, while maintaining yield and physical properties. Just extending the height of the crucible to hold the additional silicon feedstock would likely result in a ceramic piece that is difficult to produce and hard to load with feedstock. The cross-section of the crucible was modified from cylindrical to elliptical to fit around the heating elements. This change increases the volume of the crucible by approximately 20%. An elliptical crucible mold pattern was designed, built and used to make elliptical molds. The molds were used to cast elliptical crucibles. These crucibles were fired and successfully used to pour an extra 20% silicon, producing ingots with larger cross-section.

To achieve the remainder of the increase in volume, a crucible extender was designed. The extender is mounted on top of the elliptical crucible after the crucible has been loaded with silicon. The extender mold pattern has been designed, built and used to produce a mold. Extension pieces have been produced and used to cast ingots.

Two possible modifications to enlarge the casting stations were evaluated in detail. The first proposal retained all of the present chamber with the addition of a height extension. The second proposal involved replacing the pour chamber with a new larger chamber. The height extension option required less capital investment and time to implement, as well as requiring less input power to melt the silicon charge. Therefore, chamber modification was selected for the program. The necessary modifications were designed, the parts fabricated and installed and the modified system used to cast ingots.

Process Development

Casting experiments began with an intermediate size ingot, 33% larger than the standard 4 x 11.4 cm by 11.4 cm ingot. This ingot was designed to produce 4 x 15.2 cm by 11.4 cm bricks for use in the Solarex MSX-83 module. The initial casting runs produced ingots that had lower yields due to cracking of the silicon at the bottom of the ingot. Modifications to the insulation package and some minor changes to the casting program led to improved yields. The latest runs resulted in higher yields than production standard and in average cell efficiencies equivalent to co-processed production-size ingots. Ingots of this intermediate size are now being produced regularly in production.

Efforts then turned to casting full size ingots to yield 4 x 15 cm by 15 cm bricks. The first several large ingots had well-behaved runs, but had cracks extending upward from the bottom. An 11.4 cm by 11.4 cm brick was cut from one of these ingots, and then wafered and processed into cells. The cell efficiency from this brick was significantly lower than normal, with the average cell efficiency for this brick being approximately 90% of a standard production brick. A number of modifications to the insulation package and to the casting program were attempted, but none was able to eliminate the bottom cracking.

Analysis of the crystal growth and modeling of the casting process indicated that a larger separation between the bottom heater enclosure and the lower can was required. This change was made and the insulation configuration and process program optimized on standard sized ingots. We verified that this configuration could produce equivalent material by casting and processing 9 standard size ingots. There was no statistical different in yield or efficiency between these 9 ingots and the overall production line average during that time period.

Using this configuration full size ingots for 4 x 15 cm by 15 cm bricks were cast. The first two ingots were successfully cast and sized without appreciable cracking. Sample 15 cm by 15 cm bricks and all of the wafers cut from one of these bricks on the wire saw have been delivered to NREL. Cells (11.4 cm by 11.4 cm) have been processed on this material. Cell results will be presented in the poster.

Most of Solarex's products are still based on the use of 11.4 cm by 11.4 cm solar cells, so an effort is underway to develop casting of ingots large enough to produce 9 x 11.4 cm by 11.4 cm bricks. Such an ingot requires approximately 20% more silicon than the PVMaT ingot. The initial efforts to cast these "mongo" ingots required changes in the insulation and receiver, but utilized the same

pour crucible. We were able to load the added charge of silicon feedstock into the PVMaT crucible and successfully pour and freeze out the larger mongo ingot. The attached picture shows the comparison of a standard ingot (4 x 11.4 cm by 11.4 cm bricks) next to a new mongo ingot (9 x 11.4 cm by 11.4 cm bricks).

Efforts are now underway to optimize the process for casting these larger ingots. Solarex is planning to increase casting capacity by modifying all of the casting stations to produce the larger ingots.

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Figure 1: Standard and Mongo Ingots

GROWTH AND CHARACTERIZATION OF STRING RIBBON

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Evergreen Solar, a new photovoltaics company, makes solar cells and modules based on String Ribbon.

String Ribbon is a silicon sheet growth method wherein two high temperature strings are pulled through a shallow melt of silicon and a crystalline silicon sheet then grows between the two strings. The strings serve to stabilize the edges of the growing silicon sheet. The growth process is primarily meniscus controlled and, compared to other silicon ribbon growth methods such as d-web and EFG, relatively insensitive to temperature fluctuations as great as ±10°C. Growth speed is about 2 cm/minute.

String Ribbon is grown directly from a silicon melt and so all the benefits of the low segregation coefficients of the transition metals can be realized in the as-grown ribbon. The typical material grown at present is 300 μm thick and a bit over 2" wide. This material is being grown with virtually no afterheater. Material of 4" width and ribbon considerably thinner than 300μm, say 100μm, has been grown, but further work in afterheater design is needed before such material can be grown with reduced stress which will make it easier to process into solar cells.

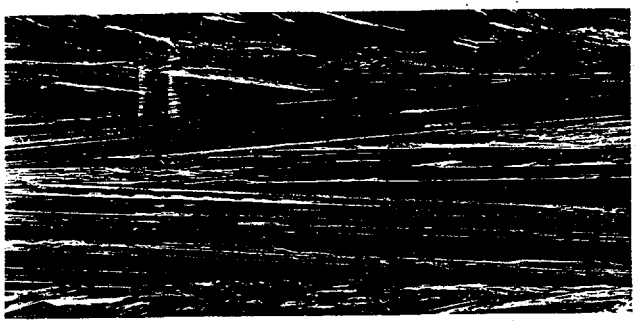
The material grown so far has been B-doped, p-type with a resistivity of 1-3 Ω-cm. The as-grown surface is quite shiny with perhaps a 50Å thick oxide layer on it. Characterization of String Ribbon has been done using RFPCD lifetime measurement. Initial results are very promising with a value of 17μsec and a variation of not more than 20% across the ribbon width.

The grain structure of the as-grown material is characterized by large grains propagating along the growth direction of the ribbon. The regions near the string contain high angle grain boundaries with a grain size on the order of a mm.
Figure 1a is a photograph of a ribbon sample that was defect etched in Sopori etch showing large grains and a qualitative distribution of defects. The black regions in the photograph are zero or low dislocation density regions. The gray scale qualitatively indicates dislocation distribution. The ribbon has a preponderance of coherent twins along <112> directions in (111) plane. Figure 1b shows a photograph

of a region containing such parallel twins with near-zero dislocation density. Figures 2a, 2b, and 2c are photographs showing typical dislocation structure. The average dislocation density is about $5x10^5/cm^2$.

FTIR studies have shown that ribbons have high concentrations of carbon, typically in the range of 7- 9 ppma, while oxygen concentrations are < 1ppma. Figure 3 is a room temperature absorption spectrum of an as-grown ribbon in the wavenumber range of C and O absorption. This spectrum shows an absorption band overlapping the interstitial oxygen band (at 1105 cm^{-1}) due to a thin surface layer of oxide. This band disappears if the ribbon is dipped in HF, as seen in the spectrum after HF dip.

Further characterization of String Ribbon will be done using various scanning techniques to determine spatial variations in grain size, lifetime, and dislocation distribution as well as FTIR to measure $[O]_i$ and $[C]_S$ and DLTS to study possible deep level recombination centers. A defect dislocation density map of a 2-in x 2-in section of a ribbon sample, taken with PVSCAN500, is shown in Figure 4.



Coherent twins

Figure 1a: Photograph of a 2-in x 4-in defect etched ribbon sample

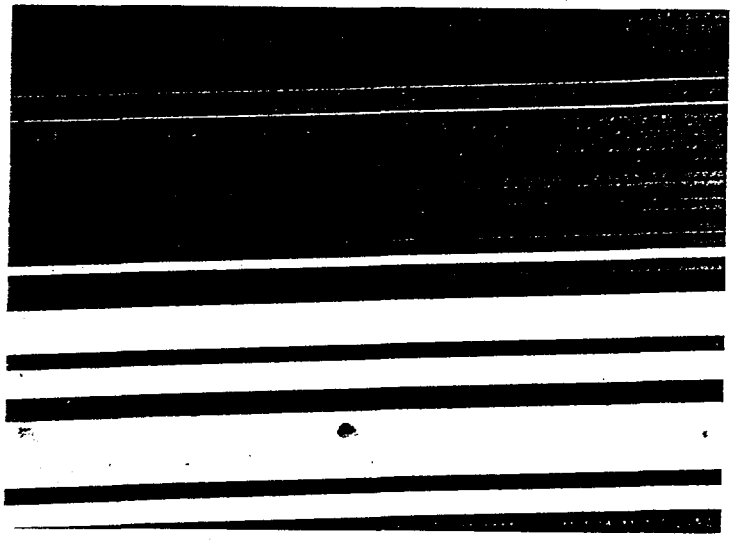
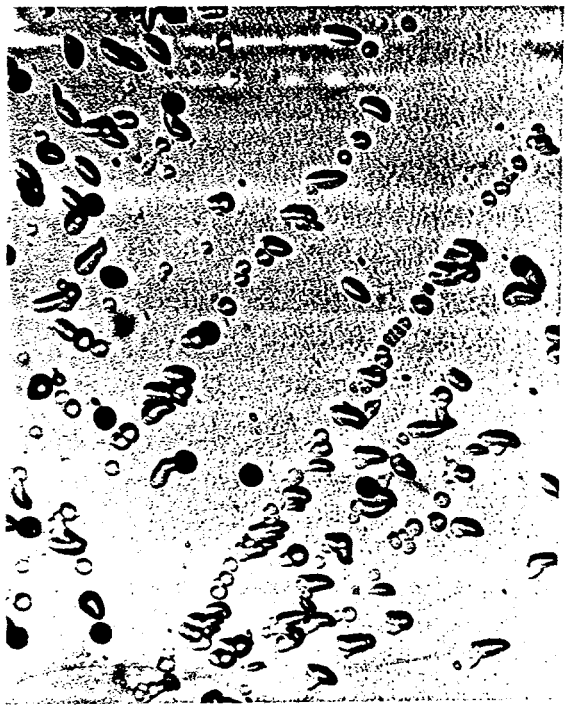


Figure 1b: Photograph showing zero-D regions of parallel twins

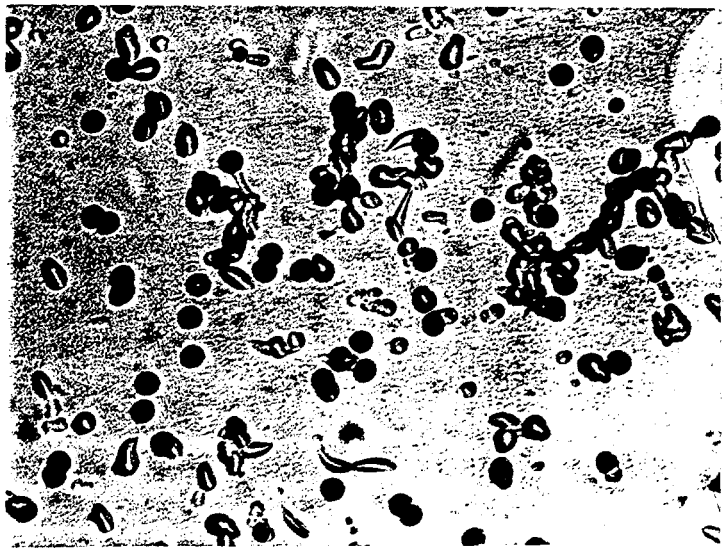
——— **400μm**

Figure 2: Photographs of a defect etched ribbon showing dislocation configurations in various regions

(a) slip dislocations in some twinned regions



(b) shallow dislocation loops



(c) dislocation networks

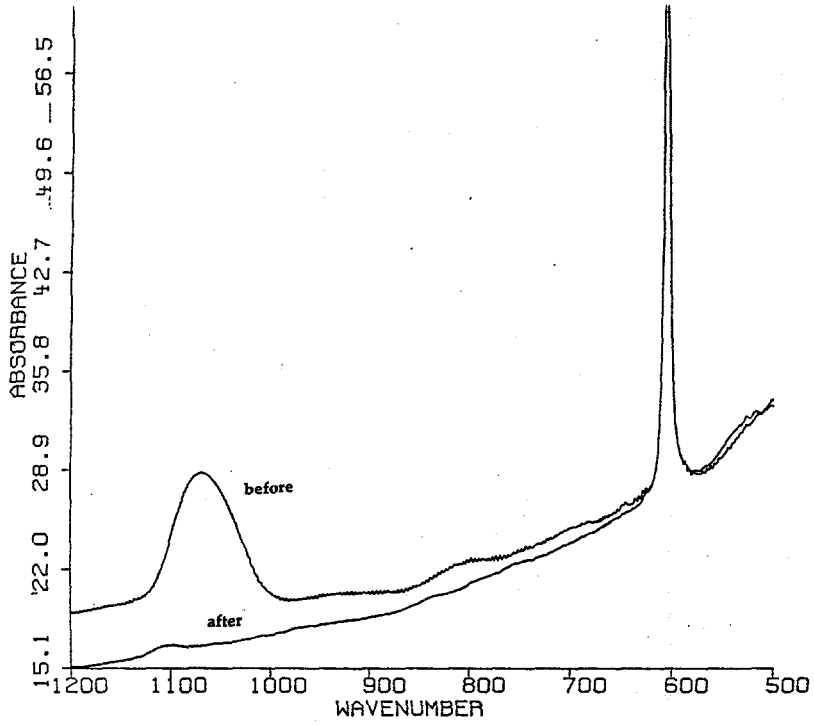


Figure 3:
FTIR spectrum of a ribbon sample in the C and O region before and after HF dip

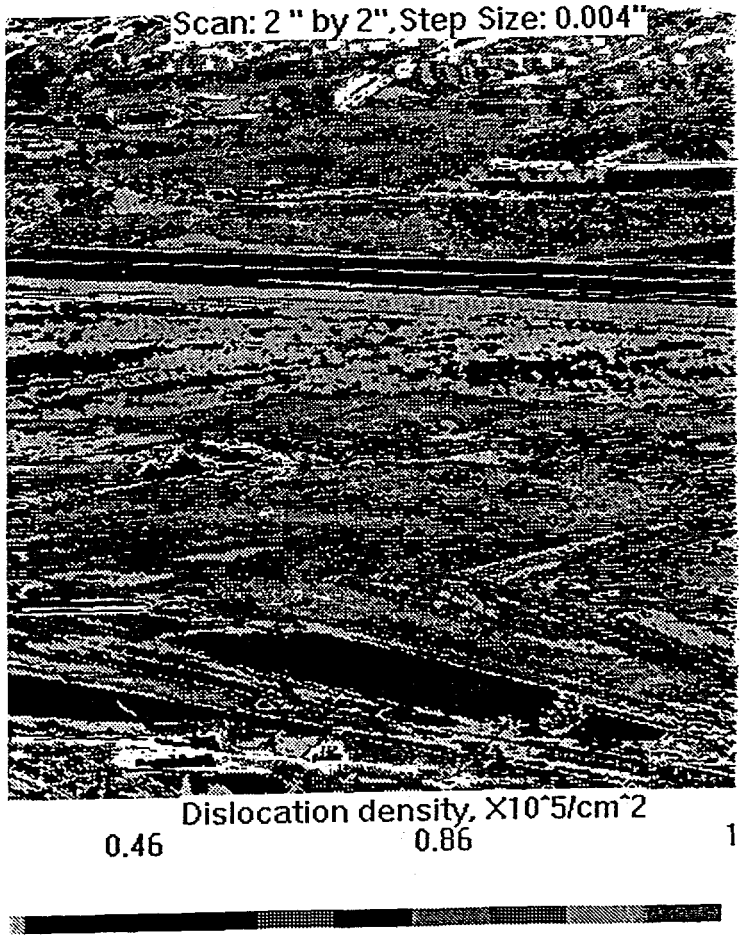


Figure 4:
Defect map of a 2-in x 2-in ribbon sample taken with PVSCAN5000

Characterization of HEM Multi-Crystalline Silicon Material for High Efficiency Solar Cells

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Silicon substrates produced by the Heat Exchanger Method (HEM) have yielded solar cells of high efficiency—17.4% for small-area cells and 15% modules, under AMl.5 illumination. These high efficiencies are the result of continued analysis of the HEM growth process, study of the impurity and defect kinetics, understanding of the solar cell process interactions with the material properties, and appropriate feedback to the thermal and ambient parameters of the process. This paper discusses the major characteristics of the technique, the material properties, and process requirements for fabrication of high efficiency devices.

Heat Exchanger Method is basically a single-crystal growth process that has been adopted for directional for economical growth multicrystalline silicon ingots. The melt is contained in a ceramic crucible coated with a silicon nitride-based separation layer that minimizes the impurity incorporation into the melt, and enables control of oxygen content in the silicon material. Control of the growth ambient also helps volatalize some of the impurities from the melt leaving a cleaner solid. The following features of material growth and cell processing have been identified as the crucial parameters for yielding high efficiency solar cells:

- **Planar solid-liquid interface during crystal growth.** The thermal profiles that produce this condition are found to minimize the thermal stresses during crystal growth and yield large-grain material of predominantly columnar nature, and low dislocation density. The HEM approach facilitates achievement of the suitable thermal conditions at reasonable growth speeds.
- **Impurity control.** Control of the growth ambient (inert gas pressure) also helps minimize impurity transport from other parts in the furnace and volatalize some of the impurities from the melt leaving a cleaner solid. HEM material grown from off-semiconductor grade feedstock shows typical oxygen and carbon concentrations of <5ppma and <10ppma, respectively. For reusable crucible the oxygen contrations are typically lower than these values (approx 1ppma). The metallic impurities are low; Fe and Cr are typically $10^{12}/cm^3$. Substrates have very low density of precipitates. In the past the precipitation was found to occur primarily as a result of local saturation associated with carbon, oxygen, and nitrogen. Suitable controls have nearly eliminated formation of precipitates except in a thin region that solidifies toward the end of the growth.
- **Dominant defects.** Dislocations are the dominant intragrain defects and have an average defect density of $10^5/cm^2$. Spatial mapping of defects in horizontal and vertical cross-sections of the ingots has shown that typically about 70% of the area of a wafer has a low or nearly zero dislocation density ($<10^4/cm^2$). However, some regions of locally high dislocation density are present where dislocation density exceeding $10^6/cm^2$. These regions contain dislocation networks generated by interactions of dislocations in different (111) planes, resulting from generation of local thermal stresses greater than the yield stress. Figure 1 is a dislocation density map of a typical 4-in x 4-in wafer taken with PVSCAN5000 showing these features. Evidence of low thermal stresses in the majority of the ingot is manifested as a high propensity of coherent twins. These regions consist of multitude of parallel twins with (111) twin planes along <110> or <112> directions.
- **The minority carrier diffusion length (MCDL).** The MCDL of as-grown material is typically about 80 -100 μm and appears to be limited by impurities like Fe and Cr. Figure 2 shows a map of MCDL taken on a 4-in x 4-in wafer using Semiconductor Diagonostics Inc. system; the map is done within a cicular aperture of 3 inches becuase this system is designed for circular wafers. Effective gettering of these impurities occurs by processes such as phosphorus diffusion, chlorine gettering, and Al alloying. The resultant diffusion length increases to about 200-300 μm.

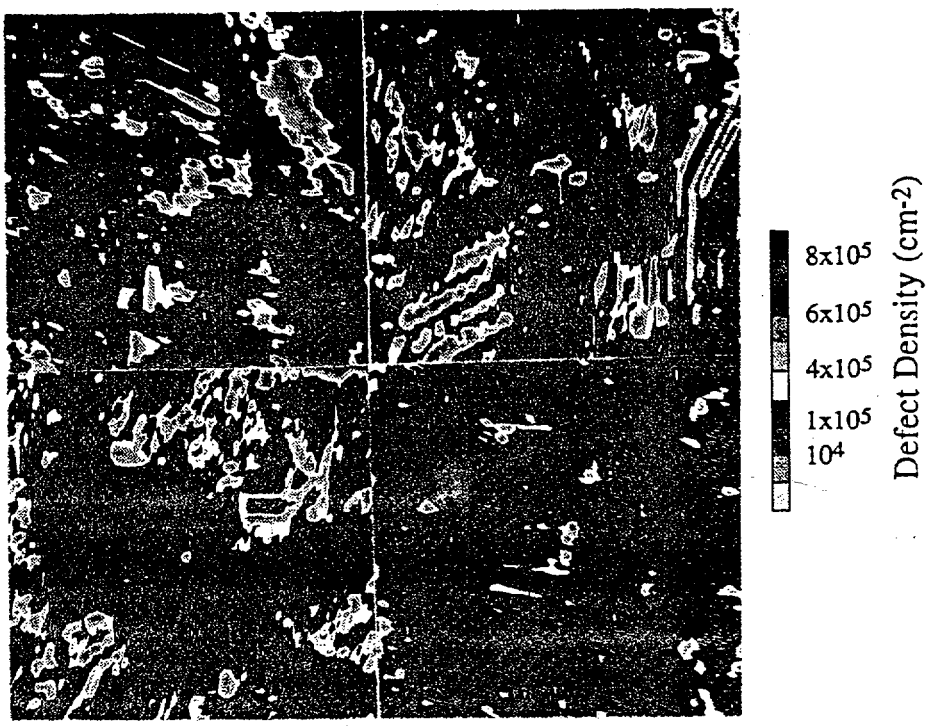

Figure 1. A dislocation density map of a 4-in x 4-in Crystal Systems wafer — Ingot 10, wafer# 91

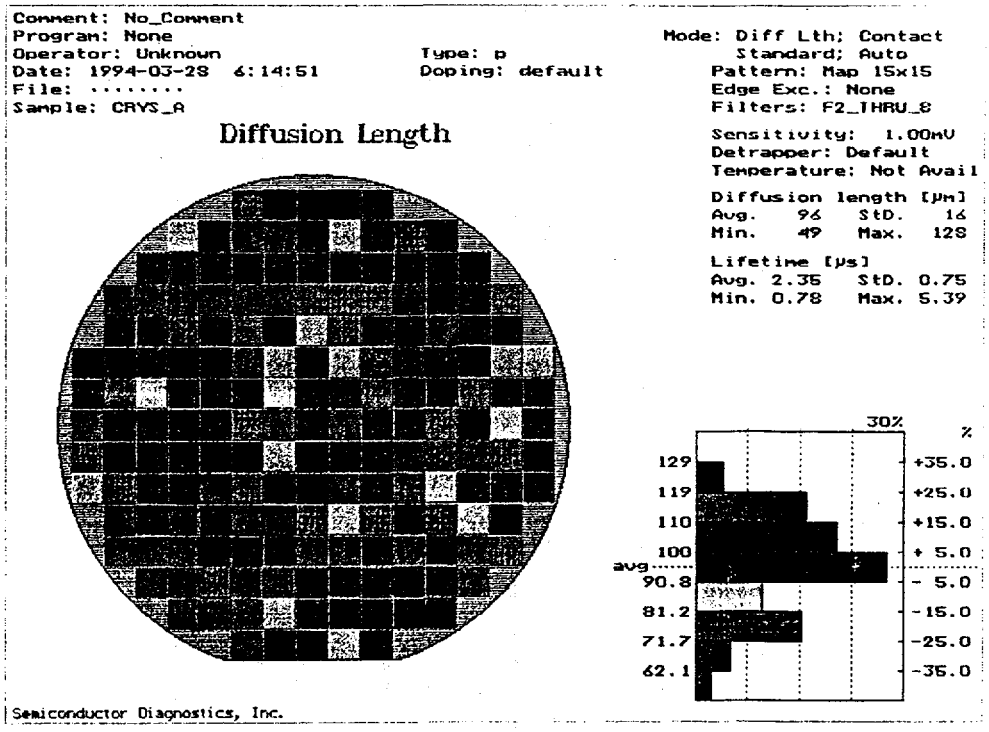

Figure 2. MCDL map of an as-grown wafer (only a 3-in dia. area of a 4-in x 4-in wafer is mapped)

• **Solar cell fabrication.** Simple n+-p-p+solar cells were fabricated on 1-2 Ω-cm , p-type HEM multi-crystalline silicon substrates. These 1-cm x 1-cm cells went through 930 °C/20 min. phosphorus and 850 °C/35 min. Al gettering steps, which also formed the n^+-emitter and p^+ back surface field. The n+ emitter was partially etched back to increase sheet resistance from 16 Ω/sq to 80 Ω/sq. A 100Å thick passivating oxide was grown during the Al drive-in followed by a 400 °C/2 hr forming gas anneal to passivate bulk and surface. Finally, the cells were coated with double layer ZnS/MgF2 antireflection coatings. Table 1 shows that the above process sequence resulted in cell efficiencies in excess of 17% . Figure 3 shows the illuminated I-V curve for a 17.4% efficient HEM cell.

TABLE 1

High Efficiency 1 cm x 1 cm cells on HEM material, measured at Sandia National Laboratories

Cell ID#	Voc	Jsc	FF	Eff %
H-1-3	610	34.6	801	17.0
H-1-4	615	35.4	797	17.3
H-1-15	615	35.4	801	17.4
H-1-16	615	35.8	791	17.4

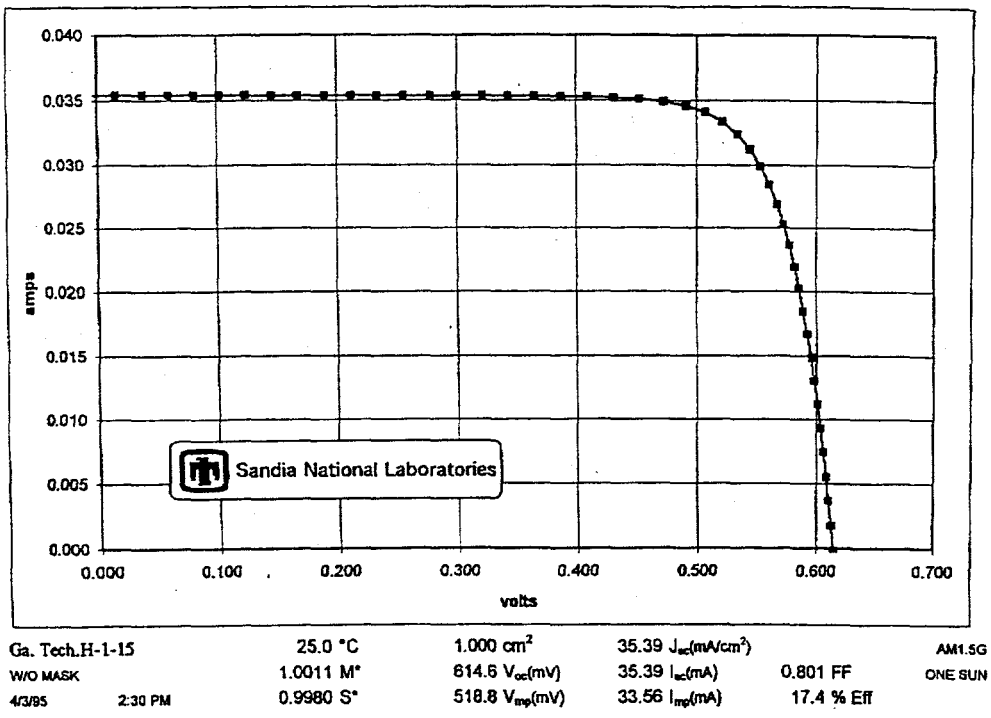

Figure 3. I-V characteristics of a 1-cm x 1-cm solar cell on HEM substrate

Defects in Polycrystalline Silicon Grown by the Edge-defined Film-fed Growth (EFG) Technique

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Crystalline silicon wafers are produced for photovoltaic device substrate material by the Edge-defined Film-fed Growth (EFG) method using a growth technique which results in most of the common extended defects and impurities typical of melt-grown silicon. The EFG technique produces the crystal in the form of hollow octagon tubes. These tubes have typical wall thicknesses, hence a wafer thickness, averaging 300 microns, and are grown continuously to lengths of 5 meters. Since the crucible containing the melt is made from carbon, these defects are superimposed, additionally, on a crystalline matrix supersaturated in carbon. This paper will review the current status of studies on theses defects and their relation to the unique growth conditions for EFG silicon material.

The most common bulk defects observed in EFG crystals are twin boundaries and dislocations. Dislocation densities are nonuniform and can be as high as 10^6/ cm^2. The twins occur in bundles typically arrayed along the growth direction. There is evidence from shallow pits produced during etching that microdefects also are present. Their origins are not known. Since the interstitial oxygen concentration is held below $10^{17}/cm^3$, these defects may be related to carbon. In addition to bulk defects, a pronounced asymmetry is produced in the EFG silicon octagon during growth by the manipulation of the ambient on each surface of the octagon tube. One surface is exposed to an inert argon ambient, while an oxygen containing gas, typically carbon monoxide, is introduced on the other surface. This produces an asymmetry in surface films that can influence the bulk oxygen concentration and results in *in situ* gettering during growth.

The results of studies using FTIR, photoluminescence and impurity decoration will be reviewed that provide some indication of the electronic quality limitations that this complex array of defects imposes on EFG silicon material.

APPLICATIONS OF THE PVSCAN 5000 FOR SOLAR CELLS AND SUBSTRATES

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ABSTRACT

A laser scanning system for the rapid characterization of crystal defects in single- and poly-crystalline semiconductors has been developed by the National Renewable Energy Laboratory and commercialized as the PVScan 5000 by Labsphere, Inc.. In the unprocessed material, the system produces digital color maps of the spatial distributions of dislocations and grain boundaries simultaneously. After device fabrication, the PVScan 5000 is used to produce photoresponsivity maps of the light beam induced current (LBIC) on a photovoltaic device such as a solar cell or a photodetector. An additional feature is that it also measures the spatial distributions of optical reflectance, both specular and diffuse, which can be applied to the LBIC maps to determine the internal responsivity of the device. The internal responsivity is proportional to the minority carrier diffusion length of silicon devices. It is possible, therefore, to determine the diffusion length for certain devices.

A New Methodology for Determining Recombination Parameters Using An RF Photoconductance Instrument

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Abstract

Measurements of minority-carrier lifetime in silicon wafers provide an effective technique for process control and device-physics optimization. for example, detailed measurements of minority-carrier lifetime vs. injection level can allow a nearly complete experimental optimization of a solar cell design and process. This extended abstract describes a methodology that allows this full characterization by using a relatively simple RF photoconductance-decay tool. By analyzing the quasi-steady-state photoconductance as a function of incident light intensity, information corresponding to an I_{sc}-V_{oc} curve can be obtained from a non-contacted silicon wafer. This information is available at various stages during the solar cell fabrication process. The use of steady-state photoconductance instead of transient photoconductance makes use of simple electronics and light sources, yet it has the capability to measure lifetimes down into the 100 ns range.

Introduction

Photoconductance decay is a common method for measuring minority-carrier lifetime. Many methods have been used to sense the photoconductivity without contacting the wafer. These include microwave reflectance, capacitive coupling to the wafer conductivity, and the use of a coil to couple inductively to the Eddy-current damping effects that are proportional to the wafer conductivity. In general, an effective lifetime for a wafer is determined by monitoring photoconductance decay transients. The photoconductance transient is monitored after a very short light pulse. This pulse should have a cut off much shorter than the wafer effective lifetime.

The procedure for a transient photoconductance measurement involves the following steps.

1) Measure the wafer conductance vs. time after the light pulse.

2) Infer the excess carrier density, Δ n, as proportional to the conductance, or calculate it using literature mobility data.

Then, the effective lifetime $=\Delta n/(d(\Delta n)/dt)$

Typically, a single parameter is extracted from this measurement, the effective lifetime. The relevance to solar cell efficiency must be determined using a device-physics model that attributes the recombination to the various surface and bulk recombination mechanisms. A weakness in this type of analysis is that frequently the "effective lifetime" is a strong function of the minority carrier density. Additionally, the effective lifetime measured under transient conditions includes factors not present in the steady-state operation of a solar cell.

Quasi-Steady-State Photoconductance Measurements

An alternative to the method described above is to measure the photoconductivity during a light pulse that decays *much slower* than the effective lifetime of the wafer.

This method follows the procedure;

1) Determine the light intensity vs. time, during a long, slowly decaying light pulse by using a reference solar cell.

2) Simultaneously, measure the sheet conductance of the Si wafer vs. time.

3) Convert this conductance to carrier density using published mobility data.

4) Evaluate the lifetime vs. carrier density by using the principle that the (generation rate * effective lifetime) is proportional to photoconductance.

Since the analysis assumes that the wafer is in steady state, the effective lifetime should be short compared to the flash duration. The generation rate is calculated based on the test-wafer antireflection coating, wafer thickness, and the optical absorption of silicon. These are generally very accurately known parameters.

An complement to the analysis in (4) would be to simply plot the carrier density product of electrons and holes vs. illumination intensity. This data is analogous to an I_{sc}-V_{oc} curve. The short-circuit current is implied by the irradiance, and since voltage is equal to $(kT/q)\ln(np/n_i^2)$, the n-p product plotted on a log scale is proportional to voltage. The usefulness of this analysis is that all the injection-level dependence in the effective lifetime is displayed in this curve. For the special case when the surfaces are passivated and the diffusion length is longer than the wafer thickness, the conversion to implied voltage is accurate. The net result is that this form of displaying photoconductance data can be directly correlated to the full I_{sc}-V_{oc} curve for finished devices.

Advantages of this steady-state method:

-Low-cost light source (photographic flash)

-Relatively slowing-varying signal envelope (simple electronics and data acquisition). Typically only 10 MHz bandwidth is required in the bridge circuit, and 100 KHz in the data acquisition.

-It is a steady-state measurement, similar to the cell in actual operation. The recombination components are weighted as in the actual cell under open-circuit-voltage conditions including the transport and non-uniform photo-generation effects on the carrier-density profiles.

-The result depends upon the absolute value of a small signal, rather than it's derivative.

Most significantly, the use of this steady-state method allows the measurement of very short lifetimes without fast electronics or short light pulses.

Experimental

A simple photoconductance testing apparatus with an 8 MHz RF coil in a bridge circuit was built. This coil couples to the conductivity of the wafer and a signal proportional to this conductivity is observed on a digital oscilloscope. This voltage signal was verified to be linear in wafer conductivity over the entire range of interest. The light source was a photographic flash lamp with a 2.3 ms time constant.

Figures 1 through 3 show the photoconductivity data displayed in 3 forms. This data corresponds to a 0.5 Ohm-cm p-type multicrystalline wafer, 190-μm thick. The surfaces were passivated by light phosphorus diffusions followed by oxidation. In Fig. 1, the inverse lifetime vs. carrier density is shown. Fig. 2 is intuitively more comprehensible. An ideality factor close to unity is seen. For each decade increase in photogeneration, the carrier density also increases by one decade. Finally, Fig. 3 plots the "implied open circuit voltage" vs. the illumination intensity.

Fig. 4 shows data taken on a small-grained polysilicon sample with surfaces passivated by boron diffusions. In this case, the inverse lifetime vs. photogenerated carrier density is shown indicating a lifetime of approximately 350 ns. This demonstrates the applicability of this measurement technique to lower quality material.

Acknowlegements

The authors would like to thank Andrew Blakers, Vaman Kuber, Michael Stuckings, Klaus Weber and the students and staff of the photovoltaic group at the Australian National University for their contributions to this work.

Fig. 1. Polycrystalline, p-type 0.5 ohm cm, P diffused

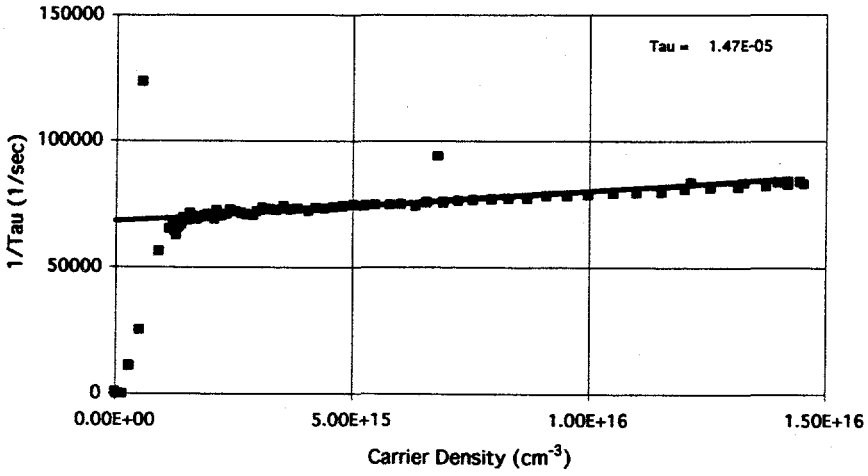


Fig. 2. Generation vs. Carrier Density

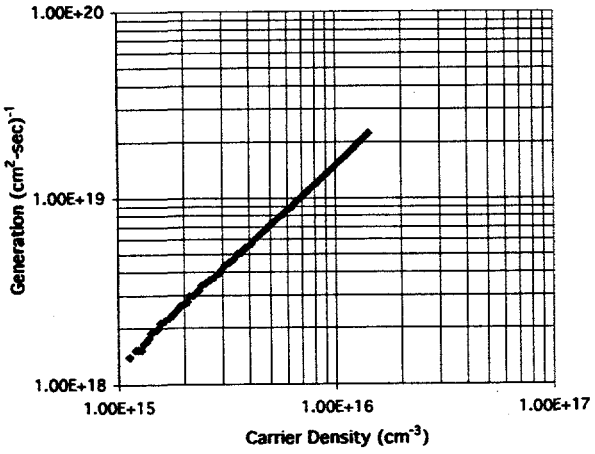


Fig. 3.

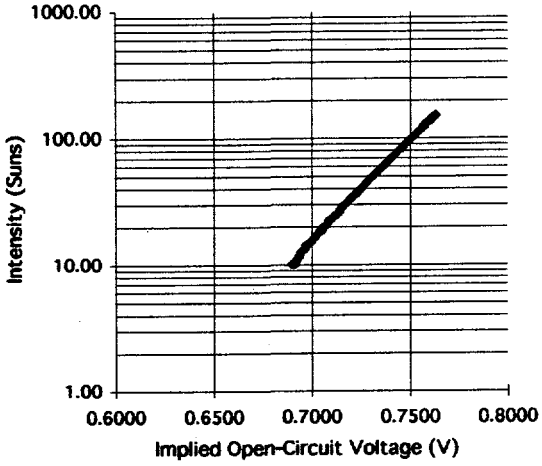
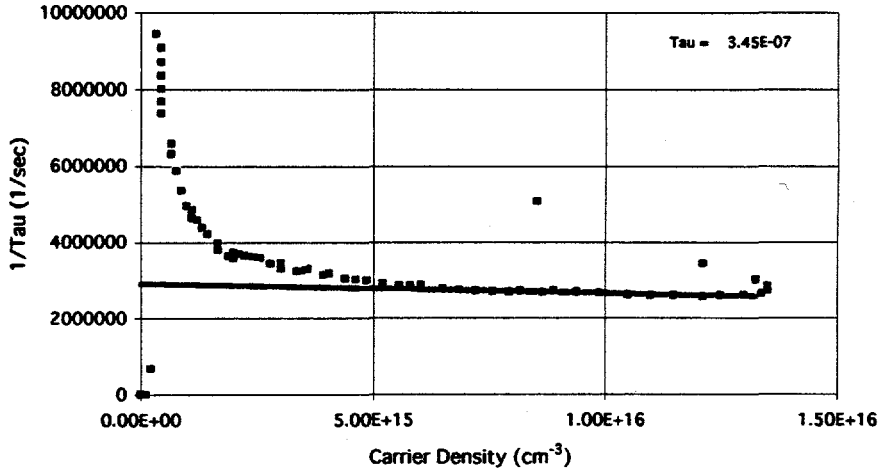


Fig. 4. Polycrystalline material with B-diffused surfaces



Optical Models for Silicon Solar Cells

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Introduction

Light trapping is an important design feature for high-efficiency silicon solar cells. Because light trapping can considerably enhance optical absorption, a thinner substrate can be used which, in turn, can lower the bulk carrier recombination and concommitantly increase open-circuit voltage, and fill factor of the cell. The basic concepts of light trapping are similar to that of excitation of an optical waveguide, where a prism or a grating structure increases the phase velocity of the incoming optical wave such that waves propagated within the waveguide are totally reflected at the interfaces. Unfortunately, these concepts break down because the entire solar cell is covered with such a structure, making it necessary to develop new analytical approaches to deal with incomplete light trapping in solar cells.

Exact analysis of light trapping due to texturing is very difficult because surface texturing produces non-planar interfaces. Several calculations have been performed to determine the approximate degree of absorption enhancement and the optimum texture shape(s) for silicon solar cells. These approaches produce satisfactory results for thick cell designs. However, as the cell thickness and the texture size decrease, a rigorous treatment of light trapping becomes increasingly important. Rigorous analyses are necessary for a physical understanding of various features that take place when light trapping is employed. For example, light trapping can produce local concentrations in the light flux, changes in the effective surface recombination effects, and greatly reduce bulk recombination. Rigorous light-trapping analysis is particularly important for thin silicon films. At this time it is not known where ray theory breaks down.

In this paper we describe our on going work to establish two models that analyze light trapping in thick and thin solar cells. The first model is a raytrace calculation in three dimensions that is valid for thick cells. Even though the raytrace calculation accurately models interference effects due to antireflection (AR) coatings, it cannot (in its present form) model the wave effects within the bulk of the cell. Hence, the second model is a wave approach that uses direct solution to Maxwell's equations that is valid for thin two-dimensional cells. This wave approach was developed for a-Si solar cells. Here we use it to establish the domains of ray theory and wave theory. A brief description of the two models is presented.

Ray Optical Model for Thick Cells

Figure 1 illustrates an optical beam illuminating a solar cell with a rough surface that may be periodic or random. The cell typically has two layers of AR coating. The incoming plane wave is split into beamlets, and each beamlet propagates as an optical ray and is multi-reflected inside the cell. This model takes into account exact reflection and transmission coefficients at each interface, as described in reference (1). Each beamlet propagates in the silicon cell with an intensity absorption coefficient.

$$I_{final} = I_{initial} \cdot e^{-\alpha z}$$

$$\text{where } \alpha = \frac{4 \cdot \pi \cdot k}{\lambda},\ n(\lambda) = n - i \cdot k$$

Here $n(\lambda)$ is the complex refractive index, and k is the extinction coefficient. The path of each beam, the angle at which the beam is reflected/transmitted at each interface during multireflections, and the total absorption along an elemental path within the cell is determined. This analysis gives net transmission, reflection, and distribution of photon absorption within the cell for a given input spectrum. The net absorbed photon flux is used to determine maximum achievable current density (MACD) for the input spectrum.

Figure 2 shows calculated MACD for a number of textured structures identified in the figure. These calculations are done for a 5 μm texture height and an AR coating consisting of Si_3N_4/SiO_2 {710 Å/100 Å}. This figure also includes results of ray analysis applied to a 5 μm cell with a texture height of 1 μm, with an AR coating.
As expected, the maximum short-circuit current (J_{SC}) is greatly reduced to 24.5 mA/cm^2 for the planar cell. However, for a cell with perpendicular slats, the maximum J_{SC} is quite high, at a value of 36.2 mA/cm^2. It should be emphasized that the accuracy of applying ray analysis to a 5 μm structure with textured surfaces is questionable.

Explicit Wave Model for Thin Films

Finite-difference time-domain numerical methods can be applied to Maxwell's equations. To produce a computation model for the propagation of electromagnetic waves through a medium, Maxwell's curl equations for a source free region with lossy materials are given by:

$$\frac{\partial \bar{H}}{\partial t} = -\frac{1}{\mu}\nabla \times \bar{E} - \frac{\rho}{\mu}\bar{H} \qquad \frac{\partial \bar{E}}{\partial t} = \frac{1}{\varepsilon}\nabla \times \bar{H} - \frac{\sigma}{\varepsilon}\bar{E}$$

These equations may be solved discretely by imposing a coordinate grid on the cell and surrounding area and by assuming that the E and H fields are constant throughout the discrete segments of the grid. This algorithm was first developed by K. S. Yee in 1966. The E and H fields alternate in space and time with the H fields occurring half a space-step and half a time step after the E fields to reduce numerical error.
To compute the discrete E and H fields, Maxwell's curl equations are broken into their vector components. For example, one of the components is explicitly written as:

$$\frac{\partial E_z}{\partial t} = \frac{1}{\varepsilon} * \left[\frac{\partial H_y}{\partial x} - \frac{\partial H_x}{\partial y} - \sigma E_z \right]$$

Each component may be written discretely be recognizing that the time derivative of a function, f, at a fixed point in space is approximately:

$$\frac{\partial f}{\partial t}_{i\Delta x, j\Delta y, k\Delta z} = \frac{f_{i,j,k}^{n+1/2} - f_{i,j,k}^{n-1/2}}{\Delta t}$$

Similarly, a first derivative in space with respect to the x dimension becomes:

$$\frac{\partial f}{\partial x}_{i\Delta x, j\Delta y, k\Delta z} = \frac{f_{i,j,k}^{n} - f_{i+1,j,k}^{n}}{\Delta x}$$

When the discrete forms of the derivatives are substituted into the curl equations, the E and H fields at a given point in space and time are known as a function of the field at a previous time step and neighboring fields. The E-field update equations are of the form:

$$E_{x|i,j,k}^{n+1} = \left[\frac{1 - \frac{\sigma_{i,j,k}\Delta t}{2\varepsilon_{i,j,k}}}{1 + \frac{\sigma_{i,j,k}\Delta t}{2\varepsilon_{i,j,k}}} \right] * E_{x|i,j,k}^{n} + \left[\frac{\frac{\Delta t}{\varepsilon_{i,j,k}}}{1 + \frac{\sigma_{i,j,k}\Delta t}{2\varepsilon_{i,j,k}}} \right] * \left[\frac{H_{z|i,j+1/2,k}^{n+1/2} - H_{z|i,j-1/2,k}^{n+1/2}}{\Delta y} - \frac{H_{y|i,j,k+1/2}^{n+1/2} - H_{y|i,j,k-1/2}^{n+1/2}}{\Delta z} \right]$$

The H-field update equations have a similar form:

$$H_{x|i,j,k}^{n+1/2} = \left[\frac{1 - \frac{\rho_{i,j,k}\Delta t}{2\mu_{i,j,k}}}{1 + \frac{\rho_{i,j,k}\Delta t}{2\mu_{i,j,k}}} \right] * H_{x|i,j,k}^{n-1/2} + \left[\frac{\frac{\Delta t}{\mu_{i,j,k}}}{1 + \frac{\rho_{i,j,k}\Delta t}{2\mu_{i,j,k}}} \right] * \left[\frac{E_{y|i,j,k+1/2}^{n} - E_{y|i,j,k-1/2}^{n}}{\Delta z} - \frac{E_{z|i,j+1/2,k}^{n} - E_{y|i,j-1/2,k}^{n}}{\Delta y} \right]$$

Examples of the results of wave analysis are shown in Figures 3 and 4. Figure 3 compares calculated absorbance of two silicon films with a thickness of 2.2 μm and a backside texture of 0.4 μm and 0.2 μm; these are referred as 1 and 2 in the figure. For comparison, we have included results of ray analysis for the same device. It is seen that the ray analysis gives higher absorbance representing nearly the envelope of fringes in the wave analysis. The effect of reducing the texture height is to reduce the fringe amplitude. Figure 4 demonstrates the effect of changing film thickness from 2.2 μm to

1.1 μm, while keeping the texture height at 0.2 μm; the data for these thicknesses are referred as 2 and 3, respectively, in the figure. Again, for comparison we show ray analysis results. The effect of changing the film thickness on the absorbance is seen to lower the envelope of the absorbance curve.

From the above results it is clear that for small thicknesses of the silicon film and for small texture size the ray analysis gives higher absorbance values than the wave analysis. The wave analysis includes the effect of both the light scattering due to texture and the interference effects associated with thin films. The results presented here are only meant to demonstrate the errors in using ray analysis for rough or textured thin-film solar cells. The method we have developed will be used to arrive at the cell designs that can optimize the cell performance. A unique feature of our analyses is that they will give three-dimensional distributions of photon flux within the cell. These absorbed photon distributions will allow accurate modelling of solar-cell parameters.

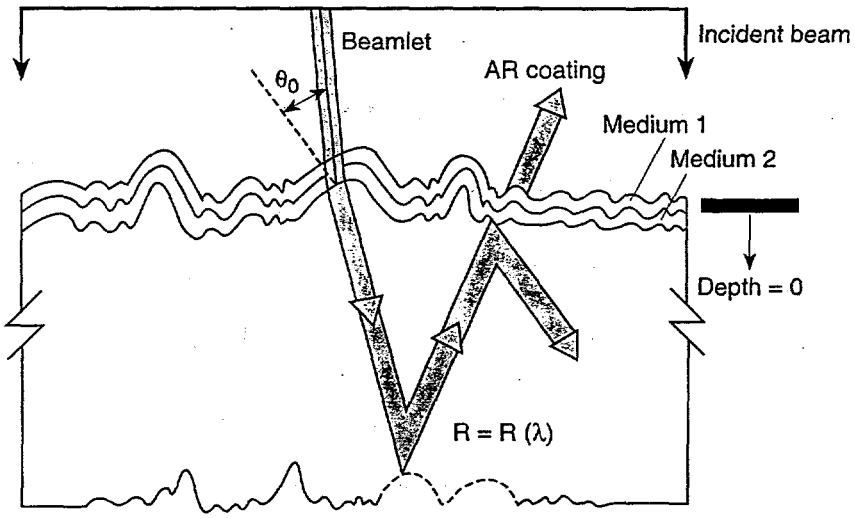

Figure 1
A schematic of the ray optics model

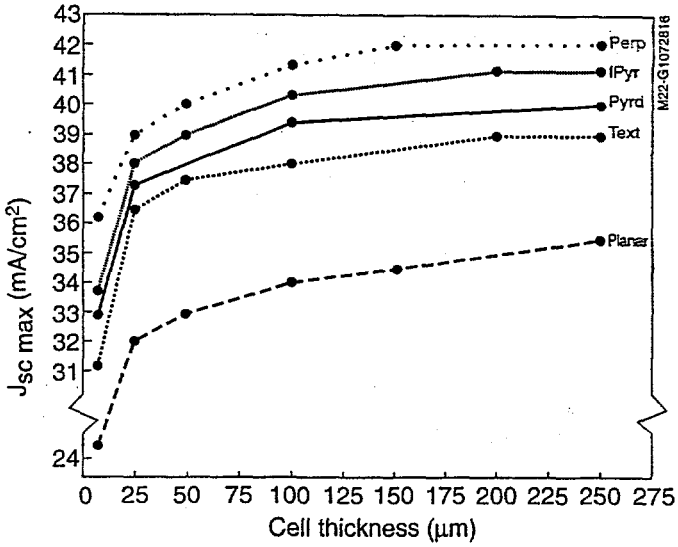

Figure 2. Calculated dependence of J_{SC}(max) on the cell thickness

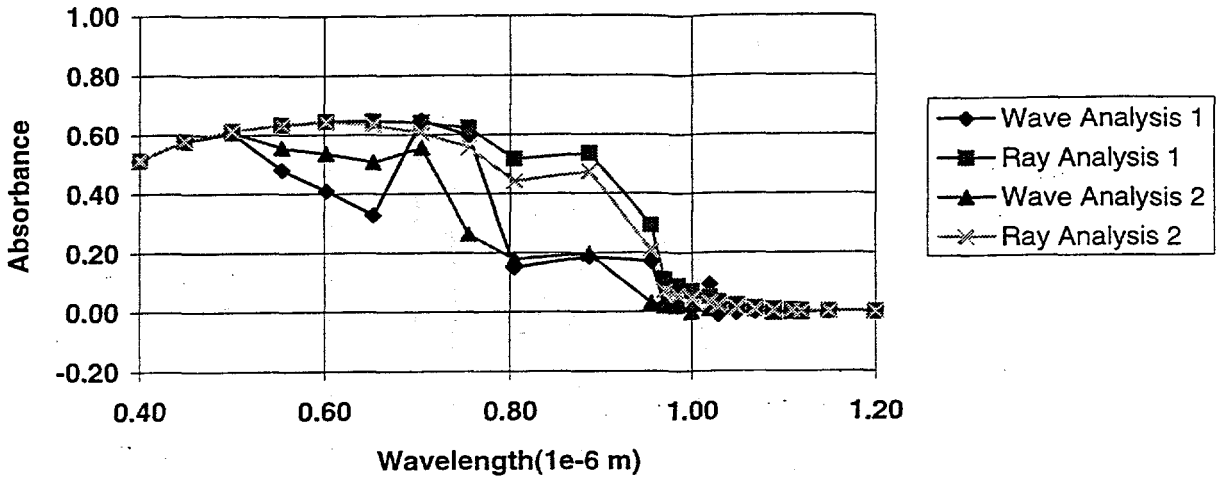

Figure 3. Calculated results showing effect of texture height on absorbance

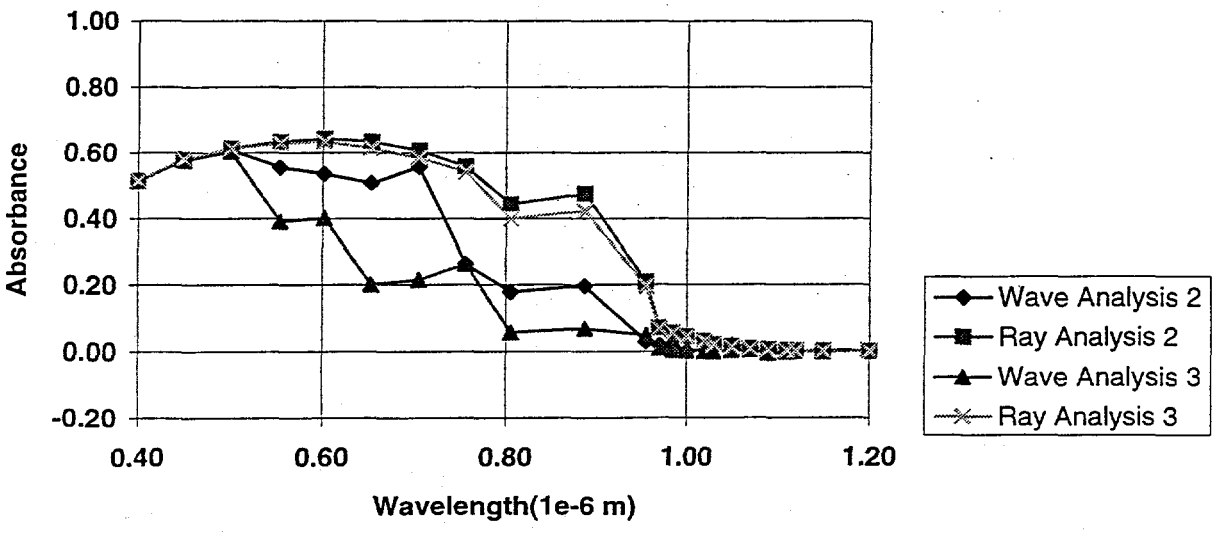

Figure 4. Calculated results showing effect of cell thickness on absorbance

Acknowledgment

This work was supported by the U.S. Department of Energy under Contract No. DE-AC02-83CH10093.

Reference

(1) B. L. Sopori and T. Marshall, Proc. 23rd IEEE PVSC127(1993), and references therein.

EXTENDED ABSTRACT

BURIED CONTACT MULTIJUNCTION THIN FILM SILICON SOLAR CELL

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1. INTRODUCTION

In early 1994, the Centre for Photovoltaic Devices and Systems announced the filing of patent applications on an improved silicon thin film photovoltaic module approach. With material costs estimated to be about 20 times lower than those in present silicon solar cell modules along with other production advantages, this technology appears likely to make low cost, high performance solar modules available for the first time.

The reasons for the anticipated low production costs are:

(i) The use of much less silicon in the completed modules, with the silicon layer being 10-20 microns thick rather than the 300-400 microns typically used in present commercial cells;
(ii) The material quality in the thin layers can be 100-1,000 times poorer than the worst material presently used in commercial production, as a consequence of the improved cell design;
(iii) Instead of the basic production unit being a cell of approximately 100 cm^2 area, the basic production unit with the new approach is a module which might typically be 1 m^2 in area, a factor of 100 times larger.

The following gives a broad outline of the fabrication steps involved in making a module as well as some of its more important performance features.

2. MODULE FABRICATION

Module fabrication is shown in Steps 1-5 of Figure 1.

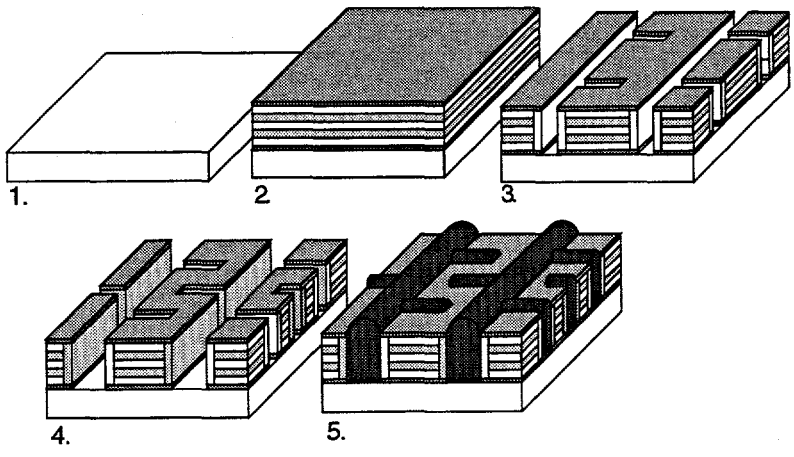

Figure 1: Fabrication of UNSW multilayer cells: 1. Glass superstrate; 2. Multilayer deposition; 3. First polarity groove; 4. Second polarity groove; 5. Metallization.

After cleaning the glass superstrate, a multilayer stack is deposited onto it by a technique such as chemical vapour deposition. The first layer is a dielectric such as silicon oxynitride/nitride followed by the deposition of several layers of silicon (typically 10) of alternating doping polarity. Finally, a silicon oxynitride/nitride layer is deposited on the top surface as a capping layer. The total thickness of the stack lies in the 10-20 micron range. Although the schematic shown in Figure 1 shows planar surfaces and interfaces, textured surfaces would be used in practice to encourage light trapping within the deposited stack. Various light trapping schemes have been demonstrated in the past.

The next stage in processing involves forming a set of grooves of one type of polarity (say, n-type) using a laser. After grooving and cleaning, the edge of this groove is doped. This is a standard technique used in the UNSW buried contact cell technology licensed to several companies for use with wafer substrates, and now being widely used in commercial product. This step essentially connects all the n-type layers within the stack in parallel.

The next stage involves the formation of a second set of grooves which then have their groove edges doped with the opposite polarity (p-type in the present example). This essentially connects all the p-type layers in the stack in parallel. Also, the p-type grooves overlap the original n-type grooves in the interconnection areas. This results in some areas which have one edge of the groove doped n-type adjacent to another edge doped p-type.

The grooved areas are then metallized as in the present example. This metallization not only performs the role of the normal fingers familiar from conventional solar cells, but also provides for automatic series interconnection of cells in the interconnection areas where n- and p-type grooves overlap.

A transparent rear cover (say, Tefzel) would then be laminated to the rear of the module.

The final module structure seen from the rear prior to this rear cover lamination is shown in Figure 2. The module would appear similar from the front but with the metal pattern somewhat finer.

In this example, the module would have a bifacial response - it would respond to light coming from either direction. Past studies by our group, using standard photovoltaic system computer modelling programs, show that about 20% extra energy would be collected by having this bifacial response in a normal "open back" mounting configuration. This is without taking any special steps to use the bifacial response to advantage. Schemes such as mounting modules in an area with a higher ground albedo (for example, by using white pebbles to cover the ground) would give additional boost from this rear response.

During fabrication, the basic processing unit would be the entire module. As apparent from Figure 2, it would consist of a predetermined number of series interconnected sub-units generating a current output determined by the size of the sub-unit and a voltage output determined by the number of sub-units connected in series (this sub-unit is the area between the horizontal stripes in Figure 2).

Although cells operate on completely different principles and are expected to have completely different performance characteristics from amorphous silicon cells, the fabrication equipment would be very similar to that used in producing present thin film modules based on amorphous silicon. Substrate cleaning steps would be similar, although there is no need for a transparent conducting oxide in the present cells designs due to the high lateral conductivity of cell material. Layer deposition would be at high temperature in the present case, narrowing the range of useable glasses. Much of the work done on deposition over large areas in the amorphous silicon area could, however, be adapted to the present technology. Laser patterning over large areas is widely used in

amorphous silicon module manufacturing and the equipment developed for this purpose would also be useful in the present production. Fewer laser patterning steps are required in the present case than for amorphous silicon. The metallization step would involve different technology from that used with amorphous silicon, although it could be similar to the plating or screen printing processes used in present bulk silicon cell manufacture.

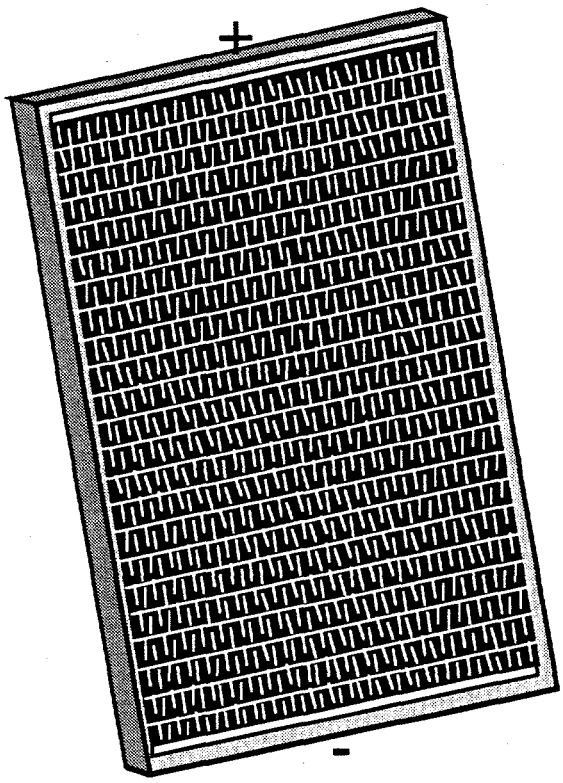

Figure 2: Module from rear. The horizontal stripes correspond to the interconnection areas. Figure 1 (Step 5) shows a close-up of the region between two consecutive stripes.

3. MODULE PERFORMANCE

Within each sub-unit, all layers of the same polarity are connected in parallel. The structure can therefore be thought of as a number of very thin cells all connected in parallel. The thickness of each layer is chosen to be smaller than the minority carrier diffusion length within that layer. (The minority carrier diffusion length is the distance a minority carrier will diffuse after generation by sunlight before recombining i.e., losing the energy given to it by the sunlight). This design feature means that all carriers generated by sunlight within the multilayer stack will be collected, i.e., contribute to the output current of the module. In a normal cell design, only those carriers generated within a diffusion length of the junction will be so collected. This is one of the main reasons why the performance of conventional cells falls off so rapidly with decreasing material quality.

Table 1 compares the performance of cells fabricated on good and bad quality material with both the conventional single junction approach and the present multijunction approach. For good material, the multijunction approach does not offer a significant performance advantage. However, as material quality deteriorates, the performance of the conventional approach drops off to unacceptably low efficiencies while the performance of the multilayer stack remains virtually unchanged, even for material 200 times poorer as shown.

Table 1: Upper limits upon the performance of thin film cells of conventional and multilayer design. The cases of good and bad material quality are compared assuming Lambertian light-trapping and a voltage cap of 650 mV.

Material Quality	Cell Junctions	Optimum Thickness	Maximum Efficiency
GOOD: 10 μs defect lifetime	Single	30 μm	21.7%
	Multiple	85 μm	22.4%
POOR: 50 ns defect lifetime	Single	2.5 μm	15.1%
	Multiple	25 μm	20.5%

This analysis simulates the case where the low material quality is a result of uniformly distributed defects. These defects may be chemical defects due to the use of less pure source materials or crystallographic defects such as due to dislocations. Another important type of defect in low quality material arises from grain boundaries between individual grains within the material. Conventional solar cell design is not particularly tolerant of such grains.

Figure 3 demonstrates the improved tolerance of the multilayer structure to a horizontal grain boundary. For an active horizontal grain boundary in a conventional cell, the grain boundary will compete with the cell junction for photogenerated carriers. This means that half the area between the grain boundary and the junction is rendered inactive as well as all regions of the cell lying on the opposite side of the grain boundary. However, in the multilayer stack, the effect of the grain boundary is localized to half the layer in which it lies.

Similarly, for a vertical grain boundary (Figure 4), all regions of the cell closer to the grain boundary than the junction will be rendered inactive from the point of view of current collection. However, in the case of the multilayer structure, only a small region adjacent to the grain is affected.

Similar considerations will apply to the more general case of grain boundaries running obliquely to the cell surface. Other effects such as shunting caused by preferential diffusion down grain boundaries can be accommodated in the new structure since layers of the same type are connected in parallel.

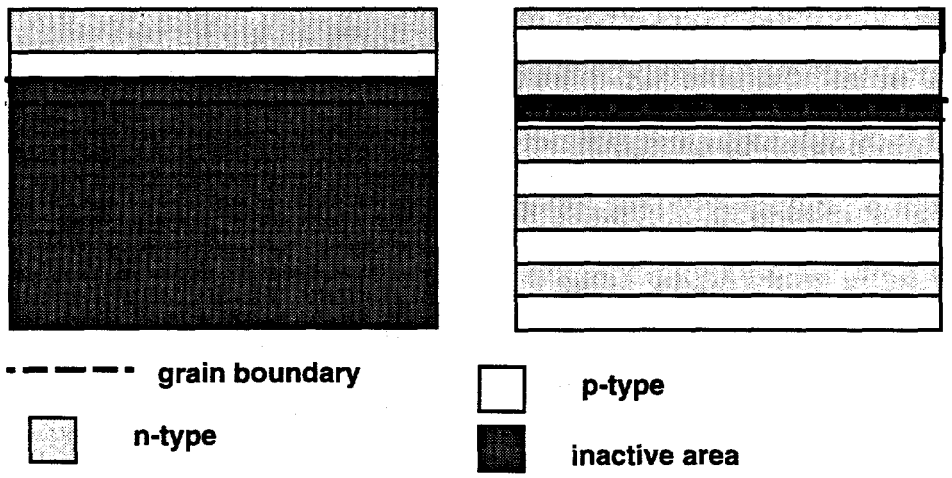

Figure 3: Conventional and multilayer cell tolerance to a horizontal grain boundary.

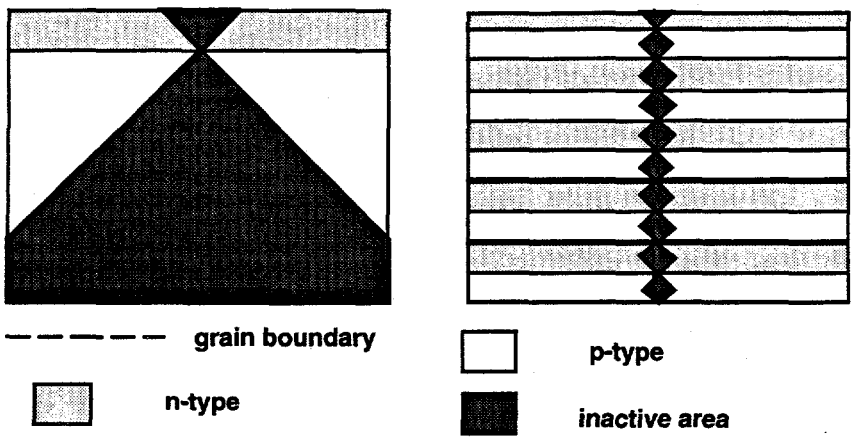

Figure 4: Conventional and multilayer cell tolerance to a vertical grain boundary.

The increased junction area in the multilayer approach will cause increased emphasis on junction processes, particularly processes such as trap-assisted tunnelling which might be expected to become important in low quality material.

For low quality material where material properties are dominated by defects, the most appropriate doping levels within the layers would be the heaviest possible without the high doping level contributing to greatly decreased diffusion lengths. This will maximize the open circuit voltage by minimizing the minority carrier densities throughout the cell.

4. RESISTIVE FEATURES

From the device analysis point of view, resistive effects within the layers are particularly interesting. This is as a consequence of the design criteria that the thickness of each multilayer be smaller than a diffusion length. This allows for carrier injection between the layers when voltage differences arise between them due to resistive current flow along them. This will have the effect of shuffling current, most of which is generated near the surface down to deeper layers for collection. An upper bound upon the effective sheet resistivity of these layers is the sheet resistivity of the uppermost layer as in conventional solar cells. However, a lower bound is the sheet resistivity of all like polarity layers in parallel, which can be over an order of magnitude lower.

5. CONCLUSION

The UNSW buried contact multijunction cell combines three innovations to produce a unique device structure which allows high efficiency cells to be produced on low quality material. The first innovation is the use of the multilayer structure, which provides the tolerance to low quality material. The second is the use of the well proven buried contact technology. In addition to the strengths that make this the most successfully commercialized of all new solar cell technology over the last 15 years, additional advantages arise in the present case in the ability of the buried contact to connect like polarity layers in parallel. The third innovation is the simple technique for connecting cells in series which relies on having grooves of different polarity either overlapping or in close proximity to each other. All three innovations are the subject of patent applications.

These three innovations combine to produce a manufacturing approach with a small number of processing steps able to produce high efficiency product with low quality starting material. The unit of production is a large module of approximately 1 m^2 in area rather than the smaller 100 cm^2 cells which are the present commercial norm.

Thin Film Polycrystalline Silicon: Promise and Problems in Displays and Solar Cells

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I. Introduction

Thin film polycrystalline Si (poly-Si) with its carrier mobilities, potentially good stability, low intragrain defect density, compatibility with silicon processing, and ease of doping activation is an interesting material for "macroelectronics" applications such as TFTs for displays and solar cells. The poly-Si films needed for these applications can be ultra-thin — in the 500Å to 1000Å thickness range for flat panel display TFTs and in the 4μm to 10μm thickness range for solar cells. Because the films needed for these macroelectronics applications can be so thin, an effective approach to producing the films is that of crystallizing a-Si precursor material. Unlike cast materials, poly-Si films made this way can be produced using low temperature processing. Unlike deposited poly-Si films, these crystallized poly-Si films can have grain widths that are much larger than the film thickness and almost atomically smooth surfaces. This thin film poly-Si crystallized from a-Si precursor films, and its promise and problems for TFTs and solar cells, is the focus of this discussion [1].

Because the energy stored in an a-Si matrix can aid in the crystallization process, the thermal budget for producing large grain poly-Si from a-Si ultra-thin precursor films can be relatively low (e.g., crystallization in 5 minutes for $T \leq 650°C$). In addition the process can be catalyzed by surface treatments further lowering the thermal budget and providing the opportunity for selective crystallization for isolation of solar cells in series, etc. [2]. Since the deposition process of the precursor a-Si film can be low temperature (e.g., PECVD, LPCVD, or sputtering) and since the crystallization process can be low temperature, inexpensive substrates such as glass can be used [1-8]. In all cases, defects remain after crystallization, at least in the grain boundary regions. Hence, grain boundary passivation is an integral part of any processing flow using the approach [1].

II. The Crystallization Process

Fig 1 shows the general poly-Si film process flow under discussion here. The a-Si is deposited by one of the well established, large-area deposition approaches shown. The deposition rates can easily be in a range acceptable for needed through-put. For example, even PECVD is capable of depositing these precursor films at rates of 20Å/sec, if microwave plasmas are used. This film is then crystallized into poly-Si using rapid thermal annealing (RTA) or furnace annealing solid phase crystallization (SPC) or using

laser annealing. Fig 2 shows a poly-Si film produced using SPC of PECVD a-Si.. This poly-Si film is on 7059 glass, is 1000Å thick and has an average grain size > 3μm. Table I lists the potential advantages of thin film poly-Si produced as shown in Fig 1.

Table II gives a summary of the results obtained to-date for the process flow outlined in Fig 1 as a function of (1) the precursor film deposition approach, (2) the crystallization step, and (3) the macroelectronics device application (i.e., solar cell or TFT). Table III gives some specific information on the various crystallization approaches; i.e., RTA SPC, furnace SPC, and laser crystallization and Table IV gives some specific information on the catalyst-assisted crystallization process.

III. The Promise and Problems for Display TFTs

Just as in the solar cell case, the principal thin film competitor to poly-Si for display applications is amorphous silicon itself. However, as shown in Table I, thin film poly-Si crystallized from a-Si precursor films offers a number of advantages for TFT applications in active matrix liquid crystal (AMLCD) and active matrix electroluminescent displays (AMELD). These advantages range from leveraging the capital investment already in place for large area a-Si deposition equipment used for a-Si solar cells and for a-Si AMLCDs to ease of doping both n-type and p-type for n-channel and p-channel devices (and, therefore, CMOS circuitry). Most importantly, poly-Si TFTs offer the advantages of potentially better stability, lower defect density, and higher mobilities (which translate into potentially faster devices with higher drive currents). Poly-Si TFTs also have additional advantages not listed in the table such as the fact that the poly-Si approach for TFTs allows the use of SiO_2 for the gate dielectrics (SiN_x is the better gate dielectric for a-Si TFTs), regular top-gate configurations (inverted gate structures are better for a-Si TFTs), and the use of self-aligned structures (cf. Fig. 3).

However, the use of poly-Si films for display TFTs is not without its problems. These are listed in Table V. From this table one can see that there are basically two classes of problems: (1) controlling the laser or SPC crystallization and (2) the fundamental band gap difference between a-Si and poly-Si. Since laser crystallization is a rastering process, it can leave "raster boundaries" in the resulting film and these can show up in device characteristics as seen in Fig. 4. RTA is a very attractive approach to SPC but it too has process control problems as seen in Table V. However, solutions have been attained at least in research environments to many of these problems.

The question of off-current for poly-Si TFTs is often raised (see Table V) and cited as the reason a-Si TFTs will continue to be used in displays. In fact the on-off ratios of poly-Si TFTs can be as good as 10^7-10^8 (see Fig. 4 and ref. 5); but, they are usually not as good as those of a-Si and the band gap difference (a-Si has $E_g \sim 1.70$eV; poly-Si has $E_g \sim 1.1$ eV) is cited as the reason. It is important to note, however, that

crystalline Si FETs have on-off ratios of ~10^{10} so reduced grain boundary effects should push poly-Si TFTs closer to this ceiling.

IV. The Promise and Problems for Solar Cells

The principal thin film competitor to ultra-thin poly-Si solar cells based on a-Si precursor films is a-Si solar cells themselves as well as copper indium diselenide solar cells. However, as seen in Table I, the crystallized ultra-thin film poly-Si approach again offers a number of advantages. Not to be overstated is the advantage of ease of silicon processing which becomes completely available in the case of poly-Si. However, the approach of crystallizing ultra-thin a-Si into poly-Si for solar cell structures also has a number of problems as noted in Table VI. The first three of these are shared with TFTs as seen by comparing with Table V and the latter two problems in Table VI have the same origin as the last problem in Table V; i.e., the band gap width and optical transition selection rules change in going from a-Si to poly-Si.

As may be noted from Table I, there is very little published solar cell work using crystallized poly-Si from a-Si precursor films. There is actually only the reports of the Japanese group (represented by ref. 8). Work from a Swiss group has focused on deposited, microcrystalline Si for solar cell applications [9]. This is a very different approach from that under discussion here.

Some preliminary simulations have been undertaken, however, exploring this ultra-thin poly-Si film approach for solar cells and results are presented in Tables VII-X. These simulations were done using the AMPS computer code. The p-i-n structure shown in Fig 5 was assumed and the i-layer thicknesses explored are shown in Tables VII-X. The results in these tables are for one-dimensional simulations; hence, the effects of the lateral grain boundary recombination are lumped into an effective intragrain defect density. However, the effects of grain boundaries perpendicular to the current flow are explicitly modeled. The grain boundary density of states (DOS) used in this modeling is seen in Fig. 6. As can be seen, both band tails and Gaussian gap states were used. The total number of states in the Gaussians in the grain boundaries was varied as listed in Tables III-IX. For the intragrain regions, the DOS was taken as flat, switching from donor-like to acceptor-like at mid-gap. The total number of these states in the intragrain regions was also varied as listed in Tables VII-X.

A possible processing flow that can then be envisaged leading to the device structure of Fig. 5 is one where a doped (n or p) ultra-thin a-Si layer is first deposited, followed by the i-layer a-Si absorber, and then by a doped (p or n) ultra-thin a-Si layer. All layers are then crystallized into poly-Si using RTA SPC. There is an existence proof that the dopants will not intermix across the 4-10μm i-layer; i.e., RTA has been

used to form poly-Si TFTs with the source and drain doping layers present and intermixing down a 5μm channel length is not a problem [5].

The simulation results of Tables VII-X show first of all that ultra-thin Si films even only in the 4μm-8μm thickness range have a good chance of easily giving stable solar cell efficiencies in the 8-10% range. Some cases also make the point that thicker is not necessarily better. It must be noted that all these results are for single junction structures; hence, multijunction structures offer more possibilities. These results also suggest that 15% efficiencies are attainable with high quality poly-Si with slightly thicker i-layers. These results very strongly underscore the critical importance of light trapping in these very thin layers of indirect-gap poly-Si.

V. Summary

There is a great deal of overlap in the advantages — and in the research and development work still needed for — ultra-thin film poly-Si for display TFTs and solar cells. This ultra-thin crystallized poly-Si approach to TFTs and solar cells using a-Si precursors leverages off of the extensive deposition technology already available for large area a-Si deposition and off of the existing, extensive silicon processing technology. Research results in our group strongly suggest that the best path to follow for this processing involves rapid thermal annealing and catalyzed crystallization.

Acknowledgment

The experimental and simulation work at Penn State is supported by ARPA, EPRI, and NREL. The AMPS computer program was developed under the auspices of EPRI.

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Process Flow

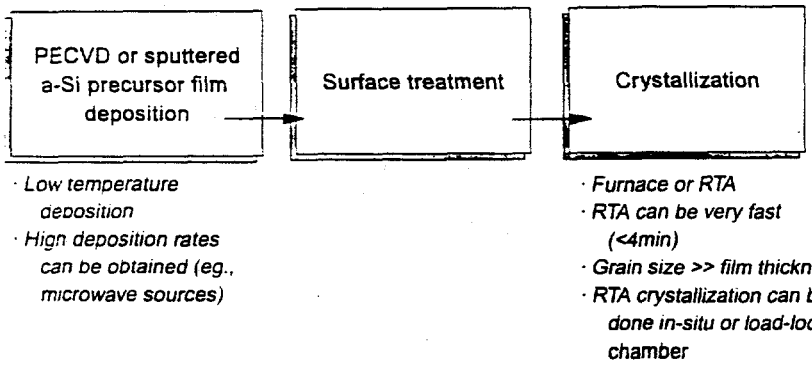

Figure 1. Low thermal budget process flow for high quality poly-Si

Fig 2: TEM micrograph of an SPC poly-Si film. This film is on 7059 glass and it was crystallized at 650°C.

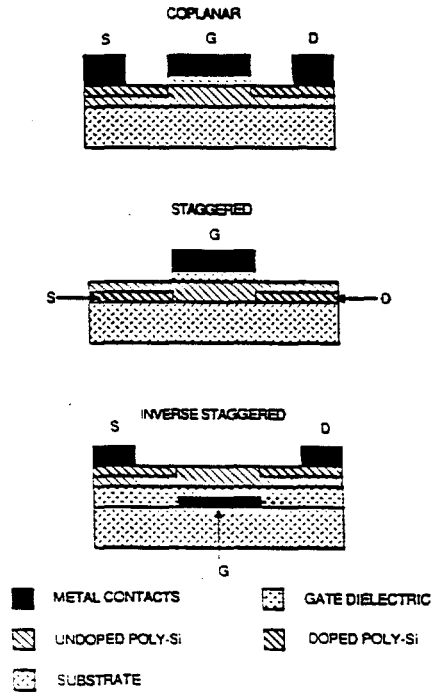

Fig 3: Three different structures of poly-Si TFTs.

Table I
Some Advantages of Thin Film Poly-Si TFTs and Solar Cells
Produced from a-Si Precursor Films

For TFTs for Displays	For Solar Cells
(1) Produced from films deposited using well-established large area deposition approaches with high through-put possible	same
(2) Extremely smooth surfaces for reduction of high field asperity regions and good interface quality	same
(3) Large grain size to thickness ratio	same
(4) Stored energy in a-Si matrix allows ease of solid phase and laser crystallization	same
(5) Selective crystallization possible	same
(6) Ease of doping activation for poly-Si compared to a-Si; n-type and p-type doping easily attained	same
(7) Resulting poly-Si is potentially more stable than a-Si	same
(8) Resulting poly-Si has higher carrier mobilities than corresponding a-Si	same
(9) Resulting poly-Si has lower (intragrain) defect density than a-Si	same

Table II
Some Results Obtained To-date
Following the Process Flow of Fig 1

Precursor film	Treatment for Catalyzing Crystallization	Crystallization Step	Macroelectronics Device	Reference
Sputtered a-Si	----	RTA SPC Furnace SPC	TFTs	3
Sputtered a-Si	----	Laser	TFTs	4
PECVD a-Si	----	RTA SPC Furnace SPC	TFTs	5, 6 (general review)
PECVD a-Si	metal catalyzed	Furnace SPC	TFTs	7
PECVD a-Si	----	Laser	TFTs	6 (general review)
LPCVD a-Si	----	Furnace SPC	TFTs	6 (general review)
LPCVD a-Si	----	Laser	TFTs	6 (general review)
PECVD a-Si	Doping and substrate texturing	Furnace SPC	Solar cells	8

Table III
Some Data on Various Crystallization Processes and Compatability with 7059 Glass

	Process	Crystallization time (min.)	Process Temperature (°C)	Glass substrate	Glass shrinkage (%)
Our Research	RTA SPC	5	700	Yes	0.04
	Pd assisted Furnace SPC	120	600	Yes	0.2†
	Selected, Pd assisted Furnace SPC	120	600	Yes	0.2†
Literature	Furnace SPC	>600	600	No	---
	Laser*	10**	---	Yes	---

*: The laser anneal process does not have a good reproducibility at present.
**: The crystallization time of this process depends on the sample size.
† Note: The longer time of furnace SPC leads to more glass shrinkage.

Table IV
Metal Catalyst Enhanced Crystallization with Different Top Metal Layers after a 650°C/5 min. Annealing

	CRYSTALLIZATION
CONTROL	No
Pd	Yes
Al	No
Au	No
Ni	Yes
Ti	No

Table V
Some Specific Problems for Poly-Si TFTs
Using the Process Flow of Fig. 1

Problem Area	Impact
Laser crystallization non-uniformities	Device behavior variations, See Fig. 4
RTA SPC thermal stress, non-uniform heating and hydrogen evolution for some films	Glass warpage, glass flow, film disruption
Furnace Annealing Times	Probably a through-put problem
Off-current	Can be high due to defects at grain boundaries and lower band gap compared to a-Si TFTs

Table VI
Some Specific Problems for Ultra-thin Film Poly-Si Solar Cells
Using the Process Flow of Fig. 1

Problem Area	Impact
Laser crystallization non-uniformities	Device behavior variations. See Fig. 4
RTA SPC thermal stress, non-uniform heating, and hydrogen evolution for some films	Glass warpage, glass flow, film disruption
Furnace Annealing times	Probably a through-put problem
Lower band gap than a-Si	Lower V_{oc}
Indirect band gap	Crucial need for light trapping structures (See Tables VII, VIII, IX, and X)

Table VII

Cases with Grain Boundaries Perpendicular to Carrier Flow
Grain Boundary Midgap Defect Density: $5.0*10^{16}$ cm^{-3}
Intragrain Mobilities: μ_n = 1350 cm^2/Vsec, μ_p = 480 cm^2/Vsec
Flat Midgap DOS in Intragrain Regions: $1.0*10^{15}$ $cm^{-3}eV^{-1}$

Thickness		4 μm		8 μm	
Optical Enhcmnt.			x		x
Grain Size	0.57 μm	7.5%	10.1%	7.9%	10.3%
	1.00 μm	8.1%	10.9%	8.6%	11.2%

Table VIII

Cases with Grain Boundaries Perpendicular to Carrier Flow
Grain Boundary Midgap Defect Density: $5.0*10^{17}$ cm^{-3}
Intragrain Mobilities: μ_n = 1350 cm^2/Vsec, μ_p = 480 cm^2/Vsec
Flat Midgap DOS in Intragrain Regions: $1.0*10^{15}$ $cm^{-3}eV^{-1}$

Thickness		4 μm		8 μm	
Optical Enhcmnt.			x		x
Grain Size	0.57 μm	5.1%	6.9%	4.1%	5.1%
	1.00 μm	6.0%	8.1%	5.4%	7.0%

Table IX

Cases with Grain Boundaries Perpendicular to Carrier Flow
Grain Boundary Midgap Defect Density: $5.0*10^{16}$ cm^{-3}
Intragrain Mobilities: μ_n = 750 cm^2/Vsec, μ_p = 250 cm^2/Vsec
Flat Midgap DOS in Intragrain Regions: $1.0*10^{15}$ $cm^{-3}eV^{-1}$

Thickness		4 μm		8 μm	
Optical Enhcmnt			x		x
Grain Size	0.57 μm	7.5%	10.1%	7.6%	10.0%
	1.00 μm	8.1%	10.8% 8.4%*	8.5%	11.0% 7.8%*

*Gaussian midgap DOS in intragrain regions: $1.0*10^{15}$ cm^{-3}

Table X

Cases with no Grain Boundaries Perpendicular to Carrier Flow
Carrier Mobilities: μ_n = 1350 cm^2/Vsec, μ_p = 480 cm^2/Vsec
Flat Midgap DOS

Thickness		4 μm		8 μm	
Optical Enhcmnt.			x		x
Midgap DOS ($cm^{-3}eV^{-1}$)	$1.0*10^{15}$	9.1%	12.1%	10.4%	13.4%
	$1.0*10^{16}$	7.5%	10.1%	8.0%	10.4%

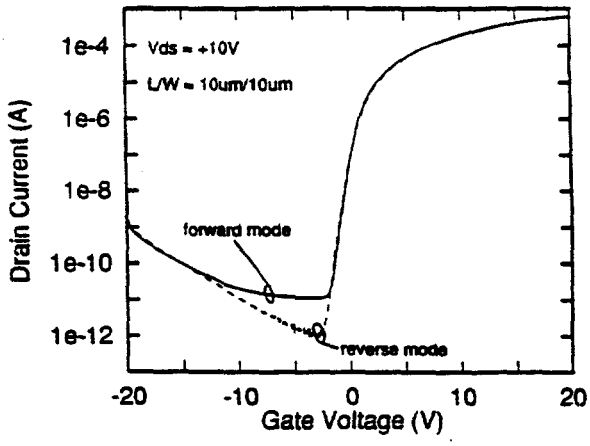

Fig 4: Poly-Si TFT using laser crystallized a-Si precursor material. Reverse mode means the role of source and drain has been switched. Forward mode reveals more defects on the side of the device near the border of the laser scan.

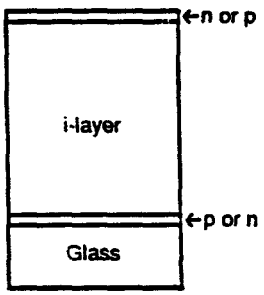

Fig 5: The p-i-n structure used for preliminary simulations. The i-layer thicknesses explored are shown in Tables VII-X.

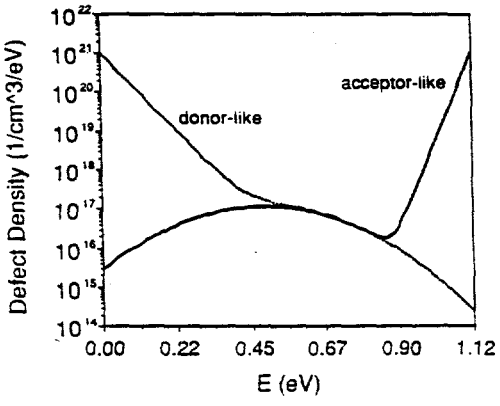

Fig 6: The grain boundary density of states used for modeling of p-i-n solar cells.

Fundamentals of Thin Solar Cells

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It is now widely recognized that thin solar cells can present certain advantages for performance and cost. This is particularly the case when light trapping in the semiconductor film is incorporated, as compensation for the diminished single path thickness of the solar cell.

In a solar cell thinner than a minority carrier diffusion length, the current collection is of course very easy. More importantly the concentration of an equivalent number of carriers in a thinner volume results in a higher Free Energy, or open circuit voltage. This extra Free Energy may be regarded as due to the concentration factor, just as it would be for photons, electrons, or for any chemical species. The final advantage of a thin solar cell is in the diminished material usage, a factor of considerable importance when we consider the material cost of the high quality semiconductors which we hope to employ.

The basic thickness reduction factor in solar cells is $4n^2 \approx 50$, where $n \approx 3.5$ is the typical semiconductor refractive index. The incorporation of the light trapping effect results in a new thickness optimization in solar cell design. The tradeoff works as follows: Greater thickness means higher current, but less voltage; and a thinner active layer means less current but higher voltage. The new optimum incorporating light trapping is usually $4n^2$ times thinner, and has $kT \ln 4n^2$ additional voltage at the operating point.

Thin solar cell designs are close to the main stream of opto-electronics. For example, there is every reason to design in a double heterostructure, as in most other types of opto-electronic devices. For solar cells however the meaning of a hetero-contact is more general as it may be represented by a Silicon Dioxide layer with a few point contacts in it or in some other innovative and creative way.

Once the design is settled, the main challenging issue is to produce high quality thin semiconducting films at a reasonable cost. The thickness reduction makes this job easier, but it is still a significant engineering and scientific task. There have been some approaches for doing this in Silicon, but these are often at the penalty of material quality. In some respects these engineering difficulties may be more tractable in the compound semiconductors.

Gettering of Metal Impurities in Silicon

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I. Gettering mechanisms

Gettering means the removal of metallic impurtities from the device-active area of the wafer by transport to a predesigned region — called gettering layer (GL). Figure 1 shows schematically the two areas. Between them we introduce an interface at $z = d_{GL}$, at which the effect of the gettering mechanism on the metal impurity distribution in the wafer is quantified, e.g. by specifying currents or by interfacial reactions of metal impurities, self interstitials etc. between GL and wafer. In response metal impurities will diffuse out of the wafer into the gettering layer. Following such a concept, in general three species of the metal impurity (M) are involved in gettering: $M_p \rightarrow M_i \rightarrow M_{GL}$.

M_p denotes immobile species in the wafer, which are precipitated into silicides or segregated at extended defects or whose diffusivity is too small to contribute noticeably to transport during the gettering procedure — like many substitutional metal species.

M_i, the mobile species is in all cases, investigated so far in the literature, the interstitial one. We mention that the 3d–elements dissolve mainly on interstitial sites in intrinsic silicon, and that especially Fe, Ni, and Cu, which have played a dominant role as impurities causing detrimental effects in silicon device technology, diffuse very fast ([1]). The diffusivities of Fe, Ni, and Cu at 900°C of $1.6 \cdot 10^{-6}\mathrm{cm}^2/\mathrm{s}$, $1.9 \cdot 10^{-5}\mathrm{cm}^2/\mathrm{s}$, and $6.6 \cdot 10^{-5}\mathrm{cm}^2/\mathrm{s}$, respectively are among the largest values known for solids. Therefore Ni and Cu cannot be quenched in their interstitial sites, instead they always precipitate into $NiSi_2$ and Cu_3Si, respectively. On the other hand, we mention that Au dissolves mainly on substitutional sites (Au_s) in silicon and only with a small fraction on interstitial sites ([2]). Yet diffusion of Au_s via a vacancy mechanism has been found to be slower than a three–step mechanism, consisting of diffusion of Au_i, its transformation to Au_s, whereby a silicon interstitial I is generated (kick-out reaction: $Au_s + I \rightleftharpoons Au_i$), and backdiffusion of I ([3]). As we shall see, the dissolution of metal silicides, the kick–out reaction of Au_s, or the diffusion of M_i in general determine the dynamics of gettering.

M_{GL}, the gettered metal impurity has been identified with a variety of species. According to the mechanism, by which the gettered species M_{GL} is generated, gettering has been arranged into three classes: relaxation–induced, segregation–induced, and injection–induced ([7]).

Relaxation-induced gettering requires supersaturation of metal impurities, which is achieved during cooling of the wafer. Along with a sufficient diffusivity a higher density of heterogeneous nucleation sites for metal impurity precipitation is needed in the gettering layer GL than in the device–active area. The higher density of nucleation sites provides metal impurity precipitation at smaller supersaturation in GL than in the device–active area, resulting in a concentration gradient of the diffusing metal impurity species. For a given distribution of nucleation sites the efficiency of this type of gettering can be optimized by choosing cooling conditions so that nucleation of precipitates is avoided in the device–active area. A well–known gettering technique of this class is internal gettering of Cz–Si, which was first introduced by Tan et al. ([4]) and has become a standard technique in silicon device technology. For polycrystalline solar silicon it might be difficult to design a procedure,

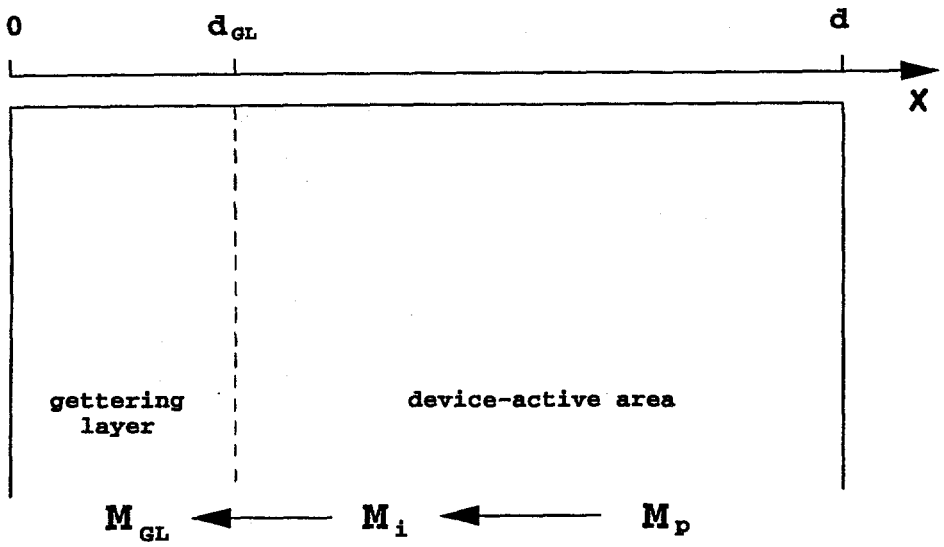

Figure 1: Gettering of metal impurities requires the transformation from its immobile state M_p (precipitated, paired with dopant atom, substitutional) to a mobile one M_i (interstitial), transport of M_i to the gettering layer, and transformatioin of M_i into the gettered species M_{GL}.

which utilizes relaxation–induced gettering, since the as–grown material already contains a significant density of effective nucleation sites (grain boundaries, dislocations, "microdefects" etc.) for metal impurity precipitation.

Segregation– and injection–induced gettering do not require a supersaturation of metal impurities in the wafer. The gettering layer collects metal impurities during the high-temperature treatment thus reducing the metal impurity concentration in the device-active area well below the solubility. Such gettering action may come about by an enhanced solubility of metal impurities, pairing of M with dopant atoms or by stabilization of a new compound in the gettering layer. It has been called segregation–induced gettering. A well–established process using this type of gettering is Al–gettering ([5]). The phase diagram of Si–Al shows a simple eutectic with a eutectic temperature of $T_{eut} = 850$K. Consequently, on top of a wafer which has been covered with an Al–layer and heated to $T > T_{eut}$, a layer of Al–Si–melt will form. The solubility of metal impurities in the Al–Si–melt is of the order of several atomic percent compared to $4.4 \cdot 10^{-4}$ at%, $1.5 \cdot 10^{-4}$ at%, and $8.5 \cdot 10^{-8}$ at% for Cu, Ni, and Fe in intrinsic silicon at 900°C ([1]). Therefore metal impurities will segregate in the melt until the ratio of their concentrations in the melt and in the wafer will be equal to the segregation coefficient. Professor Tan in his lecture will present a quantitative model of segregation dynamics as well as numerical results for the distribution of Au after Al–gettering.

Injection–induced gettering operates during high–temperature treatment as well. It is based on the coupling of metal impurities to other diffusion currents, e.g. that of silicon interstitials ([6]). Such processes have to be discribed by concepts of irreversible thermodynamics and will be outlined in some detail below for the case of phosphorus diffusion gettering.

II. Phosphorus diffusion gettering (PDG)

In a typical PDG–procedure P diffuses into the silicon wafer from a phosphorus silicate glass layer, which e.g. is generated by reaction of a gas atmosphere (constituents e.g.: nitrogen, oxygen, and $POCl_3$) with the wafer at temperatures around $900°C$. In silicon a P–profile with a maximum P–donor concentration up to $3 \cdot 10^{20}\text{cm}^{-3}$ and a width of less than 1μm is built up ([8]). In addition silicon interstitials are injected into the wafer in concentration c_I largely exceeding the equilibrium

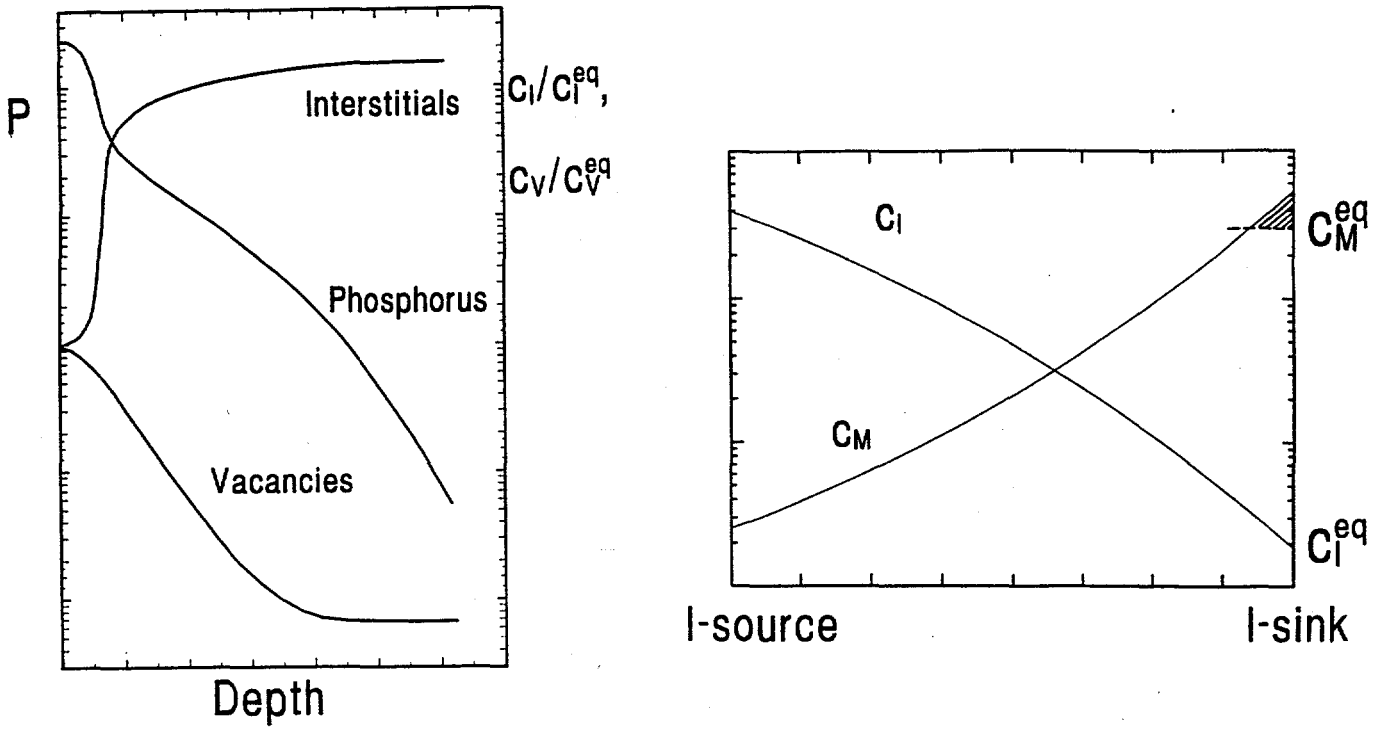

Figure 2: **a)** Schematic representation of a P–profile with the corresponding supersaturation of self-interstitials I and undersaturation of vacancies V (after Orlowski [24]). **b)** Schematic representation of the distribution of I and M between I–source and I–sink in the stationary state ($j_M = 0$). The metal atoms accumulate at the I–sink and precipitate when the solubility is exceeded.

concentration c_I^{eq} ([9]). By interaction with P they strongly affect the P–concentration profile.

In the part of the layer, where the P–concentration exceeds the intrinsic carrier concentration n_i ($4 \cdot 10^{18}\text{cm}^{-3}$ at 900°C), the Fermi level E_f is shifted upwards in the band gap from its position in intrinsic silicon. Metal impurities introducing an acceptor level E_a into the band gap then gain electronic enthalpy by accepting electrons and thereby lower their partial enthalpy of solution. It has been shown that the solubility is now the sum extended over the charged species $M^{(-n)}$, each of which increases exponentially with $n(E_f - E_a)$ ([10]). Furthermore, the negatively charged metal atom $M^{(-n)}$ attracts phosphorus donors $P^{(+1)}$ and may form pairs of the type $M^{(-n)}P^{(+1)}$ ([11]–[13]). Solubility enhancement und pairing define a segregation–induced action of the highly P–doped gettering layer, which affects all metal impurities with one or more acceptor levels.

Investigations of solubility enhancement und pairing of Au ([11], [12]), Mn, Fe, Co ([13]), and Cu ([2], [12]) in homogeneously P–doped silicon wafers have shown, that in all cases it is the substitutional species, which introduces acceptor levels into the band gap. Therefore the species M_s and M_sP dominate the solubility of these elements in heavily P–doped silicon at high temperatures.

While in the 70's it was argued that segregation–induced gettering is the dominant mechanism of PDG, detailed studies of PDG of Co, Ni, Fe and recently of Au have demonstrated, that this mechanism can only account for a small fraction of measured concentrations of M_{GL}. The solubility of Co in Si doped with $3 \cdot 10^{20}$ P–atoms/cm^3 at 920°C has been estimated, considering the Fermi level effect and pairing with P, to be 10^{16}cm^{-3} (solubility in intrinsic silicon: 10^{14}cm^{-3}), while $c_{Co_{GL}} \geq 10^{18}\text{cm}^{-3}$ has been measured ([15]). A discrepancy of the same order has been recently found for Au in Si ([20], see below).

Injection–induced gettering arises from the interaction of metal impurities with excess silicon interstitials, which are introduced during phosphorus in–diffusion up to supersaturations $c_I/c_I^{eq} \approx 500$ in the silicon wafer ([21]). This I-supersaturation plays an important role in device fabrication because it gives rise to the emitter–push and related effects ([9]). Figure 2 a) shows a typical anomalous P–profile with a kink– and tail–region. As far as it is known today, the dominant I–source is located near to the kink, where pairs of P and I dissociate ($PI \rightarrow P + I$). The excess silicon interstitials diffuse into the bulk or back to the surface, the latter current is assumed to compensate the current of in–diffusing PI–pairs. On the basis of this mechanism several models of P–diffusion have been developed in the 80's, which account for the available data ([22]–[24]). Figure 2a) shows results, which have been obtained in a simulation of P–diffusion by Orlowski. Let us summarize the characteristic feature of the I–profile: it starts with the equilibrium value c_I^{eq} at the surface, shows a steep increase in the region of high P–concentrations, and reaches near to the kink a maximum value , which spreads gradually with time into the bulk ([16], [17]). We mention, that once the supersaturation in the bulk has established, large I–currents only occur in the gettering layer GL.

As mentioned above, an adequate description of PDG has to take into account the coupling between I–current and current of metal impurities. To our knowledge there is no evidence in the literature up to now, that I interact with M_i. On the other hand, the kick–out reaction $I + M_s \rightleftharpoons M_i$ is well established for Au in Si ([25], [26]), and we consider it also for the 3d–elements as the only reaction between I and M. Currents of vacancies which of course occur during phosphorus in–diffusion as well (see fig. 2a)) induce a drift current of M, which enhances the one induced by the I–current. They are not taken into account in the following, but could be easily included:

$$\mathbf{j}_M = -D_i \nabla c_{M_i} \tag{1}$$

To quantify the effect of coupling let us assume that local equilibrium with respect to kick-out reaction is established:

$$\frac{c_{M_s} c_I}{c_{M_i}} = \frac{c_{M_s}^{eq} c_I^{eq}}{c_{M_i}^{eq}} \doteq K c_I^{eq} \tag{2}$$

In this equation c_{M_s} and c_I represent sums over all charged species of M_s and I, since the electronic exchange between charged species should be faster than the kick-out reaction:

$$c_{M_i} = c_M - c_{M_s} \tag{3}$$

By writing the right–hand side of eq. (2) as $K c_I^{eq}$ it should be noted that both, K and c_I^{eq} depend on position, reflecting solubility and concentration changes due to P–doping, respectively.

With equations (1)–(3) the total current of metal impurities is given by:

$$\mathbf{j}_M = -D \nabla c_M + D c_M \nabla \log(1 + K c_I^{eq}/c_I) \tag{4}$$

with

$$D = \frac{D_i}{1 + K c_I^{eq}/c_I}. \tag{5}$$

In equation (4) $\mathbf{j}_M$ is written as a sum of a modified diffusion current and a drift current, the latter is directed towards sinks of self interstitials. Neglecting for a moment the dependence of K and c_I^{eq} on position, one sees from eq. (4) that the drift current moves metal impurities to the I–sinks against the M–diffusion current.

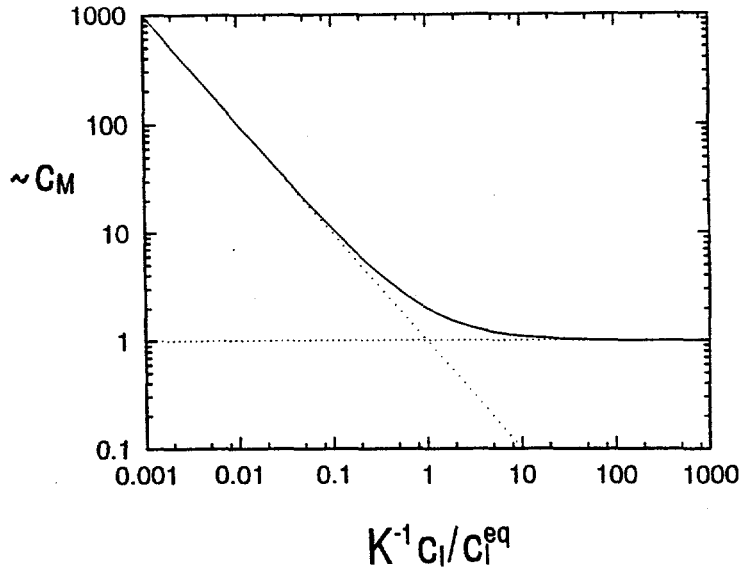

Figure 3: Metal concentration c_M in the stationary state as a function of the expression $K^{-1}c_I/c_I^{eq}$ according to eq. (6). Two limiting cases can be considered: for $K^{-1}c_I/c_I^{eq} \ll 1$, M and I couple effectively, whereas for $K^{-1}c_I/c_I^{eq} \gg 1$ no coupling is present. In the case of the 3d–elements effective coupling only occurs in the gettering layer due to solubility enhancement of the substitutional species.

The I–diffusion problem can be solved independently from eq. (4) only, if the I–current source (e.g. the region near to the kink of the P–profile) dominates the I–profile, which means, that annihilation of silicon interstitials by the kick–out reaction does not disturb the I–profile. Figure 2 b) shows M– and I–profiles between I–source and I–sink schematically for the case that drift and diffusion current become balanced. Please note that c_I, c_I^{eq} and K enter equation (4) only in the combination Kc_I^{eq}/c_I. At present computer simulation are applied to model PDG on the basis of eq. (4) with Kc_I^{eq}/c_I derived from simulations of P-diffusion.

If the M-concentration at the I–sink exceeds the M–solubility, metal silicide formation may occur (see fig. 2 b)). Indeed, after PDG of nickel and iron doped wafers $NiSi_2$– and $FeSi_2$–particles have been observed in the gettering layer by TEM, respectively ([18], [19]).

If no particles are formed in the gettering layer, equation (4) runs into a final state ($j_M = 0$), which is given by (s: surface, b: bulk)

$$c_M(x) = \frac{c_M^{(s)}}{1 + K^{(s)}}\left(1 + K(x)\frac{c_I^{eq}(x)}{c_I(x)}\right) \tag{6}$$

assuming that at the surface we have $c_I^{(s)} = c_I^{eq,(s)}$ (otherwise replace $K^{(s)}$ by $K^{(s)} \cdot c_I^{eq,(s)}/c_I^{(s)}$).

As we shall demonstrate, this relation can account for recent results on PDG of Au in Si, which have not found an explanation on the basis of segregation–induced gettering. Figure 3 shows c_M as a function of $(Kc_I^{eq}/c_I)^{-1}$). Two limiting cases can be considered: for $K^{-1}c_I/c_I^{eq} \ll 1$, M and I couple effectively, whereas for $K^{-1}c_I/c_I^{eq} \gg 1$ no coupling is present.

By making use of $c_{Au_s}^{eq} \gg c_{Au_i}^{eq}$, K can be seen to be directly proportional to the segregation

coefficient S:

$$K(x) = \frac{c_{Au_s}^{eq,(b)}}{c_{Au_i}^{eq}} \cdot S(x) \tag{7}$$

In this equation $c_{Au_s}^{eq,(b)}$ represent the solubility of Au_s in bulk silicon. The ratio of the gold concentration at the surface, $c_{Au}^{(s)}$, and of that in the bulk, $c_{Au}^{(b)}$, is related according to eq. (6) to the segregation coefficient at the surface, $S^{(s)}$ by:

$$\frac{c_{Au}^{(s)}}{c_{Au}^{(b)}} = \frac{(c_{Au_s}^{eq,(b)}/c_{Au_i}^{eq}) \cdot S^{(s)}}{1 + (c_{Au_s}^{eq,(b)}/c_{Au_i}^{eq})(c_I^{eq,(b)}/c_I^{(b)})} \tag{8}$$

$(c_I^{(eq,(b)}/c_I^{(b)})^{-1}$ denotes the supersaturation of I in the bulk.

Comparing the bulk value of I–supersaturation and the ratio of the bulk solubilities of substitutional and interstitial gold, we arrive at the two limiting cases:

$$\frac{c_{Au}^{(s)}}{c_{Au}^{(b)}} = \frac{c_I^{(b)}}{c_I^{eq,(b)}} \cdot S^{(s)} \qquad \text{for} \qquad \frac{c_I^{(b)}}{c_I^{eq,(b)}} \ll \frac{c_{Au_s}^{eq,(b)}}{c_{Au_i}^{eq}} \tag{9}$$

$$\frac{c_{Au}^{(s)}}{c_{Au}^{(b)}} = \frac{c_{Au_s}^{eq,(b)}}{c_{Au_i}^{eq}} \cdot S^{(s)} \qquad \text{for} \qquad \frac{c_I^{(b)}}{c_I^{eq,(b)}} \gg \frac{c_{Au_s}^{eq,(b)}}{c_{Au_i}^{eq}} \tag{10}$$

In either case $c_{Au}^{(s)}/c_{Au}^{(b)}$ is larger than $S^{(s)}$, the value derived from the segregation model ([14]). Sveinbjörnson et al. ([20]) have stated that their data of $c_{Au}^{(s)}/c_{Au}^{(b)}$ cannot be explained by $S^{(s)}$, but are consistent with eq.(9), which remains without justification in their work.

We further note that the temperature dependence for this ratio, as measured by Sveinbjörnson et al. (3–4 eV), can be understood, when the temperature dependence of $S^{(s)}$ and of $c_I^{(b)}/c_I^{eq,(b)}$ is taken into account with the latter being estimated from data for enhanced diffusion of P and B during P-indiffusion.

Finally we mention that the unusual sharpness of the gold profile $c_{Au}(x)$ inside the gettering layer, which had been measured by Sveinbjörnsson et al., but remained unexplained in terms of the segregation model, is accounted for in terms of our model as the superposition of $S(x)$ and of $c_I(x)/c_I^{eq}(x)$.

III. Dynamics of gettering

The development of $c_M(x,t)$ during gettering for a given $c_M(x,0)$ depends on the time scales of (1) GL-formation, (2) of the reactions or currents at the GL/wafer interface, of (3) mobilization, and of (4) diffusion of M in the wafer. The first two scales are expected as a result of computer simulations of PDG (see above), which are not yet at hand.

To study mobilization of M in the wafer and its diffusion to the GL/wafer interface, we describe precipitate dissolution by a homogeneous reaction rate, which responds linearly to M–undersaturation as long as immobile M–species are present:

$$\frac{\partial c_{M_i}}{\partial t} = D_M \frac{\partial^2 c_{M_i}}{\partial x^2} + k(c_{M_i}^{eq} - c_{M_i}) \cdot \theta(c_{M_p}) \tag{11}$$

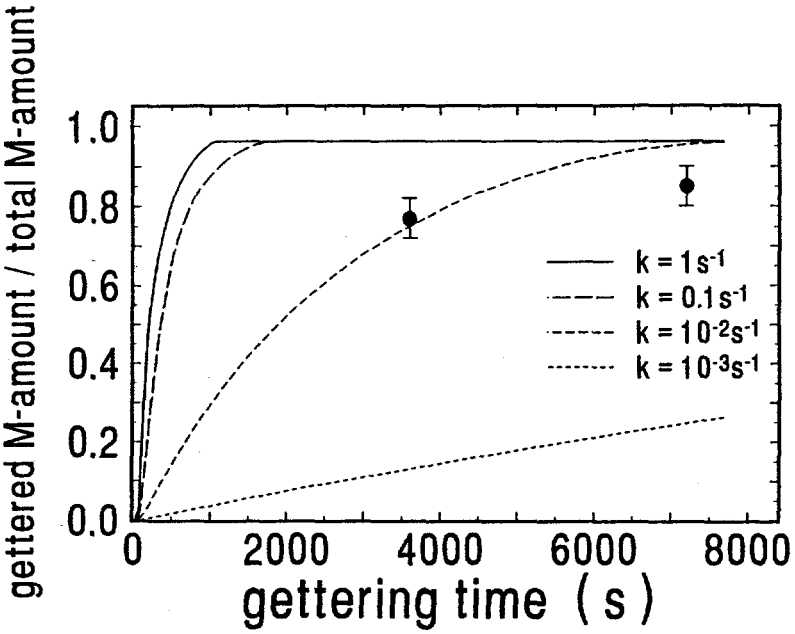

Figure 4: Gettered amount of a metal impurity normalized to its initial amount as a function of gettering time for different time constants $1/k$ of dissolution during Al–gettering of Co in FZ–Si at 820°C ($d = 350\mu$m, $d_{Al} = 40$nm, $S = 10^5$, $D_{Co} = 1 \cdot 10{-}6\text{cm}^2/\text{s}$, $c_{Co}(t=0) = 2.1 \cdot 10^{14}\text{cm}^{-3}$, $c_{Co}^{eq} = 8.9 \cdot 10^{12}\text{cm}^{-3}$)

$$\frac{\partial c_{M_p}}{\partial t} = -k(c_{M_i}^{eq} - c_{M_i}) \cdot \theta(c_{M_p}) \tag{12}$$

$$\text{with} \qquad \theta(c_{M_p}) = \begin{cases} 1 & \text{for} \quad c_{M_p} > 0 \\ 0 & \text{otherwise} \end{cases} \tag{13}$$

The experimental data, with which we want to compare, have been obtained for Co in Si after Al-gettering, whose action on the Co-concentration in the wafer is simplified to a boundary condition (assuming the reaction at the silicon/Al-Si-melt interface as fast compared to diffusion of M):

$$c_M(Si)\Big|_{x = d_{Al}} = c_M(Si)\Big|_{x = d - d_{Al}} = S \cdot c_M(Al) \tag{14}$$

$S = c_M^{eq}(Al)/c_M^{eq}(Si)$ is the distribution coefficient ([27]), $c_M(Al) = (1/d_{Al}) \cdot \int_0^t j_M(x = d_{Al})dt$.

In figure 4 the gettered amount of M normalized to the total initial amount of M is shown as function of gettering time, as obtained by computer simulation of eq. (11) (wafer thickness = 350μm, initial cobalt concentration = $2.1 \cdot 10^{14}\text{cm}^{-3}$, $D_{Co} = 1 \cdot 10^{-6}\text{cm}^2/\text{s}$, $d_{Al} = 40$nm on both wafer surfaces, $S = 10^5$, $T = 820$°C, $c_{Co}(t=0)/c_{Co}^{eq} = 23.6$) and also two experimental data points, obtained for Co in FZ-Si are shown.

One can see, that with k decreasing from 0.1 to 0.01 gettering switches from a diffusion-controlled to a dissolution-controlled process. Comparison with the experimental data shows that even in FZ-Si dissolution of $CoSi_2$-particles, whose mismatch to the Si-matrix is rather small (<1.2%), controls

gettering of M out of the wafer. Little is known at present about the mechanism of dissolution. In the literature various experimental results for polycrystalline silicon, e.g. the continuous improvement of the diffusion length during PDG at 900°C up to gettering times of 8 hours ([28]), indicate that dissolution of precipitates at extended defects will become one main mechanism, which has to be optimized to arrive at effective gettering procedures for solar silicon.

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Toward Understanding and Modeling of Impurity Gettering in Silicon

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Gettering of harmful impurities away from the device active regions has already become an integral part of manufacturing integrated circuits (IC) using Czochralski (CZ) Si wafers [1,2], and is experiencing an increasing importance in Si solar cell fabrications for improving the cell efficiency [3-12]. Gettering consists of (i) the creation of suitable gettering sites; and (ii) the gettering processes of contaminants.

Requirements for successful gettering differ between the IC and solar cell cases, because ICs are monolithic devices situated at the Si wafer surfaces while solar cells are bulk devices, and because the Si substrate materials used are different. For IC fabrications, the method used is that of intrinsic or internal gettering (IG) which utilizes oxygen precipitates and their associated defects in the CZ Si wafer bulk as gettering sites [1,2]. Because of the bulk nature of IG sites, the scheme cannot be used also for solar cells. Only some kind of extrinsic or external gettering (EG) schemes with gettering sites located at the wafer surface regions can be used for solar cells. The gettering of the harmful contaminants, usually metals, to the gettering region involves the metal dissolution from precipitated state, the metal atom diffusion to and the stabilization at the gettering sites.

For IC fabrications, the only Si substrates used are CZ wafers, which contain no metal precipitates, no dislocations, and only dissolved metal atoms with very low concentrations. For these Si wafers, there is no need to improve the starting substrate quality by gettering. The main contamination sources are processing equipment and materials, irrespective of the fact that IC fabrication facilities are maintained at very clean states at very high costs. Thus, gettering in the IC case is to prevent processing introduced contamination from affecting the devices. Because of the monolithic nature of the IC devices, the contaminants can be gettered to the wafer bulk IG sites. The involved metal diffusion distance is short, on the order of only 10 μm or less.

In solar cell fabrications a variety of Si substrates are used. High efficiency solar cells are fabricated using single crystal float-zone and some CZ wafers in clean facilities. Normal commercial solar cells are fabricated using low cost CZ wafers and large grain polycrystalline ribbons and wafers in low cost facilities that are not as clean. The polycrystalline Si ribbons and wafers are already contaminated to begin with. They contain grain boundaries, dislocations, precipitated as well as dissolved metals. Moreover, the commercial solar cell fabrication facilities are not clean and therefore would further contaminate the cells. Clearly, gettering is essential for commercial solar cell fabrications. It is necessary to improve the starting Si substrate quality as well as to prevent cell contamination from occurring during processing. To improve the substrate quality, metal precipitate dissolution is involved, and the dissolved metal atom diffusion distance is very long: over 100 μm.

The designation of IG and EG are in accordance with the gettering site locations. Classification of gettering schemes may also be according to two different types of physical mechanisms by which the gettered impurities are stabilized at the gettering sites [13]: relaxation gettering and segregation gettering. In relaxation gettering the impurity concentration in the gettering and gettered regions are the same at the gettering (annealing) temperature. During cooling after the annealing, however, the gettered region impurities rapidly diffuse to the gettering region where they are precipitated out because of easy precipitate nucleation at the gettering sites. Gettering of Fe by IG re-

lies on the relaxation gettering mechanism [14]. In segregation gettering, the impurities have already diffused to and preferentially segregated into the gettering region at the gettering temperature, which is based on the fact that the impurity solubility in the gettering region is higher than that in the gettered region. As such, the gettered region impurity concentration can become lower than its solubility at the gettering temperature, because the steady state distribution of the impurity depends only on the solubility ratio or segregation coefficient of the impurity in the two regions, but not on the actual impurity concentration. Gettering of Au during P indiffusion is such an example [15].

Cost effective gettering schemes during solar cell processing include P indiffusion gettering, Al gettering, and a combination of the two. Since both P and Al are used in the cells, it is only nature to also device means of harvesting the associated gettering benefits in cell fabrication processes.

Gettering by P indiffusion from the Si wafer surface is particularly effective for substitutionlly dissolved metal atoms diffusing via the substitutional-interstitial mechanism, including Au, Pt, and Zn. These species dissolve in Si on both substitutional and interstitial sites, designated respectively as A_s and A_i, and are commonly referred to as substitutional-interstitial (s-i) species. The thermal equilibrium concentration of A_s is larger than that of A_i to the extent that the measured total A concentration is practically just that of A_s. However, the mobility of A_i is so much larger than that of A_s that the diffusion of A_s is due to the A_s-A_i interchange and the migration of A_i. This interchange process involves Si self-interstitials I via the *kick-out* mechanism:

$$A_i \Leftrightarrow A_s + I . \qquad (1)$$

The alternative mechanism involving the Si vacancy V according to $A_i + V \Leftrightarrow A_s$ (the Longini mechanism), has been found to be not consistent with experimental results. Outdiffusion of A_s is difficult because, via reaction (1), this will incur a large I undersaturation which, once established, prevents A_s to become A_i to diffuse away. P indiffusion is highly effective in gettering A_s because it injects I, which alleviates the I undersaturation due to the processes of $A_s \rightarrow A_i$ changeover and the subsequent outdiffusion of A_i. Furthermore, A_s consists of acceptor species with very large solubilities in the high concentration P diffused region wherein electrons are abundant. Thus, P indiffusion on the one hand speeds up the effective A_s diffusion process and on the other also provides a large segregation coefficient for stabilizing A_s gettered to the high P concentration regions. It is clear that in this gettering process both A diffusion and segregation are involved.

A layer of Al deposited on the Si wafer surface can provide a gettering effect because the solubility of other metals in Al is very high, reaching 1 at% in the temperature range below the eutectic temperature of 577°C, and even higher above the eutectic temperature at which a liquid Al-Si alloy forms. In this liquid, the solubility of a typical metal can exceed 10 at%, i.e., on the order of $5 \times 10^{21} cm^{-3}$. Since the solubility of metals in Si does not exceed ~10^{17} cm^{-3}, the segregation coefficient of the metal between the liquid and Si is of the order of 10^4, which provides a tremendously large driving force for the metal to segregate into the liquid. It is obvious that the elementary process involved in Al gettering is also impurity diffusion and segregation. It is expected that Al gettering should be highly effective for interstitially dissolved metal atoms because of their large diffusivity values in Si, but less effective for the s-i species because of the I undersaturation cannot be effectively alleviated by Al which does not inject I into Si. A first evidence of Al gettering is that reported by Thompson and Tu [16]. At 540°C for which Al is a solid, they found that a Si wafer backside Al layer can dissolve a tremendous amount of Cu diffused in from the Si wafer frontside. Recently, Joshi et al. [17] reported unambiguous evidences of the effectiveness of Al gettering above the eutectic temperature in improving CZ Si wafer minority carrier diffusion lengths and in preventing furnace contamination, which deteriorate the carrier diffusion lengths, in wafer regions

protected by Al from occurring. In this case the gettered impurities are probably some fast diffusing intertitially dissolved metal species.

A number of reports on the beneficial effects of using Al or of using P and Al together for improving the performance of solar cells are available [3-12]. A beneficial effect due to gettering by Al was noticed [3,4]. The main effect, however, appears to be due to the cell back surface field [18] produced by the p^+-p junction resulting from a high concentration of Al diffused into the cell back surface [3,4]. In cases of using polycrystalline Si substrates, the benefits of Al also include the production of the p^+-p junction around a grain boundary or a dislocation core [5] due to fast Al pipe diffusion, and the catalytic effect of Al for producing atomic H which passivates grain boundaries and dislocations [6]. Incorporating the beneficial effects of P and Al together with other design and processing optimizations, solar cell structures with very high efficiencies have been fabricated using polycrystalline Si substrates [7,8]. It is specifically noted there are experimental results [9-12] showing that P and Al gettering, when performed simultaneously, exhibit a synergistic effect in that the gettering effectiveness exceeded that of either gettering scheme performed alone.

To mathematically model/simulate the gettering process of an atomically dissolved impurity species in Si, it is necessary to calculate the impurity diffusion and segregation processes simultaneously. For the simplest case of gettering an interstitially dissolved metal species by Al, the standard diffusion equation

$$\frac{\partial C}{\partial t} = D \frac{\partial^2 C}{\partial x^2} \tag{2}$$

can be used to simulate the diffusion processes in both the Al layer and the Si matrix. The special boundary condition due to Antoniadis and Dutton [19]

$$F_S = h \left(C_1 - \frac{C_2}{m_2} \right) , \tag{3}$$

can be used as a computational criterion at the Al-Si interface to describe the segregation process. In Eq. (3) F_s is the impurity flux at the interface, h is the mass transfer coefficient; C_1 is the impurity concentration at the computational grid point 1, which is in the bulk of region 1 (e.g., Si) nearest to the interface; C_2 is the same in region 2 (e.g., Al), and m_2 is the equilibrium segregation coefficient of the species in region 2 relative to region 1 (m_1=1). Equation (3) has been originally arrived at on an empirical basis. However, it has been recently shown [20] that it is of the correct form with $h = D^{eff}/\lambda$, where λ is the interatomic spacing, and D^{eff} is an effective diffusivity given by $D^{eff} = \Gamma_{1\rightarrow 2}\lambda^2$ with $\Gamma_{1\rightarrow 2}$ being the atom jump frequency from region 1 to 2. Figure 1 shows the simulation results of gettering a hypothetical interstitial impurity by an Al layer.

Except for this simplest case, Eqs. (2) and (3) cannot be used to simulate the impurity gettering process. For a substitutional or s-i species, the impurity diffusion process is closely coupled to also the Si native point defect diffusion processes, leading to the need of additional diffusion equations and the existence of appropriate coupling terms in each of the equations. For gettering by P, the gettered impurity solubilities and hence the corresponding segregation coefficients in the P diffused region are continuous functions of x due to the continuous changes in the P concentration profile as a function of x, which renders the use of Eq. (3) impractical. To treat the latter problem, a flux equation of diffusion-segregation (FEDS) and a diffusion-segregation equation (DSE) have been derived [21,22]:

$$J = -D\left(\frac{\partial C}{\partial x} - \frac{C}{m}\frac{\partial m}{\partial x}\right), \tag{4}$$

$$\frac{\partial C}{\partial t} = \frac{\partial}{\partial x}\left[D\left(\frac{\partial C}{\partial x} - \frac{C}{m}\frac{\partial m}{\partial x}\right)\right]. \tag{5}$$

In Eqs. (4) and (5) the segregation coefficient m of a species may be regarded as either a continuously changing or fairly abruptly changing quantity. That is, insofar as the impurity or point defect segregation properties are concerned, the use of Eq. (5) is sufficient for all gettering problems. It is easy to see the similarity between Eqs. (3) and (4), and it has been shown [23] that Eq. (4) reduces to Eq. (3) upon discritization at an abrupt interface. For the problem of Fig. 1, the use of Eq. (5) yielded the same results.

In accordance with reaction (1), by modifying the basic form of the DSE, Eq. (5), complete sets of differential equations have been written and solved [23] for the gettering of Au_s away from the Si bulk by P indiffusion from the wafer front surface, by a layer of Al deposited on the wafer back surface, and by the combination of the two schemes. In these sets of expressions we have accounted for (i) the coupling among the diffusing Au species and the point defect species *I*; (ii) the appropriate diffusion-segregation properties of Au and of *I* in accordance with best known physical models. Figures 2 and 3 show some simulated results wherein many interesting and important features have been revealed. For P indiffusion and for Al gettering, the gettering sites are located at only one wafer surface, yet it is seen from Fig. 2 that the gettering of Au is more effective at both wafer surface regions than in the middle section of the wafer. Gettering of Au away from the Si wafer surface region joining the gettering region is expected to be more effective than elsewhere in the wafer, because the gettered Au atoms need to only diffuse through a very short distance and because in the surface region *I* is maintained near its thermal equilibrium value by the surface. Gettering of Au away from the Si wafer surface region opposite to the gettering region location is also more effective than in the wafer interior, because *I* is also maintained near its thermal equilibrium value by this surface. According to reaction (1), the gettering of Au_s away from the Si wafer induces an *I* undersaturation, which, once established, inhibits the further gettering of Au_s. In the wafer interior, this *I* undersaturation cannot be effectively alleviated by *I* indiffusion from the two wafer surfaces and therefore the gettering efficiency becomes lower than that at the two wafer surface regions. The *optimum* gettering times for the P indiffusion and Al gettering schemes are respectively 2 and 7 hours, indicating that P gettering is faster. This is because P indiffusion injects *I* into Si which speeds up reaction (1) by alleviating the kick-out mechanism induced *I* undersaturation, while Al gettering does not inject *I* into Si. On the other hand, the capacity of P gettering is smaller than that of Al gettering, and for longer gettering times P gettering becomes also less stable than Al gettering. This is because a finite P source is assumed for which the P profile has spread out more for longer gettering times. Now, due to the decrease of the P concentrations, the Au solubility underneath the P profile is decreased and therefore the total capacity of P to stabilize Au has also been decreased. On the other hand, the solubilities of Au in Si and in Al does not change with gettering time, and hence the Al gettering scheme is more stable. Figure 3(a) shows the results of gettering Au by the combined method of P indiffusion and the Al layer. It is seen that it is fast and the gettering capacity is large. Furthermore, it is also about as stable as Al gettering [23]. These points become particularly clear when the results due to all three gettering schemes are compared, Fig. 3(b). With these simulations, the synergistic effect of the combined P and Al gettering is explained, and, it is clear that the combined scheme is the best by all measures.

It is well known that solar cell grade polycrystalline Si substrates contain bad regions wherein the minority carrier diffusion lengths are extremely low, and cannot be significantly improved by a normal gettering treatment such as P indiffusion. These regions contain high densities of dislocations observable by a variety of analytical techniques. It is possible that these regions also contain small (and therefore difficult to observe) metal silicide precipitates to a high density, and the reason

that the quality of the region is difficult to improve by gettering treatments is that now precipitate dissolution is involved in the gettering process which requires a more extensive treatment than the gettering of dissolved metal atoms. In order to model/simulate the impurity gettering process involving both precipitated and dissolved metal atoms in Si, a basic set of expressions has been written, and simulations are in progress. Here we present these equations. During gettering, to account for both the dissolved metal atom diffusion-segregation process and the metal precipitate dissolution process, Eq. (5) is rewritten as

$$\frac{\partial C}{\partial t} = \frac{\partial}{\partial x}\left[D\left(\frac{\partial C}{\partial x} - \frac{C}{m}\frac{\partial m}{\partial x}\right)\right] + \left(\frac{dC}{dt}\right)_{disso}, \qquad (6)$$

where the term $(dC/dt)_{disso}$ on the right hand side is due to precipitate dissolution. Assuming a uniform distribution of precipitates of radius r with a density of ρ in the Si matrix, this term is given by

$$\left(\frac{dC}{dt}\right)_{disso} = 4\pi r^2 \rho\, J^{\vartheta}, \qquad (7)$$

where J^{ϑ} is the C flux flowing into the matrix at the precipitate-matrix interface. In the steady state approximation, J^{ϑ} is given by

$$J^{\vartheta} = D\frac{C^{\vartheta} - C}{r}, \qquad (8)$$

where C^{ϑ} is the impurity concentration in the matrix at the precipitate-matrix interface given by

$$C^{\vartheta} = C^{eq} \exp\left[\frac{\Omega}{r}\frac{2\sigma}{k_B T}\right], \qquad (9)$$

with C^{eq} being the impurity thermal equilibrium concentration, Ω the volume of one impurity atom in the precipitate, and σ the precipitate-matrix interfacial energy density. The change of r with time is

$$\frac{dr}{dt} = \Omega\, J^{\vartheta}. \qquad (10)$$

Substituting Eqs. (7) and (8) into Eqs. (6) and (10), we obtain

$$\frac{\partial C}{\partial t} = \frac{\partial}{\partial x}\left[D\left(\frac{\partial C}{\partial x} - \frac{C}{m}\frac{\partial m}{\partial x}\right)\right] + 4\pi r \rho D\left(C^{\vartheta} - C\right), \qquad (11)$$

$$\frac{dr}{dt} = \Omega D\frac{C^{\vartheta} - C}{r}. \qquad (12)$$

With C^{ϑ} given by Eq. (9), Eqs. (11) and (12) may be solved for the gettering of an in interstitial impurity species for which the dissolution of the impurity precipitates does not incur a point defect non-equilibrium. The last condition fulfills when (i) the specific volume of the SiM_x molecule is identical to that of a Si atom; or (ii) there exist dislocations in the Si matrix to maintain the point de-

fect equilibrium. Condition (i) is in general not satisfied, but condition (ii) should have been generally satisfied in solar grade polycrystalline Si substrates, even for s-i species.

It is clear that the basic expressions for modeling/simulating the gettering process of a given impurity species, from the dissolution of the impurity precipitates to the diffusion and segregation (stabilization) of the impurity atoms, now exist. Accurate modeling/simulation parameters, such as the impurity charge states, level positions, solubilities, and diffusivities, are needed. Given sufficient time and effort, a gettering process simulator may become available.

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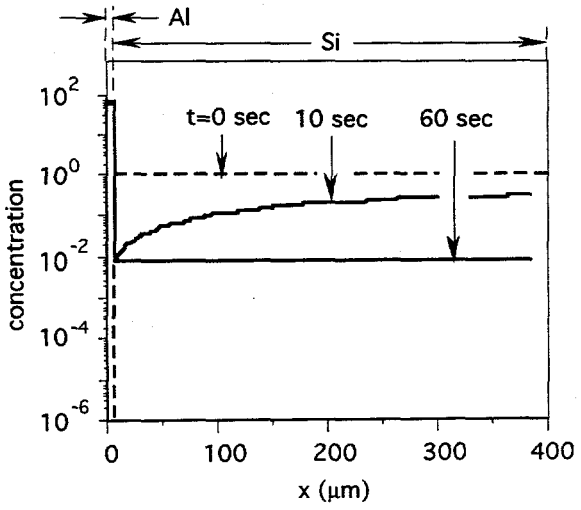

Fig. 1. Simulated results of gettering a fast moving metallic impurity from the Si bulk using a 4 μm thick liquid Al layer on one side of the Si wafer. The impurity atom diffusivity is assumed to be 10^{-4} cm^2s^{-1} and the metal atom solubility in the liquid Al layer is assumed to be 10^4 times of that in Si.

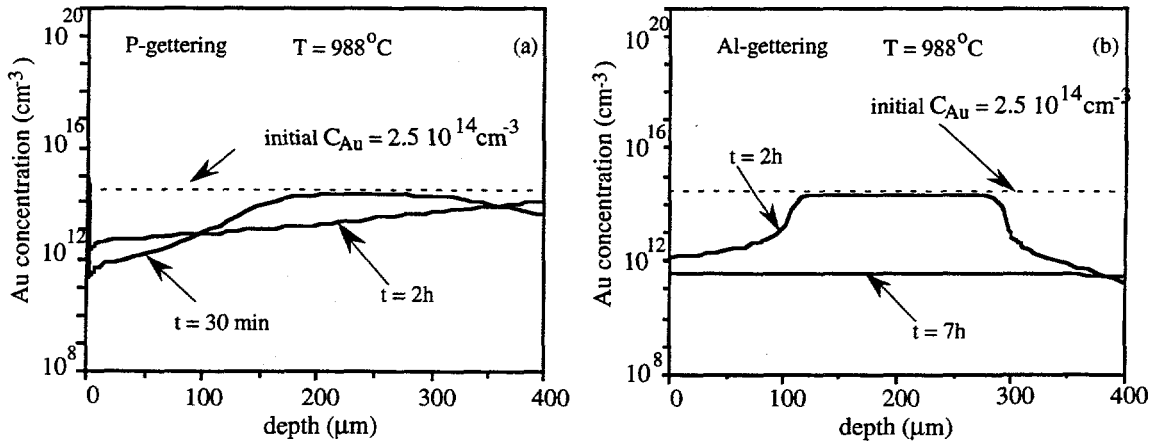

Fig. 2. Simulation results of gettering of Au by P and by Al. (a) Au concentration after 30 min and 2 h of P indiffusion gettering from the wafer left surface; (b) Au concentration after 2 and 7 h of gettering by an Al layer at the wafer right surface.

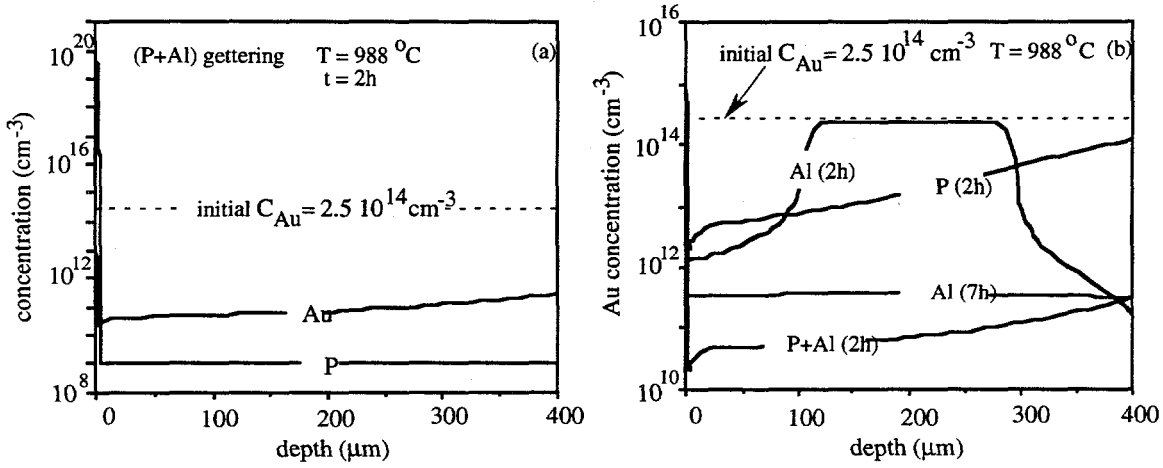

Fig. 3. (a) Au and P concentrations after 2 h of simultaneous P indiffusion gettering from the wafer left surface and Al layer gettering at the wafer right (back) surface; (b) Comparison between the three gettering techniques (P, Al, P+Al) for 2 h gettering times, and Al gettering for 7 h.

POROUS SILICON GETTERING

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We have studied a novel extrinsic gettering method that utilizes the very large surface areas, produced by porous silicon etch on both front and back surfaces of the silicon wafer, as gettering sites. In this method, a simple and low-cost chemical etching is used to generate the porous silicon layers. Then, a *high-flux solar furnace* (HFSF) [1,2] is used to provide high-temperature annealing and the required injection of silicon interstitials. The gettering sites, along with the gettered impurities, can be easily removed at the end the process. The porous silicon removal process consists of oxidizing the porous silicon near the end the gettering process followed by sample immersion in HF acid. Each porous silicon gettering process removes up to about 10 μm of wafer thickness. This gettering process can be repeated so that the desired purity level is obtained.

The method of using electrochemically etched porous silicon to getter impurities and other defects in electronic-grade silicon has been previously studied using conventional furnaces [3-6]. The significant increase of the surface area achieved with the porous silicon (nearly 600 m^2/cm^3), as well as the larger lattice parameter of porous silicon compared with that of the bulk Si, greatly enhance the probability of tying up the contaminants during the annealing step. The intense incoherent light irradiation of the HFSF may also enhance the diffusion of metallic impurities. In an earlier study using an artificial light source, Borisenko and Dorofeev [5] showed that intense electronic excitations caused by light absorption generate excess impurity interstitials in the surface layer. This enhances the diffusivity of impurities, because the diffusion of interstitial metallic atoms is an order of magnitude faster than that of substitutional atoms [7]. Recent studies of enhanced impurity gettering by nanometer-scaled cavities in silicon also indirectly confirmed that porous silicon should provide effective gettering sites [8,9].

In our gettering study, we used metallurgical grade silicon (MG-Si) prepared by directional solidification casting as the starting material. The impurity concentrations of the cast MG-Si as well as the strong, visible light emissions from porous silicon prepared from the MG-Si were reported by Menna et al. [10]. The porous silicon layers were prepared using a HNO_3/HF (1:100) etching solution [11]. This chemical etching method (also known as stain etching) is very simple (no electrodes required), fast (takes 10 minutes or less), and produces porous silicon on both sides of the silicon wafer. The porous silicon etched MG-Si wafers were then annealed in an HFSF for 15 to 30 min at a sample temperature of around 1000°C.

Secondary ion mass spectroscopy (SIMS) depth-profiling measurements done on both the front and back surfaces of the MG-Si wafers showed that the HFSF annealing treatments caused impurities in the bulk of the wafers to diffuse and segregate at the porous silicon etched surfaces. The effectiveness of this impurity gettering process increases with the HFSF treatment time. Strong gettering effects were observed for Al, B, Fe, Cu, Cr, and Ti impurities. For example, Figure 1 shows the copper impurity levels as a function of the sputtering time (which is proportional to the distance from the surface) for an as-polished MG-Si wafer, the same wafer after porous silicon etching, and the same wafer after a 30-min HFSF annealing treatment. The sharply increasing or decreasing Cu profiles very close to the surface region obtained during about the first two hundred seconds of sputtering are most likely due to measurement errors caused by variations in surface

morphology and cleanliness. The high copper concentration region near the surface of the wafer corresponds to the porous silicon etched region, which is about 2 μm thick (about 1500 s of sputtering time). We can see that there is a very significant amount of Cu atoms gettered from the bulk to the porous silicon area even before the high-temperature annealing due to the very high diffusion coefficient of of Cu [12]. The data clearly show that the combination of a porous silicon etch and an HFSF annealing treatment is effective in gettering impurities to the porous silicon etched surface layers.

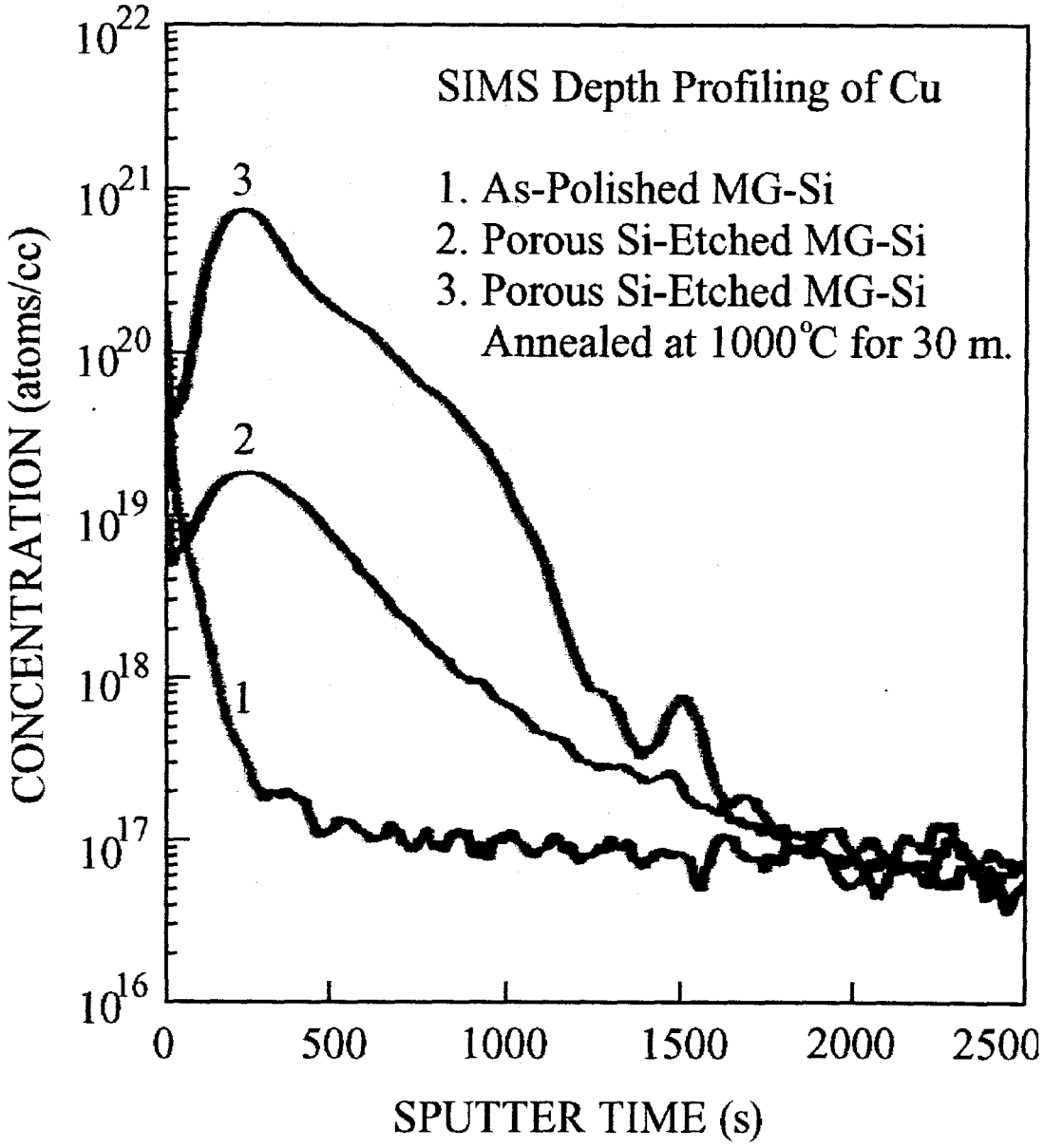

Fig. 1 SIMS depth profiling plots of the Cu impurity of (1) an as-polished cast MG-Si, (2) the same sample after porous silicon etch, and (3) the same sample after porous silicon etch and an 1,000°C, 30-min. anneal.

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Process Design for Al Backside Contacts

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It is known that properly alloyed aluminum backside contacts can improve silicon solar cell efficiency. To use this knowledge to fullest advantage, we have studied the gettering process that occurs during contact formation and the microstructure of the contact and backside junction region.[1] With an understanding of the alloying step, optimized fabrication processes can be designed.

To study gettering, single crystal silicon wafers were coated with Al on both sides and subjected to heat treatments at different temperatures and times. The results are depicted in Figure 1. Radio Frequency Photoconductance Decay (RFPCD) was used to measure

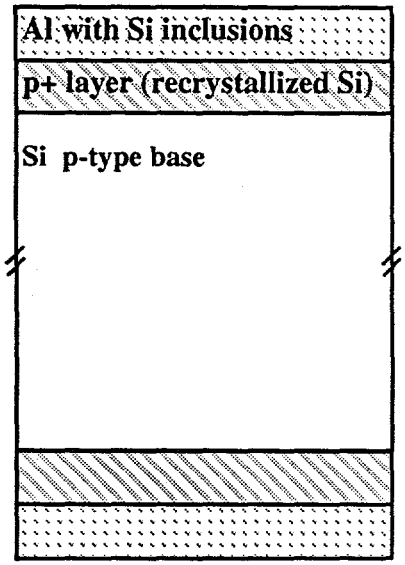

Figure 1: Schematic wafer cross section after annealing. The recrystallized p+ layer is formed on cooling and is doped to the solubility limit with Al.

minority carrier lifetime. As shown in Figure 2, we find that measured lifetime increases with annealing time for any given temperature, then levels off. For typical solar grade silicon with as grown lifetime of 30-35 μs, an alloying schedule of 850°C for one hour results in a 300% increase in lifetime. A slight decay in lifetime was observed for very short annealing times (3 minutes). Since the backside field (BSF) effect also contributes to the increase in measured lifetime by lowering the effective surface recombination velocity, EBIC studies were performed to examine gettering by charge collection efficiency.

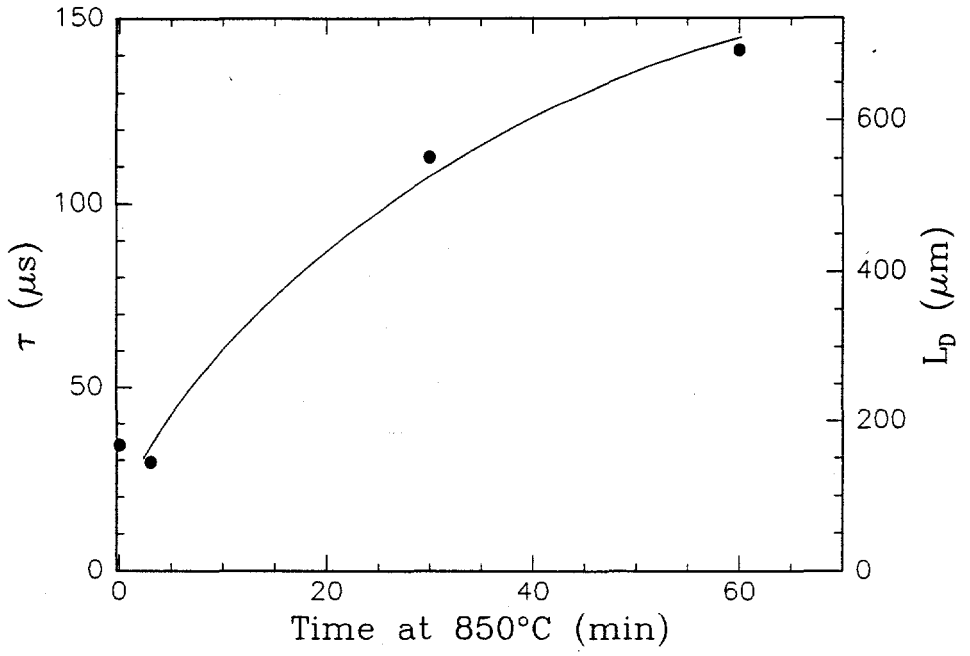

Figure 2: Minority carrier lifetime and diffusion length v. annealing time at 850°C. Here we report the best values for each time.

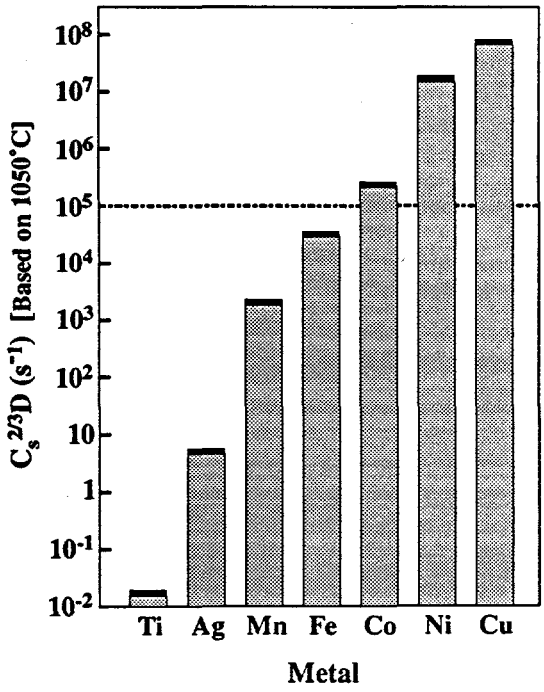

Figure 3: Values of $C_s^{2/3}D$ for various metals. Haze formation (out diffusion) is seen for $C_s^{2/3}D > 10^5 s^{-1}$.

Gettering of metals from the base relies on outdiffusion to the aluminum. For this to occur, metal solubility, Cs, must be large at the alloying temperature that metal precipitates are dissolved. Also diffusion must be fast enough for metal atoms to reach the surface during the alloying step. We have developed a figure of merit for haze formation, which relies on such outdiffusion. Haze formation is seen when $C_s^{2/3}D > 10^5 s^{-1}$. Figure 3 illustrates values of $C_s^{2/3}D$ for various metals with good agreement with experimental observations.

The surface roughening that accompanies the alloying step increases surface recombination and results in an nonuniform recrystallized p+ layer. In the optimal aluminum backside contact process, these effects must be controlled while allowing for adequate gettering. For this reason we have used SEM-EBIC, as illustrated in Figure 4, to look at the uniformity of the backside field and the microstructure of the Al-Si eutectic. Both the average junction depth and roughness of the junction interfaces were determined for various heating schedules. The average junction thickness measurements from EBIC were compared to spreading resistance results.

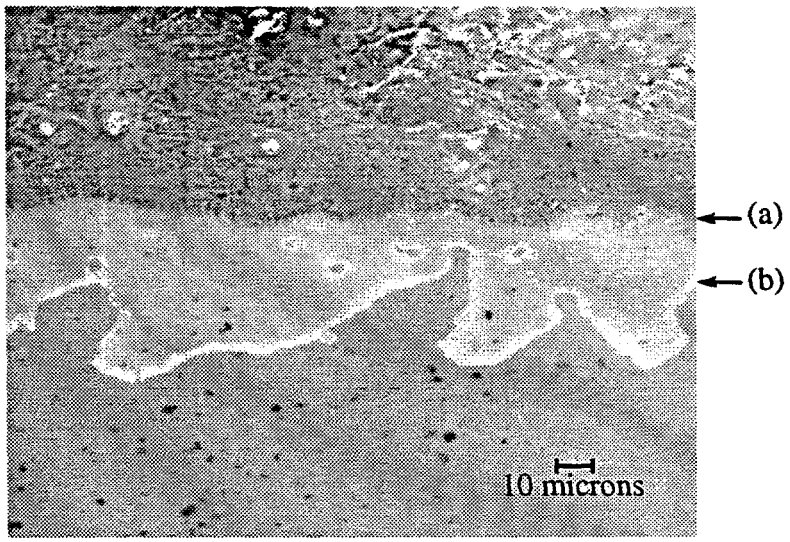

Figure 4: Combined SEM and EBIC image (3 kV) of the BSF junction region. This sample has an n-type base and was annealed at 950°C for 30 minutes. The sample was beveled (4 degrees) and shows the following: (a) the Si-Al interface, and (b) the p+-n junction. The average junction depth calculated from this micrograph is 1.9 microns, and is compared to the theoretical thickness of 1.3 microns based on the phase diagram.

By studying the effects of various processing schedules on gettering and microstructure, we aim to define optimal processing conditions for aluminum BSF contacts for silicon solar cells.

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n^+/p Diodes by Ion Implantation: Dopant, Extended Defects, and Impurity Concerns

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Introduction

The present study is concerned with the formation of defect structures resulting from phosphorus ion implantation into p-type, <100> silicon and with the rearrangement as well as removal of defect structures following high temperature annealing. The problematic interaction of background impurities with extended defects also is included in this study, as are the non-illuminated *and* illuminated electrical characteristics of n+/p diodes that are fabricated using ion implantation. Wafers and diodes that are fabricated using a phosphorus planar diffusion technique are run in parallel and serve as the controls. In this contribution, preliminary results for the cases of a 50 keV implant followed by an anneal at 900°C / 30 min and a diffusion at 825°C / 60 min are summarized.

Experimental Details

Phosphorus was implanted into a p-type (100) CZ silicon wafer (~ 10^{16} boron-cm^{-3}) at room temperature to a dose of $1x10^{15}$ ions-cm^{-2} at 50 keV and annealed at 900°C for 30 minutes in a conventional furnace and under a N_2 ambient. The control wafer was obtained by a planar diffusion technique that employs a CARBORUNDUM PH-900 solid-source. The diffusion was performed at 825°C with a soak time of 60 minutes.

Solar cells with an active area of $1cm^2$ were fabricated with both implanted/annealed and diffused junctions on 4" p-type wafers (~ 10^{16} boron-cm^{-3}). The diode structure is as follows: an isolation oxide (~ 0.2μm in thickness); a low-temperature, anti-reflection SiO_2 coating (~ 0.1μm in thickness); an evaporated Ti (~0.1μm in thickness) / Al (~0.4μm in thickness) contact bar and grid pattern ; eleven grid fingers (~ 5μm in width and of pitch ~ 800μm); a total metal coverage of ~ 2%; and a backside contact of evaporated Al (~ 0.1μm in thickness). Wafers were annealed in forming gas (400°C for 30 min) prior to electrical testing.

The as-implanted microstructure and the evolution of extended defects after the anneal were characterized by transmission electron microscopy (TEM) in both cross-sectional and plan-view modes (the diffused case was also examined in both TEM modes). Concentration/depth profiles for phosphorus, carbon and oxygen were measured for the implanted/annealed case by secondary ion mass spectroscopy. Carrier concentration/depth profiles were determined for both the implanted/annealed and diffused cases by spreading resistance analysis (Solecon Laboratories, Inc.). The I-V characteristics of solar cells were made on a conventional probe station without illumination (dark mode) and with the illumination level available from the microscope light source (~ 0.3 lumen-cm^{-2}).

Results

The TEM data show that implantation at 50keV produces a continuous amorphous layer that extends to a depth of ~ 920 Å. This depth corresponds to $R_p + \Delta R_p$, where R_p = 660 Å is the projected range and ΔR_p = 255 Å is the straggle, as determined by TRIM simulations. In addition, end-of-range defects (very small strain centers) form at a depth of $R_p + 2\Delta R_p$. After the anneal, solid-phase epitaxial regrowth occurs, small strain centers are present in the regrown layer, and resolvable loop-like image features are clearly observed at end-of-range, as illustrated in Fig. 1a. The loop-like image features have been analyzed by established diffraction contrast techniques and the result of these analyses are consistent with images that are expected from dislocation loops having Burgers vectors of type a/2<110>, {111} habit planes, and a compressive strain field. For the diffused case, no evidence for defect formation (e.g., misfit dislocations or precipitation) has been found.

SIMS depth profiles of the oxygen and carbon concentrations as a function of depth for the implanted/annealed case are shown in Fig. 1b. Since no depth dependent variation in oxygen (or carbon) was observed in the as-implanted state, it is clear that the anneal has resulted in the segregation of oxygen to the layer containing end-of-range dislocation loops. The situation regarding carbon is inconclusive. The peak in the oxygen concentration occurs at the approximate depth of the end-of-range defects. The oxygen peak corresponds to an areal density of 2×10^{13} oxygen-cm^{-2}. Quantitative analysis of plan-view images yields a total dislocation line length of $\sim 2 \times 10^5$ cm-cm^{-2}. An order of magnitude estimate of the number of lattice sites along this line length yields a total value of $\sim 10^{13}$ sites-cm^{-2}. The extent of oxygen segregation thus correlates to the dislocation line length. It is unlikely that every site along an undissociated dislocation line is occupied by an oxygen atom, since this would imply a rather unreasonable jog density. Rather, this correlation suggests that the strain field of the dislocation loops plays an important role in oxygen segregation. Such a situation would yield an oxygen level of ~ 80 ppm within a defect "layer" of 500 Å — that is a layer of width equal to the extent of the end-of-range dislocation loops. This oxygen concentration is substantially higher than the literature value (~ 0.6 ppm) of oxygen solubility at 900°C.

Spreading resistance analysis of the carrier concentration as a function of depth for the implanted/annealed case is presented in Fig. 2. This carrier profile shows a small kink at the location of the end-of-range defects. This may imply that the layer of defects affects phosphorus diffusion during the anneal. The physical characteristics of the implanted and diffused (control) diodes are compared in Table I. The junction depths for the two cases are similar; the activated fraction of implanted phosphorus is ~ 90%; however, there is a 30% difference in the total phosphorus dose within the n^+ side of the n^+/p junctions.

Typical I-V curves of the implanted and diffused diodes under dark (non-illuminated) and illuminated conditions are compared in Fig. 3. In Table II the electrical characteristics of these devices are summarized. In the absence of illumination, the most pronounced differences between the two cases appear as a change in slope under forward bias and a change in the reverse bias current. The forward bias differences imply a 80% larger series resistance in the implanted case. Assuming that the contact resistance is identical for each diode, the increase in series resistance may be tentatively attributed to the defective layer in the implanted case. Under reverse bias, the implanted diode has a factor of 10 higher leakage current than the diffused diode, suggesting an increased generation current in the implanted case. Under illumination by a tungsten filament with an intensity of ~ 0.3 lumen-cm^{-2}, the diodes show substantially different solar cell characteristics. In particular, the maximum power generated and the fill factor are 35% and 60% lower for the implanted cell.

Closing Remarks

This preliminary study reveals that a 50keV phosphorus implant and a subsequent anneal at 900°C/30min results not only in the expected end-of-range dislocations but also the unexpected segregation of background oxygen to the layer of silicon that contains the end-of-range dislocations. It is tentatively proposed that the end-of-range defective "layer" of material (i.e., dislocation loops and segregated oxygen) contributes to the series resistance of the so-called implanted diodes and acts as a recombination "layer" for carriers that otherwise would be available for the generation of of photocurrent. Hence under low-level illumination, solar cells fabricated by this ion implantation scheme have a fill factor that is approximately a factor of two smaller than cells fabricated by a solid-source diffusion technique.

Acknowledgment

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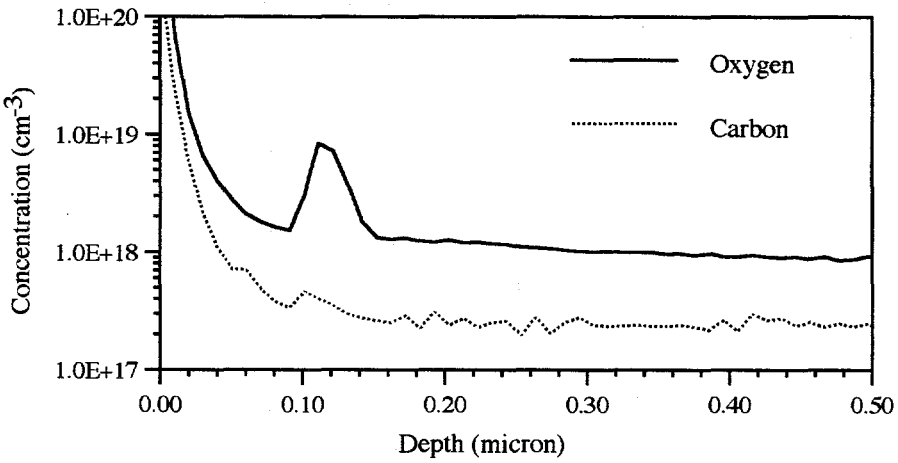
(a)



(b)

Fig.1 (a) Cross-sectional TEM micrograph recorded at (g,3g) with g[004] and (b) SIMS depth profiles of oxygen and carbon.

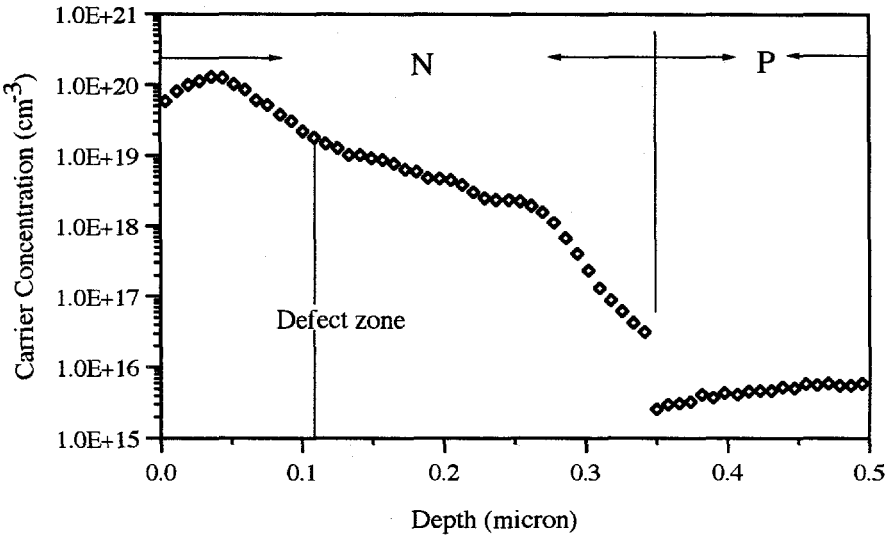


Fig.2 Carrier depth profile of n^+p diode implanted at 50keV and annealed at 900°/30 min

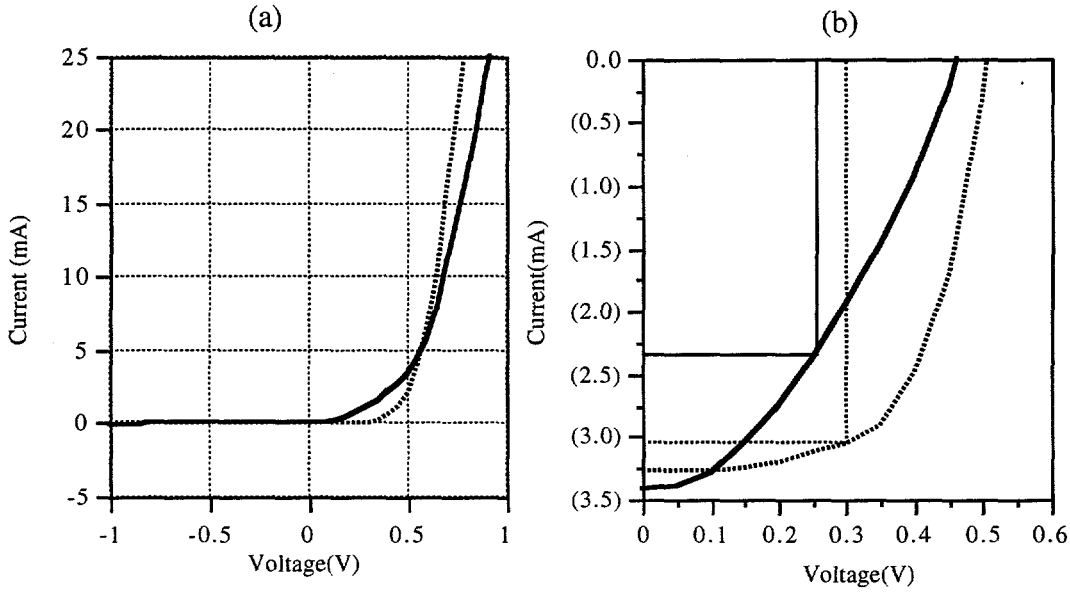


Fig.3 Current-voltage characteristics of n^+p solar cells which are implanted at 50keV and annealed at 900°C/30 min (solid line) and diffused at 825°C/60 min (dotted line): (a) in the dark and (b) when illuminated.

Table I Physical Characteristics of Diodes

	Implanted(50keV)	Diffused (825°C)	(I-D)/D (%)
Xj (μm)	0.35	0.30	17
Dose within 0.1μm (cm^{-2})	7.0e14	6.2e14	13
Dose within Xj (cm^{-2})	9.1e14	7.0e14	30

Table II Physical Characteristics of Solar Cells

	Implanted (50keV)	Diffused (825°C)	(I-D)/D (%)
I_{leak} (μA/cm^2)	90	9.0	900
Rs (ohm)	17	9.5	79
V_{oc} (V)	0.48	0.5	-5
I_{sc} (mA)	3.4	3.3	5
V_{max} (V)	0.25	0.30	-17
I_{max} (mA)	2.4	3.1	-22
P_{max} (mWatt)	0.60	0.92	-35
Fill factor	0.37	0.62	-60

Gettering effects in Si_xGe_{1-x} single crystalline wafers

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The new interest in single crystal growth of SiGe solid solutions is caused by the development of advanced electronics. The SiGe alloys are mostly used in the form of Si/Si_xGe_{1-x} epitaxial layers in heterostructures, the perfect bulk crystals are required to study fundamental properties. Furthermore, Si_xGe_{1-x} crystals can be used as a substrate material instead of Silicon in order to avoid the buffer layers between the Silicon substrate and strained Si_xGe_{1-x}. Monocrystalline SiGe alloys may be a potential candidate as a base material for infrared solar cells too because of an enhanced IR-sensitivity.

In this paper we report a new approach to the growth of Si_xGe_{1-x} single crystals (up to 2" in diameter) using the crucible free rf-heated float zone technique as well as the Czochralski-technique for solar cells.

The goal is to produce solar cells with an increased photo current in comparison to Silicon cells. based on the lower bandgap of the alloyed crystal. In order to be able to use the Si cells technology (a matter still pending to be proven), low contents of Ge are intended, desirably in the range of about x=0.2.

It is worth to mention, that in the conventional Silicon cell processes which give efficiencies up to 18-19%, this efficiency is not limited by the bulk base recombination in the lifetime is above 200 µs there.

We can conclude, that there is no basic limitation that prevents Si_xGe_{1-x} wafers to present high lifetimes, above 200µs, at least if the Ge content is below 5%. We can also conclude that the phosphorous gettering from a $POCl_3$ source, used in silicon, can be successfully used to enhance lifetimes in Si_xGe_{1-x}, at least for the Ge concentration used here.

Gettering effects in Si_xGe_{1-x} single crystalline wafers

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1. Introduction

The new interest in single crystal growth of SiGe solid solutions is caused by the development of advanced electronics. The SiGe-alloys are mostly used in the form of Si/Si_xGe_{1-x} epitaxial layers in heterostructures, the perfect bulk crystals are required to study fundamental properties. Furthermore, Si_xGe_{1-x} crystals can be used as a substrate material instead of Silicon in order to avoid the buffer layers between the Silicon substrate and strained Si_xGe_{1-x}. Monocrystalline SiGe alloys may be a potential candidate as a base material for infrared solar cells too because of an enhanced IR-sensitivity.

In this paper we report a new approach to the growth of Si_xGe_{1-x} single crystals (up to 2" in diameter) with the crucible free rf-heated float zone technique as well as the Czochralski-technique for solar cells. Both the floating crucible technique and the Czochralski-technique could be a possibility as well.

2. Experimental

2.1. Float Zone technique

Using the crucible free rf-heated float zone technique ‹111› and ‹100› - Si_xGe_{1-x} single crystals were grown containing up to 19at% Germanium. this procedure provides crystals with diameter of 25 mm and a length up to 200 mm. A specific resistance in the range of 0.2 to 3000 Ωcm (Boron) was measured. the "in situ" alloying of Silicon with Germanium has been developed to overcome the problems of the preparation of feed rod.

Silicon feed rods had been drilled axially for that purpose and had been grown in the conventional FZ technology. Pure Silicon seeds were used in all experiments. the growth processes had been started by the so-called necking and consequently the crystals grew dislocation-free during the first stage. The Germanium granules passing through the hole were added to the molten zone after reaching the required diameter. At the melt/hole boundary a solid film is formed owing to the temperature and radiation conditions. First the Germanium granule hits the film and after a certain time it melts and leaks into molten zone. The main advantage of this method is that no seed from Si_xGe_{1-x}-solid solutions is necessary to use.

2.2. Czochralsky technique

All growth experiments have been carried out with a conventional Cz equipment used for the pulling of semiconductor crystals with diameters up to 2". The crystal and the crucible can be moved very precisely with feeding rates less than 0.5 $mm.h^{-1}$. The design of inert gas flow (Ar) and thermal shields enable to diminish the sublimation of SiO (product of reaction between quartz crucible and Si melt) in the space above the melt surface and on the crucible wall during the long time of experiments. The process is generally performed under an Ar pressure of about 40 Torr and constant gas flow between 400 and 1000 $Nl.h^{-1}$.

The starting material consists of 50 Ωcm poly-Ge and undoped poly-Si or boron doped poly-Si

regrown by the FZ technique to get a resistivity of 0.5 to 1.0 Ωcm. The quartz crucible, 74 mm in diameter, was filled with Silicon and Germanium up to a melt volume of 130 ml. <111>- or <100>-Si seeds were used to grow Si_xGe_{1-x} single crystals from the melt with a starting Ge concentration up to 7at %. For a melt containing 12 at% Germanium $Si_{0.97}Ge_{0.03}$ seeds prepared from crystals grown before could be used. The grown crystals do not have a "standard" diameter and were up to 48 mm for $Si_{0.98}Ge_{0.02}$ and up to 38 mm for $Si_{0.9}Ge_{0.1}$.

3. Lifetime measurements.

The goal is to produce solar cells with an increased photo-current in comparison to silicon cells, based on the lower bandgap of the alloyed crystal. In order to be able to use the Si-cells technology (a matter still pending to be proven), low contents of Ge are intended, desirably in the range of about x=0.2.

However the lifetime measured in wafers from the Si_xGe_{1-x} ingots has resulted to be substantially lower than that of Si wafers, so far. Here we present a gettering procedure of Si_xGe_{1-x} grown by the FZ technique being able to increase this lifetime to values comparable to that of Si wafers. The results are show in Tab. 1 and 2.

Table 1. The initials Characteristics. The resistivity and Germanium content variations in the Si_xGe_{1-x} samples.

Sample	Thickness (μm)	Ge at. content(%)	Surface orientation	Resistivity type	Resistivity (Ωcm)	Measured lifetime (μs)
Si(1)	285	0	<100>	n	29.1	500
Si(2)	285	0	<100>	n	33.6	220
Si_xGe_{1-x}(1)	460	0.3-2.3	<211>	p	26.5-48.0	40
Si_xGe_{1-x}(2)	460	2.3-4.5	<211>	p	19.6 -23.3	30

Table 2. Lifetimes and sheet resistance of wafers after gettering.

Samples	Measured lifetime with diffused layer (μs)	Diffused layer sheet resistance (Ω/□)	Measured lifetime without diffused layer (μs)	Bulk sheet resistance (Ω/□)	Bulk Resistivity (Ωcm)
Si(1)	98	18.6	540	1035	28.9
Si(2)	158	21.8	500	1271	34.5
Si_xGe_{1-x}(2)	140	21.8	440	590-1024	24.8-47.1
Si_xGe_{1-x}(2)	78	20.4	240	431-508	19.8-23.4

The wafers Si(2) and Si_xGe_{1-x}(2) were previously oxidized in a wet ambient (at 1100 °C for 90 min.) in a non-gettered furnace, to evaluate the contamination introduced by this step, which is commonly used in the solar cell processing. Similar contamination may also occur in the other high temperatures steps that the wafer may suffer during the device processing. Then the lifetime has been measured after the oxide was removed and the wafer was immersed in HF. Unfortunately the

lifetime was below the detection limit of the apparatus (10 μs). This indeed a dramatic lifetime reduction confirming again the key role that processing may play killing lifetimes in high lifetime wafers.

For the gettering a phosphorus diffusion was performed for 30 min. from a $POCl_3$ source applying a furnace temperature of 900 °C. The gas flows were 1000 cm^3/min. of N_2, 40 cm^3/min. of O_2 and 40 cm^3/min. of N_2 through $POCl_3$ at 24 °C. This procedure leads to supersaturation conditions at the surface that is crucial for the achievement of the gettering in Si cells. After the phosphorus deposition, a short dry oxidation and an annealing in N_2 (10 min. each) were realized. The sheet resistance corresponding to the diffused region is in the range of 20 Ω, rather similar to that in Si and Si_xGe_{1-x} wafers.

We can conclude that there is no basic limitation that prevents Si_xGe_{1-x} wafer to present high lifetimes, above 200 μs, at least if the Ge content is below 5%. We can also conclude that the phosphorus gettering from $POCl_3$ source, used in Silicon, can be successfully used to enhance lifetimes in Si_xGe_{1-x} at least for the Germanium concentration used here.

Application of PECVD for Bulk and Surface Passivation of High Efficiency Silicon Solar Cells

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1. INTRODUCTION

Plasma enhanced chemical vapor deposition (PECVD) passivation of bulk and surface defects has been shown [1] to be an important technique to improve the performance of multicrystalline silicon (mc-Si) and single crystalline silicon solar cells. In this paper, we report the status of our on-going investigation into the bulk and surface passivation properties of PECVD insulators for photovoltaic applications. The objective of this paper is to demonstrate the ability of PECVD films to passivate the front (emitter) surface, bulk, and back surface by proper tailoring of deposition and post-PECVD annealing conditions.

2. EXPERIMENTAL

Simple n^+pp^+ solar cells were fabricated using 2 Ω-cm EFG mc-Si, with a two layer PECVD AR coating. This AR coating consisted of 60 nm SiN (index=2.3) and 95 nm of SiO_2 (index=1.46) deposited on a thin thermal oxide grown during an Al drive step. Post deposition annealing treatments were done in an AET Addax Rapid Thermal Annealing (RTA) system. Details of the PECVD AR coating and cell fabrication are given elsewhere [2].

3. RESULTS AND DISCUSSION

A. Impact of PECVD AR Coatings on Emitter Passivation

In addition to providing extremely good antireflection properties, the two layer PECVD AR coating is source of molecular and atomic hydrogen, which through proper annealing and deposition conditions can be utilized for bulk and surface passivation. Figure 1 shows the internal quantum efficiency (IQE) of a single EFG solar cell during three stages of cell fabrication: (1) after deposition of the AR coating, but before a post-deposition anneal, (2) after a 350°C anneal for 20 min in N_2, and (3) after a short anneal of 1.5 min at 650°C in N_2. The objective in this experiment was to observe the impact of annealing the PECVD films, and to determine the degree on hydrogen passivation. It is noted that in these two annealing cycles, the ambient gas was nitrogen, not forming gas (10% H_2 in N_2) as is the usual choice. The result is that the only source of hydrogen in the system is the PECVD AR coating.

It is clear from figure 1 that after a 20 min anneal at 350°C in N_2, a significant increase in both the short and long wavelength response is observed, indicating a higher degree of bulk and surface passivation than the as-deposited case. An additional anneal at 650°C for 1.5 minutes resulted in over a 60 % improvement in bulk diffusion length, but showed a slight degradation in the short wavelength response. To explain these changes in short wavelength response, J_{oe} measurements were made on single crystal silicon samples with the same emitter profile as the EFG cell used in figure 1. Measurements of J_{oe} were made using an inductively coupled photoconductive decay (PCD) tester, on samples with identical phosphorus diffusions on each side. Figure 2 shows the impact of annealing PECVD AR coatings on the emitter saturation current density (J_{oe}) for the annealing temperatures and times listed in the inset. Initially, there is a decrease in J_{oe} by a factor of 2 after a 350°C /20 min anneal in N_2 with slight

improvements by annealing at higher temperatures. Thus, the improvement in the short wavelength IQE response can be explained by the improved surface passivation resulting from annealing the PECVD AR coating at 350°C in N_2 for 20 min. However, the measurements of J_{oe} given in figure 2 do not explain the decrease in short wavelength response for the higher annealing temperature of 650°C.

To explain this phenomena, experiments were undertaken to better quantify the optical properties of the PECVD SiN film under different annealing conditions; the hypothesis being that the decrease in short wavelength response was due to increased absorption of light in the SiN film. To determine the amount of this parasitic absorption, quartz slides were coated with PECVD SiN, and reflectance and transmittance were measured before and after a post deposition anneal at 750°C, as shown in figure 3. Clearly, this absorption does in fact increase measurably at wavelengths below about 500 nm as a result of post deposition annealing treatments, which clearly explains the reduction in IQE at the shorter wavelengths.

B. Impact of PECVD AR Coatings on Bulk Recombination.

As indicated above, a significant increase in long wavelength IQE was observed as a result of post deposition annealing treatments. EFG cells without PECVD coatings showed no such improvements indicating that the enhancement is not due to the thermal treatment alone. To better understand the impact of PECVD coatings on bulk recombination, EBIC measurements were made on a finished solar cell in which the gridlines were replaced with a 200 Å semi-transparent layer of aluminum, to assure uniform contrast throughout the device. EBIC measurements were made on the same regions before and after the PECVD deposition and the 350°C/20 min anneal steps to provide the most direct proof of bulk defect passivation. Figure 4 shows that the intra-grain region demonstrated significant current collection improvement after the PECVD deposition and anneal, while the highly defective grain boundaries showed less of a current increase. This correlates well with the IQE results of figure 1, showing that PECVD and a post deposition anneal significantly improves the intra-grain bulk lifetime, leading to improved solar cell performance. Fourier Transform Infrared Spectroscopy (FTIR) measurements on the PECVD SiN film [3] show that indeed hydrogen is lost from the PECVD SiN film after successive annealing steps, thus supporting the conclusion that hydrogen originating in the SiN film is responsible for bulk defect passivation.

C. Implementation of PECVD Oxide for Back Surface Passivation.

With the improvements in J_{oe} and bulk lifetime obtained with PECVD, the next logical step toward high efficiency multicrystalline and single crystalline solar cells is a reduction in back surface recombination velocity and J_{ob} through the implementation of point back contacts. PECVD oxide is an excellent choice for back surface passivation due to the low deposition temperatures (250°C-300°C), and high deposition rates (100-1000 Å/min). To properly utilize PECVD in a cell fabrication process, it is important to understand the properties of a PECVD oxide. In general, a PECVD oxide contains a significantly higher density of oxide charge than a thermal oxide, although the density of interface states one can achieve with a PECVD oxide is comparable to a thermal oxide [4]. The density of hydrogen complexes (H_2, H, Si-OH, SiH, etc.) in PECVD oxides is high [5], revealing the potential for extensive interface passivation through a forming gas anneal, particularly in the presence of an aluminum contact. The goal of this section is to demonstrate the applicability of PECVD oxides for back surface passivation using the modeling program PC-1D, and to show the range of oxide charge and interface state density one can achieve through the proper choice of deposition conditions.

Figure 5 shows PC-1D model calculations of the open circuit voltage (V_{oc}) and efficiency as a function D_{it}, the interface state density, and Q_{ox}, the oxide charge density. The interface state density and capture cross section were included in the parameters S_n and S_p used by PC-1D, and are given as $S_n = v_{th}\sigma_n kTD_{it}$, and $S_p = v_{th}\sigma_p kTD_{it}$. The values of σ_n and σ_p are taken from previous measurements on

PECVD oxides [6], and are 10^{-14} cm^{-2} and 10^{-16} cm^{-2} respectively. Additional parameters in this model are based on measurements of a typical 3.3 Ω-cm Cz cell fabricated at our lab, including a J_{oe} of 75 fA/cm^2 and a bulk lifetime of 500 μs. The two charge densities used in these calculations were $1x10^{11}cm^{-2}$ and zero, with a range of D_{it} from $5x10^9$ to $1x10^{14}$ states/(cm^2eV). These modeling calculations show that even with high interface state densities, on the order of $1x10^{12}$ states/(cm^2 eV) it is possible to reduce the BSRV if a sufficient level of (positive) oxide charge, can be obtained. The physical mechanism behind this low BSRV is the difference in electron and hole capture cross sections, (σ_n/σ_p=100). If the oxide charge, and therefore the electron concentration is high at the back surface, then a recombination event will be limited by hole capture.

This approach to BSRV reduction is ideally suited to the PECVD process, since the level of Q_{ox} and D_{it} can be controlled over a wide range. Figure 6 shows preliminary results of high frequency and quasi-static CV measurements made on PECVD oxides deposited at temperatures ranging from 200°C to 350°C. In this figure, two sets of Q_{ox}-D_{it} data are shown: one for the case where a forming gas anneal was done before depositing the Al gate, and the other where the FGA was done after the Al gate deposition. From these results it is clear that the level of Q_{ox} and D_{it} obtained with PECVD oxides can be controlled over a wide range, and that this range is well within the requirements to produce greater than 20 % efficient Cz solar cells, as shown in figure 5.

4. CONCLUSION

In conclusion, results of a detailed investigation into the bulk and surface passivation properties of PECVD insulators are reported. Proper use of PECVD can passivate the emitter, bulk, and back surface regions of a silicon solar cell. It was shown that post deposition annealing is critical to successfully implementing PECVD into a solar cell fabrication process, but that extended annealing at high temperatures can lead to a significant increase in absorption in the short wavelengths. Thus, the possible benefits obtained through bulk defect passivation have to be weighed against increased light absorption in the SiN film. With improvements obtained in bulk lifetime, the next challenge is to reduce the BSRV. It was shown that through proper processing conditions, PECVD oxides can be used in a point contact scheme for the realization of greater than 20 % efficient Cz solar cells. These results can easily be applied to other types of material where the diffusion length is sufficiently long so as to be influenced by the back oxide-silicon interface.

ACKNOWLEDGMENT

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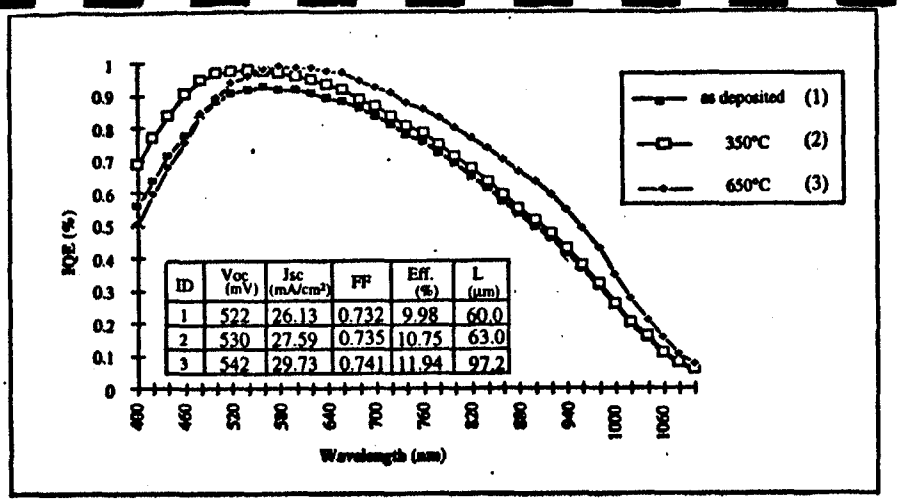

Fig. 1. Effect of post-PECVD RTA temperature on the performance of EFG cells.

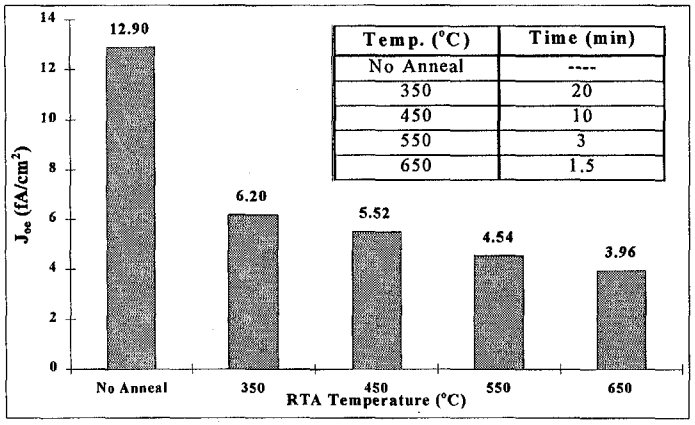

Fig. 2 Effect of post-PECVD RTA temperature on J_{oe}.

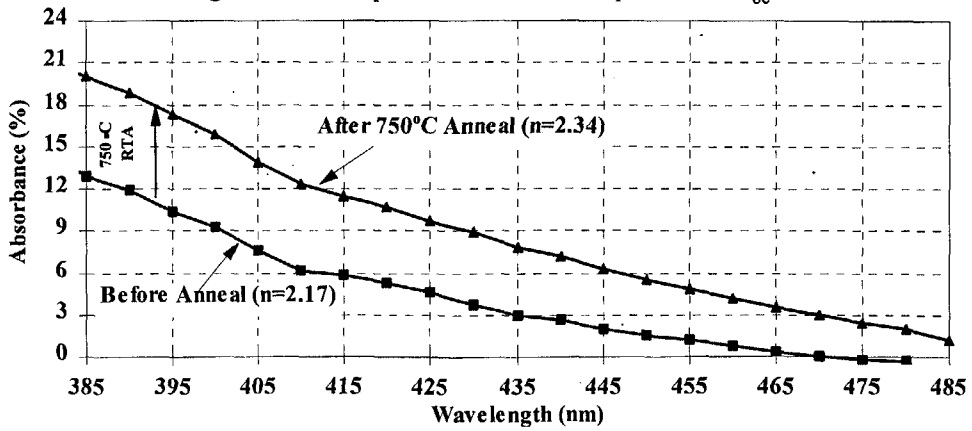

Fig. 6 Increase in percentage of photons absorbed after a post-PECVD high-temp. RTA. (A=1-T-R, where A, T, & R are the absorbance, transmittance, & reflectance, respectively.)

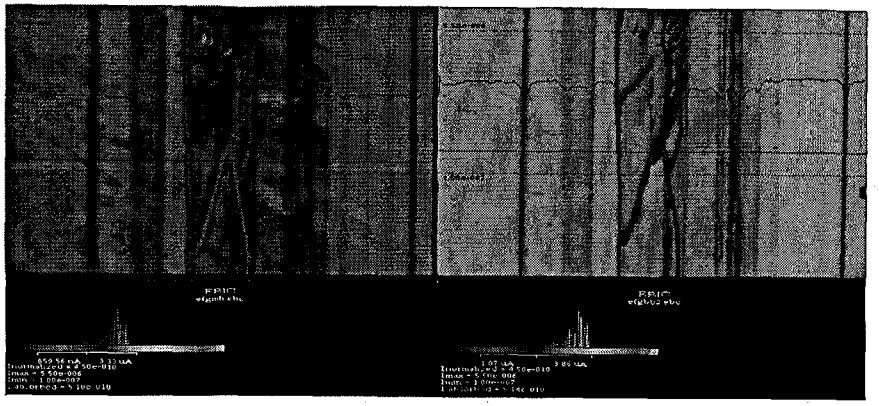

Fig. 4 EBIC image of an EFG sample before (left) and after (right) the RTA at 350°C/20 min. Lighter regions represent greater EBIC response.

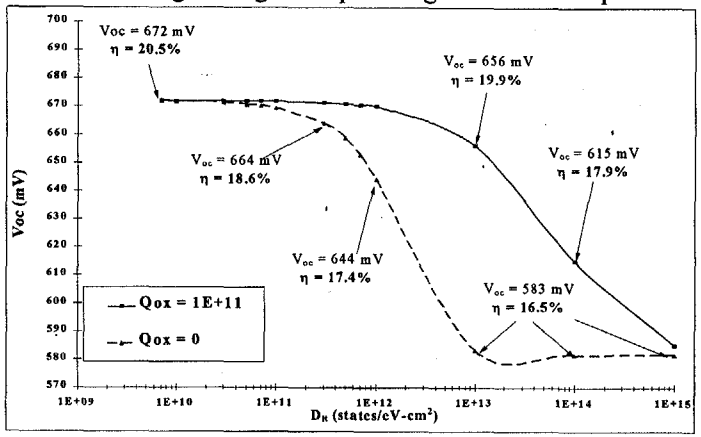

Fig. 5. Cell performance as a function of D_{it} and Q_{ox} of PECVD oxides.

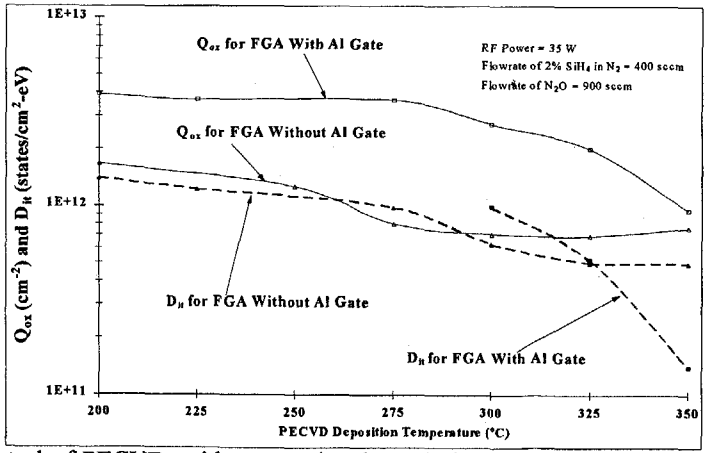

Fig. 6. Control of PECVD oxide properties through deposition and post-PECVD annealing conditions.

Degradation of Bulk Diffusion Length in CZ Silicon Solar Cells

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Introduction

Commercially-produced, unencapsulated, CZ silicon solar cells can lose 3 to 4% of their initial efficiency after exposure to light. After this initial, rapid (< 30 min.) decrease, the cell power output remains stable. The cell performance recovers in a matter of hours in the dark at room temperature, and degrades again under light exposure. The different conditions under which CZ silicon cells degrade, and the reverse process, annealing, are characterized with the methods of spectral response and current-voltage (I-V) measurements. Iron impurities are a possible cause of this effect.

Experiments and Results

Measurement and Data Analysis

The samples used to characterize the light-induced degradation (LID) effect were CZ solar cells with standard Siemens Solar Industries (SSI) processing. The cell substrate consists of boron-doped CZ silicon in the 1 Ωcm range grown at SSI. The cells have a diffused phosphorus emitter, and screen-printed metallization. The cell design incorporates surface texturing, surface passivation, and an anti-reflection coating to increase cell efficiency.

Internal quantum efficiency measured before and after a given cell treatment was the main method by which the degradation was characterized. It is crucial to measure the cells as rapidly as possible after any degradation step in order to minimize annealing. From the values of internal quantum efficiency in the wavelength range from 800nm to 1000nm the minority-carrier diffusion lengths were extracted[1]. In order to relate the measurement to impurity concentrations and to make the degradation of different samples comparable, the following model was adopted: it was assumed that an impurity or defect in the silicon substrate can be present in two states, where one state is much more effective at causing recombination than the other. Initially, in thermal equilibrium at room temperature, these recombination centers are less effective or are not effective at all in causing recombination. Once they become activated, the minority-carrier diffusion length and lifetime decrease. In order to find a relationship between the decrease in quantum efficiency and the concentration of active recombination centers the following equations were used:

$$\frac{1}{\tau} = \frac{1}{\tau_0} + \frac{1}{\tau_d}; \qquad \frac{1}{\tau_d} = cN_a \quad .$$

Here τ is the minority carrier lifetime, τ_0 the initial lifetime, and τ_d is the minority-carrier lifetime associated with the degradation mechanism. N_a is the concentration of active recombination centers, and c is a constant factor. The same equation that is used to extract the diffusion length leads to

$$\frac{1}{c}\left(\frac{1}{\tau_2} - \frac{1}{\tau_1}\right) = N_{a2} - N_{a1} = c'\left[\left(\frac{1}{Q_2} - 1\right)^2 - \left(\frac{1}{Q_1} - 1\right)^2\right]$$

where changes in internal quantum efficiency (Q_1, Q_2) are related to the changes in active recombination centers (N_{a1}, N_{a2}). By plotting $\frac{N_a - N_{ai}}{N_{af} - N_{ai}}$, where N_{ai} is the initial value and N_{af} is the final, highest concentration achievable, the concentration of active centers was normalized. In the figures to follow this value is referred to as 'Active Centers.'

Light-Induced Degradation (LID)

CZ solar cells can lose 3-4% of their initial power output due to LID. This effect takes place rapidly,

and saturates in less than 30 min. at 1 sun (0.100W/cm^2, AM1.5G) intensity. After this initial drop, the output remains stable. The light-induced degradation effect discussed in this paper is observed on unlaminated cells, and is distinct from any longer-term encapsulation or interconnection degradation issues for modules.

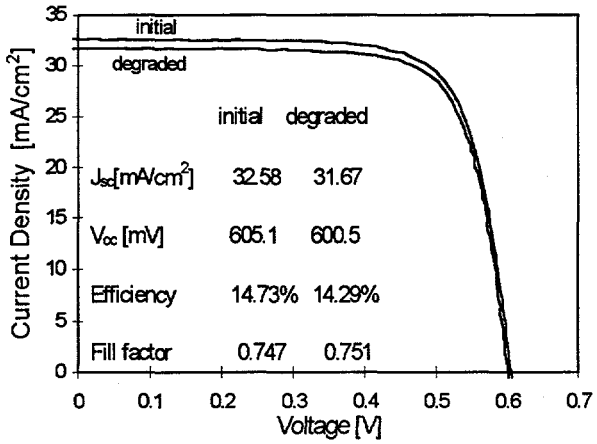

Fig. 1 Change in I-V curve after light exposure.

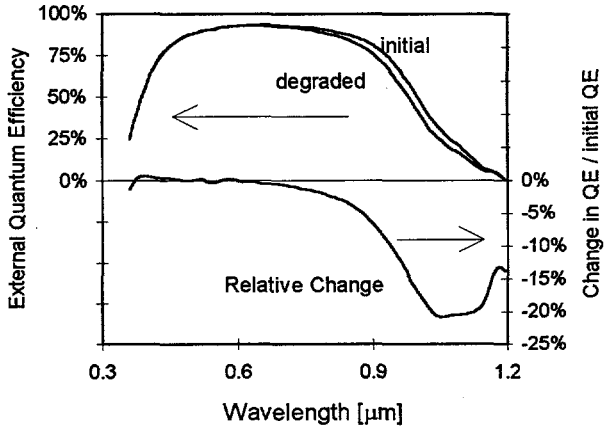

Fig. 2 Changes in external quantum efficiency after light exposure.

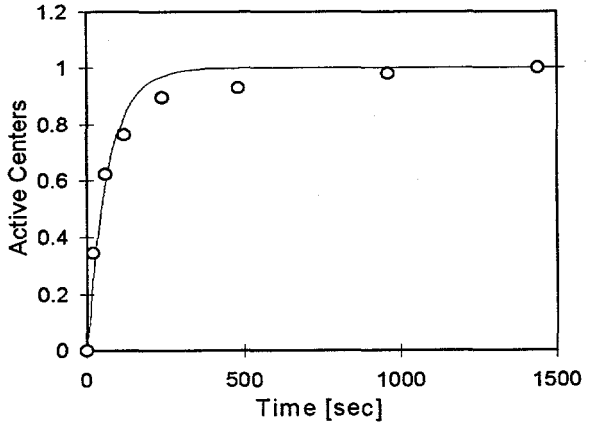

Fig. 4 Saturation of the degradation *vs.* time.

As can be seen in Fig. 1 a reduction is observed in the short-circuit current (I_{sc}), and, to a much lesser extent, in the open-circuit voltage (V_{oc}). The fill-factor is less affected for this cell than are the I_{sc} and V_{oc}. A substantial loss in quantum efficiency is observed in the infrared wavelength region. Fig. 2 shows the typical changes in external quantum efficiency after exposure to light (1 sun) under open-circuit conditions. This is caused by a reduction of the minority-carrier diffusion length, which can be seen in Fig. 3. That the effect saturates quickly can be seen in Fig. 4, where the degradation level is plotted versus time. This sample was degraded at 1 sun intensity at 25 ^{0}C under a incandescent halogen lamp. The sample degraded 90% of the way to its saturation level in less than 10 min.

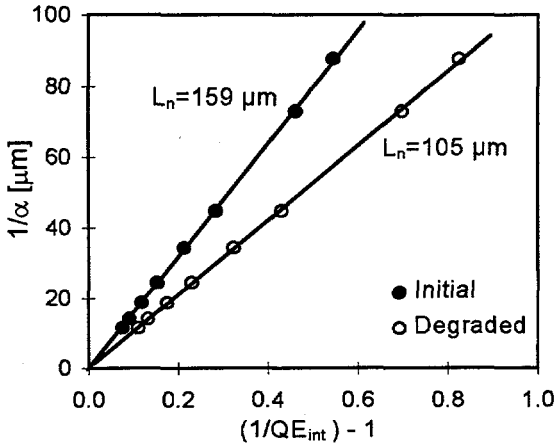

Fig. 3 Reduction of the diffusion length after light exposure.

Annealing

The LID effect is reversible. The cells anneal to their initial values even at room temperature within 12 hours. The anneal time was found to be dependent on temperature and boron concentration, as shown in Fig. 5. From the temperature dependence of the anneal time a recovery activation energy of 0.75eV was derived. The experimental result that the anneal time is shorter with higher boron concentration suggests that an impurity is coupled to boron at thermal equilibrium (T=25 ^{0}C). In this model, the impurity is much more effective in causing electron-hole recombination once it dissociates from the boron.

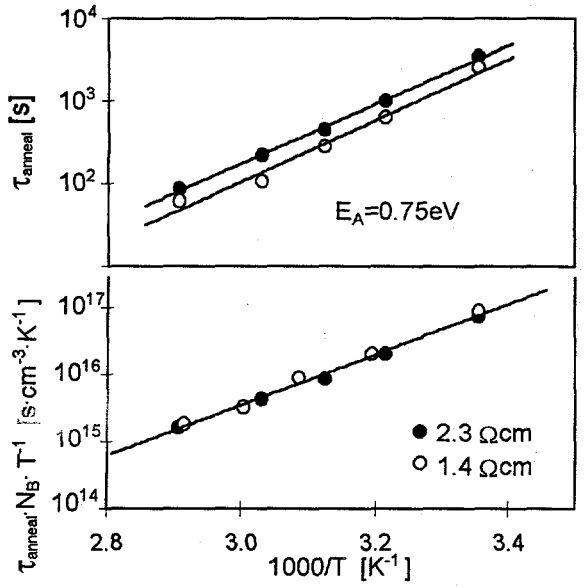

Fig. 5 Annealing time after degradation *vs.* temperature

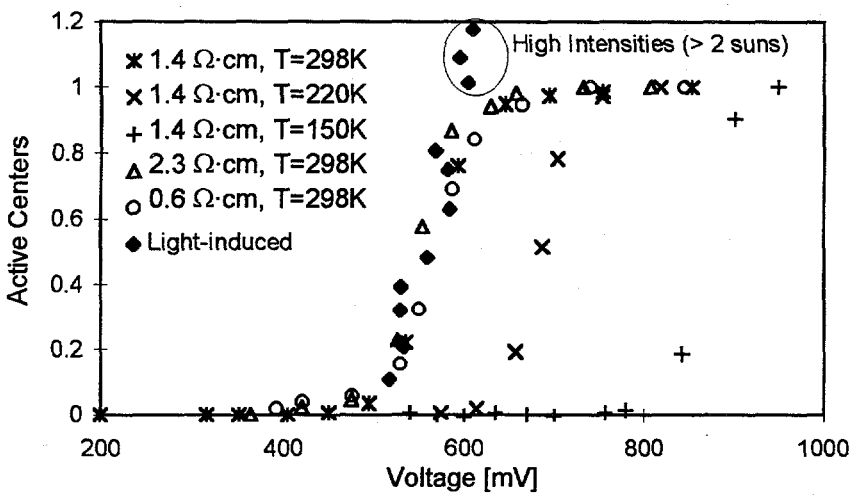

Fig. 6 Degradation of various samples under forward bias at 3 temperatures.

Forward-Bias-Induced Degradation (FBID)

CZ solar cells can also be degraded in the dark by applying a forward bias to the cell. Fig. 6 shows the degradation characteristics under forward bias of different samples. A certain threshold voltage is required to cause degradation, and at a somewhat higher voltage the degradation reaches a saturation level. The dependence on voltage, resistivity and temperature is not fully understood yet. While the data at room temperature alone can be modeled fairly well by a dependence on the Fermi-level splitting and thus a change in charge state of a trap level at 0.73eV above the valence band, this model is not consistent with the measurements at 150K and 220K. Data at these lower temperatures instead indicate a dependence on current density (minority-carrier recombination rate) or electron concentration in the conduction band. The data acquired so far is not yet consistent and is under further investigation. Fig. 6 also includes data from light-degraded cells *vs.* the measured V_{oc} values. It appears that the degradation is related to the creation of electron-hole pairs, rather than by the direct creation of recombination centers by incident photons, although at high intensities (> 2 suns) it was possible to degrade the cells somewhat more than under forward bias.

Thermal Degradation:

It was also found that the CZ solar cells can be degraded by thermal treatment. The cells show degradation above 100 ^{0}C, if they are quickly quenched down to room temperature in a water bath to minimize annealing. The degradation level depends on boron concentration as can be seen in Fig. 7. This again indicates the mechanism of dissociation of an impurity-boron pair. In thermal equilibrium:

$$\frac{N_{pair}}{N_a N_B} = C \exp\left(\frac{E_b}{kT}\right), \quad \Rightarrow \quad \frac{N_a}{N_{total}} = \frac{1}{1 + N_B C \exp\left(\frac{E_b}{kT}\right)},$$

where N_{pair} is the pair concentration, N_a the concentration of active centers, N_B the boron concentration, and N_{total} the total impurity concentration whether bound to boron or free. E_b is the binding energy and C is a constant factor. A least-squares fit results in an extracted binding energy of 0.60eV and C=1.3x10^{-22} cm^3.

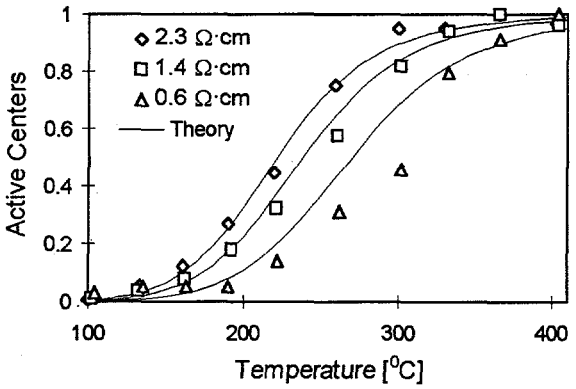

Fig. 7 Degradation level *vs.* temperature.

Discussion

The experimental findings described above suggest an impurity bound to boron at room temperature in thermal equilibrium, which becomes a more effective recombination center once it has dissociated from the boron. Iron, a common impurity in silicon is known to have very similar properties[2-8]:

- Iron in boron-doped silicon at room temperature is bound in iron-boron pairs at thermal equilibrium. Dissociation of these pairs results in interstitial iron ions with an energy level located at about 0.40eV[2-8] above the valence band. These iron ions are very effective at increasing electron-hole recombination and thus reduce the minority-carrier lifetime and diffusion length.
- The dissociation of iron-boron pairs can be caused by light, minority-carrier injection or thermal dissociation. All 3 treatments also cause degradation of CZ solar cells.
- Our experiments derive an annealing activation energy of 0.75eV. Energy values in the literature range between 0.64eV to 0.85eV[2-5,7].
- Published values of the binding energy of iron-boron pairs in silicon are 0.5eV[7] and 0.65eV[2,5], our experiments derive a binding energy of 0.60eV.

All these factors are consistent with iron-boron pair dissociation as the mechanism causing the observed diffusion length degradation in CZ solar cells. From the diffusion length data in Fig. 3 and an equation given by J. Lagowski et al.[2] , $\Delta\left(1/L^2\right) = D_n^{-1} c_i \Delta N_i \left(1 - c_p/c_i\right)$, where N_i is the interstitial iron concentration, c_i and c_p the electron capture coefficients of interstitial iron and the iron-boron pair, respectively, one would calculate an iron concentration of 3×10^{11} cm^{-3}.

Summary

The degradation of CZ solar cells can be caused by light, minority-carrier injection under forward bias, and thermal treatment above 100 °C. The efficiency loss of 3 to 4% at 1 sun is caused by a reduction of the minority-carrier diffusion length in the boron-doped substrate. It is a reversible, short-term effect, which saturates within 30 min. at 1 sun intensity. The conditions under which the solar cells degrade, the measured annealing activation energy of 0.75eV, and a binding energy of 0.60eV are consistent with iron contamination as a possible cause of the degradation. Work is ongoing to test this hypothesis, and to investigate possible interactions with other impurities.

Acknowledgments

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IMPURITY/DEFECT INTERACTIONS DURING MeV Si^+ ION IMPLANTATION ANNEALING

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INTRODUCTION

Ion implantation of dopant atoms at MeV energies is currently being explored in several integrated circuit device manufacturing processes. MeV implantation offers immediate advantages such as vertical well modulation, latch-up protection, device structure isolation, and reduced temperature processing[1,2]. Simultaneously, it presents an opportunity to achieve "proximity" gettering of impurities from the active device region by placing high impurity solubility and/or secondary defect gettering sites within microns of the surface[3]. If the MeV implanted species is a dopant ion, all three gettering mechanisms, i.e, segregation, relaxation and injection, can be involved in the gettering process, complicating the analysis and optimization of the process. However, investigation of gettering using non-dopant Si^+ ion damage allows the relaxation component of the gettering process to be isolated and examined separately. In general, gettering is verified by a reduction in impurity concentration in the region of interest, usually the device region, and/or a build-up of concentration/precipitation in a non-device sink region. An alternate and more meaningful approach is to use simple devices as materials characterization probes via changes in the electrical activity of the gettering sites[6]. Device space charge probes also allow the evolution of the defect sites upon contamination to be tracked. We report here results of the electrical, structural, and chemical characterization of MeV implanted Si^+ damage using Deep Level Transient Spectroscopy (DLTS), Transmission Electron Microscopy (TEM), and Secondary Ion Mass Spectroscopy (SIMS) . The damage has been characterized both as a function of annealing from 600 to 1100°C for 1 hr, and after contamination with Fe followed by low temperature gettering annealing.

SAMPLE PREPARATION AND STRUCTURAL PROFILING

For this study Si^+ ions were implanted at 2.0 MeV to a dose of 1×10^{15} cm^{-2} into 2 to 5 Ω-cm n-type substrates at room temperature. Pieces of the wafers were subsequently annealed at 600, 800, 900, 1000 and 1100°C for 1 hour in a nitrogen ambient. Implantation of Si^+ at 2.0 MeV results in a layer of buried damage centered approximately 1.7 μm below the surface[6]. The

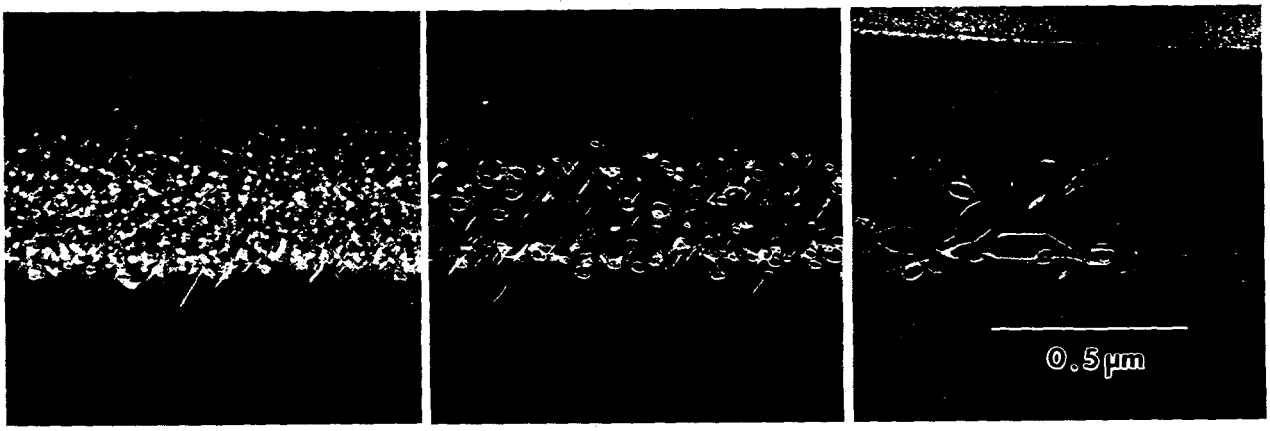

Fig. 1. Dark Field ($\mathbf{g}_{400}$·$2\mathbf{g}_{400}$) images showing dislocation loops after annealing at (left) 800°C, (middle) 900°C and (right) 1000°C.

damage is visible by XTEM as two bands of strain related dark contrast in the as-implanted sample, and as a buried layer of extended defects in the annealed samples, see Ref 6. High resolution imaging of the as implanted sample showed the buried damage to consist of amorphous pockets within a crystalline lattice. The extended defects in the annealed samples are more clearly visible in the (**g**·2**g**) dark field images, see Fig. 1, which show interstitial dislocation loops lying on {111} planes. The size of the dislocation loops varies with the annealing temperature; the average loop diam. increases from 20-30 nm for 800°C, to 40-50 nm for 900°C, and 100-150 nm for 1000°C. The width of the defected region decreases from about 0.5 μm for 800°C to almost 0.3 μm following the 1000°C annealing and the loop density, determined from plan-view TEM, decreases from 4×10^{10} cm^{-2} to 4×10^{9} cm^{-2}, respectively

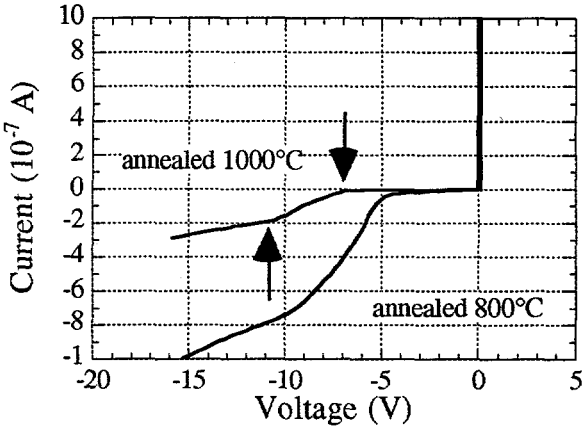

Fig. 2. I-V characterisitcs of Shottky barrier diodes on samples annealed at 800 and 1000°C.

ELECTRICAL PROFILING

For electrical characterization 1 mm diameter Schottky diodes were fabricated simultaneously on all samples by evaporation of a 100 nm thick layer of Au. Typical I-V profiles of the diodes annealed at 800 and 1000°C are shown in Fig. 2. Diodes on both as-implanted and 600°C samples failed to show proper rectifying behavior, precluding both C-V and DLTS measurements. The rectifying properties and leakage current improved with annealing temperature, as shown in Fig. 2. In the 1000°C annealed sample the conductivity increases when the expanding space charge region comes into contact with the buried damage layer, and decreases when it moves beyond the damage, see arrows at -7 and -11V in Fig. 2. For the 800°C sample the increase in conductivity begins at a lower reverse bias, indicating that residual implantation damage still exists above the buried layer.

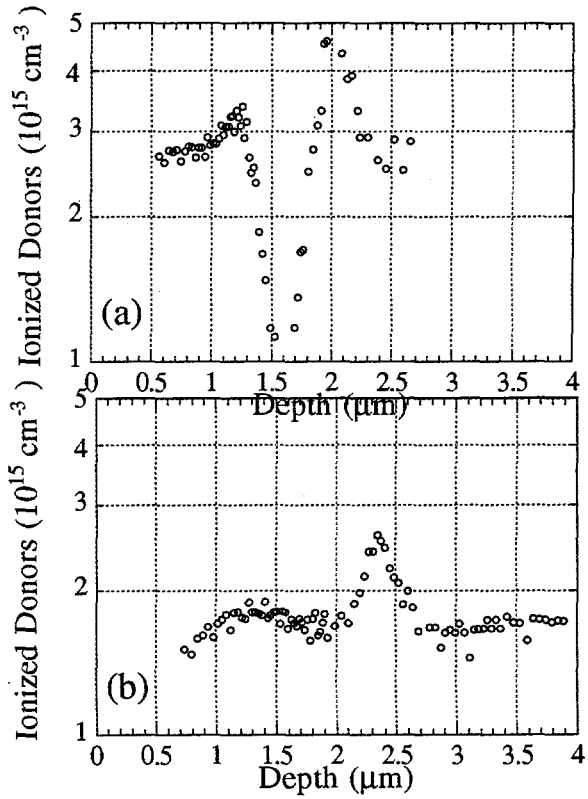

Fig. 3. Ionized donor concentration depth profile extracted from C-V meaurements of the (a) 800°C, and (b) 1000°C samples.

Ionized donor concentrations (N_d) extracted from C-V measurements made on the 800, 900, 1000, and 1100°C samples all revealed an increase in N_d over the nominal value of 2×10^{15} cm^{-3}, at depths corresponding roughly to the top and bottom interfaces of the buried extended defect layer and a decrease in the region within the layer. There is a general trend of a reduction of this effect with increasing annealing temperature. Similar N_d increases related to MeV implantation, referred to as the dopant effect, have been previously observed in carbon implanted wafers, see Skorupa,

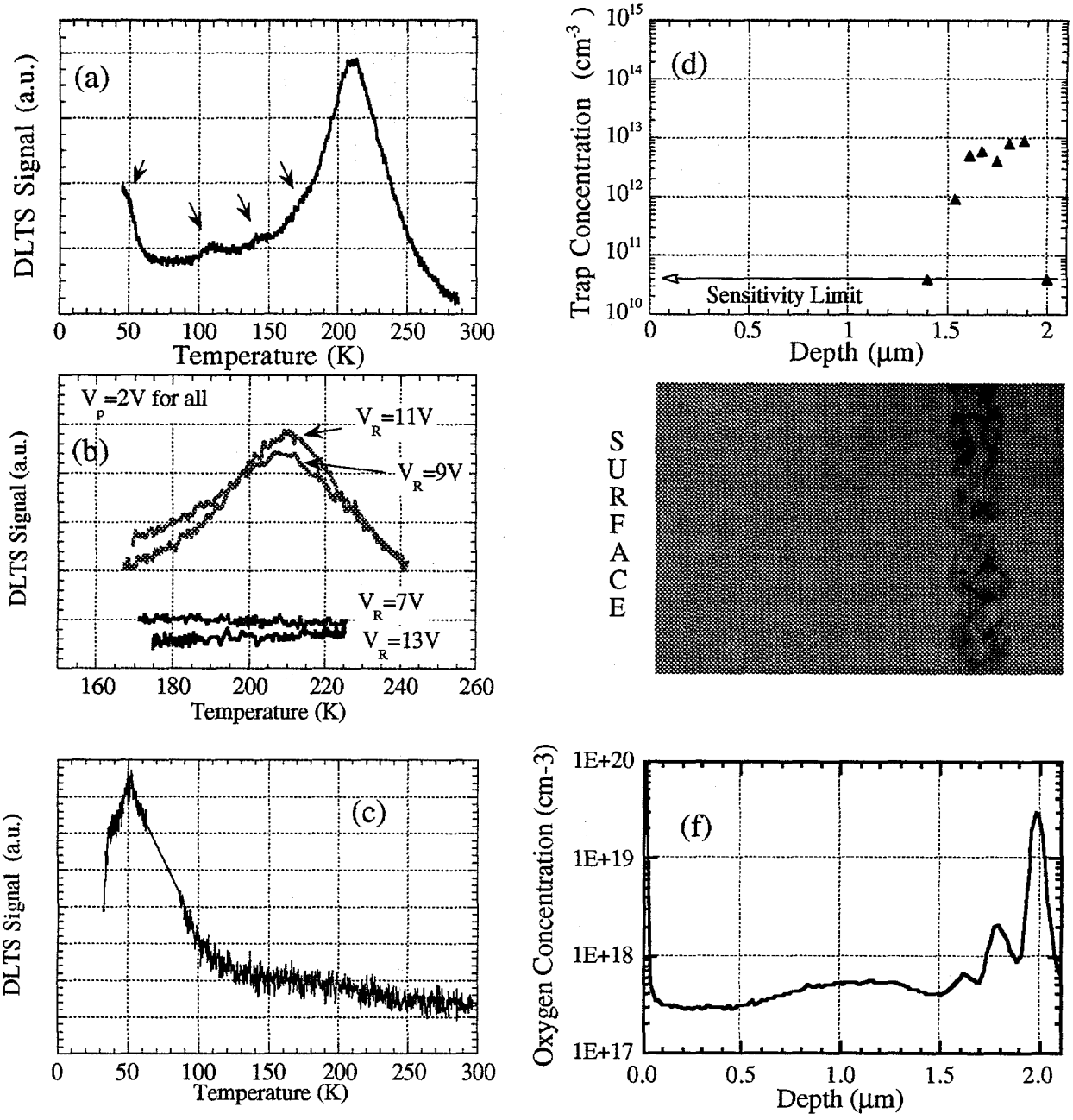

Fig. 4(a). DLTS spectra for 1000°C sample at the buried dislocation layer (b), and (c) following contamination with Fe and annealing at 600°C for 5 hours. (d) Trap concentration vs. depth. (e) XTEM image and (f) oxygen profile by SIMS. Note same horizontal scale for figures (d), (e) and (f).

et al.[4], and references therein; however, they reported that no dopant increase was observed in Si implanted wafers, as measured by spreading resistance measurements.

Depth dependant DLTS measurements were performed on samples annealed at 800, 900, 1000 and 1100°C. All samples showed deep level electrical activity arising from the buried layer of extended defects, while the 800°C sample additionally showed electrical activity in the region above, which is referred to as the device layer. The DLTS spectra corresponding to the 1000°C

sample reveals at least 4 peaks, see Fig 4a. The most prominent peak at 211K contains a shoulder at 170K, and two smaller peaks are located at approximately 135 and 100K. The activation energy for the 211K peak was found to be E_C-0.44 eV. The deep level activity is confined to the buried dislocation layer only, as demonstrated in Figs 4b and d. Spectra obtained from the constant filling pulse method are presented in Fig. 4b, where the flat scans for V_R=7 and 13V correspond to sampling volumes located above and below the defect layer. Trap concentrations derived from the constant reverse bias method are given in Fig. 4d and compared with the XTEM image of Fig. 4e. Above and below the buried dislocation layer the deep level defect concentration falls to below 10^{10} cm^{-3}, the sensitivity limit of our system. The average trap density in the buried layer was 5×10^{12} cm^{-3}. The as-implanted and 1000°C samples were also investigated by SIMS for the presence of Cu and Fe, and C, P and O. Oxygen was the only element detected and was present in concentrations as high as 3×10^{19} cm^{-3}. The oxygen segregated at the buried dislocation layer in a profile similar to that of the electrically active deep levels.

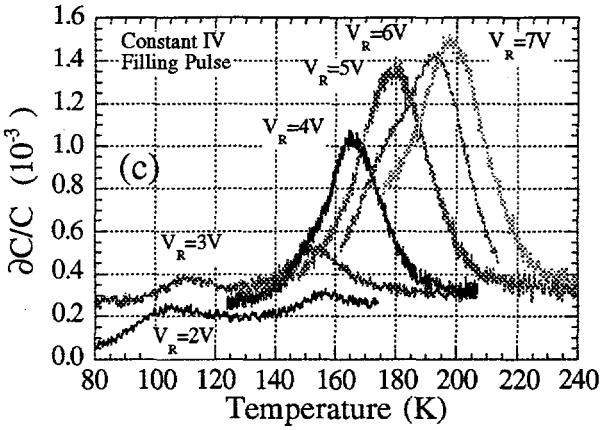

Fig. 5. (right) DLTS spectra for 800°C sample with constant V_p = 1V and V_R=2, 3, 4, 5, 6, and 7V.

The DLTS spectra for the samples annealed at 1100 and 900°C were qualitatively the same as for the sample annealed at 1000°C and only differed in the magnitude of the deep level center located at E_C-0.44 eV. This trap concentration decreased from 1×10^{13} cm^{-3} to 1×10^{12} cm^{-3} in the 900°C and 1100°C annealed samples, respectively. No deep level activity was observed at depths shallower or deeper than the buried layer of extended defects. For the sample annealed at 800°C depth dependent DLTS peaks were present above the buried dislocation layer, see Fig. 5. At least 5 distinct traps can be seen in the various spectra: at 110K and 155K (V_R=3V), 165K (V_R=4V) 180K (V_R=5V) and 198K (V_R=7V). These are the probable sources of the enhanced leakage showwn in Fig. 3.

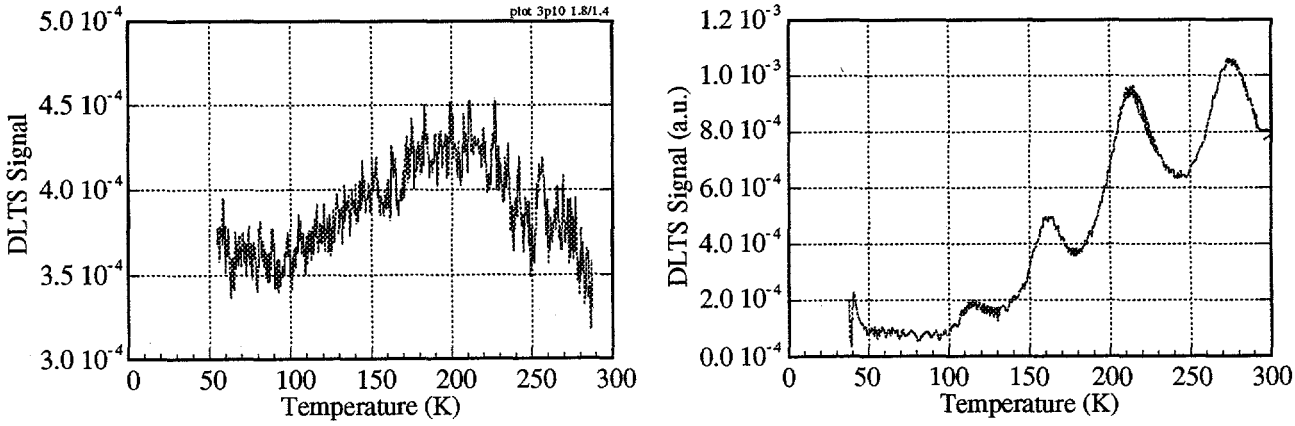

Fig. 6 - DLTS Spectra corresponding to 3×10^{14} cm^{-2}, Si$^+$ ion implantation damage in p-type substrates (a) before and (b) after contamination with Fe.

CONTAMINATION WITH Fe

DLTS measurements were repeated on the 1000°C sample following introduction of Fe by scratching the backside, and then annealing at 600°C. The deep levels in the uncontaminated sample responsible for the four peaks in Fig 4a were replaced by a much shallower level below 60K, see Fig 4c. Since the electrical activity remained confined to the region of the buried layer, it can be assumed that decoration of the dislocation loops led to a suppression of the deep level activity. In a comparison experiment on p-type substrates homogeneously contaminated with 1×10^{14} cm^{-3} of Fe and implanted with 2.0 MeV Si^{+} to a dose of 3×10^{14} cm^{-2} contamination induced reduction in deep level activity was not observed. In fact annealing of thi p-type sample at 600°C led to an enhancement of the deep level traps corresponding to the dislocation layer, compare Figs. 6a and b. Note that the absence of an Fe-B signal following the 600°C anneal, see Fig 6b, indicates that the Fe was successfully captured by the dislocation loops. These findings point to a complex relationship between dislocation loop evolution upon contamination in n- and p-type substrates and the electrical activity.

SUMMARY

In summary, MeV implantation damage has been found to exhibit a unique spectroscopic signature, which may be used to track the electrical response to contamination, gettering activity, and implantation damage. The deep level trap profile associated with the MeV damage has been shown to be enhanced or reduced depending on the substrate type. The role of the oxygen segregated at the buried layer in the gettering process or electrical behavior is not clear at this time. We are continuing investigations to determine if the dislocation gettering activity is aided by formation of SiO_x precipitates. It is anticipated that resolution of these issues will lead to viable defect engineering options for proximity MeV implantation gettering.

ACKNOWLEDGEMENTS

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PHOSPHOROUS AND ALUMINUM GETTERING IN SILICON-FILM™ PRODUCT II MATERIAL

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ABSTRACT

Gettering processes are being developed for the Silicon-Film™ Product II solar cell structure. These processes have been developed specifically for films of silicon grown on dissimilar substrates with barrier layers. Gettering with both phosphorous- and aluminum-based processing sequences has resulted in enhancement of minority carrier diffusion length. Long diffusion lengths have allowed the characterization of light trapping in thin films of silicon grown on barrier-coated substrates.

INTRODUCTION

AstroPower is in the first year of a three year program with the National Renewable Energy Laboratory to develop a polycrystalline silicon thin-film module fabrication process and manufacturing technology. The program will develop an advanced thin-film, silicon-based, 400 watt, 4 ft x 8 ft (2.97 m^2) photovoltaic panel for use in power applications. This module will combine the design and process features of the most advanced thin-silicon solar cells, including the use of light trapping, surface passivation, and lateral conductivity enhancement. These solar cells will be formed on an insulating substrate and integrated into a low-cost, interconnected sub-module.

The photovoltaic sub-module under development under this sub-contract, Product II [1], is an advanced version of the Product I [2] solar cell. It consists of a thinner film (50 μm) grown on a metallurgical barrier-coated substrate. The barrier layer affects light-trapping and back-surface passivation for improved conversion efficiency.

Gettering with both phosphorous- and aluminum-based sequences has resulted in enhancement of minority carrier diffusion length and solar cell current in the Product II solar cell structure. There are some interesting considerations when gettering this solar cell structure, namely the presence of a dissimilar substrate and metallurgical barrier, and the thickness of the photovoltaic layer. In spite of the substrate or barrier layer, we have observed good enhancement of minority carrier diffusion length with both phosphorous and aluminum gettering sequences. We have observed improved gettering efficiencies in the thinner silicon layers of the Product II structure compared to the Product I wafer. Further, long diffusion lengths have allowed the observation of light trapping effects in Product II devices.

GETTERING OF SILICON-FILM™ PRODUCT II MATERIAL

Post-growth material quality enhancement techniques play an important role in the development of Silicon-Film™ solar cells. A majority of the development of gettering processes has occurred on Product I wafers where bulk lifetime improvements have been demonstrated [3]. Optimal $POCl_3/O_2$ ratios, process times and temperatures (890°C) were used in this work.

Several authors have reported improvements by combining phosphorous gettering with a back-surface aluminum treatment [4,5,6]. However, the substrate and metallurgical barrier layer in the Product II structure prevent effective removal of impurities gettered to the back side of the wafer, reducing the benefit of using aluminum on the wafer back surface. A modification to the process whereby aluminum is deposited onto the front surface has been implemented in Product I wafers and adapted for this structure. The wafer is processed with the same time, temperature and $POCl_3/O_2$ ratios used in the phosphorous gettering process. After the process is complete, the aluminum and aluminum-silicon alloyed regions are chemically removed. The use of an evaporated aluminum layer on the front surface during the gettering sequence has been demonstrated, however, the subsequent removal of aluminum and aluminum-silicon alloy layers may create problems in very thin films (< 35 μm).

Typically, minority carrier diffusion lengths in as-grown films (60–100 μm) of silicon grown on metallurgical barrier coated substrates range between 20–40 μm. Employing the gettering process developed specifically for Product I wafers (four hours at 890°C) results in a significant improvement in diffusion length for both phosphorous and aluminum gettering processes. Testing of small-area test devices indicates diffusion lengths improve, on average, to 95 μm and 100 μm for phosphorous and aluminum gettering, respectively. Figure 1 shows the

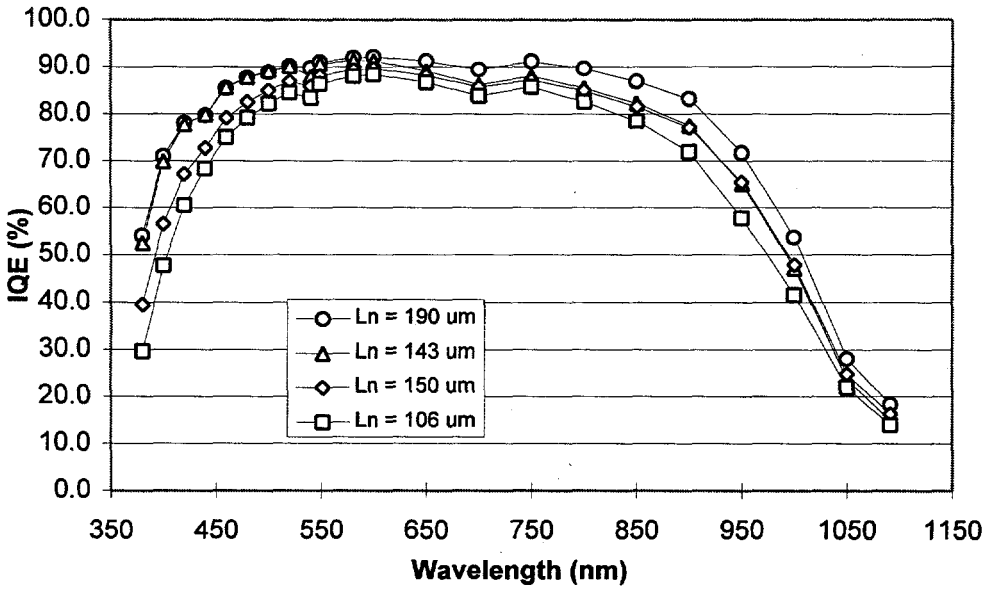

Figure 1. *Quantum efficiency curves for recent 0.5 cm^2 Product II solar cells.*

quantum efficiency curves of four recent 0.5 cm^2, Product II solar cell devices from the same sample and processed with the phosphorous only gettering sequence. A high diffusion length of 190 μm is measured on one of these four devices.

One opportunity for thin films of silicon is the reduced volume from which impurities must be gettered, possibly allowing reduced processing time or resulting in greater impurity gettering efficiency. Our initial results indicate that, compared to its Product I counterpart, Product II devices exhibit higher gettering efficiency when using identical processes. This is perhaps due to the thickness of the film or the ability of the barrier layer to sink impurities. In

any case, no optimization of the gettering process has been implemented, therefore, we believe that additional improvements in material quality can be gained by developing process specifically for this structure.

Solar cells with minority carrier diffusion lengths approaching the absorber-layer thickness allow the examination of the light trapping and back-surface recombination properties of the device structure [7]. The reflectance and spectral response of weakly absorbed, near-bandgap light can be analyzed to determine the reflectance of the back surface and the effective optical path length of near-bandgap light.

Analysis of internal quantum efficiency data taken on a small-area (approx. 0.2 cm^2) test device (60-μm thick) by examination of inverse internal quantum efficiency versus inverse absorption is shown in Figure 2. From the inverse slope of a best fit line for short wavelength light (750 to 980 nm), a diffusion length of 82 μm is calculated. From the inverse slope of the best fit line for long wavelength light (1050 to 1100 nm), an effective optical thickness of 570 μm and corresponding effective optical path length, Z, of approximately 20 is calculated. Furthermore, the reflectivity of the barrier layer to weakly absorbed light is calculated to be 29% or greater.

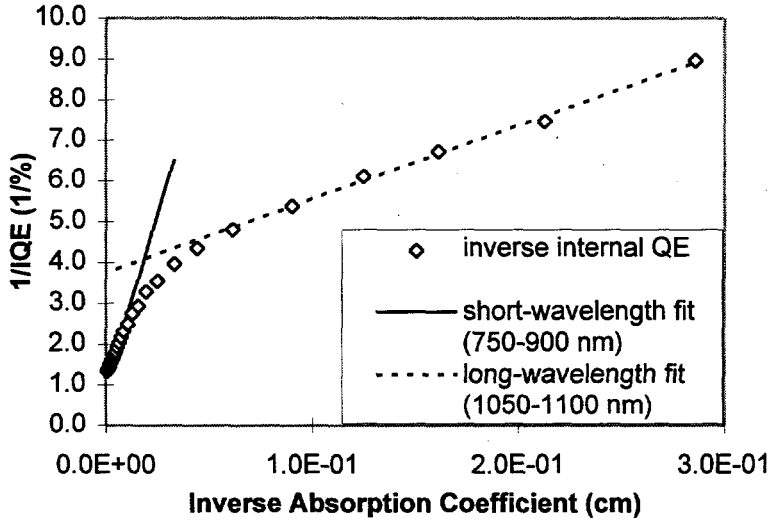

Figure 2. *Inverse internal quantum efficiency versus inverse absorption coefficient for a 60-μm thick Product II solar cell.*

The sample under study had a textured front surface and was randomly textured at the barrier. This texturing led to a significant portion of the light being internally reflected at oblique angles to produce an optical path length much greater than the device thickness. A combination of a relatively low back surface reflection (≤ 29%) and low back back-surface passivation lowered the overall collection efficiency of near-bandgap light to 28%.

CONCLUSIONS

Phosphorous and aluminum gettering techniques are being developed specifically for Silicon-Film™ material, accounting for the presence of the substrate and the metallurgical barrier in the Product II solar cell structure. We have developed aluminum gettering techniques whereby the aluminum layer is placed on the front of the wafer.

Product II material shows a strong response to both gettering processes. Diffusion lengths improve to an average of about 100 μm with phosphorous and aluminum gettering. A high of 190 μm was measured on one device. Our initial results indicate that, compared to its Product I counterpart, Product II devices exhibit higher gettering efficiency when using identical processes. This is perhaps due to the reduced thickness of the film or the ability of the barrier layer to sink impurities. We believe that additional improvements in material quality can be gained by developing the gettering processes specifically for the Product II structure.

High diffusion lengths have allowed the measurement of the light-trapping properties of Product II solar cells. A high optical path length and 82-μm diffusion length was inferred from internal quantum efficiency measurements of test devices fabricated on a 60-μm thick film.

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ALUMINUM GETTERING IN SINGLE AND MULTICRYSTALLINE SILICON

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Abstract

Al gettering has been performed on integrated circuit (I.C.) quality silicon and a variety of single and multicrystalline silicon solar cell materials. The minority carrier diffusion length, L_n, has been used to quantify the gettering response. Vast differences in response to the Al gettering treatment are observed between the I.C. quality silicon and the solar cell materials. The I.C. silicon generally responds well while the solar cell silicon performance progressively degrades with increasing gettering temperature. Preliminary data shows that by performing a Rapid Thermal Annealing treatment prior to the Al gettering, an improved or further degraded L_n emerges in solar cell material depending on the material's manufacturer. We explain these observed phenomena by suggesting that Al gettering in solar cell silicon is an impurity emission-limited process while for I.C. quality silicon it is diffusion limited.

Introduction

In order to create high efficiency solar cells, the minority carrier diffusion length, L_n, must be significantly high to allow for complete capture of carriers at the n^+/p junction. Recent work, [1], has shown a L_n of approximately 350 μm should be present to have maximum solar cell performance. As-grown L_n values are usually much lower than this value in both single crystal and multicrystalline solar-silicon which necessitates additional processing steps, specifically phosphorus and/or aluminum gettering. These gettering techniques remove metallic impurities from the silicon lattice and out of structural defects by providing a region of high impurity solubility [2-5], thus, they are referred to as segregation-type gettering processes. The removal of these impurities increases L_n by decreasing the number of minority carrier recombination paths. Kang and Schroder [6] have presented a model which describes segregation gettering as a three step process: release of the impurities from their previous site (in a precipitate form or within the Cottrell atmosphere of a defect), diffusion of the impurity to the gettering region and capture of the impurity into the gettering region. Diffusion of the impurities is the rate limiting step at low temperatures while the capture process limits impurity removal at high temperatures. With this model, one creates an optimal temperature for gettering as shown in Figure 1.

In multisilicon, it has been observed that both gettering techniques tend to only improve regions of high as-grown L_n [7,8]. The source of low L_n regions has been attributed to structural defects, specifically dislocations [7]. Since dislocations are known to increase in recombination activity with increasing metallic impurity decoration [9,10], it can be reasonably assumed that standard phosphorus and aluminum gettering do not sufficiently remove impurities from dislocations in multicrystalline silicon, since a significant improvement in L_n values is not observed.

In terms of the Kang and Schroder model, these observations for multisilicon may be rationalized in one of three manners. The first possibility is that, in these dislocated regions, there is an extremely large concentration of fast diffusing impurities, precipitated or "dissolved" in the dislocation's Cottrell atmosphere, which are not completely gettered during standard gettering times. Alternatively, a second possibility is that slow diffusing impurities are precipitated or dissolved near dislocations in multisilicon which also cannot be effectively gettered for reasonable gettering times simply due to their short diffusion distance. Both of these explanations would be expected to decrease L_n with increasing gettering temperature because an increased concentration of metallic impurities would be left in the lattice, acting as carrier recombination centers and thus lowering L_n. Additionally, the optimal gettering temperature will be significantly lowered (where little or no diffusion may occur) and, more importantly, the overall gettering efficiency is significantly decreased. This is shown graphically in Figure 1. The third possible explanation is that the metallic impurities are limited in their release from dislocations, especially at low temperatures. This may occur because of the dislocations' large strain field which significantly stabilizes metallic precipitates or the metallic precipitates are extremely large such that the driving force for dissolving them is much smaller compared to smaller metallic precipitates found in single crystal silicon. All of these possibilities assume I.C. quality silicon possesses small metallic precipitates of fast diffusers which are effectively gettered during standard gettering times. The third of these possible mechanisms would create a higher optimal temperature and again decrease the overall gettering efficiency. This is portrayed in Figure 1.

In order to better understand gettering in solar cell silicon, our work presented here analyzes the dependence of L_n improvement on Al gettering temperature in a variety of IC quality silicon and solar cell silicon, both single crystal and multicrystalline. With this work, we hope to understand the failings of Al gettering on improving L_n values in solar cell silicon in terms of metallic impurity-structural defect interactions. Additionally, we introduce a Rapid Thermal Annealing (RTA) process step which is designed to augment the standard Al gettering process in solar cell silicon by enhancing the dissolution of large impurity precipitates.

Experimental Procedure

For this study we have used Float Zone (FZ) and I.C. quality Czochralski (CZ) single crystal silicon, both of which are low in carbon content ($< 1x10^{16}$ atoms/cm^3) while the CZ material has $\approx 8x10^{17}$ oxygen atoms/cm^3. We also have used solar cell quality CZ from two different manufacturers. The CZ silicon from manufacturer A is low in carbon content and possesses $\approx 8x10^{17}$ oxygen atoms/cm^3. From manufacturer B, we have utilized low and high carbon content ($\approx 2x10^{17}$ atoms/cm^3) CZ silicon. Both materials have an oxygen concentration of $\approx 8x10^{17}$ oxygen atoms/cm^3. Additionally, we have studied cast and ribbon grown multicrystalline solar silicon. These cast and ribbon materials have oxygen concentrations of $< 1x10^{17}$ atoms/cm^3 and carbon contents of $< 1x10^{17}$ atoms/cm^3 and $\approx 8x10^{17}$ atoms/cm^3, respectively. Of particular note is the selection of ribbon multisilicon samples. Since the microstructure of this material can change drastically over mm distances, we carefully selected samples along the growth direction which was such that the microstructure was kept approximately the same from sample to sample. We call these correlated-ribbon multisilicon samples. This could not be accomplished with our supply of cast multisilicon but instead we chose uniformly low L_n samples. If any inconsistencies in data were present, microstructural analysis was performed with preferential etching and optical inspection.

2.5μm of Al was sputtered onto each sample under high vacuum, $\approx 2x10^{-7}$ torr. Al gettering was performed at 800, 850, 900 and 950°C in a nitrogen ambient for 3 hours on a number of samples from each material type. The gettering was performed in a clean furnace used for daily I.C. device fabrication. On a select number of samples, two types of RTA treatments were performed prior to Al deposition and gettering. The first uses a commercially available Heatpulse RTA chamber in which the samples were annealed for 45 seconds at 1100°C in a nitrogen ambient and cooled to 500°C within 5 seconds and to 300°C within 3 minutes. The second RTA treatment was performed in a vertical quenching RTA furnace which was designed and built at U.C. Berkeley. We refer to this appartus as the RTAQ furnace. This heat treatment was also carried out for 45 seconds at 1100°C in a nitrogen ambient but rapidly quenched into ethylene glycol at room temperature with a quench rate of $\approx$ 1000K/sec. Following these RTA and RTAQ treatments the samples were then subjected to Al deposition and gettering at 900°C. Prior to all heat treatments, all samples were "piranha" (5 H_2SO_4:1 H_2O_2 at 120°C) cleaned and etched to remove 10-20 μm and avoid contamination from the sample surface. Each material's diffusion length was measured with the Surface Photovoltage (SPV) method [11] in the as-grown state, after RTA or RTAQ treatment and after Al gettering. This technique measures an average L_n value over a 5mm spot size. Prior to SPV measurement, all samples were "piranha" cleaned and dipped in HF to ensure a clean, oxide-free surface for measurement.

Results

Figure 2a shows the final L_n value for I.C. quality FZ and CZ subjected to the various Al gettering treatments. Although the data is slightly scattered, one can see an optimal temperature, as predicted by the model of Kang and Schroder, of 850°C for both materials. The Float Zone material has slightly improved from its original value while the CZ material has significantly improved. In Figure 2b, the same graph as 2a is shown for solar grade CZ and a much different result is present. Here we see manufacturer A's CZ is unaffected by all gettering treatments, essentially retaining its original L_n values. However, manufacturer B's CZ material L_n has severely decreased from its original L_n with increasing gettering temperature. Figure 3a shows the response of the correlated-ribbon multisilicon. Although not as pronounced as in manufacturer B's solar CZ material, again there is a decrease in L_n with increasing gettering temperature regardless of as-grown L_n value. The same trend is found in Figure 3b for cast multisilicon. However, the cast material's Ln has improved greatly from its as-grown value at all gettering temperatures.

The RTA/RTAQ results are shown in Figure 4. Here we see the I.C. quality CZ has a slightly decreased final L_n value with RTA or RTAQ treatment as compared to Al gettering only. The response of the solar grade material varies greatly. Manufacturer A's CZ silicon was degraded with the RTAQ treatment while both low C and high C CZ from manufacturer B benefited greatly from the RTA or RTAQ treatments. The ribbon multisilicon response varied with some regions benefiting and others degrading especially with the RTAQ treatment. In order to determine the cause for this varying response, preferential etching was performed on each of these regions. In general, for the ribbon multisilicon, regions of very low dislocation densities ($<10^4$ cm^{-2}), i.e. region 6, degrade with RTA or RTAQ treatment while regions with significant dislocation densities ($\approx$ mid-10^7 cm^{-2}), i.e. regions 2&3, improve with the treatments. Finally, the cast multisilicon's L_n greatly improved with RTA and RTAQ treatments.

Discussion & Conclusions

The results of I.C. quality material re-establish a common belief that this material possesses a low concentration of metallic impurities which can be removed with Al gettering. Additionally, an optimal temperature with a high gettering efficiency exists with this material. The RTA and RTAQ treatments did degrade L_n values for the I.C. CZ but only slightly which shows the cleanliness of these processes.

For solar grade materials a variety of responses to treatments was observed. All but two materials, manufacturer A CZ and low dislocation density ribbon multisilicon, Ln degraded with increasing gettering temperature. This may be explained by the as-grown material's contamination level The low dislocation density ribbon region possesses a lower impurity concentration than heavily dislocated regions via impurity "gettering" during the slow cool of ribbon growth. Based on the discussion in the introduction, this indicates the remaining materials possess slow diffusing impurities or a large concentration of fast diffusing impurities which are left in material after gettering and lower L_n values. Considering that slow diffusers would likely remain in low dislocation density multisilicon during the slow cool of ribbon growth and we do not see degradation of this material with increasing gettering temperature, we suggest there is a large concentration of fast diffusers in the materials which degrade L_n with increasing gettering temperature. The RTA and RTAQ treatments significantly improved the gettering response of numerous materials, specifically, manufacturer B's high and low C CZ and the heavily dislocated ribbon multisilicon. This effect originates from the these material's high as-grown contamination level. During the slow cool from growth, the impurities in material with higher contamination levels will begin precipitate out at a higher temperature than impurities in a material with lower contamination levels. This necessitates the growth of larger impurity precipitates in the highly contaminated material than the purer material. The RTA and RTAQ treatments assist in dissolving the larger impurity precipitates. The cast multisilicon degraded with these treatments, however, the samples were not correlated as with the ribbon multisilicon and single crystal silicon.

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Figures

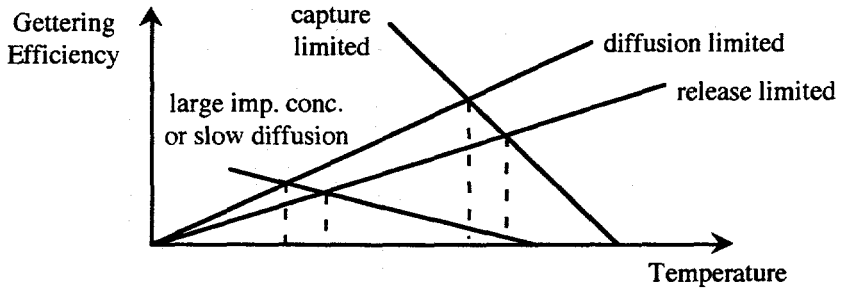

Figure 1: An arbitrary gettering efficiency versus gettering temperature for various limiting cases.

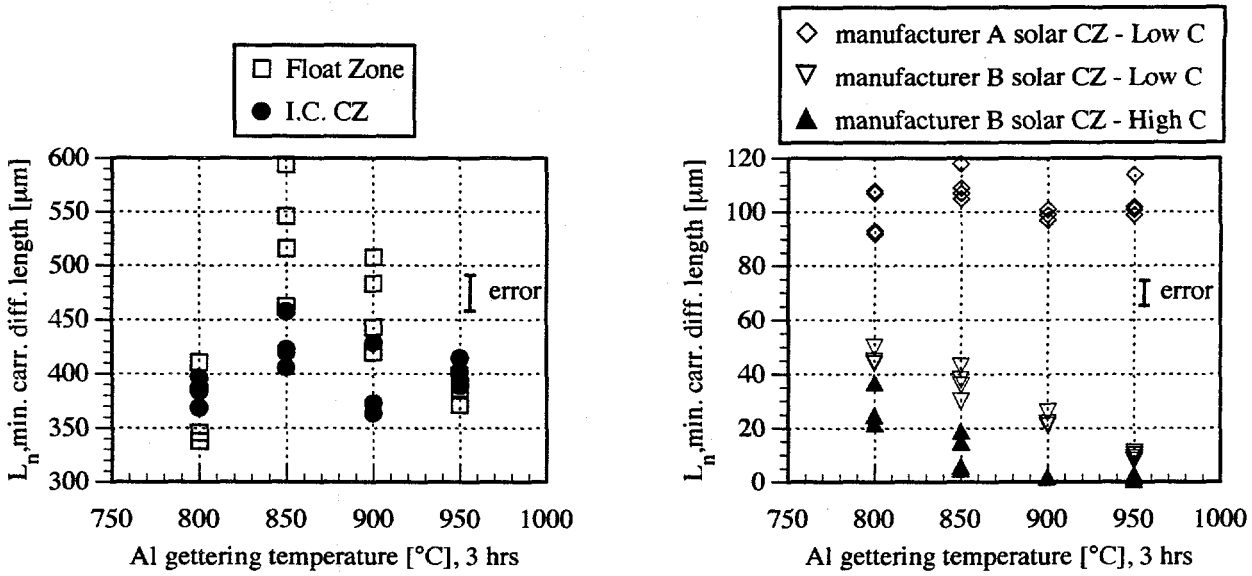

Figure 2: a) Gettering response of Float Zone and I.C. CZ with as-grown L_n values of ≈425μm and ≈155μm respectively. b) Gettering response of manufacturer A and B's solar grade CZ. As-grown Ln values are: A - low C: ≈110μm, B - low C: ≈72μm and B - high C: ≈70μm.

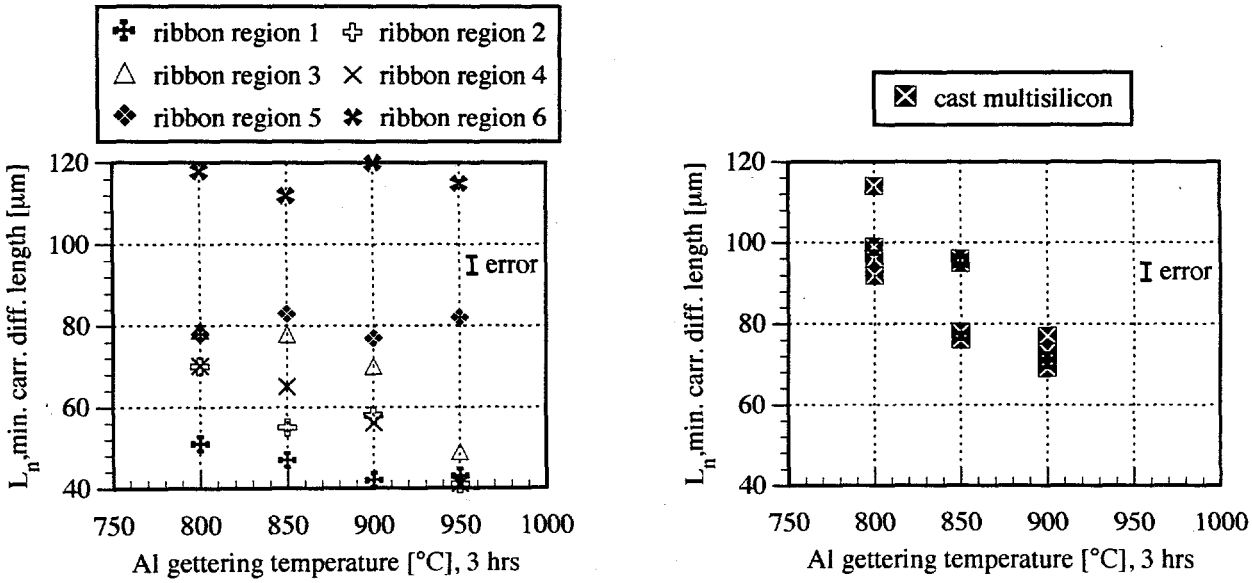

Figure 3: a) Gettering response of ribbon multisilicon with as-grown L_n values of: region 1: ≈36μm, region 2: ≈43μm, region 3: ≈48μm, region 4: ≈33μm, region 5: ≈75μm and region 6: ≈115μm. b) Gettering response of cast multisilicon with as-grown Ln values of ≈27μm.

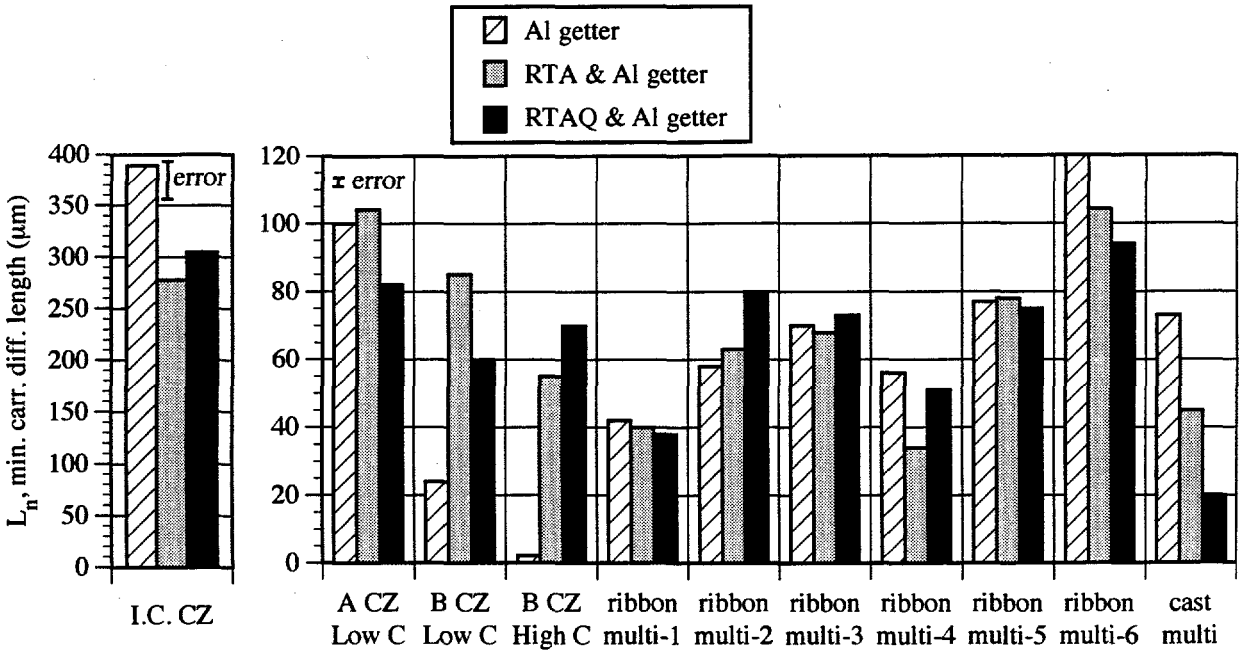

Figure 4: Gettering response comparison between Al gettering only, RTA & Al gettering and RTAQ & Al gettering for a variety of I.C. and solar grade silicon.

New monocrystalline $Si_{1-x}Ge_x$ solar cells

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The development of solar cells on $Si_{1-x}Ge_x$ might be interesting because they might present more current photo-response than the silicon cells, based on the lower bandgap of the alloyed crystal. In particular the use of $Si_{1-x}Ge_x$ solar cells in dual bandgap concentration structures as GaAs/$Si_{1-x}Ge_x$ can lead to total efficiency increase of about 1% as compared to the GaAs/Si structure, according to our calculations.

Our effort is devoted to solar cells with low content of Ge, lower than 20%at. This choice is based on two previous hypothesis

1.- A low content of Ge suggests that the well known silicon cell process, slightly modified, can be applied to the $Si_{1-x}Ge_x$ cells.

2.- Calculations suggest that for utilisation in tandem with GaAs cells, the gain of efficiency is low above 20at % Ge.

To this end high lifetime bulk monocrystalline $Si_{1-x}Ge_x$ has been grown, by CZ and FZ technology, and the procedures and results are being presented independently. In this paper we are presenting the first results of $Si_{1-x}Ge_x$ cells. All this work is being performed as part of the MONOCHESS II project within the frame of the EC JOULE programme.

It is important to mention that the high lifetime in the starting material is achieved through a gettering process, that leads to base lifetimes in excess of 100 μs.

Si solar cells are simultaneously processed for monitoring the fabrication process. The cells $Si_{1-x}Ge_x$ show an efficiency of 9.5% .

The open circuit voltage, of 576 mV is not bad for a first attempt taking into account the high base resistivity that generally gives lower values and makes this voltage more dependent on the base life time.

On the contrary the short circuit current, of $Si_{1-x}Ge_x$ cell, is too low. This is due, in part to a larger reflectivity measured on the SiGe wafer in the short wavelengths and to the existence of an absorbing dead layer, as revealed by internal quantum efficiency measurements that shows a poor collection of the shorter wavelengths. This odd behaviour deserves more study, but we think that it is due to complex segregation structures, that have been proposed by several authors, for the SiGe/oxide interface. The existence of a thin film Ge-rich could explain this fact. This hypothesis is supported by the low sheet resistance found in the cell after drive-in, much lower that the one of the Si cell used for control.

The fill factor is 0.75, that can be considered reasonable. No leakage is visible in these cells showing the feasibility of our processing approach from a manufacturing viewpoint.

For comparison the Si cells fabricated in the same batch and with the same process give an efficiency of 15.4%,, a J_{sc}=34,5mA/cm_2, V_{oc}=600 mV and fill factor of 0.75

The quantum efficiency in the longer wavelengths is found to be exactly the same than the one of Si cells. Thus, despite no improvement is found so far, the problems visible at the short wavelengths can be responsible for a reduction of the overall photo-response that if solved, seems to announce a potential improvement. Yet these problems might find solution as they are certainly associated to a superficial structure that will probably be possible to remove. In conclusion, it can be established that $Si_{1-x}Ge_x$ solar cells can be processed successfully by procedures related to silicon cell processing, at least if Ge atomic fractions are in the range minor of 2.3% . The field remains probably open for very substantial improvements.

New Monocrystalline $Si_{1-x}Ge_x$ solar cells

Introduction.

To complete and support the statements in the abstract we describe the cell fabrication process and present some experimental results.

Processing of the $Si_{1-x}Ge_x$ wafers.

We carried out our typical process of fabrication of Si solar cells plus a first step of gettering treatment for increasing the initial low minority carrier lifetime (40ms) to above 100ms, in $Si_{1-x}Ge_x$ samples. The $Si_{1-x}Ge_x$ wafers have been processed, jointly with two Si wafers as test of process.

1) Pre-gettering by $POCl_3$ at 900 °C for 30'
2) Clean organics and chemical polish etch by CP4
3) Oxidation at 1000 °C, 2 hours wet oxidation and 1.5 hours dry oxidation
4) Photolithography process to open the active area of 0.671 cm^2
5) Random upright pyramid texturing by KOH etch
6) Phosphorus pre-deposition using a $POCl_3$ source; 10' at 850 °C
7) Evaporation of Al on the back surface
8) Drive-in 3 hours at 1050 °C
9) Grid definition by lithography.
10) Metallization of Ti/Pd/Ag and lift-off
11)Electrolytic Ag growth
12) Al/Ag back surface metallization
13) Annealing at 450 °C in forming gas during 2.5 hours
14) Deposition of a double anti-reflection coating, (DARC), 45nm ZnS &105nm MgF_2

Results:

During the fabrication we performed several analysis of the process:
1) Thickness measurements carried out after the thermal oxidation have shown that oxidation thickness is larger in the $Si_{1-x}Ge_x$ samples (715 nm) than in pure Si wafers (630 nm)
2) A larger sheet resistivity is found in the $Si_{1-x}Ge_x$ cells after drive-in. This is a sensible point that affects to the cell behaviour and that therefore must be investigated further (see Table1).
3) No problem was found in the texturing. Nice pyramids were formed. However their shape was different than in Si wafer due to the different surface orientation.
4) Strong difference of reflectance between $Si_{1-x}Ge_x$ and Si solar cells, This difference is quite clearly after DARC deposition, Figure 3. The possible presence of a Ge-rich segregated thin film can be the explanation of this fact and of the larger sheet resistance before mentioned.

Name	Oxide thickness (nm)	Rs (Ω/□) Deposition	Rs (Ω/□) Drive-in	J_{sc} (mA/cm^2)	J_{sc} DARC (mA/cm^2)	V_{oc} (mV)
Si(1)	630	140	63	31.2	34.6	600
$Si_{1-x}Ge_x$	715	140	12	21.6	21.9	576

Table 1. Initial oxide thickness, sheet resistances after deposition and drive-in and short circuit currents without and with a double anti-reflecting coating. The values of J_{sc} have been obtained considering mismatch factor.

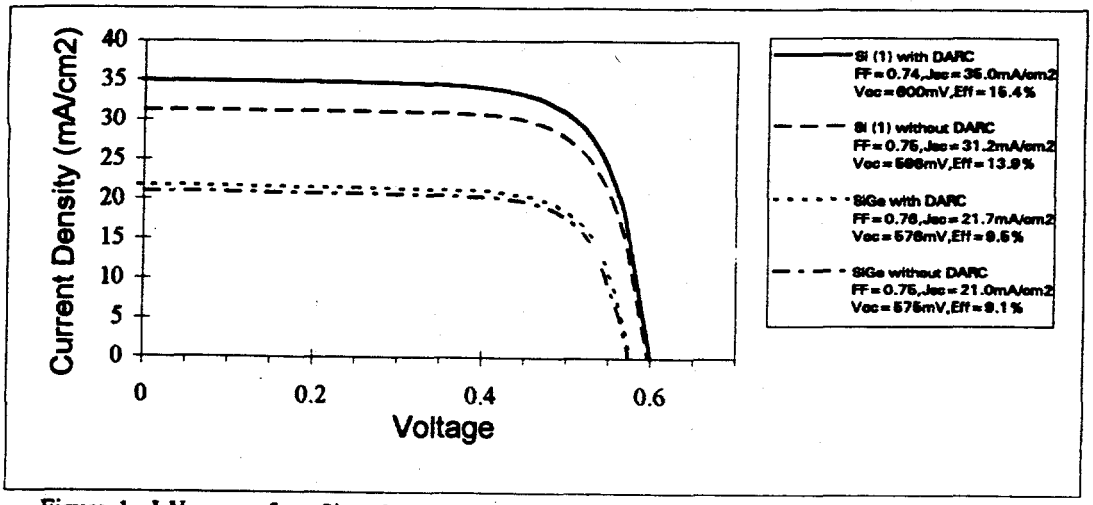

Figure 1. J-V curve for Si and $Si_{1-x}Ge_x$ cells with and without DARC. (Data for curves are measured before applying mismatch factors).

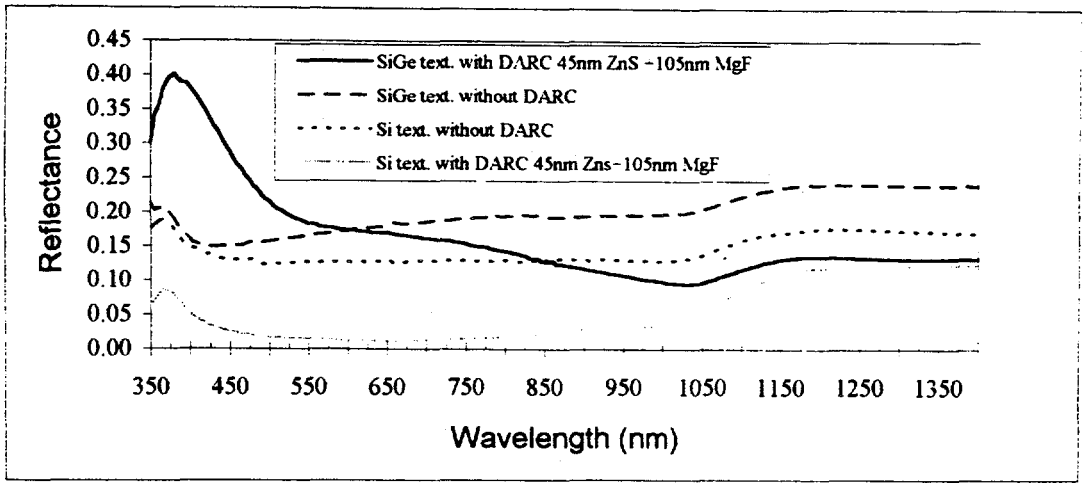

Figure 2. Reflectance of a Si and $Si_{1-x}Ge_x$ cell with and without DARC.

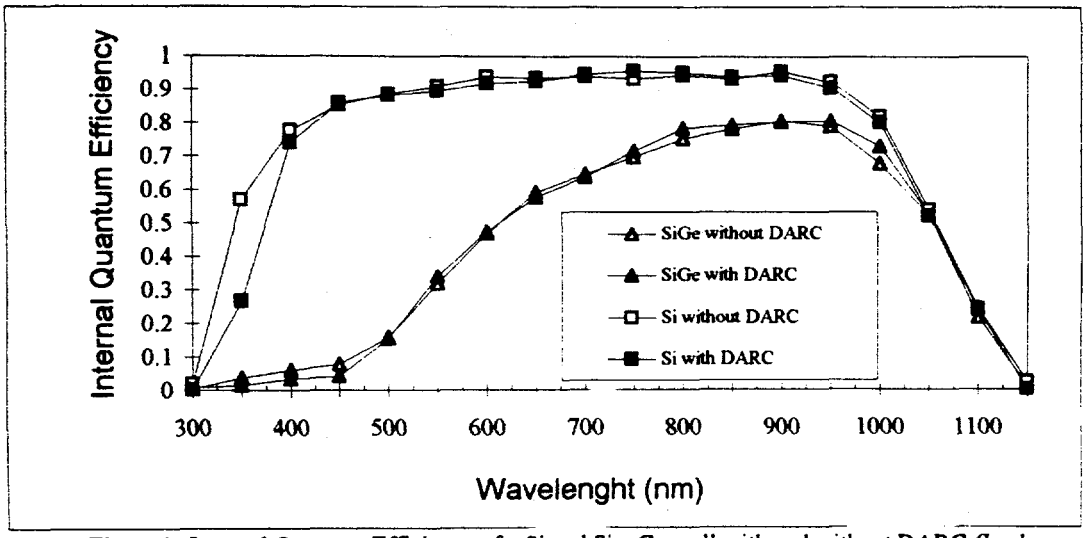

Figure 3. Internal Quantum Efficiency of a Si and $Si_{1-x}Ge_x$ cell with and without DARC.(In absence of DARC absorption I.Q.E with and without DARC should be the same).

Implantation Induced Extended Defects and Transient Enhanced diffusion in Silicon

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Transient enhanced diffusion (TED) of dopant in silicon caused by point defects during annealing of implanted Si has become one of the essential concerns in miniaturization of silicon device technology. In order to control and minimize the TED effect, a fundamental understanding of the evolution of the point defects upon annealing and the interaction between point defects and extended defects and their effect on dopant diffusion is necessary. Our studies were carried out by two parts: 1. For understanding the evolution of <311> and <110> defects, B^+ and Si^+ implantation at energies (from 5 keV to 40 keV) and doses in the range from $5x10^{12}$ to $1x10^{14}/cm^2$ were used. The annealing kinetics were investigated using a N_2 ambient with temperatures for time ranging from 500°C to 1100°C for time ranging from 3 min to 3 hours. A matrix of implant energy vs. dose on formation threshold of <311> and <110> defect, interstitials trapped and dissolved condition were obtained. 2. For Understanding the interaction between Type II dislocation loop and point defect a B doped buried marker layer was used. The oxidation of silicon surface used as a interstitials injection source and a buried type II loop layer as a point defect detector used to quantify the flux of interstitials injected. Combining the flux measured by loops and dopant diffusion the $D_IC_I^*$ was determined. The diffusion limited kinetics was concluded. The TED from <311> and EOR (End of Range) <110> defect was studied using 8keV B^+ implanted Si to a dose of 1e14 and 190keV Ge^+ implanted to a dose of 1e15. Subsequent

anneals are done for 5 min and 30 min, respectively. These defects affect dopant diffusion by trapping and releasing point defects. The differential enhancement in diffusivity and the capture of implantation induced interstitials were quantified by SIMS and plan-view TEM examination. Understanding the interactions between point defect and dislocation loops is important for understanding the influence of dislocation loops on dopant diffusion and for using the loops to quantify point defect perturbations.

IMPROVEMENT OF MINORITY CARRIER DIFFUSION LENGTH IN SILICON BY ALUMINUM GETTERING

S. M. Joshi, U. M. Goesele, and T. Y. Tan

ABSTRACT NOT AVAILABLE
AT THE TIME OF PRINTING

Beneficial Effects of the Aluminum Alloy Process as Practiced in the Photovoltaic Device Fabrication Laboratory

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ABSTRACT - The aluminum alloy process implemented in Sandia's Photovoltaic Device Fabrication Laboratory (PDFL) has major beneficial effects on the performance of commercial multicrystalline-silicon (mc-Si) substrates. Careful analysis of identically processed cells (except for the alloyed layer) in matched mc-Si substrates clearly indicates that the majority of the benefit arises from improved bulk minority carrier diffusion length. Based on spectral response measurements and PC-1D modeling we have observed improvements due to the alloy process of up to 400% in the "average" diffusion length in moderate-area cells and around 50% in large-area cells. The diffusion length is dramatically improved in the interior of the silicon grains in alloyed substrates, resulting in the majority of the recombination occurring at the grain boundaries and localized areas with high defect densities.

1.0 The Challenge

The challenge for all solar cell technologies is to lower the cost per watt. One approach is to improve the conversion efficiency without disproportionately raising the cost. High-efficiency enhancements are only useful if they can be implemented cost-effectively. A informative review of several efficiency enhancement techniques and their costs for mc-Si cell processing is found in [1]. One of the potentially viable techniques identified in that review is the aluminum-alloy back-surface-field process. Several groups have investigated the beneficial effects of this process and some of the best cell results using the process are reported in [2-5]. The aluminum-alloy back-surface-field process can improve cell efficiency both through gettering of fast-diffusing impurities [6] and reflection of carriers from the back contact. The latter mechanism is important only if the minority carrier diffusion length (L) is comparable to, or larger than the cell thickness (W). For most mc-Si cells to date the benefit of the alloy process must come primarily from the gettering effects, since L/W is typically less than unity.

This paper reports on our experience in Sandia's Photovoltaic Device Fabrication Laboratory (PDFL) using the aluminum-alloy process on mc-Si cells. In the past we have reported the results of a statistically designed gettering study on several commercial mc-Si materials which included both phosphorus diffusions and aluminum-alloy treatments [7]. The present work looks more carefully at the effects of the aluminum alloy treatment alone on just one of those materials (cast mc-Si material manufactured by Solarex Corporation). In [7] we were unable to identify an optimal combination of times and temperatures for the phosphorus and aluminum treatments for this material. In addition, we observed no interactions between the two processes for Solarex material. However, the previous study did not include omitting the aluminum-alloy treatment completely (alloying temperatures from 700 to 900°C were used, all of which are above the Al-Si eutectic temperature). In this study we compare the

This work was performed by Sandia National Laboratories for the US Department of Energy under contract DE-AC04-94AL85000.

performance of both moderate- and large-area cells produced with and without the aluminum-alloy treatment in substrates with matched grain structures.

2.0 Materials and Methods

2.1 Cell Processing

The mc-Si cell process used in the PDFL has been discussed in detail elsewhere [5]. The process is summarized in Table 1. This process produces passivated emitter cells with evaporated, photolithographically defined grids, and a double-layer antireflection (DLAR) coating of TiO_2/Al_2O_3.

Results of two experiments will be discussed in this paper, both using 1-Ωcm mc-Si produced by Solarex. In both experiments, substrates with matched grain structures (vertical near neighbors from the same ingot) were used to minimize differences in as-grown material quality. In the first experiment, nine-cell arrays of 4.65-cm^2 cells were produced in collaboration with Solarex to compare two backside processing sequences. Half the cells in this experiment went through the complete PDFL process as outlined in Table 1. The second half of the cells skipped the aluminum deposition steps for the alloy process and the back contact but did go through all of the furnace steps. PDFL processing was stopped after the forming gas anneal, and processing was then completed at Solarex with their conventional non-alloyed aluminum back contact and the deposition of a single-layer antireflection (SLAR) coating of TiO_2. Therefore, the two splits differed in the back surface treatment (alloyed vs. non-alloyed aluminum) and the antireflection coating (Sandia's DLAR vs Solarex's SLAR). The second experiment was similar, except that all processing was done in the PDFL and large-area (42 cm^2) cells were used. In this second experiment, the only processing difference was that half the cells did not get the aluminum deposition for the alloy formation.

2.2 Cell Characterization

One-sun measurements were done to characterize all cells, and matched cells were selected for more thorough testing, including dark current-voltage (I-V), spectral hemispherical reflectance, absolute spectral response, and laser-beam-induced current (LBIC) mapping. A two-diode model was used to fit the one-sun and dark I-V curves. The model incorporates four fitting parameters (series resistance R_s, shunt resistance R_{sh}, n = 1 saturation current I_{01}, and n = 2 saturation current I_{02} where n is the diode ideality factor) to obtain a reasonable fit to the I-V curves, particularly in the region around the maximum power voltage. Mijnarends, *et al* [8] have pointed out that in materials with laterally nonuniform spectral response, the distribution of diffusion lengths (in addition to nonideal recombination) affects the magnitude of I_{02} determined from such a model. The absolute spectral response and reflectance were used to calculate the external and internal quantum efficiency (EQE and IQE respectively). Extended analysis of the IQE was used to determine the minority carrier diffusion length (L), back surface reflectance, and where possible, the back surface recombination velocity (S_b). Parameters determined from the above analyses were used in PC-1D to model the cells. Laser-beam-induced current mapping was done at 1060 nm to generate carriers throughout

the entire thickness of the cells. Comparison of LBIC maps for matched cells gives a qualitative indication of the magnitude and uniformity of the gettering effects.

3.0 Results and Discussion

Table 2 summarizes the results of the first experiment using moderate-area cells. The currents and efficiencies of the cells with the Solarex SLAR have been adjusted upward to account for the higher solar-weighted front-surface reflectance in comparison with the Sandia DLAR. The major differences in performance occur in the short-circuit current and open-circuit voltage.

Matched cells (with respect to grain structure) with both types of back surface treatment, and with closely matched fill factors, were chosen for further characterization and analysis. Two-diode modeling indicated that the series and shunt resistance values for the two cells were very similar and inflicted no performance penalty. Furthermore, the n = 1 and n = 2 saturation current densities (I_{01} and I_{02}) were such that the performance limitation due to n = 2 recombination was essentially the same in both cells (25 to 30% of the total recombination losses at the maximum power point).

Analysis of the absolute spectral response measured in a small area (approximately 5-mm X 5-mm) near the center of each cell indicated that the minority carrier diffusion length (L) increased from about 70 μm in the cell with the aluminum-sprayed back contact, to about 180 μm in the cell receiving the aluminum alloy treatment. LBIC maps for the two cells are shown in the upper panels of Fig.1. Clearly the alloy treatment has improved the carrier lifetime in most of the grain interiors, leaving the grain boundaries and a few small grains as the most prominent recombination features. Histograms of the LBIC response (see the lower panels of Fig. 1) provide a good description of the distribution of diffusion lengths. The LBIC histogram of the unalloyed cell has a nearly symmetric response peak, while the LBIC histogram of the alloyed cell has a sharply asymmetric response peak with the bulk of the response pushed toward higher currents. The shape of these histograms could be used to determine the distribution of diffusion lengths used in the two-diode model of [8].

Measured or calculated values were used wherever possible to model the cells of Fig. 1 using PC-1D. Slightly improved agreement with the measured performance was achieved by assuming L = 50 μm (rather than the 70 μm determined at the center) for the non-alloyed cell and 220 μm (rather than 180 μm) for the alloyed cell. This implies that the "average" diffusion length was improved by about a factor of four by the alloy treatment.

Table 3 shows the one-sun performance for large-area (42-cm^2) cells produced in the second experiment using a different batch of Solarex mc-Si material. Although the difference is not as large as with the smaller cells discussed above, the performance of the alloyed large-area cells is significantly better than that of the sintered cells. The LBIC maps for two cells (Fig. 2) again show that the alloy treatment has cleaned up the majority of the grain interiors, leaving the grain boundaries and scattered small "ungettered" areas as the performance inhibitors. As

expected, the LBIC histograms in the lower panels of Fig. 2 show the same shift of the weight of the response distribution to higher currents in the alloyed cell. Two-diode modeling of the two types of cells again showed no difference in the relative amount of non-ideal recombination between the alloyed and sintered cells.

4.0 Conclusions

It is clear from the present results that the aluminum alloy treatment effectively getters mc-Si substrates. This is in agreement with prior studies in other laboratories. Although the present study does not attempt to eliminate interactions with the emitter diffusion treatment, it appears from our experience that the preponderance of the gettering occurs during the subsequent aluminum alloy anneal. The aluminum alloy treatment used here does not eliminate all high-recombination areas in the Solarex mc-Si. Localized regions with (apparently) high dislocation densities are not significantly improved and become the dominant recombination centers in the alloyed cells.

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Table 1. PDFL High-Efficiency Single-Photomask Process for mc-Si Solar Cells

Moderate-Area	Both	Large-Area
	70°C KOH, or HNO_3/HF damage removal etch	
	HCl clean	
	APCVD-oxide - Back, 400°C (optional)	
	$POCl_3$ One-step emitter diffusion/drive-in (80-100Ω/□, 875°C)	
APCVD-oxide - Front, 400°C		
Laser scribe isolation grooves		
KOH groove etch		
	Deglaze front and back	
	HCl clean	
	Aluminum deposition (back, 1 μm)	
	Aluminum-alloy anneal, ≤ 900°C (also grows passivation oxide on front)	
	Photolithographic definition of front grid	
	Contact oxide etch	
	TiPdAg deposition (front)	
	Al deposition (back, plus TiPdAg if cell will be soldered)	
	Lift-off	
	Forming gas anneal/Metal Sintering (400°C)	
		Ag electroplating
	TiO_2/Al_2O_3 DLAR deposition	
		Separation laser scribe and cleave (back)

Table 2. Wafer-average performance summary for 4.65-cm^2 cells with either an aluminum-alloyed back surface treatment (wafers 1 and 5) or an unalloyed aluminum back surface treatment (wafers 2 and 6).

Wafer	Back Surface Treatment	V_{oc} (volts)	V_{oc} s.d. (volts)	J_{sc} (mA/cm^2)	J_{sc} s.d. (mA/cm^2)	Fill Factor	Fill Factor s.d.	Eff. (%)	Eff. s.d. (%)
1	PDFL Al-Alloy	0.611	0.003	33.5	0.2	0.792	0.004	16.3	0.3
5	PDFL Al-Alloy	0.610	0.003	33.5	0.2	0.790	0.015	16.2	0.4
2	Solarex Al-Spray	0.574	0.002	29.9*	0.4	0.772	0.014	13.2*	0.2
6	Solarex Al-Spray	0.581	0.003	31.4*	0.6	0.767	0.027	13.9*	0.4

* These entries were adjusted upward to account for the difference in solar-weighted reflectance between Sandia's DLAR (6.6%) and Solarex's SLAR (15.6%).

Table 3. One-sun performance for large-area cells without and with the aluminum alloy treatment.

Cell Name	Back Surface Treatment	V_{oc} (volts)	J_{sc} (mA/cm^2)	Fill Factor	Eff. (%)
SOL-4/W 2	sintered	0.593	30.0	0.759	13.5
SOL-4/W 3	sintered	0.594	30.1	0.765	13.7
SOL-4/W 4	sintered	0.595	30.1	0.772	13.8
SOL-4/W 5	sintered	0.594	30.0	0.773	13.8
SOL-4/W 6	sintered	0.594	30.0	0.768	13.7
Avg.	*sintered*	*0.594*	*30.0*	*0.767*	*13.7*
s.d.	*sintered*	*0.001*	*0.04*	*0.005*	*0.10*
SOL-4/W 8	alloyed	0.604	31.8	0.764	14.7
SOL-4/W 9	alloyed	0.605	31.6	0.771	14.8
SOL-4/W 11	alloyed	0.605	31.7	0.771	14.8
SOL-4/W 12	alloyed	0.604	31.7	0.771	14.8
SOL-4/W 13	alloyed	0.605	31.6	0.770	14.8
Avg.	*alloyed*	*0.605*	*31.7*	*0.770*	*14.8*
s.d.	*alloyed*	*0.0004*	*0.06*	*0.003*	*0.04*

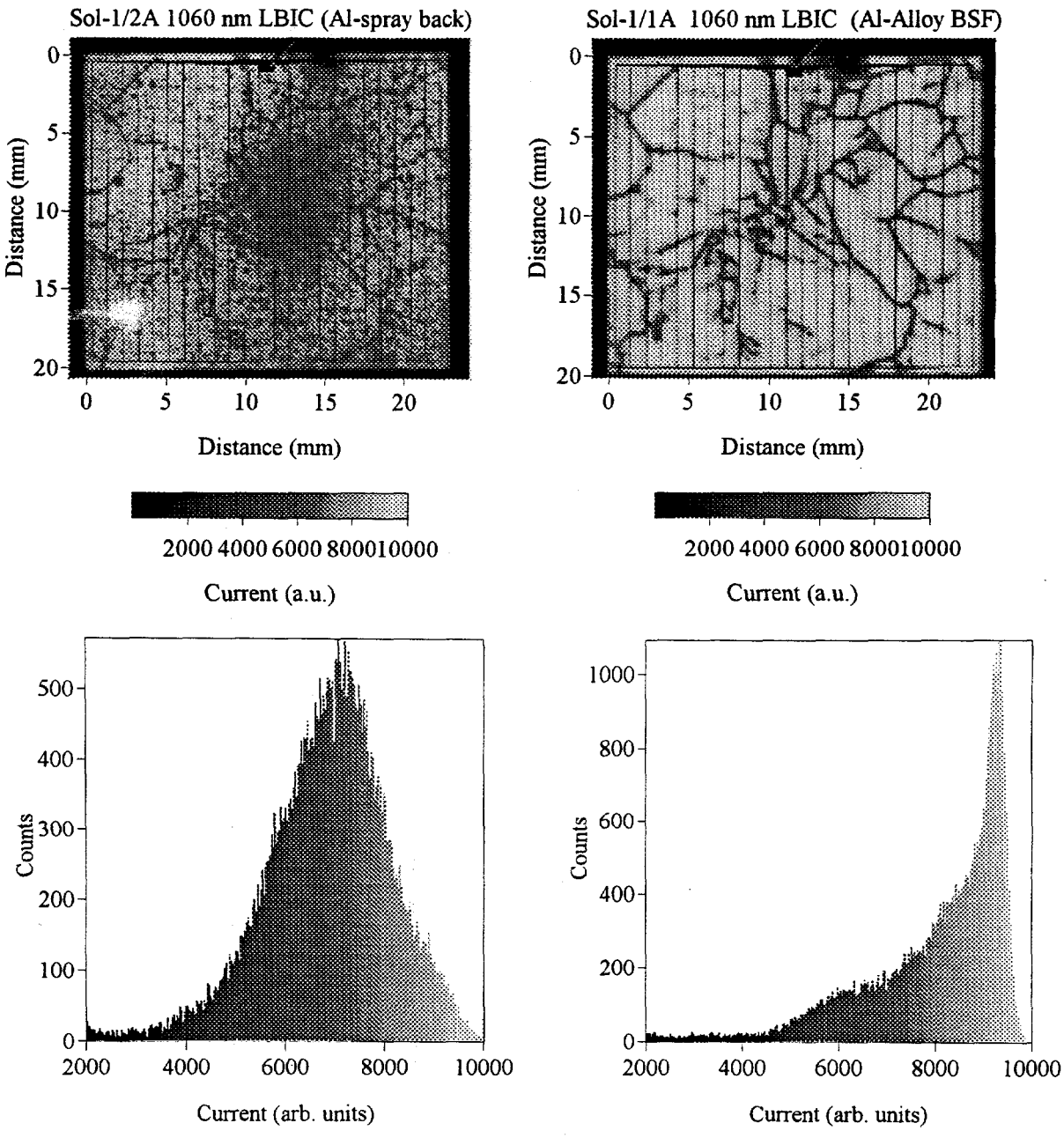

Fig. 1. The upper panels show laser-beam-induced current (LBIC) maps taken at 1060 nm of moderate-area mc-Si solar cells with matched grain structures. The map on the left is of a cell with a non-alloyed aluminum back contact. The map on the right is of a cell with an aluminum-alloyed back contact. The alloy process has clearly eliminated much of the recombination occurring in the grain interiors. The histograms in the lower panels illustrate how the alloy process has affected the distribution of localized diffusion lengths (note the difference in vertical scales).

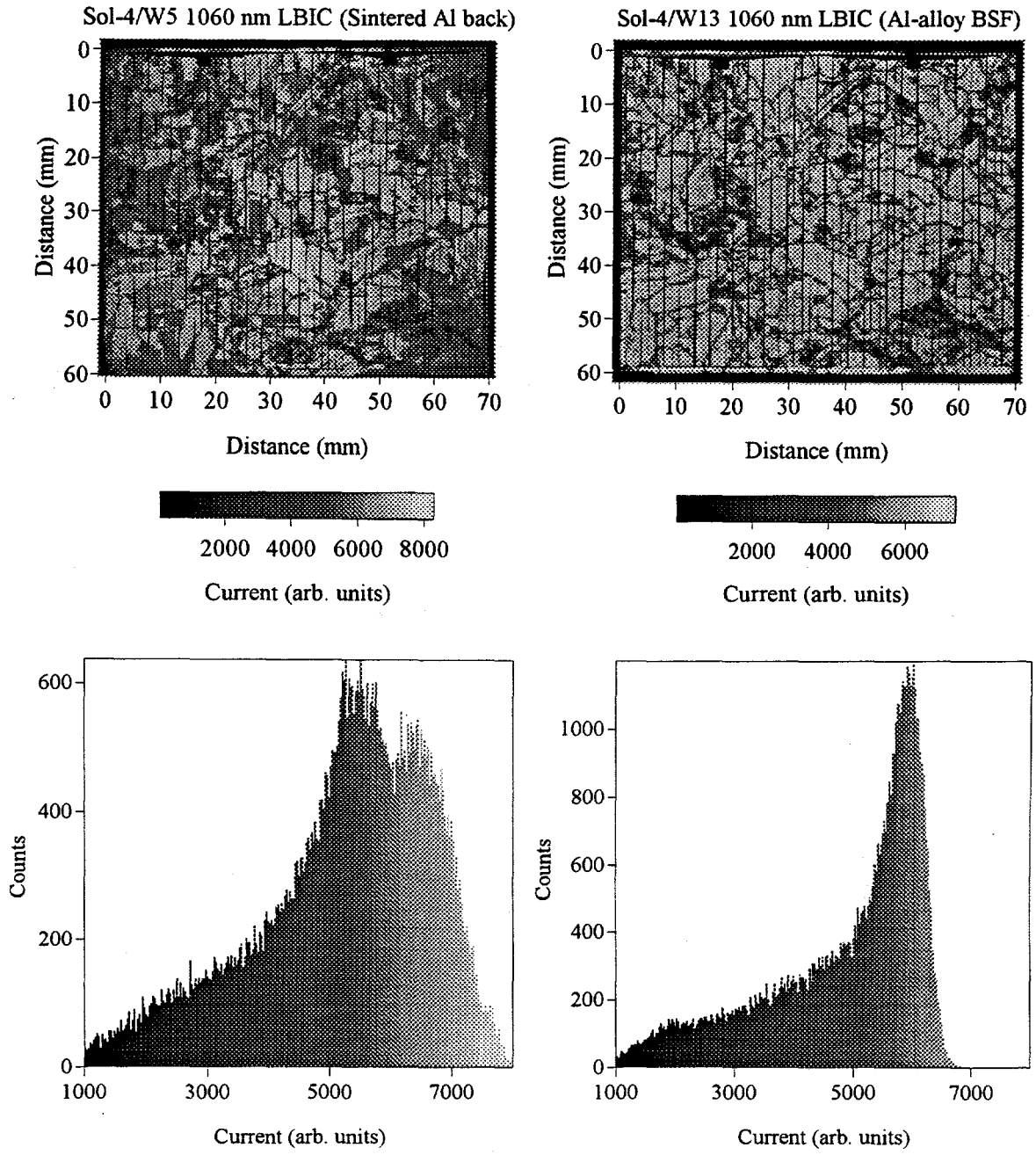

Fig. 2. LBIC maps of large-area cells again illustrating how the alloy process has reduced carrier recombination in most of the grain interiors. Remaining regions of high recombination are still apparent even in the alloyed cell (right-hand panel). The histograms in the lower panels qualitatively illustrate the shift of the distribution of localized diffusion lengths to longer values. Note the different vertical scales for the histograms, and that the current scales are not directly related.

DEFECT ENGINEERING BY ULTRASOUND TREATMENT IN POLYCRYSTALLINE SILICON

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By applying ultrasound treatment (UST) to bulk and thin film polycrystalline Si (poly-Si) we have found a dramatic improvement of recombination and transport properties. The increasing of minority carrier lifetime by as much as one order of magnitude was found in short diffusion length regions, while exhibiting a strong dispersion for entire solar-grade poly-Si wafer. Relevant mechanisms are attributed to ultrasound processing on crystallographic defects, as well as UST stimulated dissociation of Fe-B pairs followed by Fe_i gettering. A spectacular improvement of hydrogenation efficiency in poly-Si thin-films on glass substrate is demonstrated by resistivity study and confirmed using spatially resolved photoluminescence and nanoscale contact potential difference mapping. By applying UST to commercial solar cells we found the increasing of cell efficiency at low light excitation.

Introduction. Ultrasound waves propagated through the bulk of a semiconductor can affect properties of point and extended defects [1]. A corresponding ultrasound treatment (UST) applied to single crystals and polycrystalline semiconductors was exhibited as: (a) ultrasound stimulated dissociation of complex centers [2], (b) ultrasound enhanced diffusion of point defects [3], and (c) ultrasound stimulated point defect capture by dislocations, grain boundaries and/or precipitates [4,5]. Consecutive processes (a), (b) and (c) can be considered as a schematic of ultrasound stimulated point defect gettering. It has been recognized that extended lattice defects such as dislocations, grain boundaries and precipitates efficiently transfer the energy of ultrasound vibrations to point defects. In these regards, UST can be a particularly important processing in solar-grade poly-Si. Only recently, the UST effect on increasing of minority carrier lifetime has been observed in Cz-Si [6] and poly-Si [7]. In particular, it was experimentally proved that the mechanism of Fe-B pair stimulated dissociation can be triggered by UST [8]. A successful attempt to improve poly-Si solar cell efficiency has been reported [9]. However so far, a lack of deep understanding of the complex phenomena involved in UST processing prevented it from becoming a useful tool of defect engineering. We report here the UST effect on increasing of minority carrier lifetime in bulk poly-Si wafers and improvement of hydrogenation efficiency in poly-Si thin-films. The mechanisms of UST stimulated gettering and UST enhanced hydrogenation can be responsible for observed improvement of solar cell parameters. We argue that UST processing can be implemented to solar-grade materials and devices.

Experiment. Polycrystalline cast p-type Si wafers (B-doped, 2-10Ω·cm) were studied. Samples of 0.5mm thickness were cut to 50x50mm^2 squares from a poly-Si wafer to match the size of the piezoelectric transducer used as a source of ultrasound vibrations. The effect of UST enhanced hydrogenation have been studied on 0.5μm thickness LPCVD poly-Si thin films deposited on glass substrate at 625°C. Hydrogenation was performed at 300°C in a plasma system operating at 100cm^3 H_2 flow with 0.3Torr pressure and 200W RF power. Ultrasound transducers had diameters from 25 to 74mm and thicknesses of 1.5 or 3mm (PZT-5H ceramics covered by plain Cr/Au electrodes). First harmonics of a radial vibration mode at the frequencies ranged from 25 to 80 kHz or thickness vibration modes at 590 and 1200kHz were selected using an appropriate resonance frequency of a transducer. Transducers were driven by an AC voltage supplied

from a function generator (HP 3312a) coupled with a wide-band power amplifier (ENI 240L). Under UST poly-Si samples were gently pressed to a transducer using a spring contact. By using this mounting, we realized a non-contact UST approach with respect to the front sample surface as depicted in Fig.1. Each UST is specified by the set of following parameters: 1) the amplitude of acoustic strain measured in a sample by miniature acoustic wave detector, $\varepsilon_{us}=10^{-6}$-10^{-5}, which is proportional to the amplitude of AC voltage applied to transducer, V_{us}=4 - 40V; 2) UST holding time, t_{us}= 10 - 60 min; 3) temperature of the sample, T_{us}=20 - 100°C, which was measured in-situ with an infrared pyrometer OS610; and 4) frequency or mode of ultrasound vibrations (radial or thickness); 5) rate of post-UST recovery at particular temperature.

A) Change of diffusion length in solar-grade poly-Si. Two line scans of diffusion length before (L_{ref}) and after the sample was subjected to UST (L_{ust}) are shown in Figure 2. The increase of L is observed in this sample after UST with the parameters specified in the Figure. The strongest UST effect (2.7 times increase of L which corresponds to more than 7 times lifetime increasing) is found in a region with the shortest diffusion length values of L =10 to 15μm. The increase of L reaches 12-60% for regions with larger L.

By mapping the entire wafer, we found that the effect of UST can be significantly different for various regions of a sample. This result is consistent with the strong inhomogeneity of recombination parameters in solar-grade poly-Si[10]. In Figure 3, the line scans of diffusion length for the same part of a sample are shown: (a) as L distribution prior to UST; (b) the UST change of diffusion length in terms of the quantity $\Delta L/L = (L_{ust} - L_{ref})/L_{ref}$; and (c) as a post-UST relaxation of $\Delta L/L$. Three consecutive treatments were applied to this sample with following parameters: UST1:{V_{us}=40V, t_{us}=30min, T_{us}=40°C, f=48kHz}; UST2:{55V, 30min, 50°C, 48kHz}; UST3:{32V, 80min, 50°C, 48kHz}. The sign of ΔL is different in various regions of a sample. Positive variations of L are observed for the regions with the shortest diffusion length while negative values of ΔL are found in regions with relatively large L > 25μm.

The following can be considered as distinctive features of UST effect. a) The increasing of short diffusion length is a function of UST parameters and critically depends upon UST temperature (Figure 4). The increase of T_{us} above 35°C results in larger UST effect, which exhibits the maximum at 55 to 65°C. The decreasing of UST effect is observed at higher temperature. This result indicate that at least two processes with different temeprature dependence are superimposed. b) The change of L versus UST time, t_{us}, expressed in terms of $\Delta(L^{-2}) = L_{ref}^{-2} - L_{ust}^{-2}$, which is proportional to the change of the concentration of recombination centers, can be approximated by first order kinetic:

$$\Delta(L^{-2}) = \Delta(L_{max}^{-2})(1-\exp(-t_{us}/\tau)) \qquad (1)$$

The characteristic time of the UST process, τ, is about 20min at 40°C. We estimated the UST activation energy as ε_{ust} =0.17 $^{+}$0.05eV using the Arrhenius plot of ln(τ) versus T_{us}^{-1}. c). By mapping an entire poly-Si wafer (177-point map) prior to and immediately after UST we confirmed the strongest increasing of diffusion length in a short diffusion length region with L=7 to 15μm, while $\Delta L/L$ is ranged for a whole wafer from -25% to 58%. This values are typical for different poly-Si samples.

We carefully analyzed a stability of UST effect. Two different post-UST behaviors of $\Delta L/L$ are observed (Fig.3c). The first is a stable positive change of L which

did not show a noticeable relaxation for a few days at room temperature or after the annealing of a treated sample for 1h at 80°C. This behavior characterizes wafer regions with the shortest L as shown in Figure 3c. The second is a complete recovery of ΔL or its partial relaxation to a new stable value after 5 to 10h sample storage at room temperature. In a general case, the UST exhibits both a stable and unstable behavior. Therefore, the net UST effect has to be measured after treatment followed by post-UST relaxation. The kinetics of UST relaxation shows a characteristic time of 14min at 75°C as shown in Figure 5. We compared this relaxation curve with the kinetics of Fe and B pairing (see the following discussion) which was performed after Fe-B optical dissociation and mesured at the same sample point. The characteristic Fe-B pairing time was determined as 2 min at 75°C which is consistent with published data in Cz-Si, while UST recovery shows a noticeable longer decay. These experiments provide a background for the following UST model.

The identification of different recombination processes in solar-grade poly-Si which contribute to the L value is not adequate at present to provide the quantitative separation of contributions from precipitates, dislocations, grain boundaries and point defects. In this study, we were able to separate in the UST effect only the role of Fe impurity which is a typical contamination in Si. Dissolved interstitial Fe in B-doped p-type Si tends to form Fe-B pairs stable at room temperature. These pairs can be dissociated either thermally at about 200° or by using the enhanced dissociation processes, such as minority carrier injection[11] or light illumination [12]. Recently, it was demonstrated the UST stimulated dissociation of Fe-B pairs in Cz-Si [?]. We can assume this UST mechanism dominates in poly-Si regions which show post-UST relaxation. By using the optical dissociation technique [12], we determined the concentration of Fe-B pairs in our 8samples to be in the range of 10^{12} to $10^{13}cm^{-3}$. If one assumes that part of UST effect is the result of Fe-B pair dissociation, it can be estimated that for L_{ref}=20μm and $\Delta L/L$=-25% the required change in Fe-B pair concentration would be about $5 \cdot 10^{12}cm^{-3}$ which is within the limits of available Fe-B pair concentration in our samples. We noticed that post-UST relaxation rate is much slower in poly-Si as compared to Fe-B pairing kinetics (Figure 5). This can be interpreted as a capture of released Fe_i by sinks, if such a trapping is a rate limiting process for Fe and B pairing after UST. Summarizing the UST effect with regards to Fe-B pairs, we assert that the ultrasound enhanced dissociation of Fe-B pairs and their capture by sinks is a possible process contributing to the post-UST relaxation of diffusion length in poly-Si.

In sample regions with relatively short diffusion lengths, L=10 to 15μm, showing a positive change of L (Fig.2), which is stable versus post-UST time, the concentration of Fe-B pairs is too low to account for an observed UST effect. Therefore, we may assume that the recombination characteristics of crystallographic defects such as dislocations, grain boundaries and precipitates contribute to short diffusion length regions and can also be affected by UST. It is known that dislocation network in poly-Si solar grade material can be an effective place for Fe precipitation [13]. This process of extended defect decoration by impurities exhibits a strong reduction of diffusion length [10]. We can postulate, based on our study, that such crystallographic defects decorated by impurities can also be a subject of UST. This was observed in Cz-Si containing "ring defect" [14]. In particular, dislocations can effectively absorb ultrasound vibrations [15]. A dislocation line vibrating in the ultrasonic field generates an alternate strain field which provides a driving force to dissolve the impurity atmosphere decorating dislocations. This would lead to an increase of diffusion length in the relevant sample regions. Further experiments are necessary to establish a validity of a suggested process.

B. UST enhanced hydrogenation in poly-Si thin films. The hydrogen passivation of grain boundary defects (e.g. dangling bonds), dislocations as well as point defects is recognized as an important processing of improving poly-Si solar cell efficiency [16]. We report here a new approach to enhance hydrogenation efficiency in poly-Si by using UST. For this study we used as-deposited and plasma hydrogenated poly-Si thin films on glass substrates. In this material the techniques of hydrogen introduction and diagnostics are well developed.

Atomic hydrogen can passivate grain-boundary defects and eventually reduces inter-grain barriers in poly-Si. This can be studied by four-point probe resistance measurements. The results of UST on sheet resistance of hydrogenated and non-hydrogenated samples are shown in Figure 6. The hydrogenated sample demonstrates a dramatic one to two orders of magnitude decrease in resistance after UST. In comparison, the same UST applied to non-hydrogenated sample produced only 30 to 40% reduction of resistance. The UST effect is specified by a time constant of 25 min at 55°C.

We have observed that UST also improves homogeneity of a hydrogenated poly-Si film. In Figure 7 the resistivity change in two different regions of the same plasma hydrogenated sample are compared. Beside the decreasing in absolute value of a film resistivity, the UST reduces differences between film regions. In the case presented in Figure 7, the resistivity ratio in two regions was reduced from more than one order of magnitude prior to UST to about 10% after treatment. This effect of poly-Si homogenization due to UST is consistent with measurements of spatially resolved photoluminescence (PL) mapping. This is presented in Figure 8 as two PL intensity histograms of oxygen-related luminescence (maximum at 0.8eV) on exactly the same film region prior to and after the UST. The effects of histogram narrowing and PL intensity increasing are accounted for by the process of UST enhanced hydrogenation of non-radiative recombination centers at grain boundaries. This is demonstrated in Figure 9 by nanoscale atomic force microscopy mapping of contact potential difference contrast across the grain boundaries (dark regions in a map). The origin of CPD contrast is the extra charge trapping at grain boundary defects. This contrast can be gradually decreased with hydrogenation time [17], and therefore, is a measure of hydrogenation efficiency. It is straightforward, that after UST the same poly-Si film shows a decreasing of CPD contrast, i.e. hydrogenation improvement.

Presented results imply that poly-Si film hydrogenation can be substantially enhanced by UST. We propose the following mechanism to tentatively account for the UST effect on hydrogenation in poly-Si. It is known that after hydrogenation of poly-Si total [H] exceeds concentration of dangling bonds by as much as two orders of magnitude [18]. Furthermore, it is also known that the fraction of passivated dangling bonds is often very low. Therefore, a significant reservoir of hydrogen is available in the hydrogenated film for the passivation of dangling bonds. It had been observed that this hydrogen in the reservoir is weakly bound, and can be thermally liberated with the activation energy of about 1eV [19]. This atomic hydrogen after fast diffusion to grain boundary regions can be captured by dangling bonds and form stable at room temperature centers. We can postulate that UST enhances the hydrogen liberation from reservoir and can also accelerate its diffusion to grain-boundaries.

C. UST of poly-Si solar cells. Both UST processes of increasing of minority carrier lifetime and enhanced hydrogenation could be very beneficial to improve solar cell parameters. We applied the same UST processing to commercial solar cells (Solarex and Mobil). In Figure 10 the relative change of cell efficiency and fill factor after UST versus light intensity are shown. We observed UST improvement of these two critical solar cell parameters in the region of light intensities from 0.01 to 0.1sun. This increase, however, is reduced with light intensity and begins to be a negligible at 1sun. The maximum improvement of efficiency, $\Delta\eta/\eta$, was ranged from 10 to 20% in different samples. This

first UST processing applied to solar cells demonstrated the ability of ultrasound to improve devise parameters, however, a relevant mechanism is not identified yet. More efforts are required to make the UST approach commercially useful.

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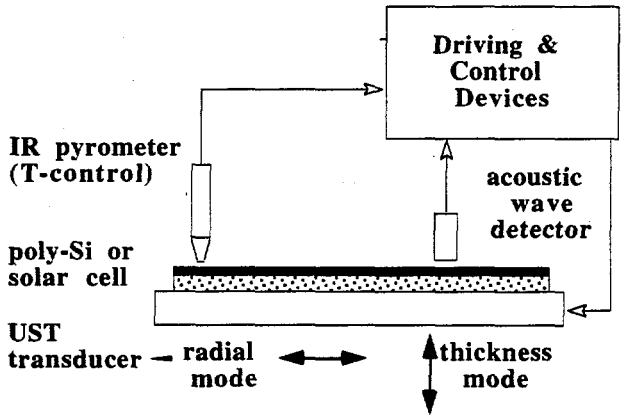


Fig.1 Principal scheme for UST in poly-Si and solar cells

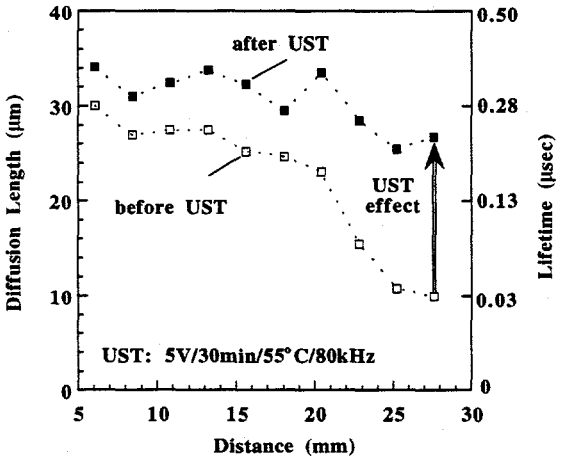


Fig.2 UST change of diffusion length in cast poly-Si

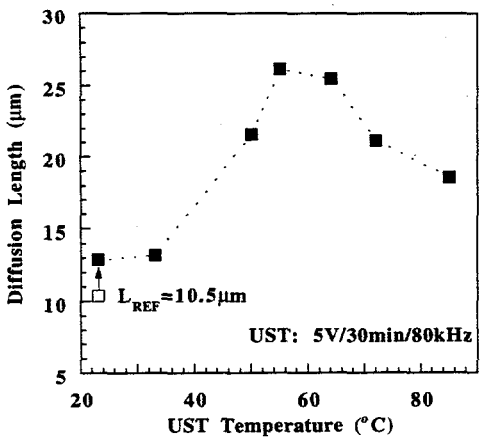
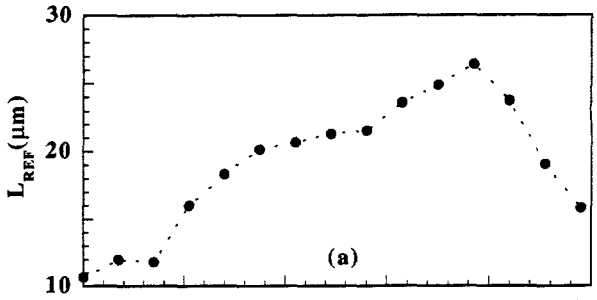
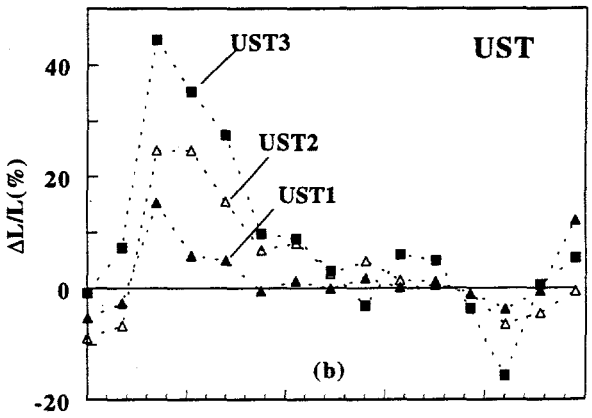


Fig.4 Temperature dependence of UST effect





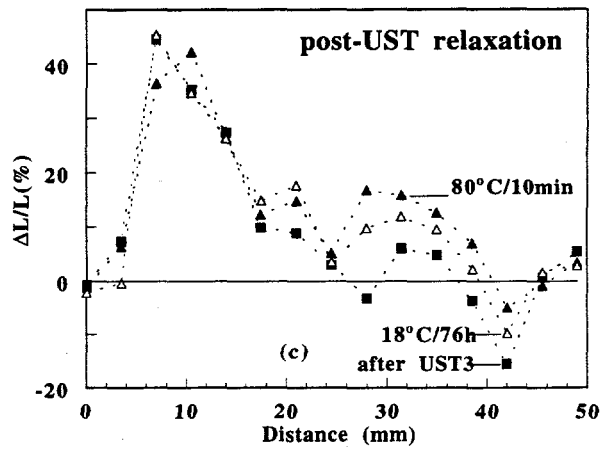


Fig.3 SPV line-scans of diffusion length in cast poly-Si: (a)-initial L, (b)- relative change of L after three different UST, (c)- post-UST relaxtaion

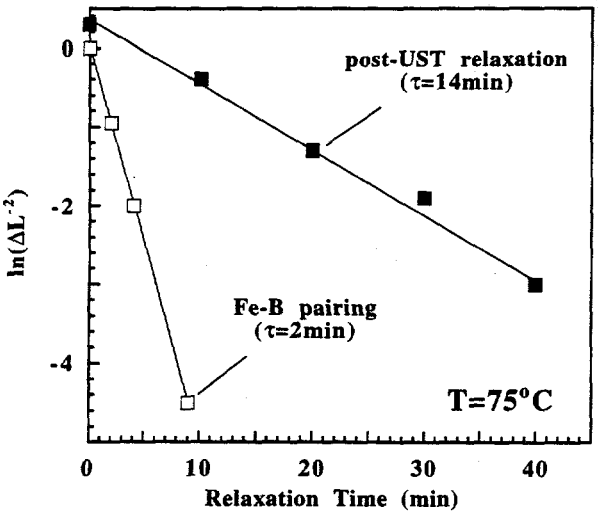


Fig.5 Comparison of post-UST relaxation rate with Fe and B pairing rate measured at the same temperature and sample point

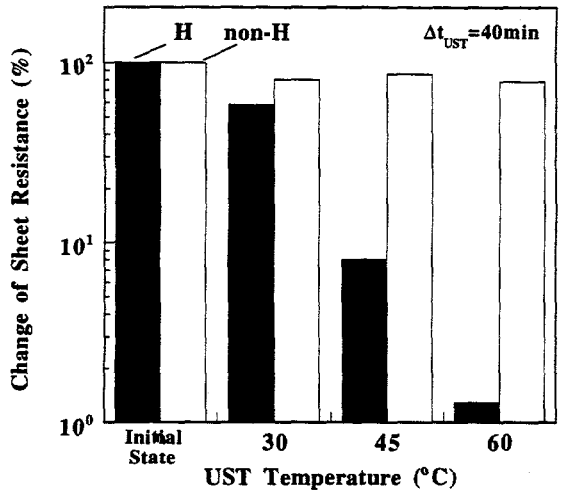


Fig.6 Change of sheet resistance in hydrogenated poly-Si thin films subjected to consecutive UST

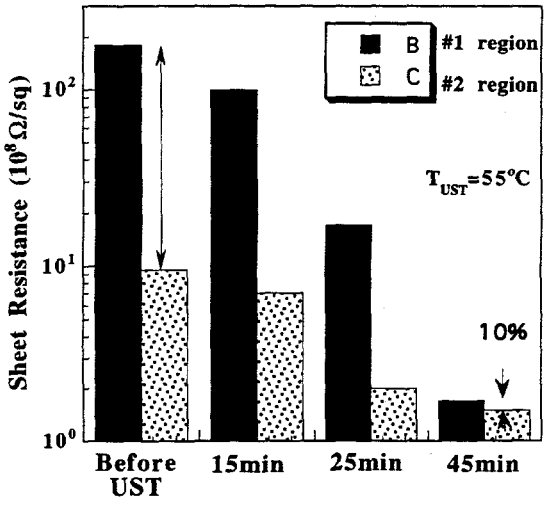


Fig.7 UST improvement of resistance homogeneity in plasma-hydrogenated poly-Si film

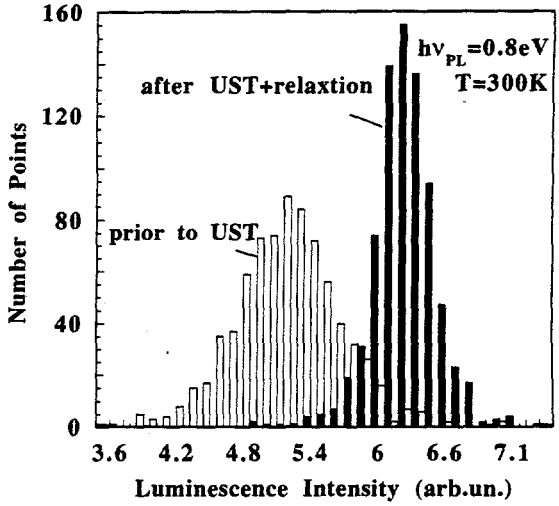
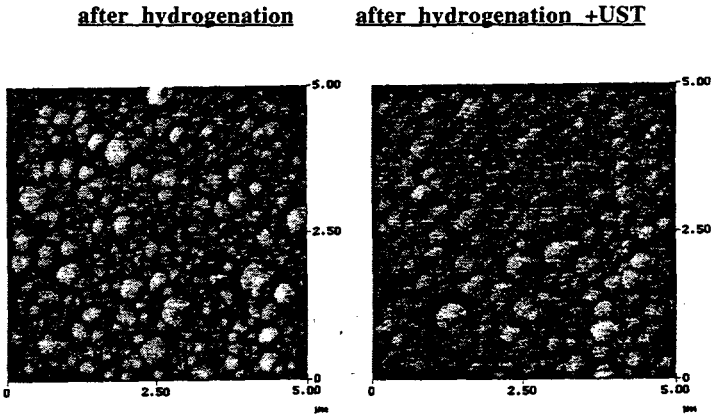


Fig.8 Two histogarms of room-temperature PL mapping (192 points) in poly-Si thin film before and after UST. Mapping size: 6x8mm, step:0.25mm

Fig.9 Very High Resolution Contact Potential Maps of Hydrogenated Poly-Si Thin Film Before and After UST (mapping size:5x5μm)



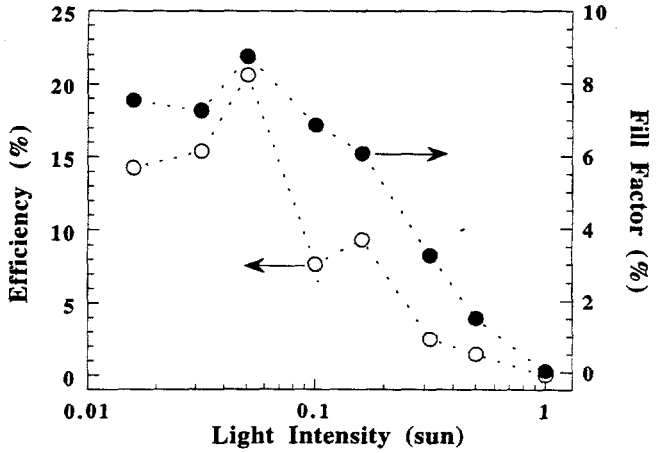


Fig.10 Relative change of solar cell efficiency and fill factor (Mobil) due to UST versus light intensity (100W halogen lamp)

A REVIEW OF RECENT PROGRESS IN LOW-TEMPERATURE SILICON SURFACE PASSIVATION

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ABSTRACT NOT AVAILABLE
AT THE TIME OF PRINTING

LOW-TEMPERATURE OPTICAL PROCESSING OF SEMICONDUCTOR DEVICES USING PHOTON EFFECTS

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Lubek Jatrzebski¶, and Kamal Mishra#

In an RTA process the primary purpose of the optical energy incident on the semiconductor sample is to increase its temperature rapidly. The activation of reactions involved in processes such as the formation of junctions, metal contacts, deposition of oxides or nitrides, takes place purely by the temperature effects.

We describe the observation of a number of new photonic effects that take place within the bulk and at the interfaces of a semiconductor when a semiconductor device is illuminated with a spectrally broad-band light. Such effects include changes in the diffusion properties of impurities in the semiconductor, increased diffusivity of impurities across interfaces, and generation of electric fields that can alter physical and chemical properties of the interface. These phenomena lead to certain unique effects in an RTA process that do not occur during conventional furnace annealing under the same temperature conditions. Of particular interest are observations of low-temperature alloying of Si-Al interfaces, enhanced activation of phosphorus in Si during drive-in, low-temperature oxidation of Si, and gettering of impurities at low-temperatures under optical illumination. These optically induced effects, in general, diminish with an increase in the temperature, thus allowing thermally activated reaction rates to dominate at higher temperatures.

We discuss some of these new phenomena and their applications in low-resistivity contact formation, growth of high quality thin oxides in Si, and impurity gettering in semiconductor device fabrication. Because of the photonic enhancement of the reaction rates, these processes can be applied to fabricate devices at considerably lower temperatures (typically < 500°C) and shorter times as compared to the thermal effect alone. Processes utilizing these effects also offer the advantage of high throughput, "cold-wall" nature, high process uniformity, and a high degree of process control.

Optical Processing can be used to either induce reactions at the interfaces of a multilayer device or in the bulk of a semiconductor. The selection can be made by suitable choice of process parameters such as the spectrum of light, intensity, and the process time. The interface effects include:

- Formation of low resistivity ohmic contacts/simultaneous formation of front and back contacts on a solar cell
- Formation of low resistivity, optically reflecting ohmic contacts
- Interface texturing for light trapping in solar cells
- Formation of a graded alloy interface
- Growth of low-temperature, high quality thin oxide

The bulk effects include:

- Enhanced impurity diffusion
- Low-temperature hydrogen passivation

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