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ERRORS AND ERROR COMPENSATION
IN

HYBRID COMPUTERS

R. A. Burnett

May 1970

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ERRORS AND ERROR COMPENSATION
IN
HYBRID COMPUTERS

By

R. A. Burnett

Control and Instrumentation Department
Systems and Electronics Division

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ABSTRACT

The major types of computing errors generated by the analog-to-digital and digital-to-analog converters and the digital computer in a hybrid system are identified and discussed. Included are quantization, roundoff, and time-delay errors. Compensation methods for reducing these errors are proposed and discussed. Sample problems were run in which digital computer and hybrid interface parameters such as speed and word length were effectively varied by software methods to simulate different levels of equipment capability. The resulting effects upon solution errors are documented. The effects of various compensation techniques are also documented. Conclusions indicate that many simulation problems can be solved quite satisfactorily with relatively inexpensive, and unsophisticated hybrid computing equipment.

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INTRODUCTION

The success of a computer simulation depends upon the validity and accuracy of the mathematical model, the efficiency of the programmer, and the ability of the computer to quickly and accurately solve the model equations. Since a perfectly accurate computer has not yet been invented, it is important to identify the sources of error which do exist in computing systems. Optimum programming techniques can then be used to minimize these errors. It is also important to evaluate the relative magnitudes of these errors in terms of computer performance characteristics. Such knowledge will aid the purchaser in his selection of the equipment which will most economically meet his specific requirements.

This report concerns itself with hybrid computers and concentrates on the errors generated in the ADC-Digital-DAC portion of the hybrid loop. The objectives of this report can be stated as follows:

- To identify and measure the most significant sources of computational error affecting typical hybrid simulation studies, and develop methods of correcting or minimizing these errors; and
- To provide guidelines from a problem solution accuracy standpoint for the specification of equipment for future hybrid systems.

SUMMARY AND CONCLUSIONS

The major error sources within the ADC-Digital-DAC portion of the hybrid loop are enumerated and discussed, along with various methods of compensating for these errors. Several hybrid problems of varying

nature and complexity were set up and run on the Battelle-Northwest PDP-7 - EASE 2133 Hybrid computer, "Hybrid 1." Digital computer and converter performance parameters such as effective speed and word length were individually varied in order to obtain quantitative information on the effects of each error source on solution errors. Compensation methods were then similarly evaluated. An all-analog solution or a full-capability hybrid solution was provided as a reference solution for each problem.

Although the test problems provided only a small sampling of the world of hybrid simulation, some tentative conclusions can be drawn from the results. These conclusions, some of which are discussed in the following paragraphs, indicate that further study on a much larger range of problems is indicated. The result of such a study could be a tremendous savings in capital equipment cost for computer users.

It appears that there is a large class of simulation studies which can be performed with sufficient accuracy on hybrid systems consisting of an analog computer, a 16-bit (or less) fixed-point digital computer, and 12-bit (or less) converters. (Other factors, such as problem size and equipment capacity, are not discussed here.) The "or less" receives even more emphasis when the accuracy improvement potential of roundoff compensation is considered. The compensated solution to one of the test problems, computed with an effective computer word length of 16-bits and effective A-D and D-A word lengths of 12 bits, showed no deterioration in accuracy compared to an 18 bit/14 bit solution. Acceptable solutions were also obtained at 14 bits/12 bits, and at 18 bits/10 bits.

The use of roundoff compensation and time-delay compensation resulted in significant improvements in all cases. In one case, time-delay compensation resulted in an accuracy improvement factor of greater than 20. The use of time-delay compensation can thus offset a "slow" digital computer by making longer frame-times more tolerable in hybrid simulation.

ERROR IDENTIFICATION AND COMPENSATION TECHNIQUES

Karplus⁽¹⁾ identifies the potential sources of error in hybrid systems and provides a detailed discussion of the major sources together with some schemes to compensate for these errors. In the ADC-Digital-DAC operation, the major errors are:

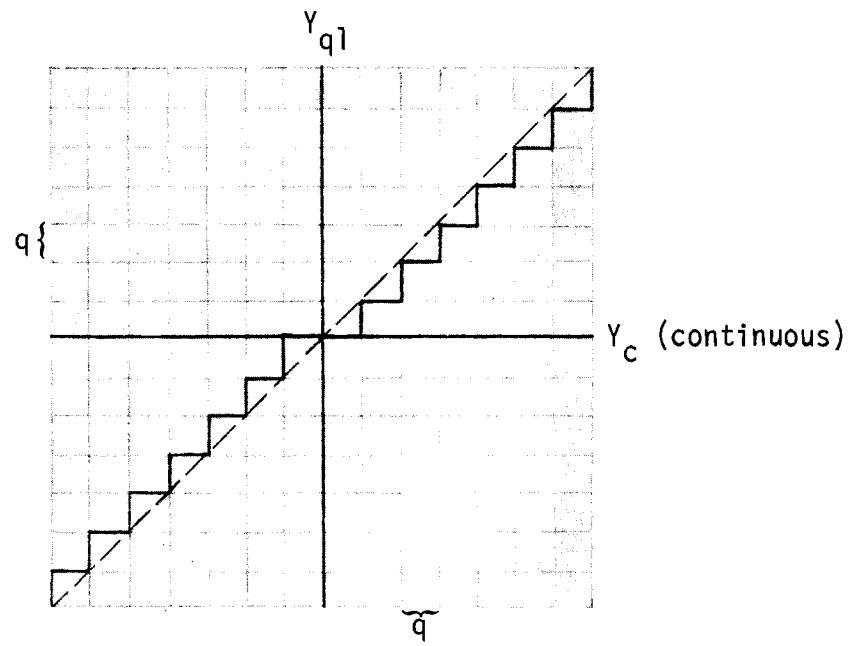
- Quantization errors in the A-D and D-A converters;
- Roundoff errors within the digital computer;
- Time-delay and slewing errors;
- Data reconstruction errors; and
- Inherent sampling errors.

Quantization Errors

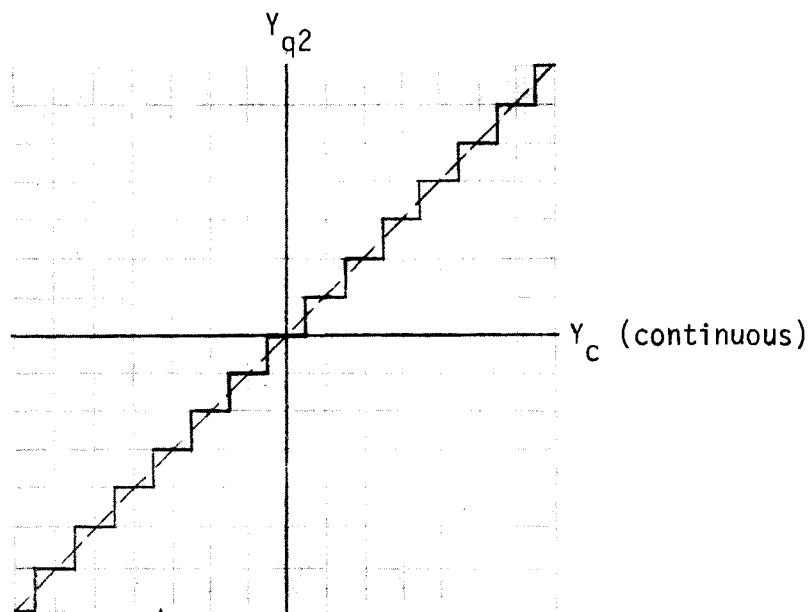
Analog-to-digital and digital-to-analog quantization errors occur because the converters must represent a continuously variable voltage with one of a finite set of binary numbers or equivalent binary "voltage" levels.* The quantization process is depicted in Figure 1. The dashed lines represent the ideal one-to-one conversion characteristic, while the solid lines are the actual quantized transfer characteristics. The maximum possible error per conversion is decreased as the quantization grid size q is decreased (i.e., as the number of converter bits is increased). A table of the values of q for a 100-volt analog computer and for converter word lengths of 8 to 14 bits is given below:

| <u>Number of Converter Bits (sign bit included)</u> | <u>Quantization Grid Size q (equivalent voltage resolution)</u> |
|---|--|
| 14 | 0.0122 volts |
| 13 | 0.0244 " |
| 12 | 0.0488 " |
| 11 | 0.0977 " |
| 10 | 0.1953 " |
| 9 | 0.3906 " |
| 8 | 0.7812 " |

(*) 2^n possible levels, where n = number of converter bits



(a) Quantized



(b) Quantized and rounded off

FIGURE 1. Transfer characteristics of A-D and D-A converters

For any given converter word length, optimum accuracy can be obtained by insuring that the transfer characteristic of the converter is that of Y_{q2} in Figure 1(b) and not Y_{q1} or some other characteristic. In Figure 1(a), the maximum error in Y_{q1} is equal to q . Since Y_{q2} is rounded off to the digital level nearest to the continuous input Y_c , the maximum error in Y_{q2} is $q/2$. An A-D converter with a Y_{q1} transfer characteristic can be compensated to produce a Y_{q2} output by the addition of $\pm q/2^*$ to the analog signal Y_c before converting. For the D-A converters, the problem lies in arriving at the optimum binary number to be loaded into the converter. This can be achieved by the use of digital roundoff compensation, which is discussed in the next subsection.

The precision of the analog computer components must be considered when determining the optimum size of converters to be purchased for a particular hybrid facility. The increased accuracy with each additional converter bit becomes a diminishing return as the resolution of the converter approaches and passes that of the analog components themselves. Thus, for analog components with a noise level of 50 millivolts peak-to-peak, the uncertainty in each reading is ± 25 mv; a 14-bit converter with an uncertainty of $\pm \frac{1}{2}q = \pm 6.1$ mv would in this case be expected to provide only a very slight increase, if any, in problem solution accuracy over that of a 12-bit converter with a ± 24.4 mv uncertainty.

Roundoff Errors

The digital computer must perform a prescribed set of operations on the quantized variables provided by the ADC's in order to arrive at the proper variables to be sent back to the analog computer through the DAC's. If fixed-point single-precision arithmetic is used, the final result and all intermediate results of these calculations are restricted to 2^m discrete levels, where m is the number of bits in a computer word. Roundoff errors thus accumulate in these calculations. These errors can be minimized in much the same fashion as the A-D quantization error. For example:

$$(*) + q/2 \text{ for } Y_c > 0, - q/2 \text{ for } Y_c < 0$$

The PDP-7 "multiply" instruction generates a 36-bit product in the combined accumulator (AC) and multiplier-quotient (MQ) registers. The binary point is assumed to lie between the AC and MQ, with the resultant scale factor taken into consideration. Unless a divide instruction follows immediately, the contents of the MQ are normally disregarded. The result is a quantization effect similar to that of Y_{q1} . Improved accuracy can be obtained by rounding off the AC to the next higher binary integer if the binary fraction in the MQ is $\geq 2^{-1}$. The result of this roundoff compensation is a Y_{q2} -type quantization characteristic.

The PDP-7 divide instruction produces an 18-bit quotient in the MQ and an 18-bit remainder in the AC. In this case roundoff compensation is achieved by adding* a binary 1 to the MQ if the remainder is greater than half the divisor.

Right-shift instructions are often used to rescale a variable by a factor of 2^{-n} , where n is the shift count. The bits to be shifted out of the accumulator can be considered as a binary fraction-to-be; if the absolute value of this fraction is $\geq 2^{-1}$, then a binary 1 should be added* to the AC after shifting.

The D-A converters, if calibrated properly, will automatically convert a given binary "voltage" into the correct equivalent analog voltage. The binary voltage to be converted, however, is the result of a series of digital computer operations; of particular interest is the operation immediately preceding the D-A conversion. The digital computer word length is normally greater than that of the converters. The range of voltages allowable within the digital computer is $2^{(m-n)}$ times the analog reference voltage (here assumed to be 100 volts), where m is the number of bits in a computer word, and n is the number of converter bits.** Thus, the digital calculation of a parameter required by the analog computer will often result in a scaled voltage greater than 100. This parameter obviously must be scaled down to less than 100 volts before it can be converted.

(*) Subtract a binary 1 if the number is negative.

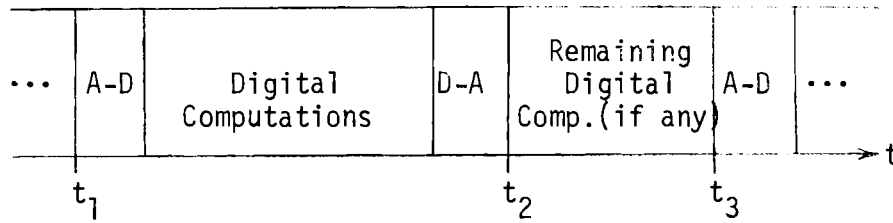
(**) If the A-D and D-A word lengths are unequal, n refers to the longer word length.

A shift or a multiplication will accomplish this scale change; roundoff compensation should thus be used with this operation in order to minimize the quantization error in the variable to be converted. A distinction will be made at this point: D-A roundoff compensation will refer to compensation only in the digital operation immediately preceding or affecting a D-A conversion; computer roundoff compensation will refer to compensation of all the multiply, divide, and right-shift operations performed by the digital computer.

It is important to remember that one of the primary advantages of hybrid computation over all-analog techniques is the increased accuracy provided by the digital computer for non-linear operations such as multiplication, division, and function generation. Computer roundoff compensation thus minimizes errors which have already been reduced quite sufficiently for most applications merely by the use of the digital computer. Above a certain number of bits, then, it can be expected that neither a further increase in the digital computer word length nor the use of roundoff compensation will cause a significant increase in solution accuracy. In other words, roundoff errors are not a serious problem in most hybrid simulations.

Time Delay and Slewing Errors

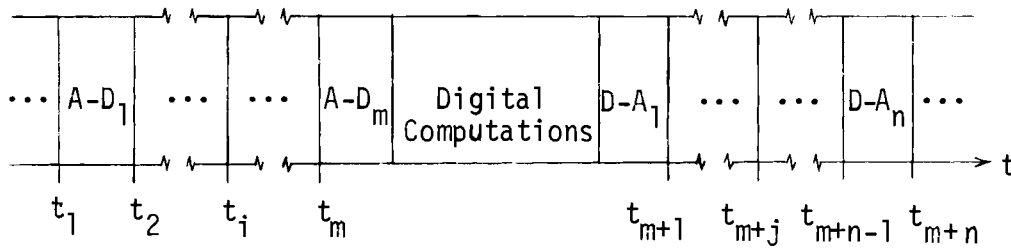
The analog computer solves equations continuously, in phase with real-time, while the digital computer requires a finite length of time for each set of calculations and thus cannot respond instantaneously to a parameter change. In hybrid computation, the digital output arrives at the analog computer τ seconds too late, where τ is the total elapsed time between the sampling of an analog variable to be converted A-D and the completion of the returning D-A conversion. Let us consider a simple hybrid problem in which there is only one A-D variable and one D-A variable to be converted during each frame of digital calculations. This case is shown graphically in Figure 2(a). It is seen that τ includes the A-D conversion time, the digital calculation time, and the D-A conversion time. Note that the time delay may or may not equal the digital frame time T , depending upon the timing sequence of the digital computations.



$$\tau = t_2 - t_1 = \text{ADC-digital-DAC time delay}$$

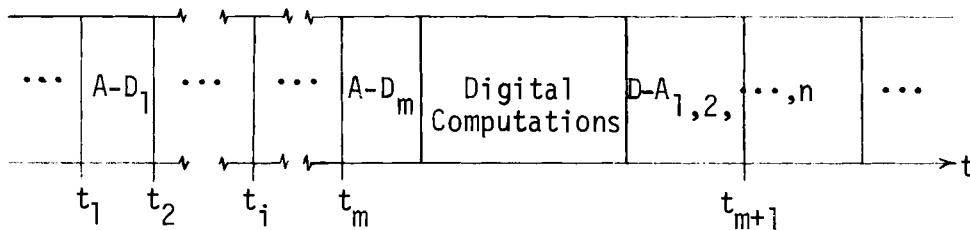
$$T = t_3 - t_1 = \text{sampling interval (digital frame time)}$$

(a) One A-D and one D-A conversion per frame.



$$\tau_{ij} = t_{m+j} - t_i = \text{time delay between } i\text{th A-D conversion and } j\text{th D-A conversion}$$

(b) Multiple A-D and D-A conversions.



$$\tau_i = t_{m+1} - t_i = \text{approximate time delay for } i\text{th A-D conversion}$$

(c) Lumped D-A conversion approximation.

FIGURE 2. Time delays in hybrid computation

Additional errors may be introduced if the digital computer requires two or more analog variables to complete one frame of calculations. The calculations are based on the assumption that all the converted analog variables were sampled at the same instant of time, but in reality the sampling and converting is a sequential process. Separate sample-hold amplifiers for each A-D channel would allow parallel sampling but would create an increase in equipment expense. A similar situation exists when there are two or more D-A variables to be converted at the end of each digital frame. Errors resulting from these situations are called slewing or skewing errors. They can, however, be related to the time delay error as shown in Figure 2.

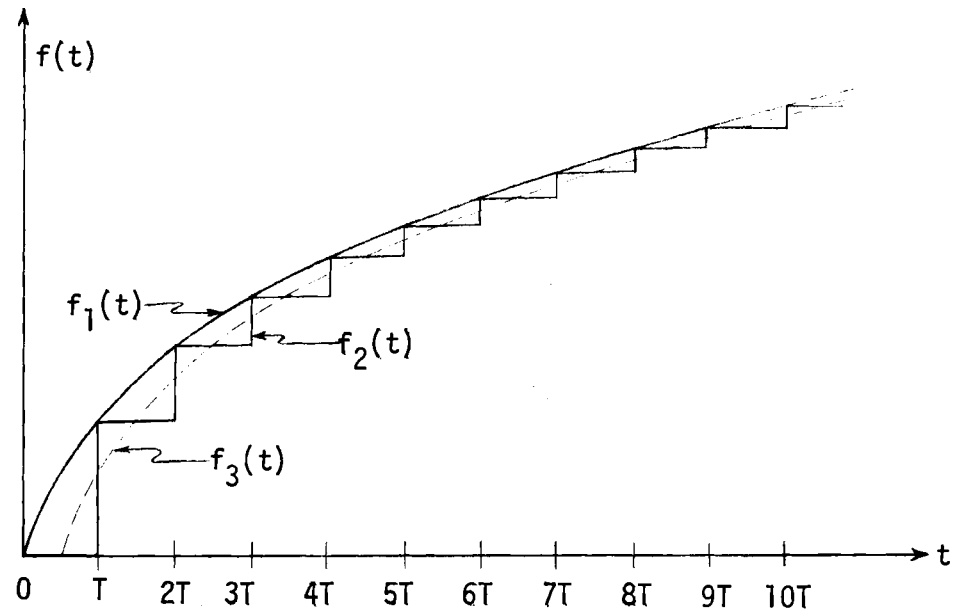
If there are two or more A-D variables and/or two or more D-A variables to be converted during each solution frame (as illustrated in Figure 2(b)), then a separate and distinct delay time τ_{ij} can be associated with each possible input-output pair. Thus, if there are m A-D variables and n D-A variables, there are (mn) distinct delay times. The D-A converters are usually several times faster than the A-D converter, however, resulting in a very small skewing error in the D-A conversion block. Thus it is quite reasonable, unless the number of D-A conversions per frame is excessively large, to lump the D-A conversions together (see Figure 2(c)) and assign a median time t_{m+1} as the approximate time at which all D-A conversions are assumed to be completed. Now there are only m distinct delay times with which to be concerned.

Data Reconstruction Errors

Another type of error is introduced at the D-A output, which is essentially defined only at discrete and usually regularly-spaced instants of time. In order to provide a continuous signal for compatibility with the analog computer, some means of interpolating between these points is required. An analog-hold circuit at the output of the DAC is used for this purpose. A zero-order, first-order, or fractional-order hold may be mechanized, but in either case the resulting interpolation will not provide a perfectly smooth waveform. Deviations from this ideally smooth waveform are called data reconstruction errors.

If a zero-order-hold circuit is used, the DAC output is held constant at the last converted value until it is updated by the next discrete DAC output. The result is a staircase waveform similar to $f_2(t)$ as shown in Figure 3. It has been shown by Miura and Iwata⁽³⁾ and others⁽¹⁾⁽²⁾ (and verified on Hybrid 1, as shown later in this report) that this staircase signal is approximately equivalent to a continuous curve passing thru the midpoint of each step. This equivalent curve is indicated by the dashed line $f_3(t)$ in Figure 3. Here it is assumed that (1) the high-frequency Fourier components introduced by the zero-order-hold circuit are small in comparison to the fundamental components of the reconstructed waveform, and/or (2) that the analog computer is relatively insensitive to these high-frequency components. The latter assumption is strengthened when the DAC output is an input to an analog integrator, and the former statement is strengthened when the sampling interval is small. With this continuous curve approximation, it is seen that the zero-order-hold circuit effectively introduces an additional time delay of $T/2$ seconds, or one-half the sampling period. The total combined time delay and data reconstruction error is thus equivalent to an effective time delay of $\lambda = (\tau + T/2)$ seconds.

If first-order-hold circuits were substituted for the zero-order-hold circuits at the D-A outputs, the $T/2$ delay would be eliminated. A zero-order-hold output may be modified, as shown in Figure 4, by adding an integrator and another D-A channel to produce a first-order-hold signal. This technique uses the present and past values of the variable to predict the slope of the variable during the next interval $t_n < t < t_{n+1}$. At the end of this interval a new value is sent over D-A channel 2, the integrator is momentarily switched to the IC mode to update its output, a new slope is calculated by sending the past value of the variable over D-A channel 1, and the integrator is returned to the compute mode. Since the frame-time T is normally quite small, some rescaling will be necessary to avoid having greater-than-unity pot settings as shown. If T is very small,



$f_1(t)$ = Ideal reconstructed analog signal at D-A output

$f_2(t)$ = Actual reconstructed analog signal for zero-order-hold

$f_3(t)$ = Approximate equivalent of $f_2(t)$

FIGURE 3. Data reconstruction error: zero-order-hold.

the required scale factors may prohibit the use of first-order-hold; however, as T is reduced, the zero-order-hold reconstruction error become smaller and the need for first-order-hold diminishes. In general, the additional equipment and computing overhead required to implement a first-order-hold in this manner is not justified by the slight increase in accuracy potentially gained by such action. First-order-hold performance was thus not evaluated in this study.

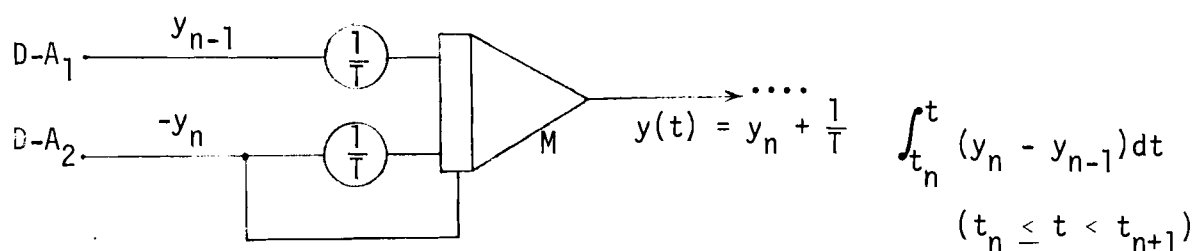


FIGURE 4. Synthesis of first-order-hold.

Inherent Sampling Errors

A certain amount of error is inherent in the sampling process associated with the A-D conversions. A sampled-data signal cannot be uniquely representative of the continuous signal which was sampled due to the lack of information about the behavior of the signal during the interval between samples. However, if the sampling rate is fast enough compared with the highest frequency component of the signal being sampled, the sampling error will be small enough that it may be neglected. A general rule of thumb is that 10 to 20 samples per cycle of the highest frequency component is sufficient. All of the test problems described in the next section of

this report were run at sampling rates which exceeded this requirement; hence sampling errors were considered to be insignificant. The sampling error was not evaluated since in most cases it is much less serious than the others.

Time Delay Compensation

In order to compensate for time delays and related errors, a prediction scheme is needed. As shown in the references⁽¹⁾⁽³⁾, the time delay error can be written in analytical form as a series involving the first, second, and higher derivatives of the affected variable:

$$e_d = y_d - y = -\lambda \frac{dy}{dt} + \frac{\lambda^2}{2!} \frac{d^2y}{dt^2} - \frac{\lambda^3}{3!} \frac{d^3y}{dt^3} + \dots$$

where e_d is the time delay error, y_d is the delayed variable, y is the correct undelayed variable, and λ is the total effective delay time. Compensation involves the cancellation of one or more of these error terms. For small time delays, the second and higher order terms of the error series are much smaller than the first term. A first-order prediction method thus seeks to eliminate the first term only, by the addition of $\lambda \frac{dy}{dt}$ to the solution. Since the correct undelayed variable and its derivative are not available, the derivative of the delayed variable must be used. The predicted variable y_p thus becomes

$$y_p = y_d + \lambda \frac{dy_d}{dt} \approx y_d + \lambda \frac{dy}{dt}.$$

Time delay compensation by first-order prediction can be mechanized in several different ways. Analog compensation, shown in Figure 5, is convenient for the single ADC - single DAC case if a derivative is available as the input to an analog integrator within the hybrid loop. Compensation may be applied just ahead of the A-D conversion or just after the D-A conversion.

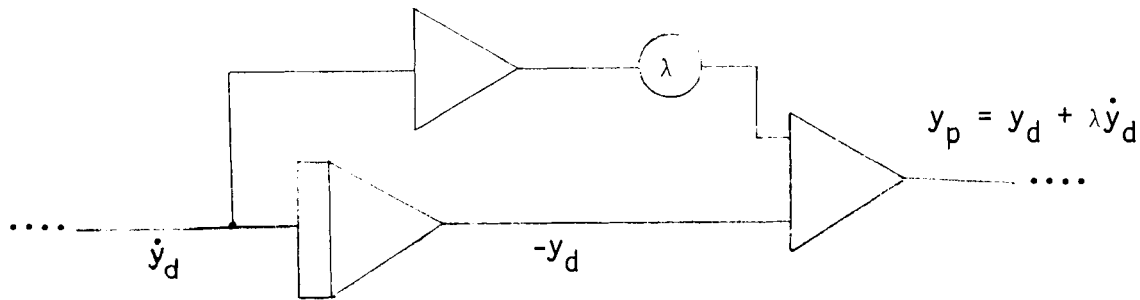


FIGURE 5. Analog time delay compensation

Alternatively, time delay compensation may be applied digitally with a first-order backward difference approximation for the derivative:

$$\left. \frac{dy}{dt} \right|_{t_n} \approx \frac{1}{T} [y(t_n) - y(t_{n-1})]$$

Digital compensation by predicted outputs is thus achieved by adding a prediction term to the digital output $y_d(t_n)$ before converting:

$$y_p(t_n) = y_d(t_n) + \frac{\lambda}{T} [y_d(t_n) - y_d(t_{n-1})]$$

This requires the lumping and averaging of multiple A-D input times in the same manner as multiple D-A conversions were treated in Figure 2(c).

If instead the compensation is applied to the A-D inputs, the distinct delays τ_i associated with each of the m inputs may be taken into account. A compensation term can be added to each digital input $x_i(t_n)$:

$$x_{ip}(t_n) = x_i(t_n) + \frac{\lambda_i}{T} [x_i(t_n) - x_i(t_{n-1})]$$

where $\lambda_i = \tau_i + T/2$ if zero-order-holds are used. The D-A outputs are then calculated from these predicted inputs x_{ip} rather than the actual inputs at time t_n . In this manner compensation is provided for both the basic time delay error and the A-D slewing error.

TEST PROBLEMS AND RESULTS

Four hybrid problems were solved on Hybrid 1 and the results were evaluated in terms of error sources and computer parameters. The digital portion of Hybrid 1 is an 18-bit fixed-point PDP-7 computer with an 8K core and a 1.75 μ sec memory cycle time. The 24-channel multiplexer/A-D converter unit has a digital word length of 14 bits (13 + sign), as do the 24 D-A converters. The D-A conversion time is 3.36 μ sec. The ADC can complete a conversion in 12 μ sec; however, successive conversions require a minimum interval of 19.25 μ sec between conversions in order to read and store each converted variable in memory. The computer and converter parameter variations were thus upper-bounded at the above capabilities; e.g., the effective A-D word length could be cut by two bits to simulate a 12-bit converter, but a 16-bit converter could not be represented.

All of the test problems, with the exception of the Sine Wave Reconstruction, were of the closed-loop type; i.e., there was feedback from the analog to the digital computer and vice versa. The approximate error during each time step can easily be calculated for open-loop hybrid problems, whereas in closed-loop problems the per-step errors remain in the loop and thus the solution error cannot easily be predicted.

Sine Wave Reconstruction

The purpose of this problem was merely to test the assumption that the zero-order-hold data reconstruction error is equivalent to a time delay of $T/2$ seconds. A simple harmonic oscillator was patched on the analog computer. The output of this oscillator was sent to the digital computer, delayed by τ seconds, and returned unaltered (except for the delay) to the

analog via a D-A converter with a zero-order-hold output. The A-D conversion was made at the beginning of each digital frame and the D-A conversion at the end of each frame; hence the delay τ was approximately equal to the frame time T . A continuous analog comparison was made between the delayed signal and the original undelayed sine wave. The resulting sinusoidal error signal was recorded for varying values of oscillator frequency and delay time.

The time delay obviously caused a phase lag in the sine wave. However, the amplitude of the error signal, which is much easier to measure on a strip-chart recording, can be directly related to the phase error θ . The maximum error occurs near 0° , where the derivative of $\sin \omega t$ is a maximum. For a sine wave of unit amplitude, the error at this point is:

$$E_{\max} = \sin(0^\circ) - \sin(-\theta) = \sin \theta \approx \theta \text{ for small angles.}$$

But $\theta = \omega \lambda$, where ω is the angular frequency in radians per second, λ is the effective delay time in seconds, and θ is the phase error in radians. Thus

$$\begin{aligned} \omega \lambda &\approx E_{\max} \\ \text{or } \lambda &= \frac{E_{\max}}{\omega} \end{aligned}$$

If the zero-order-hold delay theory is true, the above calculated value for λ should be

$$\lambda = \tau + T/2 \approx 1.5T$$

which yields

$$\frac{E_{\max}}{\omega T} = 1.5$$

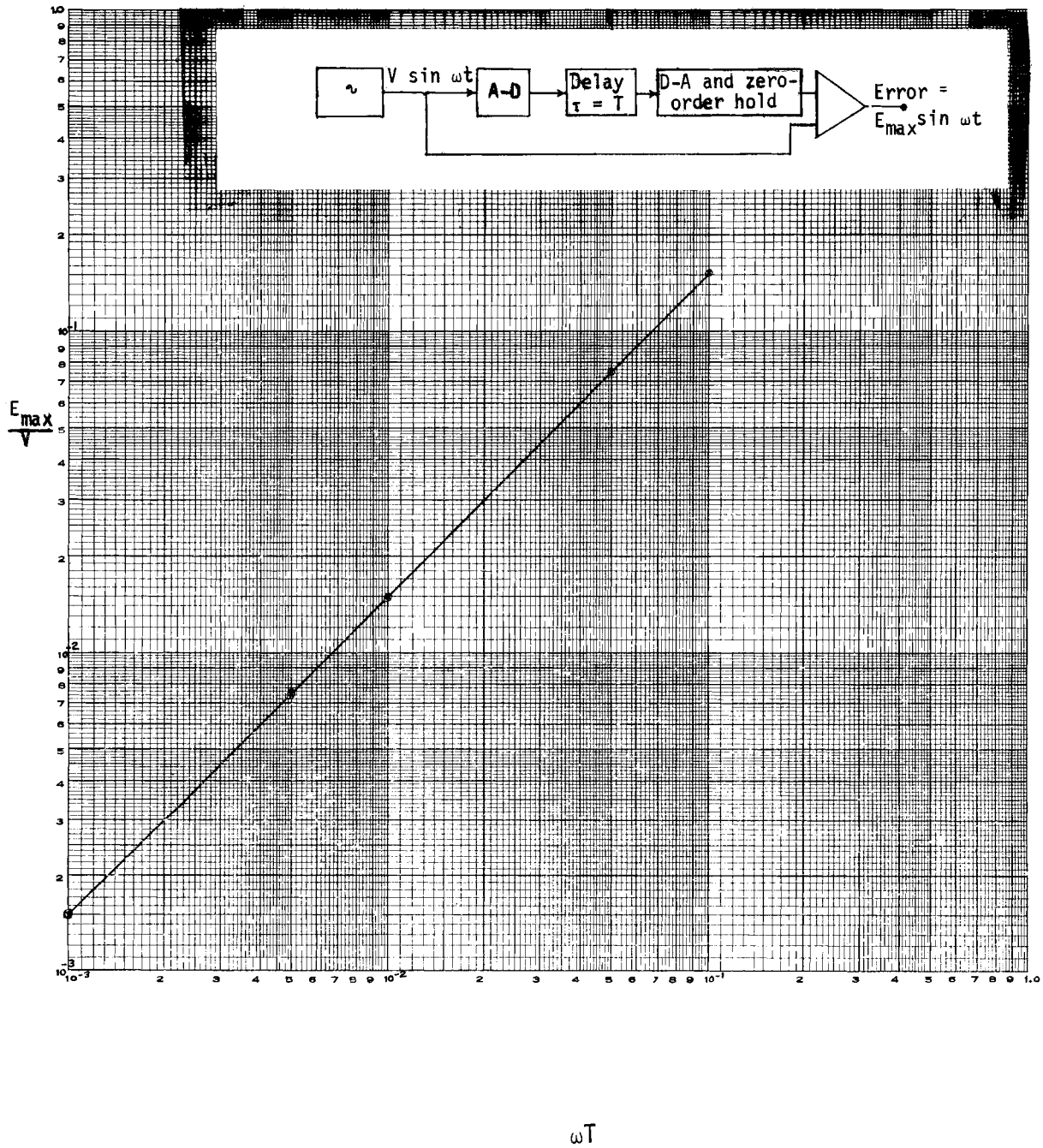


FIGURE 6. Sine wave reconstruction

The actual results are presented in Figure 6. The amplitude of the error signal is expressed as a fraction of the amplitude of the oscillator output. The graph shows that the ratio of the error amplitude to the angular frequency - frame time product was indeed 1.5, thus verifying the $T/2$ time delay effect of the zero-order hold over the range of ωT which was tested. (The maximum tested value, $\omega T = 0.1$, is equivalent to a sampling rate of 10 samples/radian or 62.8 samples/cycle.)

Pilot Ejection Study

The pilot of an aircraft flying at constant speed is ejected from the cockpit at time $t = 0$ with a given ejection velocity at a given angle backward from the vertical. This hybrid problem calculates the pilot's trajectory in order to determine whether or not he will clear the vertical stabilizer of the aircraft. Four simultaneous non-linear first order differential equations describe the relative motion of the pilot with respect to the aircraft. Four analog integrators perform the integrations; the remaining calculations are all performed by the digital computer. The integrator outputs are X , the pilot's horizontal displacement measured from the cockpit; Y , the vertical displacement from the cockpit; V , the absolute velocity of the pilot; and θ , the angle between the instantaneous velocity vector of the ejected pilot and that of the aircraft. A further description of this problem together with the governing equations and constants can be found in Appendix M of reference (5), or in SEG-TR-67-31, "MIMIC Programming Manual."

Quantization errors were investigated by programming two separate hybrid solutions to be run simultaneously, one with the standard Hybrid 1 computer and interface parameters as a reference solution (see Figure 7), and the other with the effective number of converter and/or digital computer bits reduced by software methods. A hybrid reference was used instead of an all-analog reference in order to isolate the quantization errors from time delays and other error sources. The A-D conversions for both solutions were grouped together in a single block, as were the D-A conversions, such that the time delays were approximately the same for both solutions.

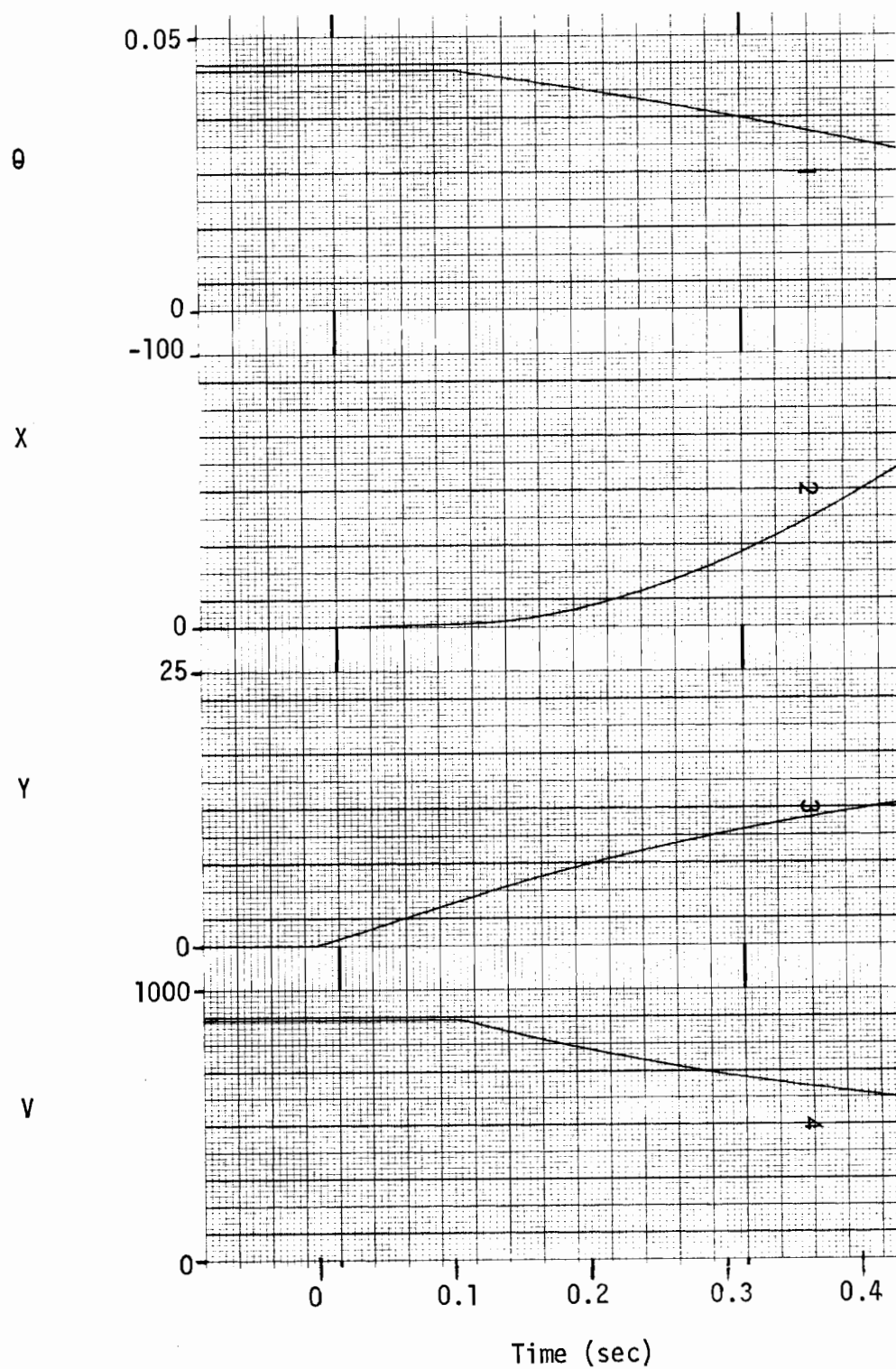


FIGURE 7. Pilot ejection study hybrid solution. Fourteen converter bits (reference solution)

The effect of a reduction in the word length of the A-D and D-A converters can be seen in Figures 8 and 9. Notice that at 14 converter bits a solution error is indicated even though the test solution and reference solution parameters were identical. This residual error was apparently due to slightly unequal time delays and/or analog component inaccuracies. A reduction in the word length of the converters to 12 bits made almost no difference in X, while a slight increase in the Y error was observed. The uncompensated errors grew more rapidly as the number of bits was further reduced, but A-D and D-A roundoff compensation effectively held the errors quite low, even for as few as nine converter bits. At ten bits the maximum compensated errors were 0.333% and 0.077% for X and Y, respectively.

Figures 10 and 11 display the results of a reduction in the effective digital computer word length with a compensated A-D and D-A word length of 12 bits. The solution errors remained quite small down to 15 digital bits. Over this range computer roundoff compensation did not provide a significant decrease in solution errors. At 14 bits there was a large increase in the uncompensated errors, while the compensated errors remained relatively small. At this point, then, computer roundoff compensation became significant. Thus with a 14-bit computer, 12-bit A-D and D-A converters, and the use of compensation techniques, the quantization and roundoff errors caused solution errors of only 0.467% and 0.192% for X and Y, respectively, referenced to an 18-bit computer/14-bit converter solution.

It should be noted that the method used to reduce the effective computer word length was to mask off one or more bits of the data word, beginning with the least significant bit, before and after each arithmetic operation. Problem scaling remained the same for all runs (see reference 5). If the problem had been rescaled to minimize variable ranges such that some of the most significant bits could have been "removed" in place of those on the lower end of the word, it is probable that the indicated errors could have been further reduced in all cases.

FIGURE 8. Pilot Ejection Study: Horizontal displacement error vs. converter word length. Computer word length = 18 bits.

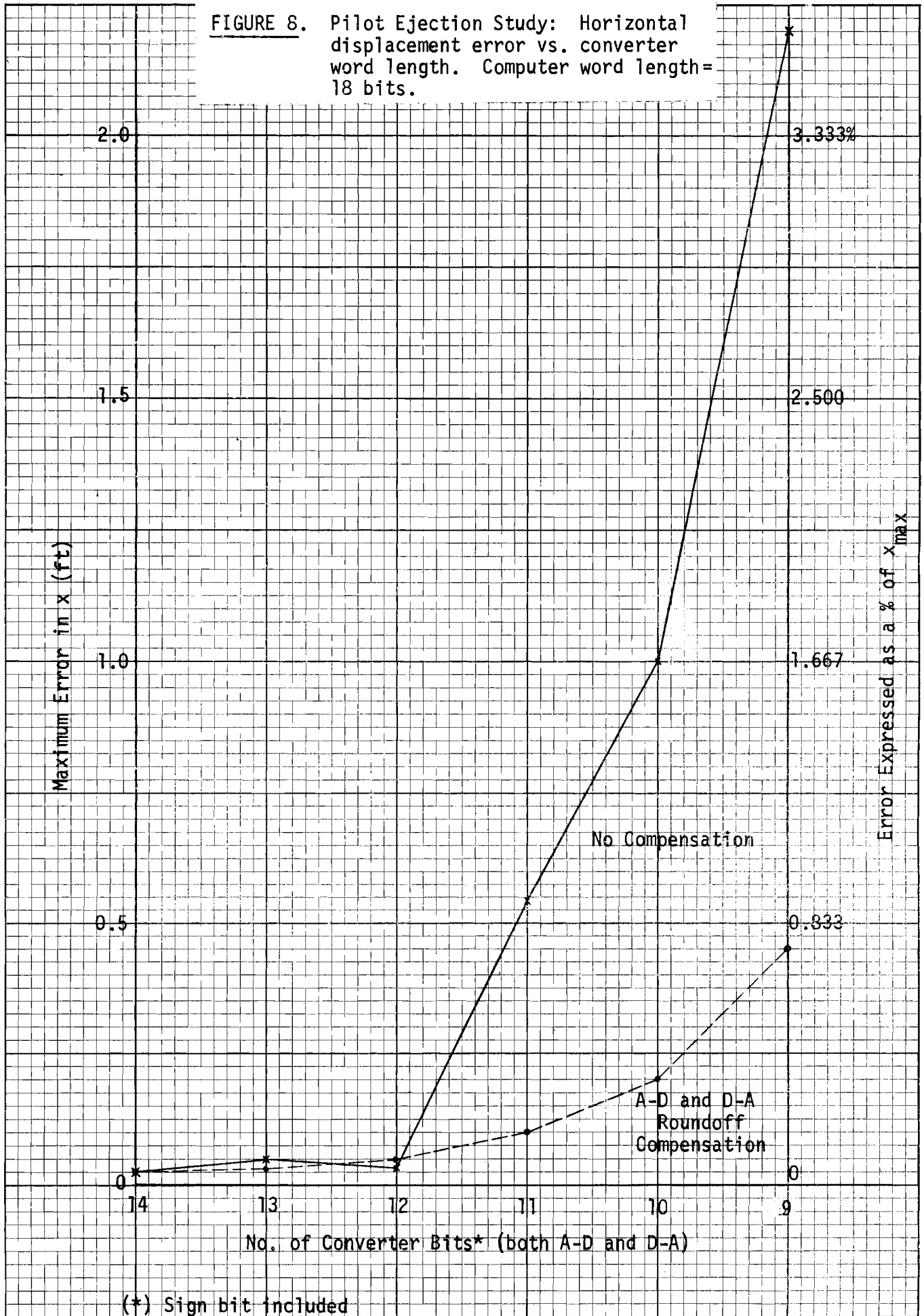


FIGURE 9. Pilot Ejection Study: Vertical displacement error vs. converter word length. Computer word length = 18 bits.

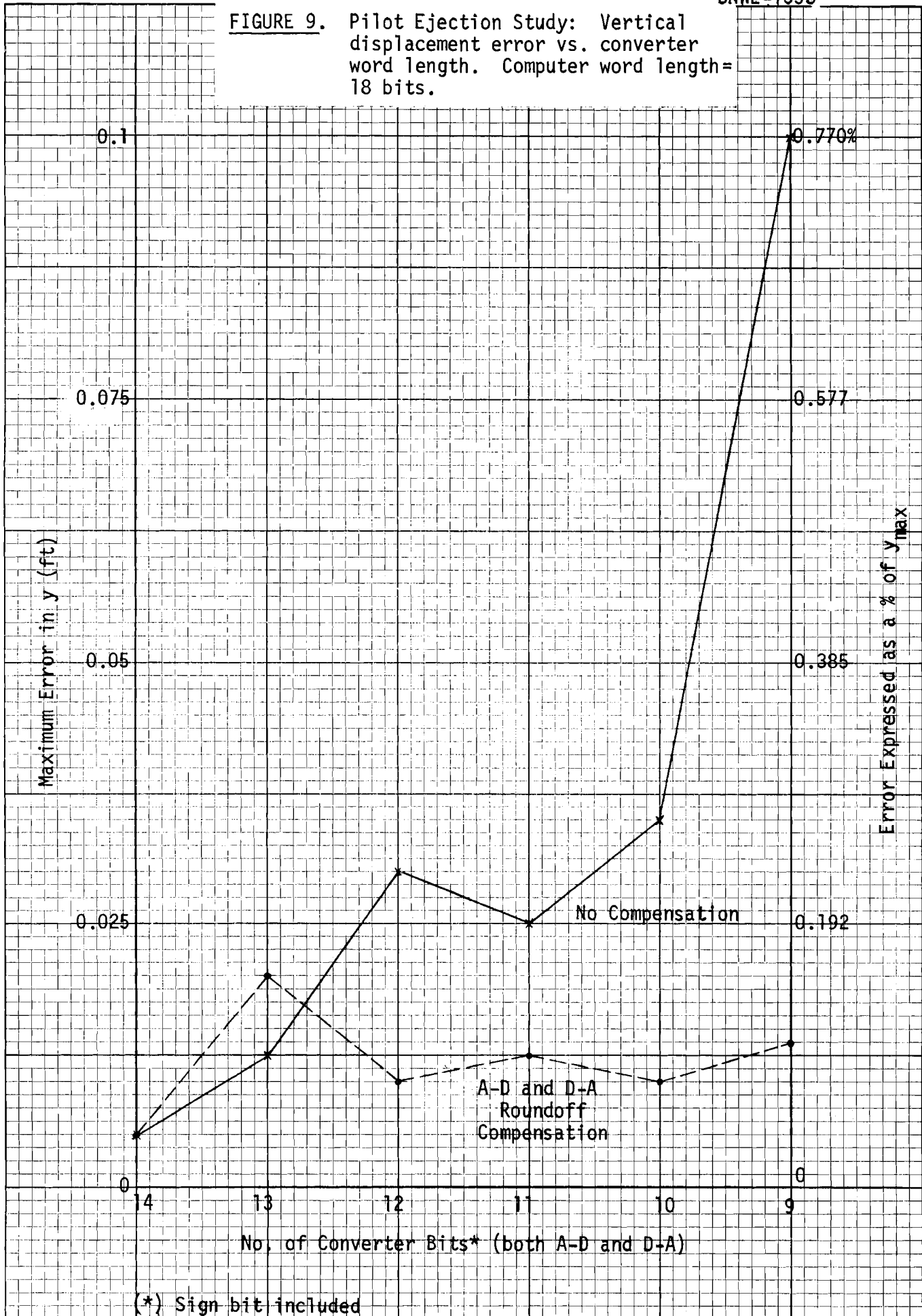


FIGURE 10. Pilot Ejection Study: Horizontal displacement error vs. computer word length. Converters: 12 bits, compensated.

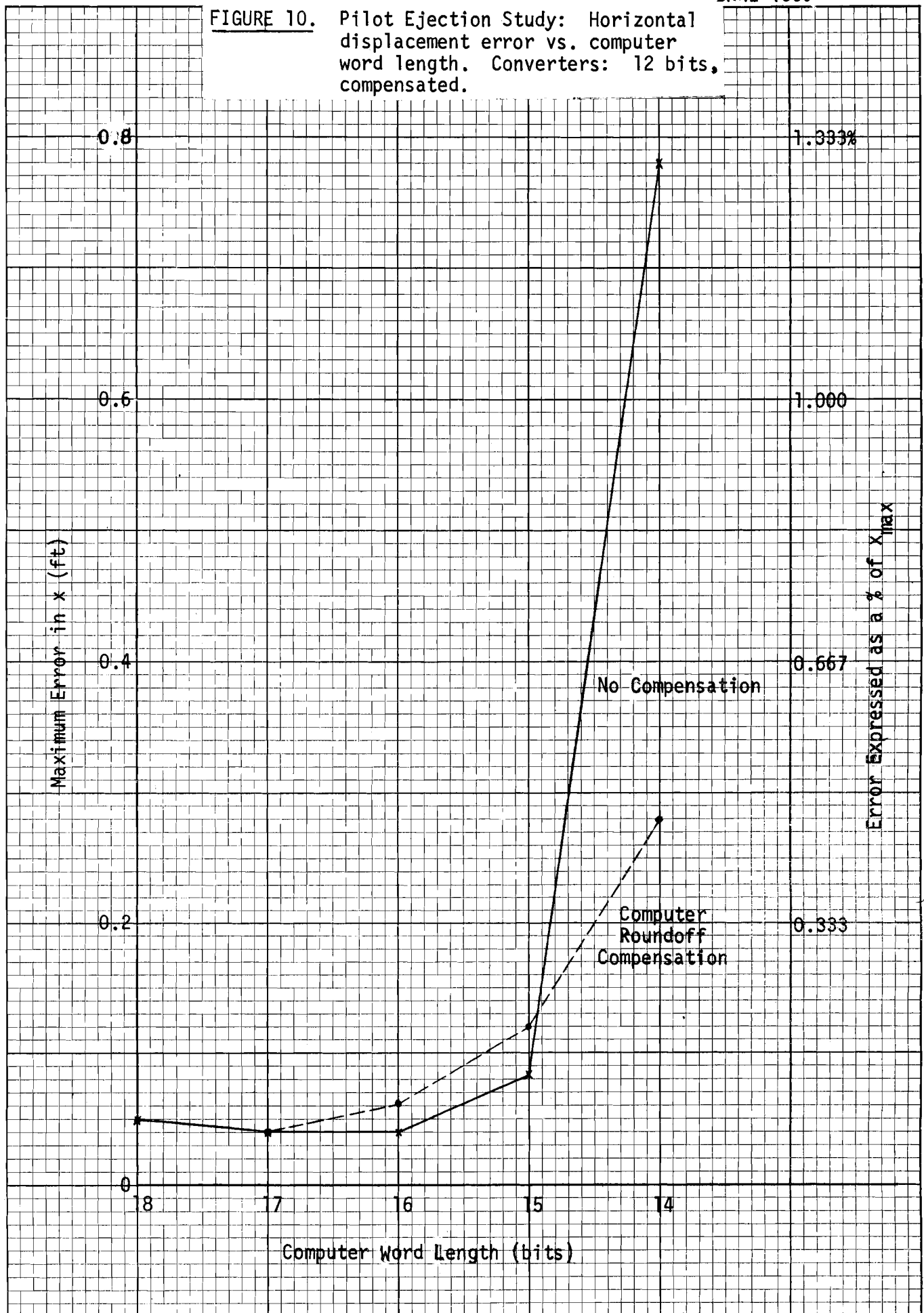
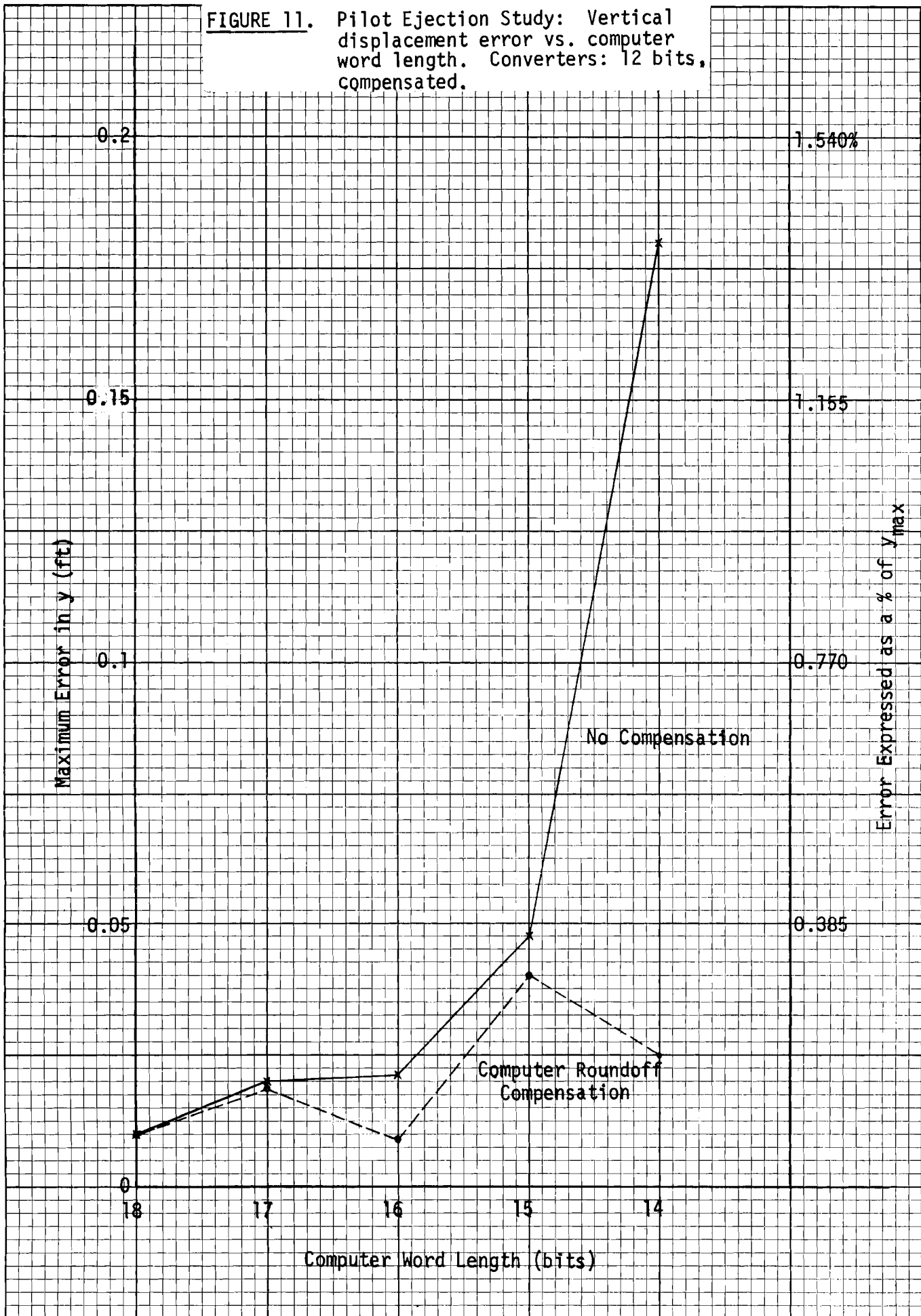


FIGURE 11. Pilot Ejection Study: Vertical displacement error vs. computer word length. Converters: 12 bits, compensated.



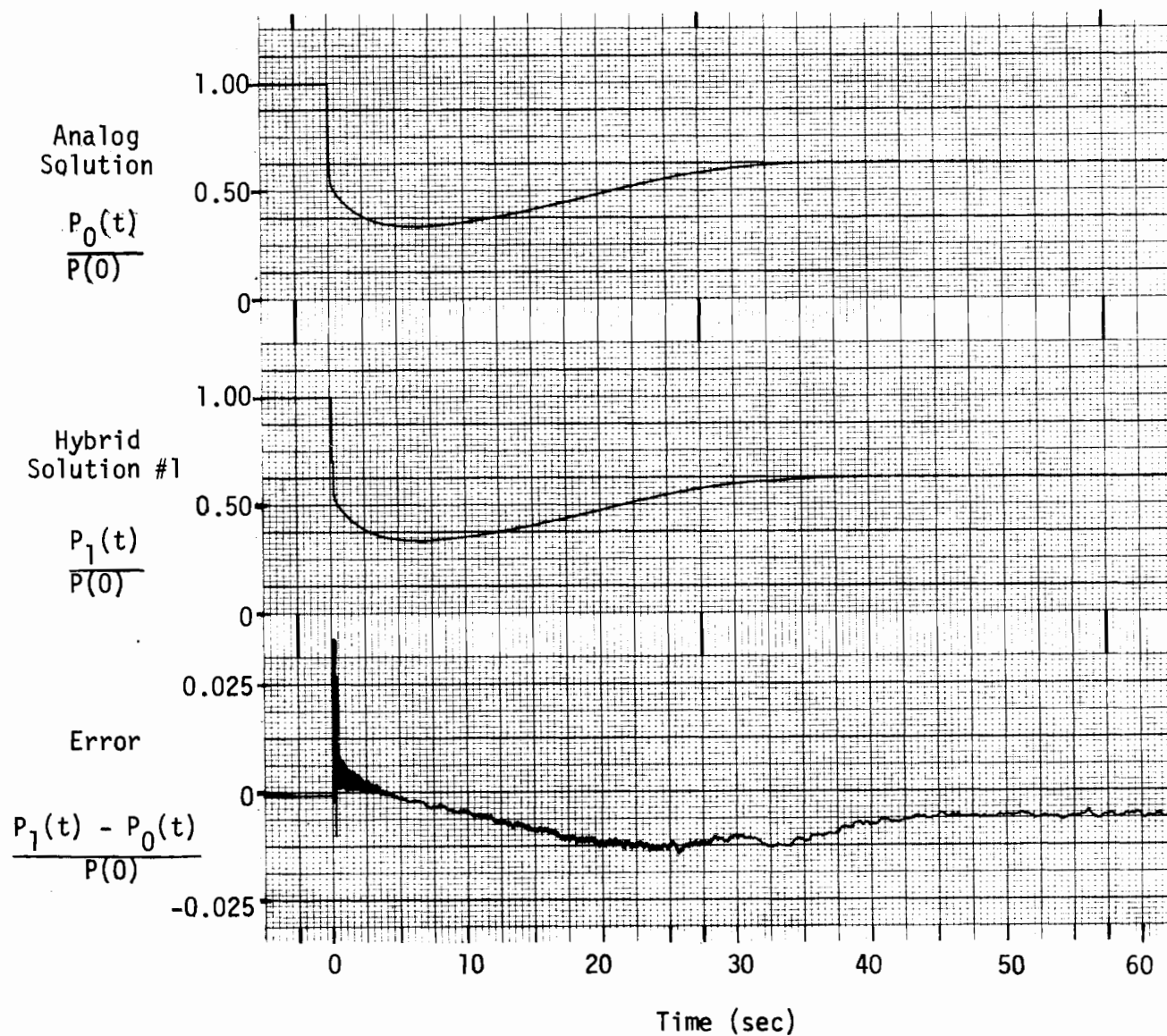


FIGURE 13. Reactor Kinetics: Response to -0.005 reactivity step.
Fourteen-bit A-D and D-A converters (Hybrid Solution #1)

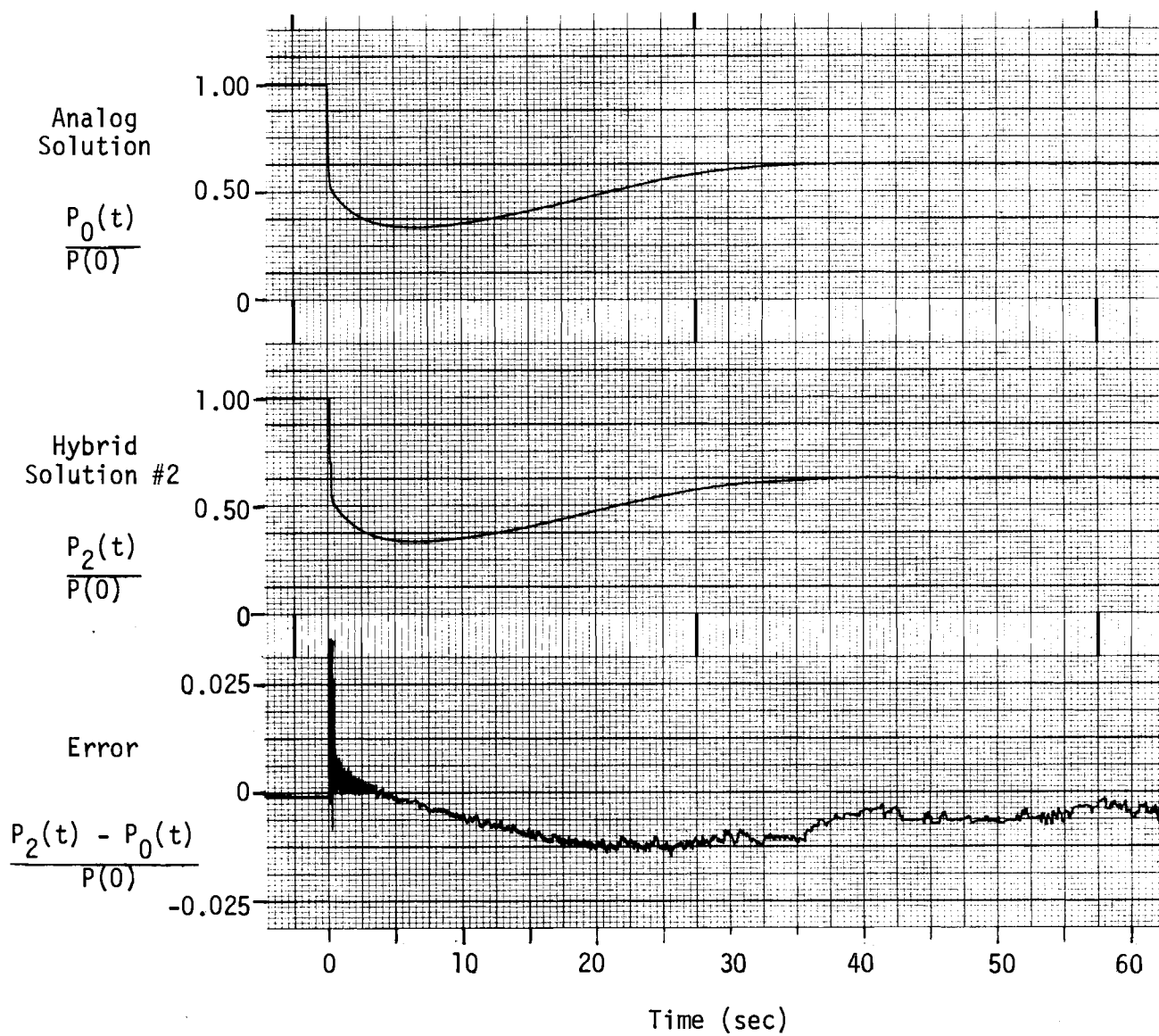


FIGURE 14. Reactor Kinetics: Response to -0.005 reactivity step. Twelve-bit A-D and D-A converters, compensated. (Hybrid Solution #2)

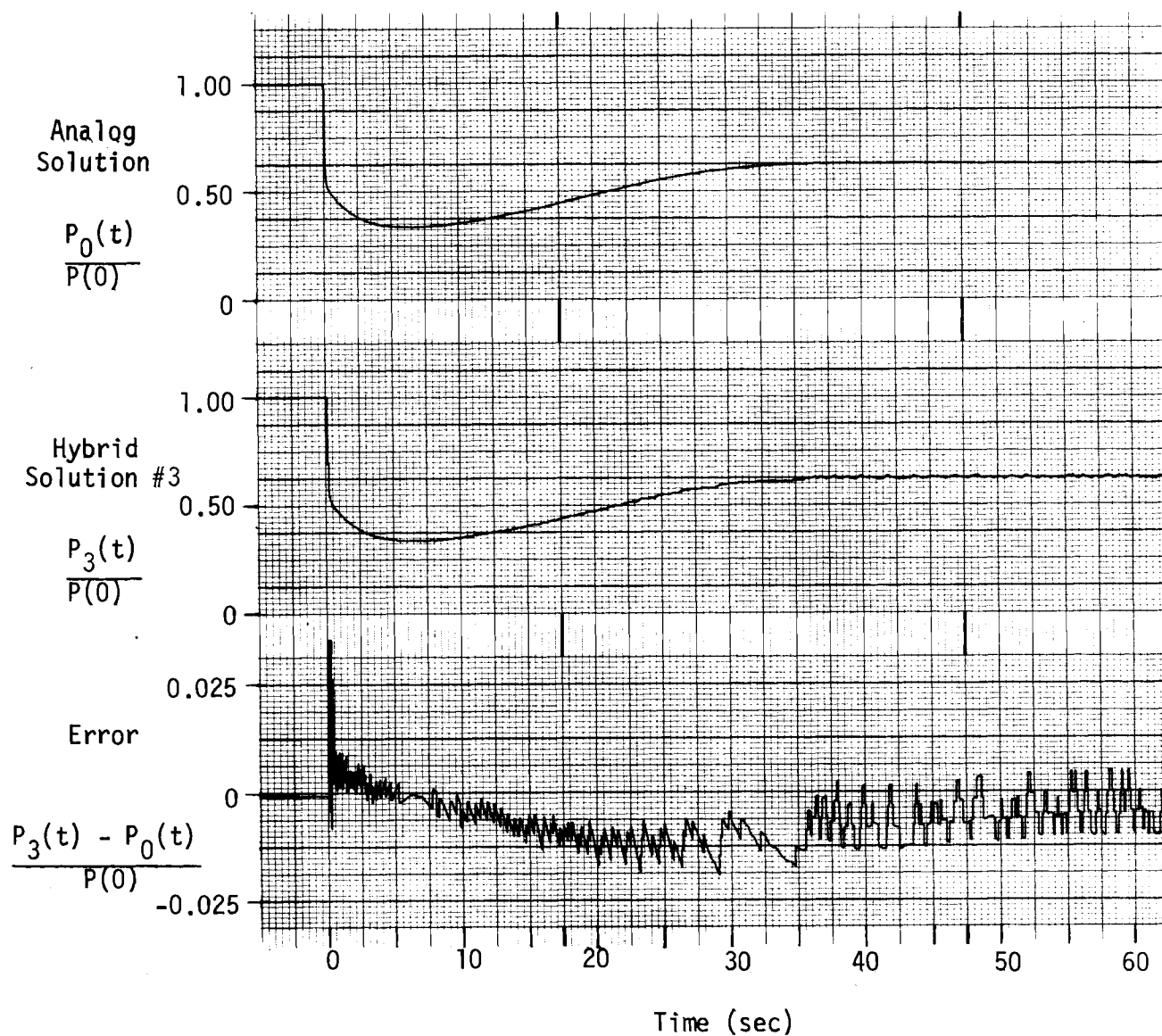


FIGURE 15. Reactor Kinetics: Response to -0.005 reactivity step. Ten-bit A-D and D-A converters, compensated. (Hybrid Solution #3)

solution was about the same for all three runs. If one ignores the quantization oscillation, the steady-state errors at the end of one minute of simulation were nearly identical. The test was then repeated for a positive reactivity step input of +0.003, and the results were similar. The hybrid solutions shown employed A-D and D-A roundoff compensation; however, there was no detectable difference in the solutions when converter roundoff compensation was not used. Thus, the accuracy of this simulation is a very weak function of the number of converter bits.

The same model was used to check the effect of time-delay compensation and digital roundoff compensation. All 14 converter bits and all 18 computer bits were used in these tests. Figure 16 shows the normal uncompensated hybrid solution and error signal for a reactivity step input of +0.003. Figure 17 shows the error signals for the same problem when (a) digital time-delay compensation by predicted input, (b) digital roundoff compensation, and (c) both time-delay and roundoff compensation were applied. The computation delay between A-D and D-A conversions was approximately 1.5 msec which, when added to half the update interval, gives a total effective delay of 51.5 msec. The addition of time-delay compensation resulted in only a slight decrease in error over the majority of the length of the run; the early part of the transient actually showed a larger error than the uncompensated case. In contrast, a significant improvement was noted when digital roundoff compensation was separately applied, even though there was again a temporarily larger error at the beginning of the run. When both of the compensation techniques were applied together, the best solution of the four was obtained.

The kinetics simulation emphasized the obvious fact that it does little or no good to compensate for an error source which contributes only a small fraction of the total solution error. As verified by the results, this problem was relatively insensitive to A-D and D-A quantization errors. Likewise, the time-delay was small relative to problem frequencies, leading to a small time-delay error. On the other hand,

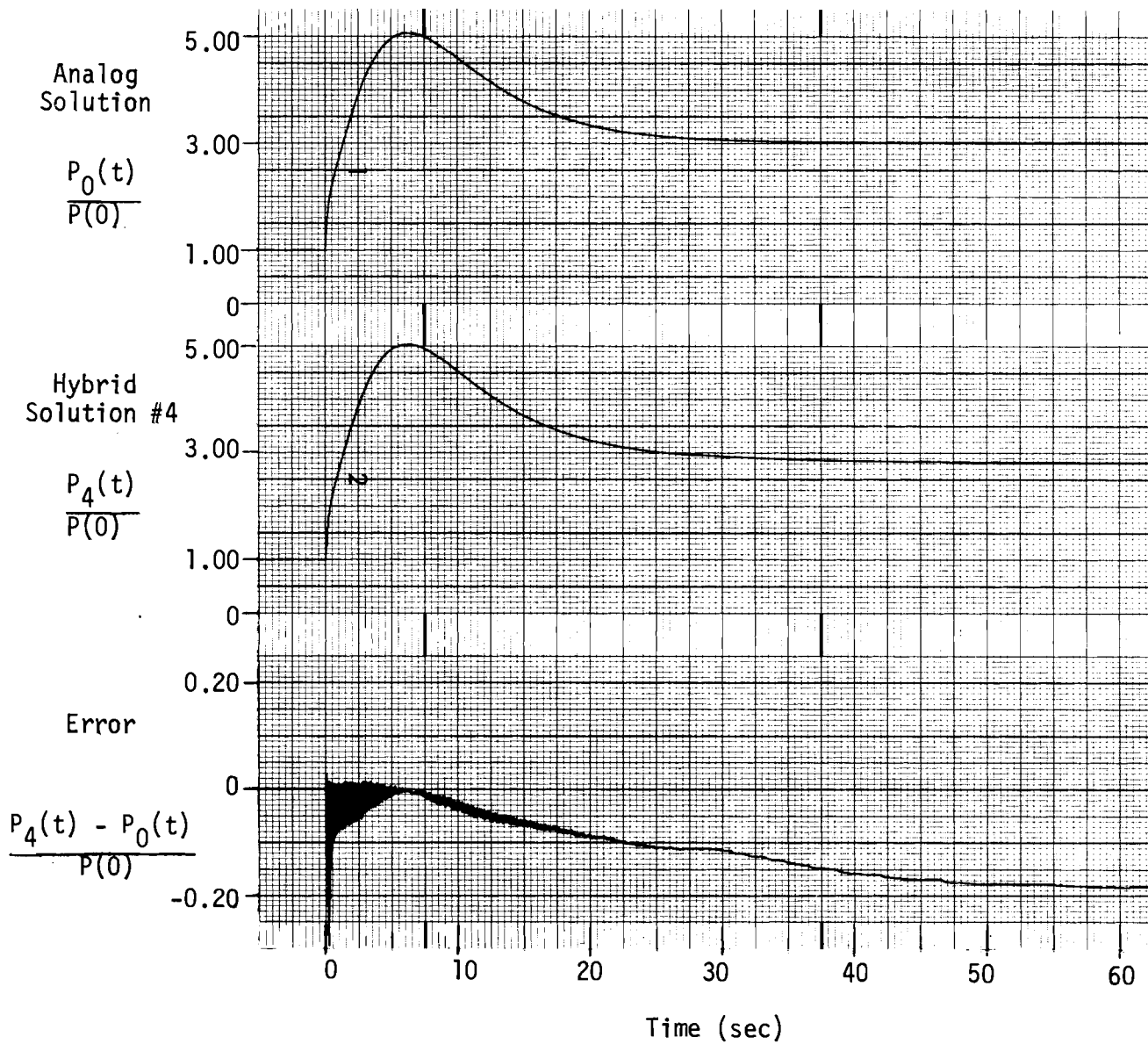
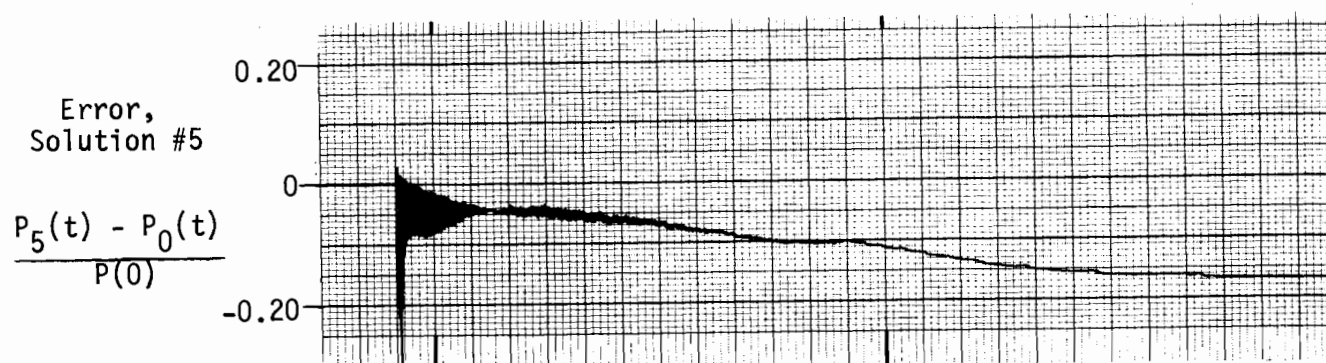
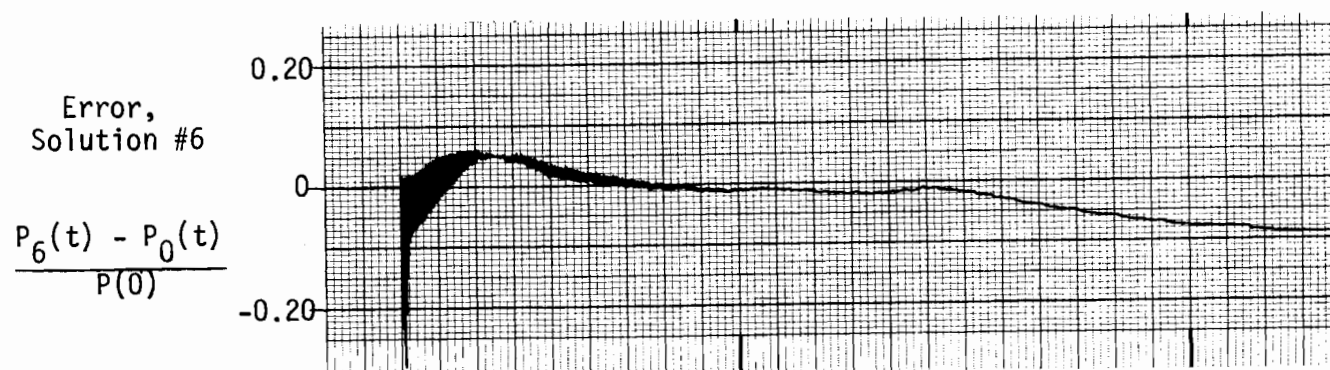


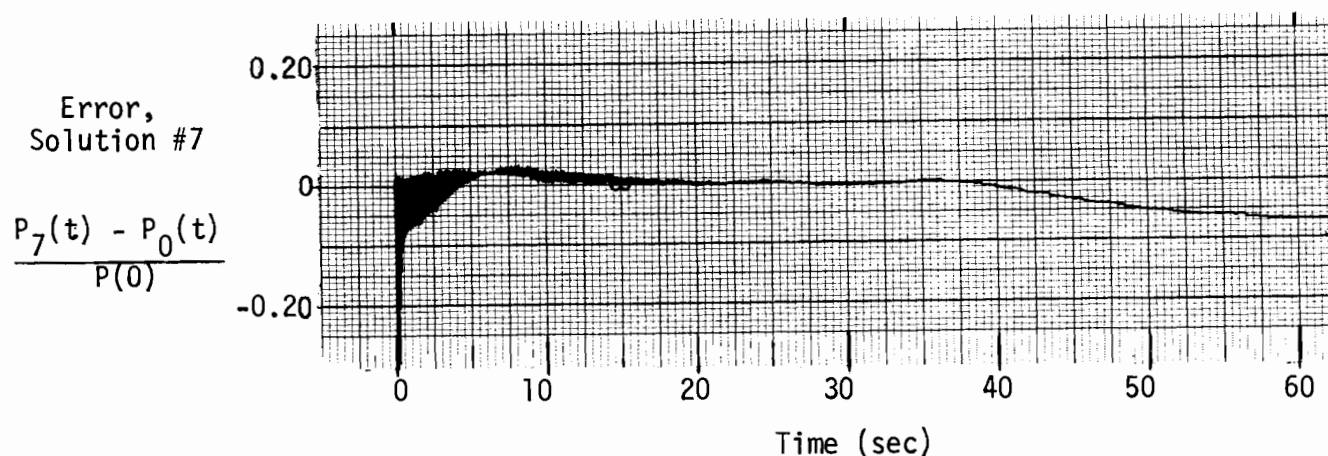
FIGURE 16. Reactor Kinetics: Normal uncompensated hybrid solution to a reactivity step change of +0.003.



(a) Time Delay Compensation



(b) Digital Roundoff Compensation



(c) Time Delay Compensation and Digital Roundoff Compensation

FIGURE 17. Reactor Kinetics: Effects of time delay compensation and digital roundoff compensation on hybrid response to reactivity step change of +0.003.

there were a large number of digital calculations; the magnitude of improvement gained by the use of digital roundoff compensation verified that digital roundoff error was the greatest offender in this problem.

Nonlinear Oscillator

The following nonlinear second-order differential equation was programmed on the analog computer:

$$\frac{d^2x}{dt^2} = -A \frac{dx}{dt} + B x \sin \omega t$$

$$A = 5.0$$

$$B = 50.0$$

$$\omega = 8.0$$

$$x(0) = 40.0$$

$$\frac{dx(0)}{dt} = -200.0$$

A hybrid simulation of the equation was also programmed for comparison with the all-analog reference solution. This equation was chosen as a "worst case" problem, as it is very sensitive to computational errors.

The hybrid solution was obtained by performing all operations, except the multiplication of x by $B \sin \omega t$, on the analog computer; this multiplication was the sole task of the digital computer. Two A-D conversions and one D-A conversion were thus required. A typical run is shown in Figure 18.

The first test consisted of holding the A-D word length fixed at 14 bits, varying the number of D-A bits, and recording the solution errors. Next the D-A word length was fixed at 14 bits and the number of A-D bits was varied. The above tests were then repeated with the addition of roundoff compensation. The results are plotted in Figure 19. When roundoff compensation was used, the solution errors remained almost constant all the way down to 10 D-A bits in the first case, and 9 A-D bits in the second case. Note that the error scale indicates the maximum amplitude of the oscillating error signal. Because of the nature of the problem, the accumulation of phase errors can cause large instantaneous solution errors; hence the magnitude of the error scale.

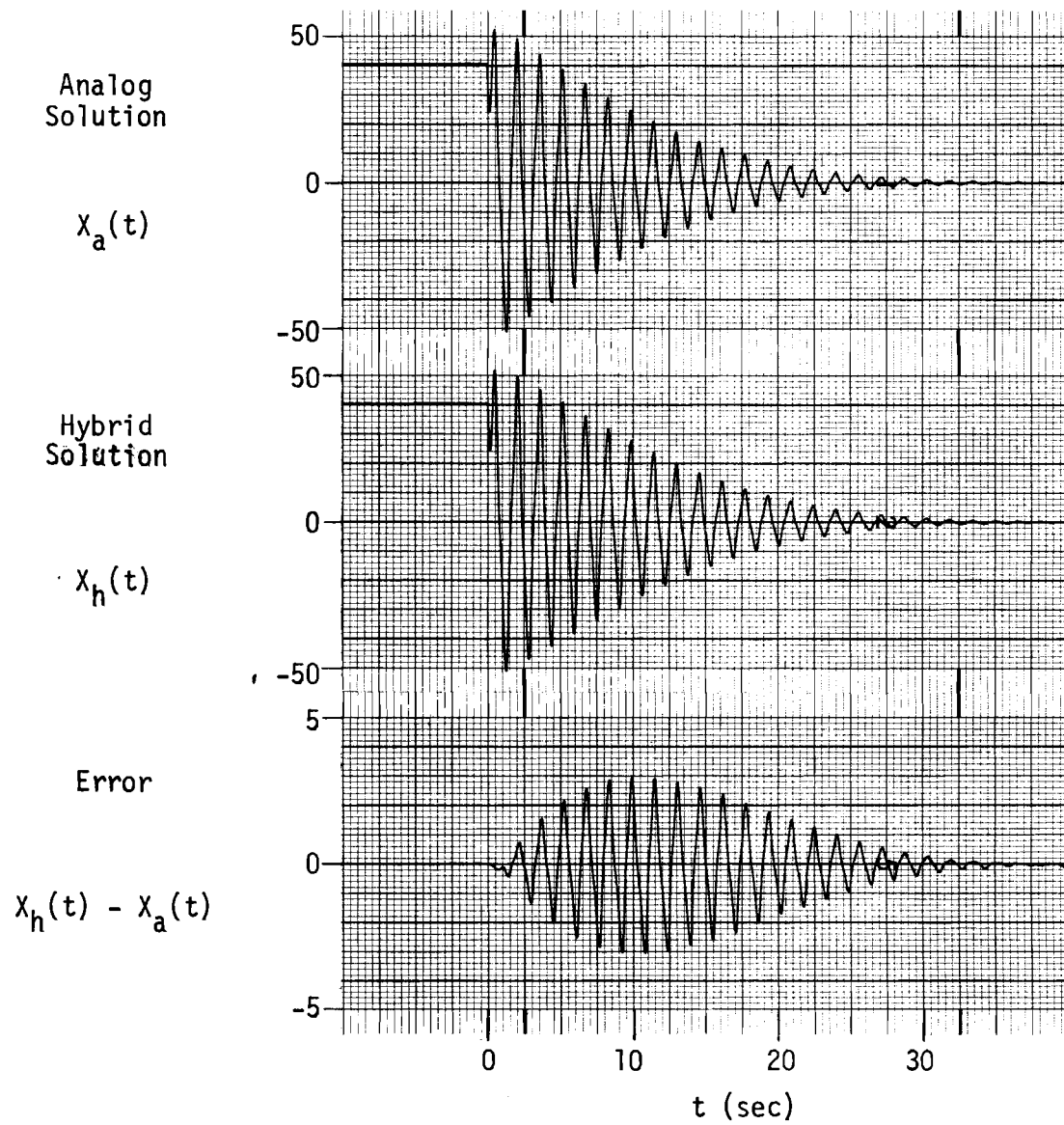
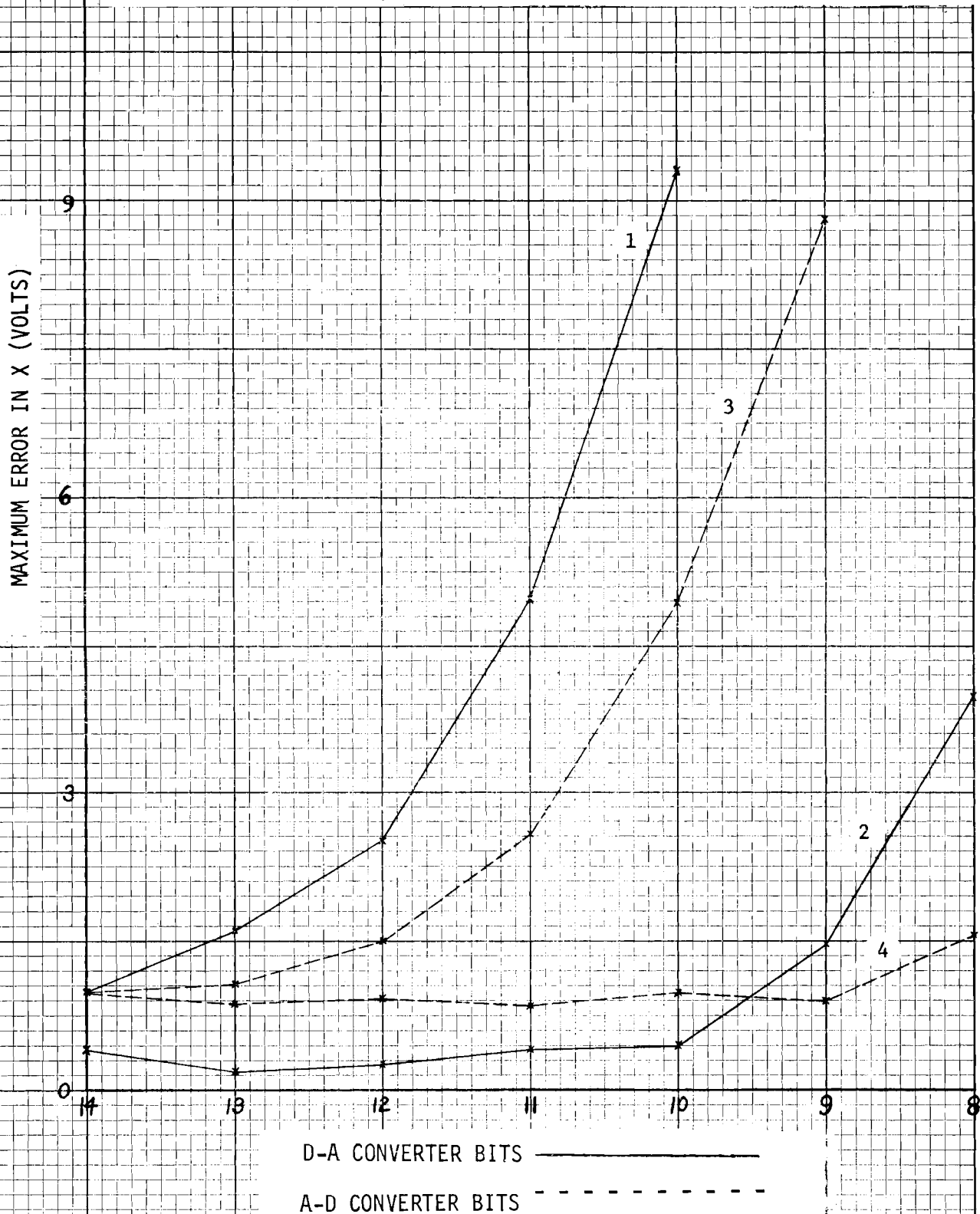


FIGURE 18. Nonlinear oscillator: Typical run.

FIGURE 19. Nonlinear oscillator: Quantization errors; converter word lengths varied separately.

1. D-A word length varied, A-D word length = 14 bits. No compensation
2. D-A roundoff compensation added to 1
3. A-D word length varied, D-A word length 14 bits. No compensation
4. A-D roundoff compensation added to 3



Next, the A-D and D-A word lengths were varied together (A-D bits = D-A bits). Four sets of runs were made, in which no compensation, A-D roundoff compensation, D-A roundoff compensation, and both A-D and D-A compensation were successively applied. This time the fully compensated solution error was held constant down to 11 conversion bits (see Figure 20). In this problem the D-A quantization error appeared to affect the solution more than the A-D error.

Finally, time delay errors and compensation techniques were tested on this problem. A variable time delay was inserted into the digital program. The maximum errors were plotted as functions of the product of frequency and frame time (delay time \sim frame time) for the following time-delay compensation schemes: (a) no compensation; (b) digital compensation by predicted inputs; (c) digital compensation by predicted output; and (d) analog compensation. The results, displayed in Figure 21, show a nearly constant improvement factor of about 4 for analog compensation above abscissa values of 1.5×10^{-3} . The digitally compensated error curves dip even lower, at times reducing the error by a factor of more than 20 over the uncompensated case. The predicted output method gave somewhat better results than the method of predicted inputs. Above 5×10^{-3} cycles/sample, both of the digitally compensated error curves rose with a greater slope than either of the other two curves. For large frequency-frame time products ($> 3 \times 10^{-2}$), it appears that analog compensation would be the preferred method. The continuous compensation afforded by the analog technique gives it the edge when large delays are present, whereas the accuracy of the digital computer in calculating prediction terms involving small delays is superior to analog compensation requiring a small potentiometer coefficient.

FIGURE 20. Nonlinear oscillator: Quantization errors; converter word lengths varied simultaneously

1. D-A word length = A-D word length (both varied).
No compensation
2. A-D roundoff compensation added to 1
3. D-A roundoff compensation added to 1
4. Both A-D and D-A compensation added to 1.

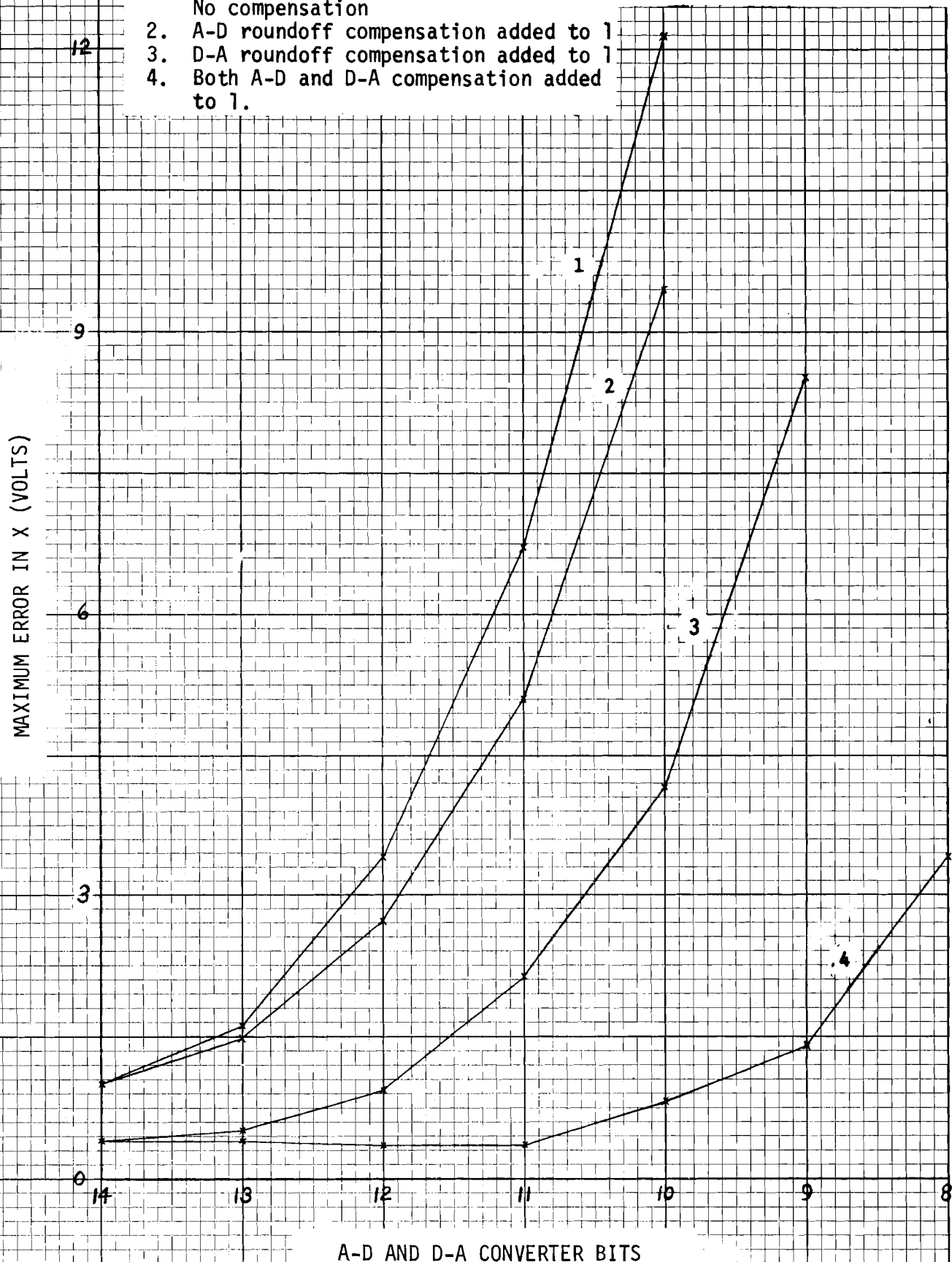
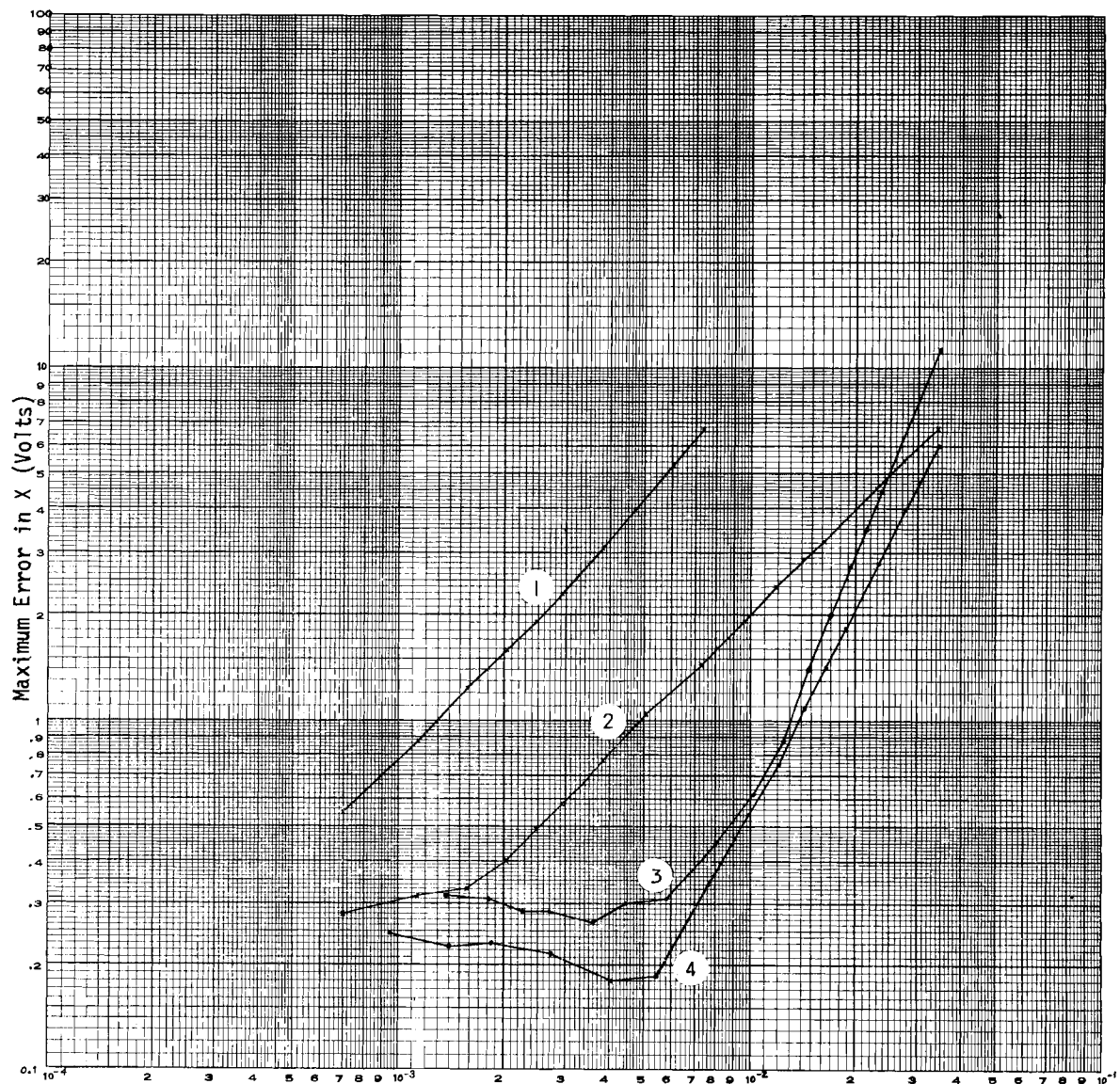


FIGURE 21. NONLINEAR OSCILLATOR: TIME DELAY ERRORS

1. No compensation
2. Analog time delay compensation
3. Digital input compensation
4. Digital output compensation



$$\frac{\omega T}{2\pi} \left(\frac{\text{Samples}}{\text{Cycle}} \right)^{-1}$$

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