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Investigation of Polycrystalline Thin Film $CuInSe_2$ Solar Cells Based on ZnSe Windows

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L. C. Olsen
Washington State University at Tri-Cities
Richland, Washington

NREL technical monitor: B. von Roedern

NREL

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ABSTRACT

This report concerns studies of CIS solar cells based on ZnSe window layers. ZnSe/CIS devices are fabricated by growing ZnSe films by MOCVD onto Siemens CIS and graded absorber substrates. ZnSe films are grown by reacting H_2Se with a zinc adduct. ZnSe/CIS heterojunctions have been studied by depositing transparent aluminum contacts onto ZnSe. These studies indicate that ZnSe/CIS solar cells can be fabricated with an efficiency greater than 14 %. Open circuit voltages are typically larger than 500 mV and the optimum range of ZnSe film thickness for maximum efficiency is between 100 Å and 250 Å. Photocurrents are significantly reduced as the film thickness exceeds 250 Å. Photoluminescence spectroscopy has been utilized to characterize the physical nature of CIS substrate surfaces, and ZnSe-CIS interfaces. These studies indicate that a segregated phase(s) exists at the surface of as received Siemens substrates. Additionally, it is determined that the segregated phase(s) still exist after the ZnSe growth process. To date, sputtered ZnO top contact layers have caused degradation of the photovoltaic properties of the ZnSe/CIS structure. Investigations of the effects of MOCVD grown ZnO upon ZnSe/CIS structures will soon be initiated. To establish the feasibility of ZnSe as a window layer, cells have been fabricated by incorporating a protective layer of CdS between the ZnSe and ZnO. A total area efficiency of 11 % was obtained with such a structure.

1. INTRODUCTION AND BACKGROUND MATERIAL

This report concerns work carried out during the second year of a three year effort to investigate $CuInSe_2$ (CIS) and CIS alloy solar cells based on ZnSe windows. Background information, program objectives and the technical approach are discussed in the remainder of this section, and technical progress made during the second year is discussed in subsequent sections.

1.1 Background Material

The key objective of this effort is to determine if ZnSe represents a viable alternative to CdS for the wide bandgap, n-type window layer in CIS cells. Although efficiencies > 15 % have been achieved for laboratory cells with CdS windows, an alternative to CdS is desirable because of the potential problems presented by the use of Cd in a production process. In particular, even though efficient CIS and CIS alloy cells may incorporate CdS layers with thicknesses of only 200 Å to 400 Å, the problems associated with waste handling in a production facility may present serious problems.

Other studies of ZnSe/CIS cells are rather limited. Nouhi, et al, reported on ZnSe/CIS solar cells fabricated by depositing ZnSe films onto CIS substrates supplied by industrial laboratories [1]. ZnSe films were deposited by reactive magnetron co-sputtering of Zn and In dopant in Ar/H_2Se. The ZnSe films were relatively low in resistivity, say, 20 ohm-cm. Efficiencies of 7 to 8.5% were obtained with ARCO supplied CIS substrates. Work was also carried out by Yoo, et al. [2]. This study involved fabrication of cells with a thin insulating layer of ZnSe between the base CIS layer and the CdS emitter. Cells were fabricated by depositing ZnSe onto CIS substrates provided by ARCO. The ZnSe films were deposited by physical vapor deposition. Cells exhibited low efficiencies primarily due to the ZnSe layers being highly resistive.

More recently, the European group reported on studies of Cd-free CIS cells, including results for devices with ZnSe buffer (window) layers [3]. The

ZnSe layers were grown by CBD, whereas our work involves ZnSe films grown by MOCVD. An open circuit voltage of 423 mV and a fill factor of 56 % was reported for a ZnSe/CIS cell in Reference 3.

1.2 Program Objectives

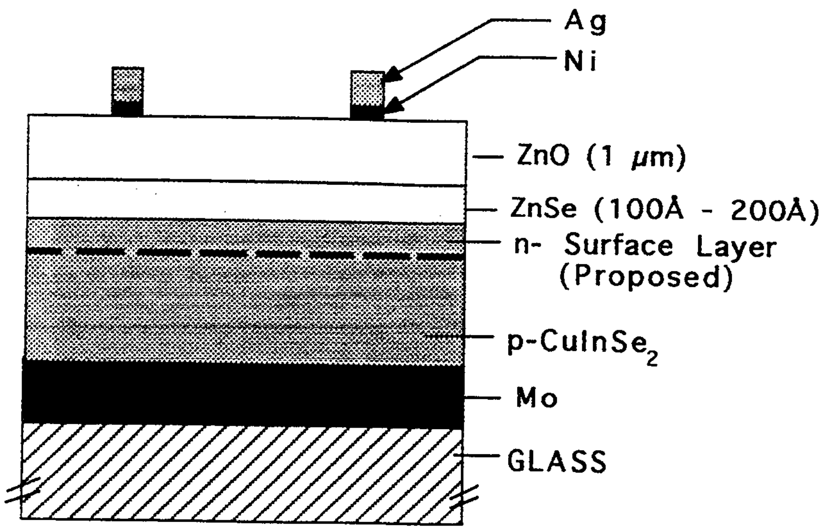
The primary objective of this program is to provide an alternative to CdS for the window layer material for efficient CIS and CIS-alloy solar cells. In particular, the use of ZnSe window layers is expected to lead to solar cell structures with a conversion efficiencies > 14 %. A discussion of the technical approach being used to meet these objectives follows.

1.3 Technical Approach

It is anticipated that cells will ultimately be fabricated with a structure as described by Figure 1A. A proposed electron band structure is shown in Figure 1B. Note that an n-type layer is included in these figures. Recent photoluminescence studies of Siemens Solar CIS substrates and structures with ZnSe films deposited onto CIS substrates have established that a segregated phase(s) exists at the CIS surface. The band diagram is based on the assumption that the segregated phase is n-type, and has a bandgap of 1.3 eV. The photoluminescence studies are discussed in a subsequent section. In order to fabricate ZnSe/CIS cells, procedures must be developed for growing conductive ZnO onto the ZnSe/CIS structures without degrading the properties of the ZnSe/CIS junction. To attain these goals, the program is structured into three tasks: (1) CIS and CIGS cells with ZnSe windows; (2) Material and device characterization; and, (3) Device modeling. Task 1 comprises the major thrust of the program. This task has involved characterization of CIS substrates, MOCVD growth of ZnSe and ZnO and fabrication of ZnO/ZnSe/CIS solar cells. Task 2 has included T-I-V analyses and collaboration with NREL to conduct photoluminescence studies of CIS substrates and ZnSe/CIS structures. Finally, Task 3 concentrates on device modeling to support experimental studies.

Key results of the second year effort are discussed in the following sections.

(A)



(B)

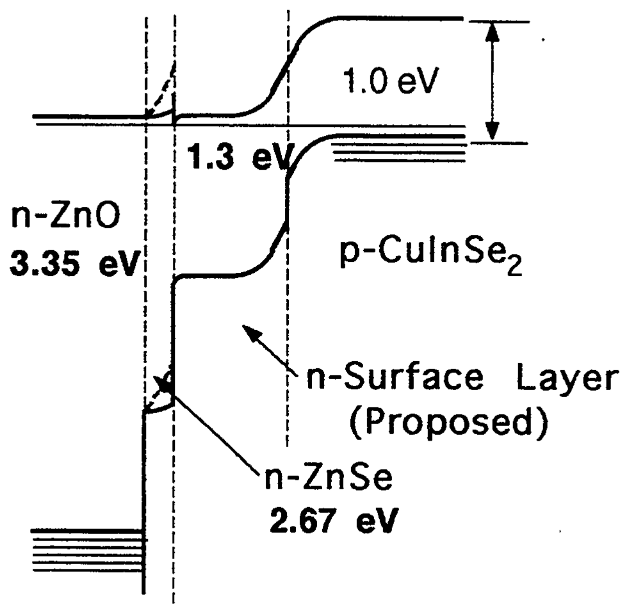


Figure 1. (A) Structure of ZnO/ZnSe/CIS solar cells assuming the existence of an n-type surface layer; (B) Proposed electron band diagram for the cell structure. See Section 3 for discussion of the possible conduction band spike.

2. MOCVD GROWTH OF ZnSe AND ZnO

ZnSe and ZnO films are grown by MOCVD. Procedures for ZnSe growth are established and ZnO deposition will begin in the near future. A discussion of the status of these growth technologies follows.

2.1 MOCVD Growth Of ZnSe

Growth of ZnSe is accomplished in a SPIRE 500XT reactor housed in the Electronic Materials Laboratory at WSU Tri-Cities by reacting a zinc adduct with H_2Se. The zinc adduct is formed (by a vendor) by reacting triethylamine (TEN) and dimethylzinc (DMZn). The triethylamine was mixed to give a vapor pressure of 16 torr at 20°C. Growth rate of ZnSe is controlled by adjusting the flow of hydrogen through the metalorganic bubbler. The growth rate varies linearly with the flow of hydrogen through the DMZn/TEN bubbler. Typical growth conditions that result in a ZnSe growth rate of 1 Å/s and a VI/II ratio of 5 are as follows: a total pressure of 65 torr, 6000 sccm of palladium-diffused hydrogen; 25 sccm hydrogen bubbled through the DMZn/TEN bubbler at 20°C; and 270 sccm hydrogen selenide (1% in H_2); and a substrate temperature of 250°C.

ZnSe films grown on CIS substrates have a strong (111) orientation. Figure 2 gives X-ray diffraction results for a ZnSe film grown by MOCVD on a Siemens substrate at 200°C. Note the strong ZnSe (111) line intensity along with the CIS (112) line intensity. Most of the growth of ZnSe has been carried out at substrate temperatures between 200°C and 250°C. X-ray diffraction studies indicate that the ZnSe films grown on CIS exhibit a strong (111) orientation while the CIS substrates exhibit a strong (112) orientation.

Iodine has been used to dope ZnSe n-type. In particular, ethyliodide mixed with helium (1000 ppm) is utilized as a source of iodine. It is straight forward to grow ZnSe with a resistivity on the order of .05 ohm-cm on single crystal surfaces at 250°C. Iodine-doped ZnSe films grown on CIS have a much higher resistivity, however. The flow of the ethyliodide/helium mixture is

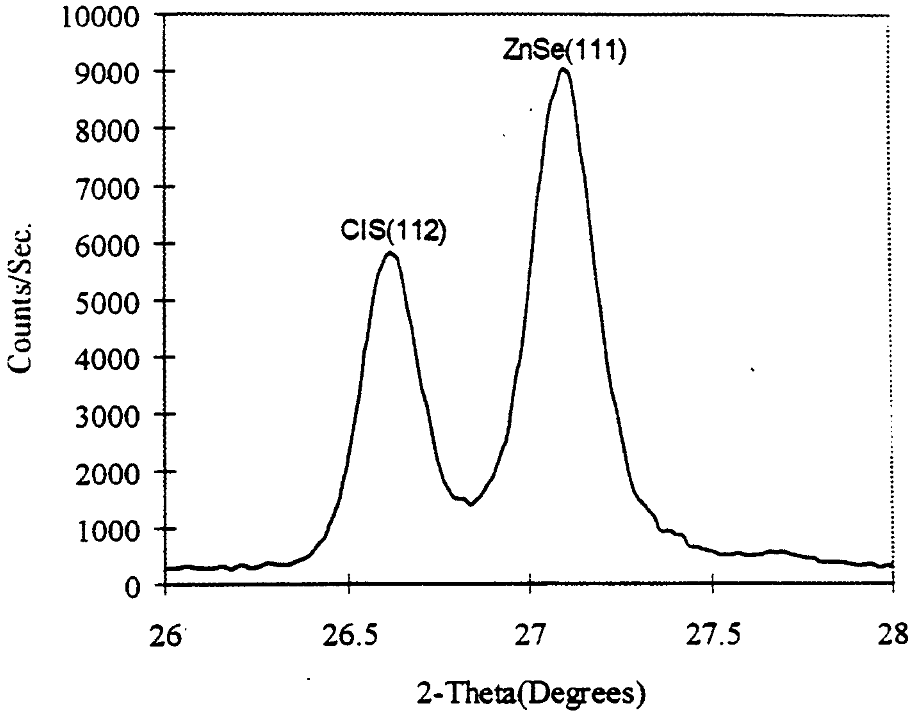


Figure 2. XRD plot showing the (112) reflection of the CIS substrate and the (111) re4flection from ZnSe.

usually set at 100 sccm.

2.2 MOCVD Growth Of ZnO

The WSU SPIRE 500XT reactor has been modified for ZnO growth. Tetrahydrofuran (THF) is utilized as a source of oxygen, while the zinc adduct used for the growth of ZnSe is also utilized for ZnO growth. Thus, tetrahydrofuran is reacted with the zinc adduct to grow ZnO. The THF liquid is stored in a room temperature bubbler and introduction of THF vapor into the reactor is controlled by a PFD Model 1004 gas flow control system. THF has been used with DMZn by Wright [4] and Wessels [5] to grow ZnO at substrate temperatures ≥ 300°C. Results for a few runs were reported in the annual report for the first year effort. After those first runs, problems were experienced with seals in mass flow controllers in the THF delivery system. A low level effort was devoted to rebuilding the THF delivery system this past year. The system is nearly ready for use.

3. Al/ZnSe/CIS TEST CELLS

ZnSe/CIS structures have been studied by depositing an array of aluminum circular areas 2.8 mm in diameter onto the ZnSe film to serve as contacts as depicted in Figure 3. Al films are deposited with a thickness of 100 to 120 Å and at a rate ≥ 10 Å/sec so that light can pass through the film and to minimize the sheet resistance. Illuminated characteristics for three test cells are shown in Figure 4. The I-V characteristics shown in Figure 4A are for an Al/CIS structure, that is, one without any ZnSe layer. The I-V characteristics given in Figure 4B are for Al/CIS structure for which the CIS substrate had been selenized (subjected to H_2Se). Finally, Figure 4C shows characteristics of an Al/ZnSe/CIS structure. Illuminated characteristics of test cells are taken by illuminating the device with an intensity such that the short-circuit current is approximately 40 mA/cm^2. Since the Al film typically transmits only 20 % of the incident light, the illumination intensity is five times greater than would normally be used to simulate an AM1.5 spectrum. It is important to note, however, that the actual photon flux entering the CIS or ZnSe/CIS layer structure is approximately correct for AM1.5 simulation. Since there are no collector grids on test cells to shadow incident light, we consider the test cell values of J_{sc} and efficiency to be active area numbers. Although it may be rather unusual for researchers to attain an active area current density

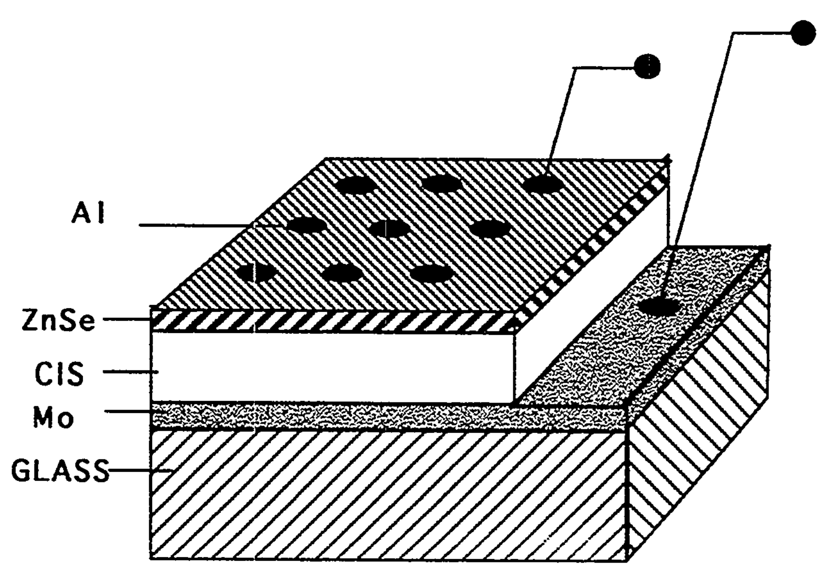
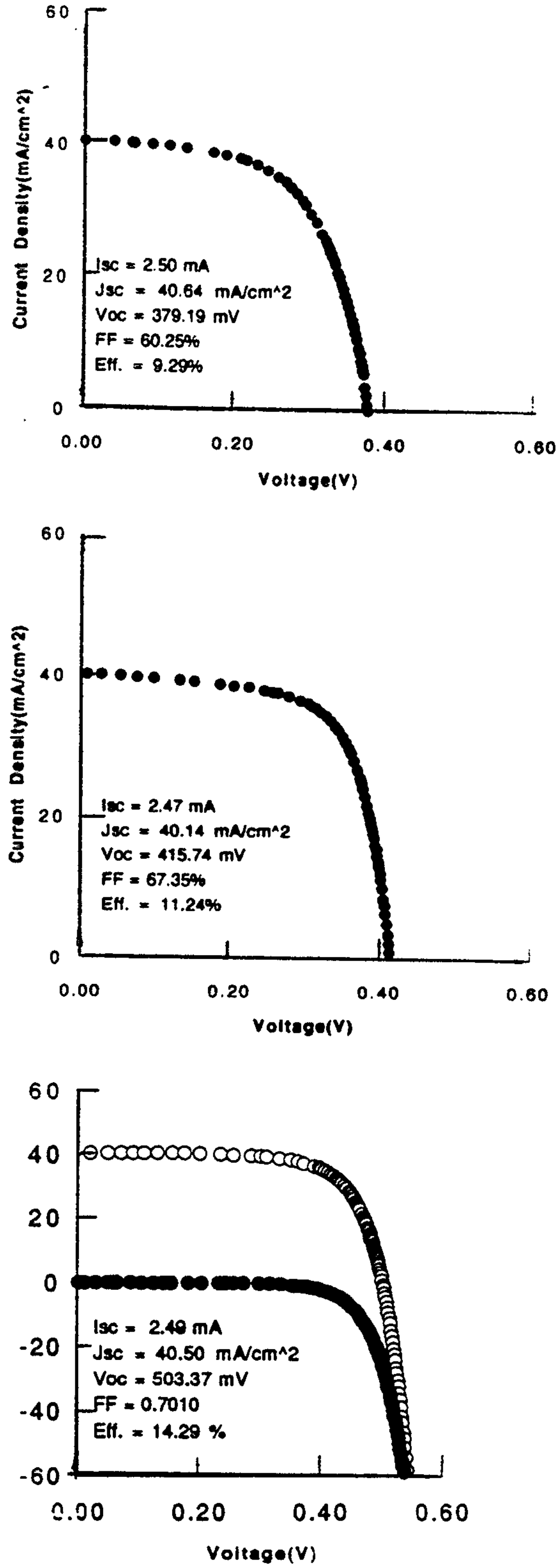


Figure 3. Configuration of test cells on ZnSe/CIS structure.

(A) (B) (C)



PROCESS:

(A)
- Cleaned & Etched
- Deposition of Al

(B)
- Cleaned & Etched
-Subjected To H_2Se at 250 °C
- Deposition of Al

(C)
- Cleaned & Etched
- Growth Of 100Å ZnSe
- Deposition Of Al

Figure 4. Illuminated characteristics for: (A) Al/CIS on cleaned and etched substrate; (B) Al/CIS on substrate selenized at 250°C; (C) Al/ZnSe/CIS test cell 94ZC439 formed on a CIS substrate.

of 40 mA/cm^2, this value of active area J_{SC} has been obtained. Therefore, we have standardized our test cell evaluation procedure to consist of setting the value of J_{SC} to ≈ 40 mA/cm2. We are; of course, assuming that values of fill factor (FF) and Voc determined for test cells can translate to completed solar cells. This translation has definitely been verified for V_{OC}. Since there are several ways that FF can be affected by the deposition of the top contact layer and the collector grid, the value of fill factor for a completed cell is typically less than that obtained for a test cell. However, it seems reasonable to assume that the test cell result may be considered a limiting value.

Descriptions of the processing are included for the three types of devices considered in Figure 4. The characteristics in Figure 4A are for an above-average Al/CIS cell structure. Estimated active area efficiencies of such structures are typically in the range of 7 to 9 %. As indicated, CIS substrates are cleaned and etched prior to Al deposition. The cleaning process involves the use of TCA, acetone and methanol, whereas the etching procedure involves the use of a 10 % solution of KCN. The improved I-V characteristics shown in Figure 4B are typical of an Al/CIS configuration for which the CIS substrate is subjected to H_2Se at 250°C, prior to deposition of Al. This type of structure is not stable, however. The properties of a 'selenized' device gradually degrade to a normal Al/CIS device over a period of two to three days. The effect of a ZnSe layer in an Al/ZnSe/CIS device is shown by the I-V characteristics in Figure 4C. Values of the fill-factor and Voc are greatly increased, as one proceeds from an Al/CIS to an Al/ZnSe/CIS device structure. Finally, the properties of an Al/ZnSe/CIS device are quite stable.

Figure 5 describes the range of results for ZnSe/CIS structures as the ZnSe thickness is varied. Generally, it is found that for ZnSe thicknesses > 250 Å, inflected I-V curves result and values of J_{SC} are reduced. The reduction of photocurrent can be interpreted to be a result of the formation of a significant conduction band spike at the ZnSe-CIS interface, as predicted (0.85 to 0.9 eV) in Reference 3 for an interface between relaxed, bulk layers of ZnSe and CIS. Numerous test cells have been fabricated with properties similar to those shown in Figure 4C. The ZnSe film was estimated to be 195 Å for 94ZC439. Note that with Jsc set equal to approximately 40 mA/cm2, FF = 0.70, Voc = 503 mV and the estimated active area efficiency is 14.29 %.

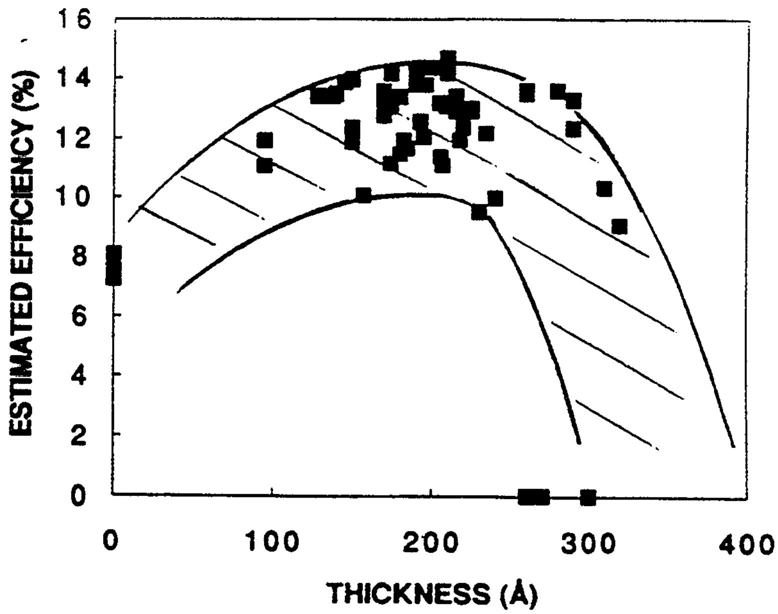


Figure 5. Estimated active area efficiency for test cell structures vs ZnSe thickness.

We have recently begun studies with the Siemens graded absorber (GA) material, which is characterized by a significant sulfur concentration at the surface. The Siemens graded absorber material has been described in Reference 6. As shown by Auger profiles in Reference 6 the GA material is a graded $Cu(In,Ga)(Se,S)_2$ structure with higher sulfur concentration at the front and back surfaces, and also higher Ga concentration at the back surface. The spectral response of Siemens cells made with the GA material is very similar to one based on the standard CIS material. However, values of FF and Voc obtained with the GA material are slightly larger than results achieved with the standard material. Apparently, the sulfur concentration at the front surface allows for reduced loss currents.

The key difference between test cells made on CIS substrates and graded absorber substrates seems to be that the required ZnSe thickness for maximum performance is less in the case of the GA substrates. Figure 6 gives illuminated I-V characteristics for a test cell formed on a GA substrate, 94ZC480. When Jsc is set to 40 mA/cm^2, the estimated active area efficiency is 14.82 %. This is the best test cell result to date.

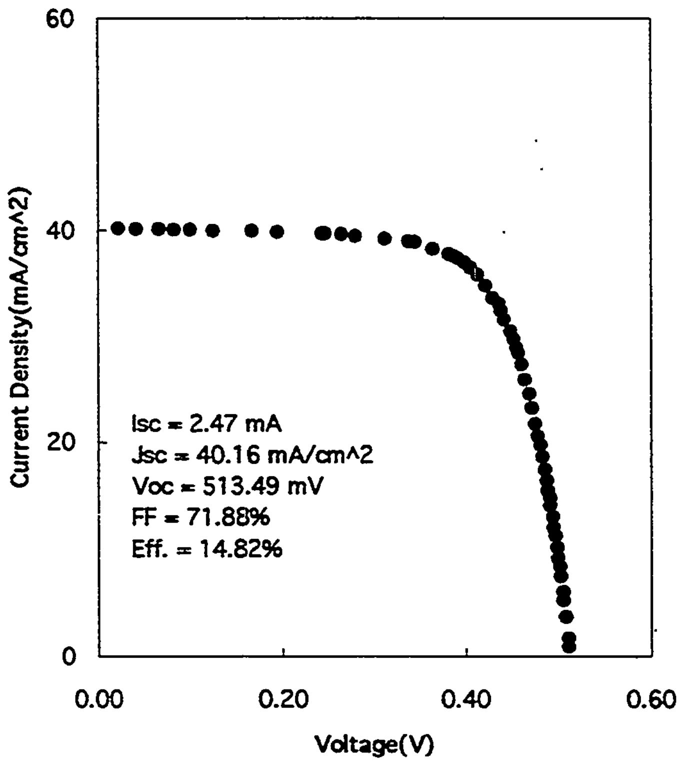


Figure 6. Illuminated characteristics for a test cell formed on graded absorber material (94ZC480).

Temperature dependent current-voltage (T-I-V) analyses have been conducted for numerous devices. The effect of depositing the ZnSe layer is apparent from results of the T-I-V analyses carried out for Al/CIS and Al/ZnSe/CIS structures. Dark I-V data taken at various temperatures for an Al/CIS device are plotted in Figure 7, and parameters determined by fitting the data are tabulated in Table 1. The Al/CIS device characteristics can be interpreted as being due to a single current mechanism. As discussed below, the current mechanism can be regarded as a being due to a tunneling mechanism. Typical dark characteristics for a Al/ZnSe/CIS structure are plotted in Figure 8, and fitting parameters are given in Table 2. As is always the case for Al/ZnSe/CIS devices, two current mechanisms are required to fit the T-I-V data. These results are discussed further below after a brief discussion is given concerning our approach to modeling I-V characteristics.

Table 1 – I-V Parameters For Al/CIS Device 94CIS002

$\phi = 0.155$ eV and $J_{00} = 9.40E-02$.

T(°C)	J_0(A/cm²)	n	B(1/eV)	R_s(Ω)	R_{sh}(Ω)
-30.0	6.99E-05	3.54	13.46	87.0	1.16E+05
-20.0	8.45E-05	3.36	13.64	72.3	1.14E+05
-10.0	1.12E-04	3.28	13.46	57.3	1.00E+05
0.0	1.00E-04	3.09	13.77	49.9	1.00E+05
10.0	1.43E-04	3.04	13.49	36.4	5.85E+06
20.0	1.67E-04	2.87	13.80	27.6	5.85E+06
30.0	2.38E-04	2.85	13.44	19.0	5.84E+06
40.0	3.22E-04	2.76	13.44	12.3	5.84E+06
50.0	3.94E-04	2.58	13.91	8.65	5.84E+06
60.0	5.29E-04	2.50	13.93	4.86	5.84E+06

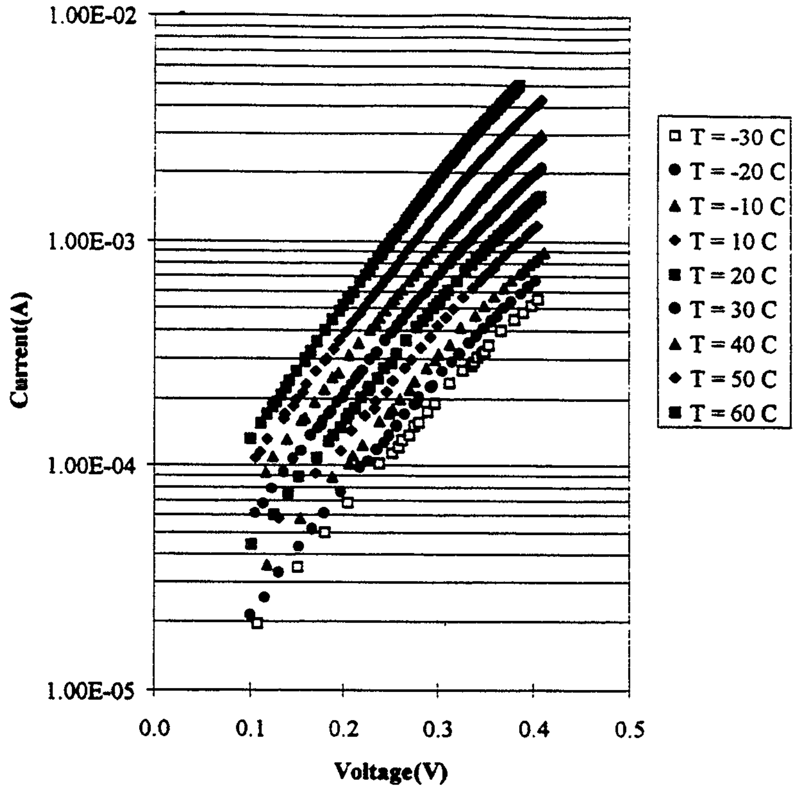


Figure 7. T-I-V data for Al/CIS Test Device 94CIS002.

Table 2 -- I-V Parameters For Al/ZnSe/CIS Device 94ZC436

$\phi_1 = 0.198$ eV and $J_{00,1} = 0.688$. $\phi_2 = 0.405$ eV and $J_{00,2} = 0.654$.

T(°C)	J_{01}(A/cm²)	B_1(1/eV)	J_{02}(A/cm²)	n_2	B_2(1/eV)	R_s(Ω)	R_{sh}(Ω)
-30	5.05E-05	6.42	2.54E-09	1.94	24.57	12.5	1.92E+05
-20	8.68E-05	5.65	7.90E-09	1.92	23.85	9.71	1.26E+05
-10	1.16E-04	5.59	1.03E-08	1.82	24.33	7.86	2.93E+05
0	1.47E-04	5.54	1.59E-08	1.72	24.76	8.17	1.37E+05
10	1.96E-04	5.51	1.26E-08	1.55	26.48	8.26	1.16E+05
20	2.16E-04	5.93	9.60E-09	1.40	28.37	8.74	6.30E+04
30	2.10E-04	5.82	4.21E-09	1.21	31.69	10.1	2.37E+04
40	4.78E-04	4.93	1.68E-07	1.49	25.03	5.91	2.75E+04
50	5.95E-04	5.03	4.08E-07	1.49	24.09	1.68	1.86E+04

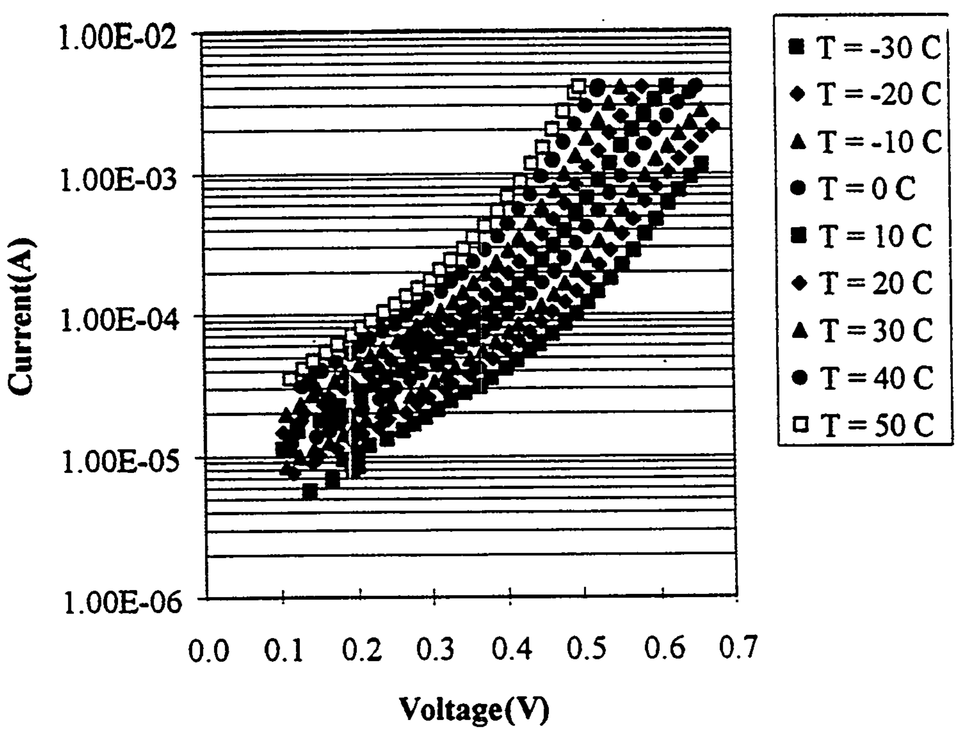


Figure 8. T-I-V data for Al/ZnSe/CIS Test Device 94ZC436.

In general, we assume the dark I-V characteristics can be interpreted in terms of

$$I_j = I_1 + I_2$$

where

$$I_1 = I_{01}\,[\exp(B_1 V_j) - 1]$$

$$I_2 = I_{02}\exp(B_2 V_j) \quad , \qquad V_j >> n_2 kT$$

$$B_1 = (A_1 / kT)$$

$$B_2 = (A_2 / kT)$$

$$V_j = V - R_s I = \text{Voltage Across Junction}$$

$$I_j = I - V_j/R_{sh}$$

$$R_s = \text{Lumped Series Resistance}$$

$$R_{sh} = \text{Lumped Shunt Resistance}$$

It should be noted that the B-parameters may be temperature-independent, and in that case it is not appropriate to relate B_i to A_i, where $i = 1$ or 2.

The data for the two types of devices were fit in terms of the above model using a computer aided analysis. The procedure utilized to fit I-V data is discussed in Reference 7. As noted above, the characteristics for the Al/CIS device can be understood quite well in terms of a single mechanism. Referring to Table 1, the B-factor is essentially independent of temperature. Current due to multiple step tunneling leads to such a behavior [8}. If the Al/CIS device were an ideal Schottky barrier, the B-factor would be given by 1/kT (which is temperature dependent) and the J_o-value would be on the order of 10^{-6} A/cm^2. Thus, either the Al/CIS structure is a Schottky barrier dominated by tunneling or must be interpreted in terms of a different physical model. If the Siemens substrates have a n-type surface layer, then the proper model for an Al/CIS device would consist of a buried heterojunction below the CIS surface. All we can determine from the I-V analysis is that the dominant current mechanism in Al/CIS structures appears to be a tunneling mechanism.

I-V characteristics of ZnSe/CIS structures always exhibit two current mechanisms, one dominant at low voltages (0.1 to 0.4 Volts) and one at higher voltages (0.4 to 0.6 Volts). The low voltage mechanism appears to be due to tunneling since usually the B-factor is fairly independent of temperature. The tunneling current component at low voltages in the ZnSe/CIS devices is always less in magnitude than the tunneling current which dominates the Al/CIS structures. The J_{o1} - value for the tunneling components are approximately the same, but the B-value for a typical Al/CIS device is much larger than the corresponding parameter for a ZnSe/CIS structure. The J_{o1} - values being similar suggests that the same activation energy is involved for both structures. Assuming a tunneling mechanism, the B-value is inversely proportional to the number of tunneling steps required for a multiple step tunneling process. These results are therefore consistent with the average distance traveled in the individual tunneling steps being longer in the case of ZnSe/CIS devices. Thus, a possible explanation of the reduced value of B in the Al/ZnSe/CIS structures relative to Al/CIS devices is that the layer of ZnSe, the process of growing ZnSe or a combination thereof results in passivation of electronic levels that act as tunneling sites.

Identification of the large-voltage current mechanism is not straight forward for this particular device. Both the A-factor and B-factor exhibit a slight temperature dependence. Since the A-factor is on the order of 1.5, it seems reasonable to assume that the dominant current loss is due to space charge recombination. However, a tunneling/recombination model may be more appropriate in this case [9]. The values for J_{o2} and A_2 for 94ZC436 are similar to those reported for efficient CIS solar cells using CdS windows. In general, we find that T-I-V analyses conducted for Al/ZnSe/CIS test cells indicate that the ZnSe buffer layer suppresses the tunneling currents dominant in the Al/CIS structures.

4. PHOTOLUMINESCENCE STUDIES

Dr. Fuad Abulfotuh has carried out photoluminescence studies of samples in an effort to characterize the surface of Siemens substrates. Two types of samples were examined, namely, a CIS substrate that had been cleaned and etched, and a ZnSe/CIS device structure (94ZC439). To examine the surface of the CIS substrate, PL emission spectra were taken using low angles of incidence with respect to the plane of the interface, that is, the CIS surface for the bare sample and the ZnSe-CIS interface for Sample 94ZC439. Figure 9 shows a PL emission spectrum taken at a low angle of incidence with respect to the plane of the interface on Sample 94ZC439. This PL spectrum due to emission from the top surface CIS layer is dominated by three emissions of 1.26 eV, 1.22 eV and 1.15 eV. Low energy emission from a deeper point (measured at a slightly larger angle) shows the typical emission from a bulk CIS film which is attributed mainly to donor-acceptor recombinations. PL spectra obtained for bare Siemens CIS substrates have also established that a segregated phase or phases exist at the substrate surfaces. Thus, we conclude that a segregated phase(s) exists on as received Siemens CIS material, and after deposition of ZnSe. The PL studies do not

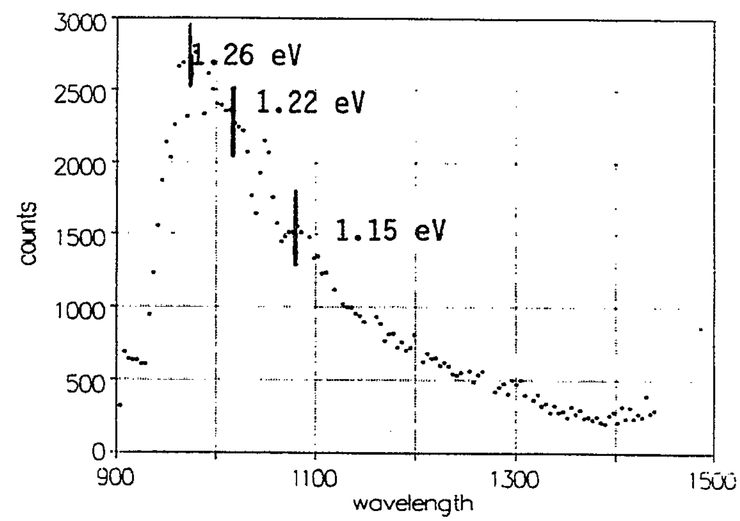


Figure 9. PL emission for ZnSe/CIS structure taken a low angle and at room temperature.

determine whether the surface layer is n-type or p-type. However, based on results obtained by the EUROCIS group, it seems very likely that a n/p heterojunction exists at the surface of as-received Siemens CIS substrates. If this were the case, one might assume that deposition of ZnSe leads to passivation of active tunneling sites which exist in the depletion region of the buried heterojunction.

5. SOLAR CELLS BASED ON THE ZnSe/CIS JUNCTION

Our approach to developing ZnSe/CIS cells has included plans to grow ZnO by MOCVD. In particular, it was planned to grow ZnO by reacting tetrahydrofuran (THF) and a zinc adduct. Since THF and the zinc adduct are two large molecules, parasitic reactions at the substrate surface should be minimized. A layer of ZnO was grown onto a ZnSe/CIS structure at 350°C early in the program, which resulted in encouraging results. Shortly after this experiment, some components in the THF delivery system failed. This system has been rebuilt recently and will be placed into operation in the near future.

While the THF delivery system was being rebuilt, several ZnSe/CIS structures were sent to various laboratories for ZnO deposition -- usually by RF sputtering. In all cases, the ZnO deposition process resulted in inflected I-V curves, or shorted cells. Thus, the results achieved with MOCVD growth of ZnO are very significant, and may lead the way for non-cadmium buffer layers to be possible.

In addition to sending ZnSe/CIS structures to other laboratories for ZnO deposition, another approach was utilized for investigating the properties of solar cells based on ZnSe/CIS structures. Solar cells were fabricated with a CdS protective layer, that is, a ZnO/CdS/ZnSe/CIS configuration. After growing ZnSe layers, several hundred Å of CdS were grown by CBD. The structure was then sent to Siemens Solar for deposition of highly conducting ZnO. Although these cells receive an extraordinary amount of handling, reasonable efficiencies have been achieved. Figure 10

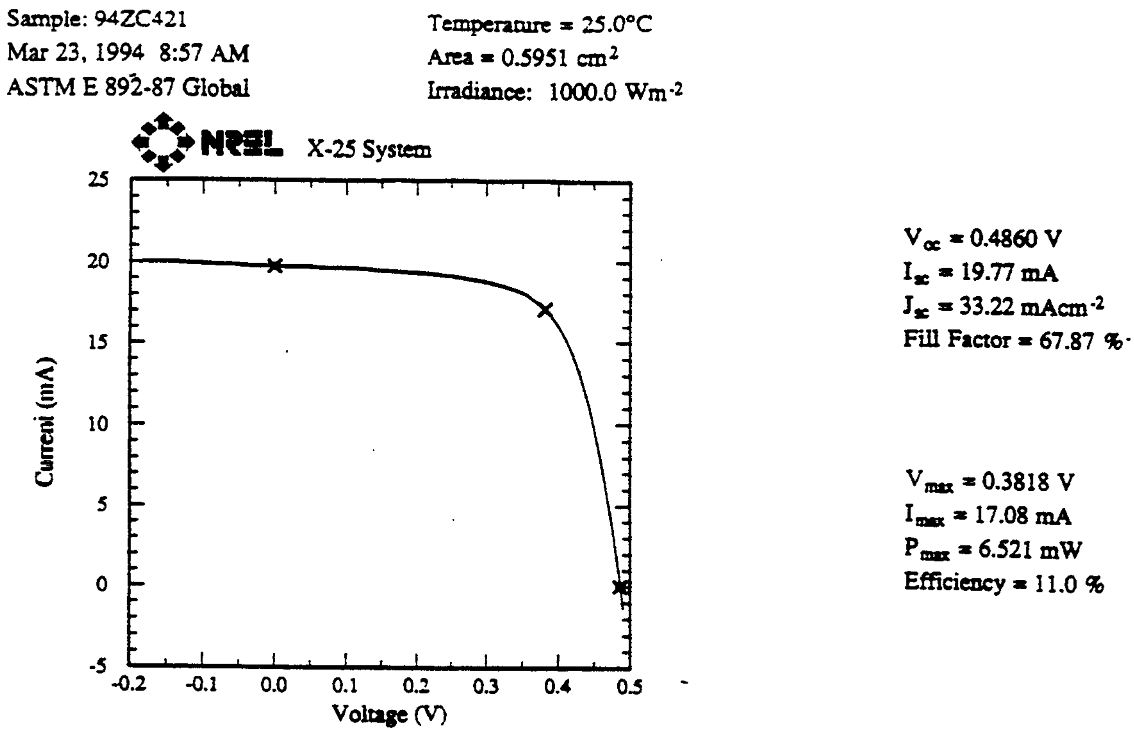


Figure 10. Illuminated I-V characteristics measured by NREL for a 0.6 cm^2 ZnSe/CIS solar cell with a ZnO top contact layer and a CdS protective layer between the ZnSe and ZnO layers.

shows illuminated characteristics of such a cell as measured by NREL. The total area efficiency is 11% and the active area efficiency is > 12%. I-V characteristics of test cells measured before and after CdS deposition were essentially identical. Although this result is not for an actual non-cadmium structure, it demonstrates the potential of achieving efficient ZnSe/CIS solar cells.

6. CONCLUSIONS AND FUTURE WORK

Some of the key results of this past year effort are: (1) MOCVD deposition of ZnSe onto Siemens CIS material results in Al/ZnSe/CIS test devices with greatly improved I-V characteristics relative to Al/CIS test cells; (2) ZnSe can act as an effective window (or buffer) layer in a non-cadmium

CIS solar cell if an approach for depositing a top contact layer of ZnO can be developed that does not degrade the properties of the ZnSe/CIS structure; (3) the optimum ZnSe film thickness for an efficient ZnSe/CIS solar cell is in the range of 100Å to 200 Å (as measured on a silicon witness). Future work will concentrate on fabricating complete Cd-free solar cells based on a ZnSe window layer. A major part of this study will involve investigations of the effects of MOCVD grown ZnO on the properties of ZnSe/CIS solar cells.

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L. C. Olsen

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Washington State University at Tri-Cities
100 Sprout Road
Richland, WA 99352

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13. ABSTRACT *(Maximum 200 words)*

This report describes studies of $CuInSe_2$ (CIS) solar cells based on ZnSe window layers. ZnSe/CIS devices are fabricated by growing ZnSe films by metal-organic chemical vapor deposition (MOCVD) onto Siemens CIS and graded absorber substrates. ZnSe films are grown by reacting H_2Se with a zinc adduct. ZnSe/CIS heterojunctions have been studied by depositing transparent aluminum contacts onto ZnSe. These studies indicate that ZnSe/CIS solar cells can be fabricated with an efficiency greater than 14%. Open-circuit voltages are typically higher than 500 mV, and the optimum range of ZnSe film thickness for maximum efficiency is between 100 and 250 Å. Photocurrents are significantly reduced as the film thickness exceeds 250 Å. Photoluminescence spectroscopy has been used to characterize the physical nature of CIS substrate surfaces and ZnSe/CIS interfaces. These studies indicate that one or more segregated phase exists at the surface of as-received Siemens substrates. Additionally, it is determined that the segregated phase(s) still exists after the ZnSe growth process. To date, sputtered ZnO top contact layers have caused degradation of the photovoltaic properties of the ZnSe/CIS structure. Investigations of the effects of MOCVD-grown ZnO upon ZnSe/CIS structures will soon be started. To establish the feasibility of Zn/Se as a window layer, cells were fabricated by incorporating a protective layer of CdS between the ZnSe and ZnO. A total-area efficiency of 11% was obtained with such a structure.

14. SUBJECT TERMS

polycrystalline thin films ; copper indium diselenide ; zinc selenide ; photovoltaics ; solar cells

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