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Final Report: High-Efficiency One-Sun Photovoltaic Module Demonstration Using Solar-Grade Cz Silicon

James M. Gee

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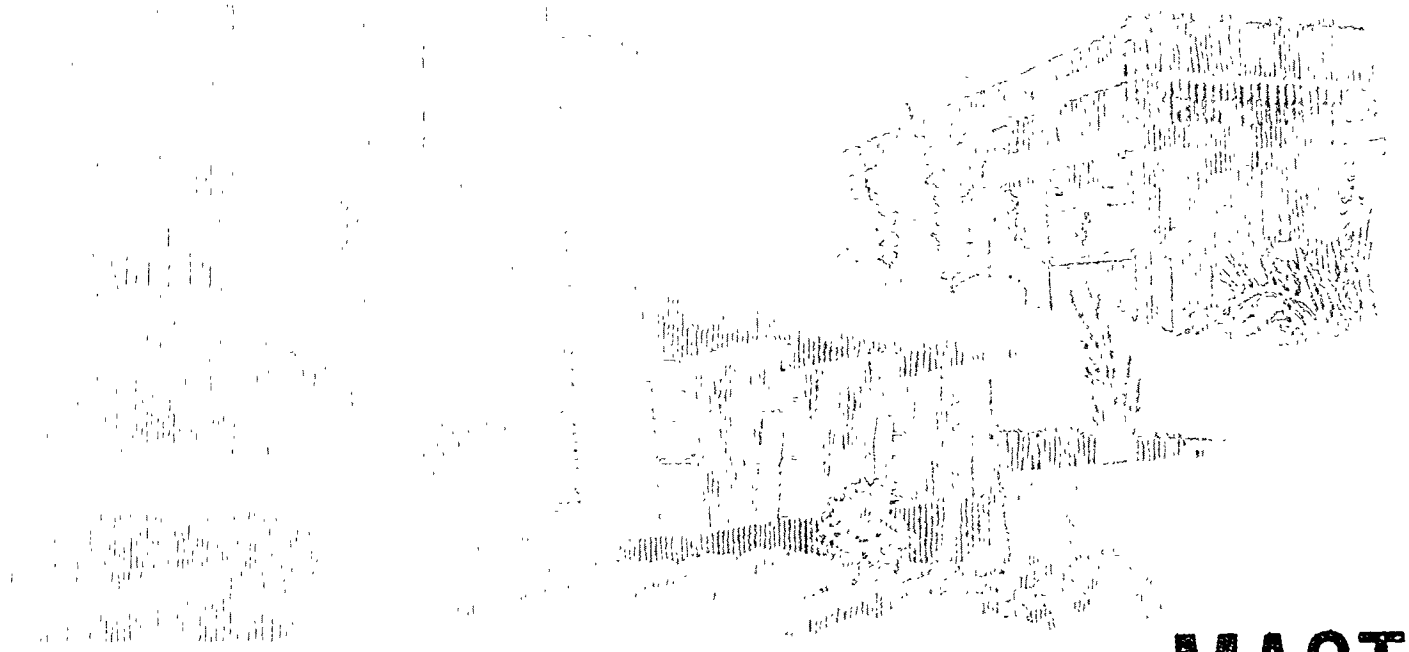

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FINAL REPORT

HIGH-EFFICIENCY ONE-SUN PHOTOVOLTAIC MODULE DEMONSTRATION USING SOLAR-GRADE CZ SILICON

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Final Report for CRADA #1248.

ABSTRACT

This work was performed jointly by Sandia National Laboratories (Albuquerque, NM) and Siemens Solar Industries (Camarillo, CA) under a Cooperative Research and Development Agreement (CRADA #1248). The work covers the period May 1994 to March 1996. The purpose of the work was to explore the performance potential of commercial, photovoltaic-grade Czochralski (Cz) silicon, and to demonstrate this potential through fabrication of high-efficiency cells and a module. Fabrication of the module was omitted in order to pursue further development of advanced device structures. The work included investigation of response of the material to various fabrication processes, development of advanced cell structures using the commercial material, and investigation of the stability of Cz silicon solar cells. Some important achievements of this work include the following: post-diffusion oxidations were found to be a possible source of material contamination; bulk lifetimes around 75 μs were achieved; efficiencies of 17.6% and 15.7% were achieved for large-area cells using advanced cell structures (back-surface fields and emitter wrap-through); and preliminary investigations into photodegradation in Cz silicon solar cells found that oxygen thermal donors might be involved. Efficiencies around 20% should be possible with commercial, photovoltaic-grade silicon using properly optimized processes and device structures.

ACKNOWLEDGMENTS

The author would like to acknowledge the contributions of Dr. Richard R. King and Dr. Kim W. Mitchell of Siemens Solar Industries. They provided much guidance to this work through many detailed discussions, and Dr. Richard King provided many suggestions for and/or helped design specific experiments in this project. The author would also like to acknowledge many useful discussions with other staff in photovoltaic research at Sandia, including Douglas S. Ruby, W. Kent Schubert, and David L. King. Kent Schubert provided some unpublished data on gettering, and David King provided much of the data and text for section 4.1 on photodegradation in commercial Cz cells and modules. The device fabrication in the Photovoltaic Device Fabrication Laboratory at Sandia was ably performed by M. Elaine Buck, Beverly L. Silva, and Jeffrey W. Tingley, and device measurements in the Photovoltaic Device Measurements Laboratory at Sandia were ably performed by J. Kurt Snyder, Lloyd W. Irwin, and Barry R. Hansen. This work was performed by Sandia National Laboratories for the United States Department of Energy under contract DE-AC04-94AL85000.

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EXECUTIVE SUMMARY

Requirements for high efficiencies are now well established for crystalline-silicon (c-Si) solar cells. High-efficiency c-Si cells feature long injected-carrier lifetimes and well-passivated surfaces in order to minimize intrinsic loss mechanisms -- i.e., maximize internal collection efficiency and minimize recombination losses. High-efficiency c-Si cells also feature sophisticated grids and antireflection coatings to minimize extrinsic loss mechanisms (series resistance and reflectance). Efficiencies of 24% and 21% have been demonstrated in laboratory-scale 4-cm^2 cells with float-zone-refined (FZ) c-Si substrates and with high-purity Czochralski (Cz) c-Si substrates, respectively. These cells used sophisticated device structures that required multiple high-temperature process steps for the device fabrication, and have long bulk lifetimes due to the use of high-quality processing and high-purity c-Si substrates. In contrast to the high-efficiency laboratory cells, commercial solar cells have efficiencies between 10 and 15% due to use of high-throughput processing and less-than-optimal materials. The photovoltaic industry uses c-Si substrates ("photovoltaic-grade") with possibly higher metallic impurity concentrations, higher oxygen and/or carbon concentrations, or higher microdefect densities due to use of higher crystal growth rates and low-cost silicon feedstock. These materials require a new process optimization compared to more-optimal materials to fully determine their performance potential.

The purpose of the present project was to explore the performance potential of commercial, photovoltaic-grade single-crystal silicon grown by the Cz method, and to demonstrate this potential through fabrication of high-efficiency cells and a module. The results of this work is expected to provide guidelines for improving commercial c-Si solar cell performance. This work was performed jointly by Sandia National Laboratories (Albuquerque, NM) and Siemens Solar Industries (Camarillo, CA) under a Cooperative Research and Development Agreement (CRADA #1248). The work covers the period May 1994 to March 1996.

The study included optimization of the fabrication process to maintain and/or upgrade (e.g., gettering) the bulk lifetime, development of advanced device structures, and some preliminary investigations of the stability of Cz-silicon solar cells. The photovoltaic-grade Cz silicon was from a commercial c-Si fabrication line (Siemens Solar Industries -- SSI) that is the world's largest photovoltaic manufacturing plant; the material was not specially selected for this project. Some important achievements of this work include the following:

- effect of phosphorus diffusions, oxidations, and aluminum alloys on bulk lifetime was investigated;
- bulk lifetimes around 75 μs were achieved;
- efficiencies of 17.6% and 15.7% were achieved for large-area cells using advanced cell structures (back-surface fields and emitter wrap-through;
- photodegradation of c-Si Cz modules of between 2 and 5% was found, and preliminary investigations of photodegradation in Cz silicon solar cells found that oxygen thermal donors might be involved;
- detailed modeling based on the present work project efficiencies around 20% with commercial, photovoltaic-grade silicon using properly optimized processes and device structures.

1.0 INTRODUCTION

Requirements for high efficiencies are now well established for crystalline-silicon (c-Si) solar cells. High-efficiency c-Si cells feature long injected-carrier lifetimes and well-passivated surfaces in order to minimize intrinsic loss mechanisms -- i.e., maximize internal collection efficiency and minimize recombination losses. High-efficiency c-Si cells also feature sophisticated grids and antireflection coatings to minimize extrinsic loss mechanisms (series resistance and reflectance). Efficiencies of 24% and 21% have been demonstrated in laboratory-scale 4-cm^2 cells with float-zone-refined (FZ) c-Si substrates and with high-purity Czochralski (Cz) c-Si substrates, respectively [1,2]. These cells used sophisticated device structures that required multiple high-temperature process steps for the device fabrication, and have long bulk lifetimes due to the use of high-quality processing and high-purity c-Si substrates.

In contrast to the integrated-circuit industry, the photovoltaic industry typically uses c-Si substrates ("photovoltaic-grade") with possibly higher metallic impurity concentrations, higher oxygen and/or carbon concentrations, or higher microdefect densities due to use of higher crystal growth rates and low-cost silicon feedstock. For example, crystallographic defects are believed responsible for low-lifetime regions in multicrystalline-silicon (mc-Si) substrates, while high-lifetime regions are limited by Fe-related recombination sites [3]. Similarly, recombination that is possibly related to FeB pairs has been recently implicated in photon degradation in Cz c-Si solar cells [4]. In our experience, the bulk lifetime of photovoltaic-grade c-Si is more easily degraded with thermal processing, and some photovoltaic-grade c-Si materials degrade continuously with multiple high-temperature furnace steps [5]. On the other hand, Czochralski (Cz) silicon substrates used for ULSI integrated-circuit fabrication have such low concentrations of metallic impurities that residual recombination is due to intrinsic oxygen-related recombination centers [6]. The net result is that process optimization may be different for photovoltaic-grade c-Si materials than for more ideal c-Si materials. As an example of process optimization using commercial c-Si materials, we recently reported on development of high-efficiency cells using low-oxygen mc-Si substrates grown by the Heat Exchanger Method™ (HEM); this work culminated in the demonstration of a world-record 15%-efficient mc-Si module [7].

The purpose of the present work was to explore the performance potential of commercial, photovoltaic-grade single-crystal silicon grown by the Cz method. The study included optimization of the fabrication process to maintain and/or upgrade (e.g., gettering) the bulk lifetime, development of advanced device structures, and some preliminary investigations of the stability of Cz-silicon solar cells. Most of the work was performed at Sandia National Laboratories in a Class 100 cleanroom facility (Photovoltaic Device Fabrication Laboratory -- PDFL) with high-purity chemicals and tightly controlled processing. This portion of the work used evaporated metallization and antireflection coating technologies in order to minimize extrinsic loss mechanisms. The cells were characterized in a world-class photovoltaic measurements laboratory (Photovoltaic Device Measurements Laboratory -- PDML). Work on advanced back-surface structures was also performed at Siemens Solar Industries using commercial manufacturing processes (screen-printed metallizations, etc.) [8]. The photovoltaic-grade Cz silicon was from a commercial c-Si fabrication line (Siemens Solar Industries -- SSI) that is the world's largest photovoltaic manufacturing plant; the material was not specially selected for this project. This material is p-type (boron) with a bulk resistivity around 1 Ωcm, has an interstitial oxygen concentration around 30 pmma (ASTM F121-80), uses a variety of non-prime polysilicon feedstocks, and is grown with a diameter of 5.3 inches.

The work is reported in three chapters: Material Evaluation; Advanced Device Development; and Cz-Silicon Cell Stability. The last chapter -- Conclusions -- presents some suggestions for further

work and projections on the ultimate performance available with photovoltaic-grade Cz silicon. The appendices include representative runsheets that describe the process details for fabrication of high-efficiency cells, and two publications resulting from this work. Table 1 presents a summary of all the experiments performed in the PDFL related to this project. Many experiments are referenced in this report by the PDFL lot name. This report also includes selected results from related projects and/or prior work at Sandia.

Table 1. Summary of experiments performed in the PDFL using SSI Cz material and/or related to the SSI CRADA project. *Start* and *Finish* refers to the start and finish dates of the experiment, and *Hours* refers to the number of PDFL-process hours in the experiment.

Lot Name	Start	Finish	Hours	Description
SSI-41	5/27/94	7/1/94	9	PCD and Joe measurements for R. King, SSI.
SSI-42	7/6/94	7/8/94	16.3	BSF cells w/ Al-alloy at SSI.
SSI-43	7/22/94	8/4/94	33.5	New material & Al- and boron-BSF cells.
SSI-44	8/5/94	8/26/94	38	Emitter passivation exp w/ SSI - group A.
SSI-45	8/5/94	8/26/94	29.7	Passivated emitter exp w/ SSI; Group B.
SSI-46	8/5/94	9/20/94	29.4	Emitter passivation experiment w/SSI; Group C.
SSI-42A	8/24/94	9/16/94	25.9	Completion of Al-alloy experiment w/ SSI.
SSI-44a	9/2/94	9/8/94	2.1	Forming gas anneal of SSI-44 cells.
SSI-47	9/12/94	10/24/94	29.4	Emitter passivation experiment w/ SSI; Group L.
SSI-45a	9/15/94	10/2/94	2.8	Test SSI-45 cells.
SSI-48	10/4/94	10/13/94	1.8	BSG depositions for SSI - rounds.
SSI-49	10/4/94	10/13/94	9.6	BSG depositions for SSI - square samples.
SSI-50	10/25/94	11/14/94	38.5	Boron-diffused BSF cells on SSI Cz.
SSI-51	11/8/94	12/23/94	44.6	Thin large-area boron-BSF SSI-Cz cells.
SSI-53	11/14/94	11/15/94	4	PCD on boron-diffused SSI samples.
SSI-53a	11/15/94	11/15/94	1.3	PCD on boron-diffused SSI samples.
SSI-52	11/17/94	11/23/94	18.1	PCD lifetime study of SSI material.
SSI-55	1/5/95	1/23/95	30.7	SSI-Cz cells w/ SSI diffusion.
SSI-56	1/16/95	2/15/95	98.3	Al-alloy main-effects experiment.
SSI-57	2/21/95	3/15/95	43.6	Optimized Al-BSF SSI-Cz cells.
SSI-54	2/28/95	3/8/95	20.8	PCD lifetime study of B&P diffusion.
SSI-58	3/14/95	3/22/95	12.7	PCD lifetime study.
SSI-59	3/24/95	4/3/95	12.7	PCD lifetime of planar/textured surfaces.
CzStbl-2	4/11/95	4/25/95	37.3	Oxygen thermal donors and Cz stability.
SSI-60	4/20/95	5/30/95	68	Main-effects experiment on bulk lifetime.
SSI-61	6/1/95	7/21/95	71	B/Al-alloy main-effects experiment
SSI-62	7/20/95	7/26/95	2.5	Provide BSG and SiO2 CVD films, FZ wafers.
SSI-63	7/31/95	11/1/95	40.6	Compare Al and Al/B (thru BSG) LA2 cells.
SSI-64	8/15/95	11/2/95	42.2	Compare Al and Al/B (B-doped Al) LA2 cells.
SSI-65	9/14/95	9/24/95	51	LAPERC and LAPERF SSI-Cz cells.
SSI-66	10/9/95		48.8	LAPERC and LAPERF SSI-Cz cells.
SSI-67	11/27/95		22.1	LAPERF lifetime study.
SSI-68	11/27/95		46.9	Boron-BSF SSI-Cz and 2-ohm*cm FZ cells.
SSI-69	1/3/96	1/4/96	1.7	PCD study of photon degradation.
LAPERF11	2/9/96	3/21/96	46.6	LAPERF and EWT cells on SSI-Cz
SSI-70	3/12/96		34.4	Cells on SSI-diffused SSI-Cz substrates.

2.0 MATERIAL EVALUATION

The first part of our study examined process optimization to maintain and/or upgrade bulk lifetimes. Development of new processes (aluminum alloy, boron diffusion, oxidation, etc.) for advanced device structures is discussed in the next chapter (Advanced Device Development). Material evaluation generally involves either measurement of an effective lifetime for minority carriers by microwave-detected photoconductance decay (PCD) or, in some cases, fabrication of cells and evaluation of bulk recombination properties through analysis of spectral data.

2.1 Material Evaluation

All c-Si solar cells presently use at least one high-temperature (>800°C) step subsequent to the crystal growth -- a phosphorus diffusion. The first experiment evaluated the bulk lifetime of photovoltaic-grade Cz silicon as a function of phosphorus-diffusion temperature (Fig.1). This evaluation used PCD to measure the effective lifetime of phosphorus-diffused samples. The phosphorus diffusion parameters for each temperature were selected to yield similar diffusion profiles that are also typical of high-efficiency cells (i.e., a sheet resistance around 100 Ω/□ and surface concentration less than 10^{20} cm^{-3}). These phosphorus diffusions also provide excellent surface passivation (estimated surface recombination velocity less than 300 cm/s), so that the effective PCD lifetime is a good indication of bulk lifetime. This evaluation is performed on each new set of SSI Cz silicon slices received at Sandia, so the experiment was performed on materials from a variety of ingots and over a span of several years.

The experiment found a distinct preference for lower diffusion temperatures, with a peak PCD lifetime around 30 μs for 850°C diffused samples. The effective lifetime measured by PCD is a well known function of the surface and bulk recombination parameters. Due to the similarity in surface passivations for the different diffusion conditions, the degradation in PCD lifetime with higher phosphorus diffusion temperature is primarily due to degradation in the bulk lifetime. In addition, the surface recombination velocity can be estimated from the measured bulk resistivity and the measured emitter saturation current density (J_{oe}). J_{oe} is measured independently on intrinsic FZ wafers, and is between 100 and 300 fA/cm^2. The net result is that the bulk lifetime can be estimated from the effective PCD lifetime. The effective PCD lifetime of 30 μs corresponds to an estimated bulk lifetime between 50 and 100 μs, which agrees with an independent measurement of 75 μs by Rohatgi [9]. Subsequent to the present work, Dr. Richard King of Siemens Solar Industries suggested an experiment to examine the effect of much higher diffusion temperatures on lifetime.

2.2 Diffusion Optimization and Gettering

Experiment *SSI-60* systematically examined the effect of various phosphorus-diffusion and material- preparation parameters on the bulk lifetime using a statistically based, experimental design. The PDFL $POCl_3$ diffusion process consists of a phosphorus-glass deposition step, an inert soak, and an oxygen soak; a wide variety of diffusion profiles can be obtained with this $POCl_3$ diffusion process [10]. The experiment examined the effect of six different parameters (material, anisotropic (i.e., texture) etch time, isotropic etch time, inert soak time, oxygen soak time, and diffusion temperature) on PCD lifetime and on finished cell parameters (effective diffusion length -- L_{eff}, V_{oc}, J_{sc}, FF, and η). The most significant factors for PCD lifetime and cell performance were associated with the phosphorus diffusion; lower diffusion temperature, longer

inert soaks, and shorter oxygen soaks were preferred for longer lifetime and better cell performance (Fig. 2).

One important observation from *SSI-60* for commercial production cells is that textured and planar surfaces produce similar bulk lifetimes. A second important observation concerns the trends of lifetime with the phosphorus diffusion parameters. These trends suggest that the lifetime is improved due to gettering during the inert soak while there is further phosphorus diffusion, but is degraded when the phosphorus diffusion is ceased during the oxygen soak. Similar results were found in other experiments using phosphorus diffusions performed at other institutions with very different processes. In these experiments, significant lifetime degradation was observed due to high-temperature oxidations subsequent to the phosphorus diffusion [11]. The results from these experiments collectively suggest that metallic impurities gettered by the phosphorus diffusion are re-released during a subsequent oxidation. This observation is potentially very important because there are several steps with temperatures above 700°C after the phosphorus diffusion in most commercial fabrication sequences. On the other hand, no degradation of lifetime was observed at process temperatures up to 1000°C if the subsequent high-temperature step had aluminum present (see Advanced Device Development).

Knobloch *et al.* report that the temperature ramp rates are important parameters for processing Cz silicon [2]. An experiment (*SSIPush1*) was therefore performed to examine temperature ramp rate effects on SSI Cz silicon. The largest change in temperature occurs during the insertion (push) or removal (pull) of the wafers from the furnace, so the experiment examined the effect of several push/pull temperatures and boat insertion rates on the bulk diffusion length and on the performance of cells using photovoltaic-grade Cz silicon (Fig. 3). The low-temperature push with slow ramp rate produced the lowest PCD lifetime and lowest cell performance. The preference for a high push/pull temperature and rapid ramp rates agrees with previous studies using high-oxygen-content silicon, and is believed to be related to the kinetics of oxygen precipitation and/or agglomeration. All work reported in this project used a push/pull temperature of 800°C and temperature ramp rates of 5°C per minute.

Most high-efficiency laboratory cells use several high-temperature steps in their fabrication sequence, while some c-Si materials are sensitive to multiple thermal steps [5]. A relatively low-temperature oxidation (800°C, 30 minutes) is used prior to a phosphorus diffusion in some PDFL process sequences for advanced device structures. Experiment *SSI-67* examined the effect of a pre-diffusion oxidation on PCD lifetime with three different diffusion temperatures (Fig. 4). Similar to our previous studies, the lower diffusion temperature (850°C) produced higher PCD lifetimes compared to the higher diffusion temperatures. Of more interest, however, is the observation that the pre-diffusion oxidation also degraded lifetimes at the higher diffusion temperatures, but had no affect on PCD lifetime for phosphorus diffusions performed at 850°C. The samples were from the same ingot and processed together, so extrinsic sources (e.g., metallic contamination) are not believed to be the cause the lifetime degradation. Similar to the ramp rate study, the degradation in bulk lifetime due to the higher diffusion temperature and the pre-diffusion oxidation is believed to be related to the kinetics of oxygen precipitation

A parallel project at Sandia is investigating several gettering sequences with various c-Si materials. This study found that gettering sequences using aluminum and/or phosphorus improved the PCD lifetime nearly fourfold in SSI Cz material [12]. Cells were then fabricated with the

gettering sequence applied before the cell fabrication; i.e., the gettering (phosphorus diffusion and/or aluminum alloy) was performed, the gettering layer was removed, and then the cell was fabricated using the PDFL baseline sequence (phosphorus diffusion, metallization, and antireflection coating). A control split ("baseline") fabricated cells without the additional furnace steps required for the gettering. Cells with the gettering sequence had either lower or similar performance to the baseline cells (Fig. 5). The lower performance of the gettered cells is believed to be due to material degradation from the multiple thermal steps [12]. These observations suggest that gettering sequences should be implemented as a part of the cell fabrication sequence rather than as additional thermal steps for both cost and performance considerations.

2.3 Summary

Important observations concerning the SSI Cz material from this section include the following:

- Textured surfaces do not degrade bulk lifetime compared to planar surfaces.
- Lower phosphorus-diffusion temperatures are preferred due to degradation of bulk lifetime.
- High-temperature processes after the phosphorus diffusion can degrade lifetime through release of gettered impurities if no gettering agent is present during the step.
- Rapid ramp rates for and minimal number of high-temperature processes are preferred, which is believed to be related to oxygen precipitation.
- The bulk lifetime after an 850°C phosphorus diffusion is around 75 μs.

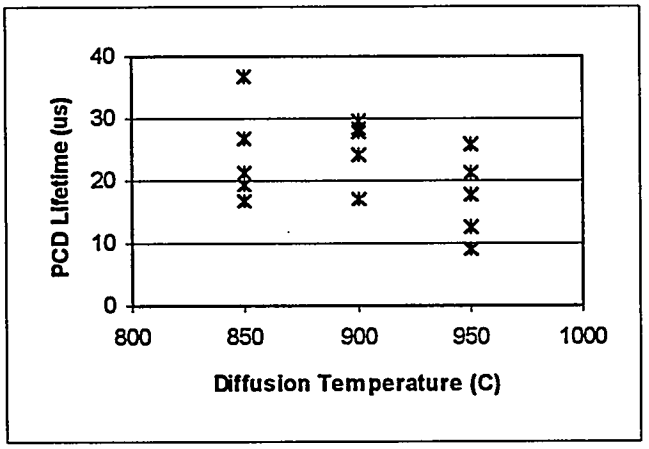

Figure 1. Effective lifetime of phosphorus-diffused samples as a function of diffusion temperature. The data includes experiments performed over a period of three years using material from several different ingots. Each data point represents average of 10 measurements.

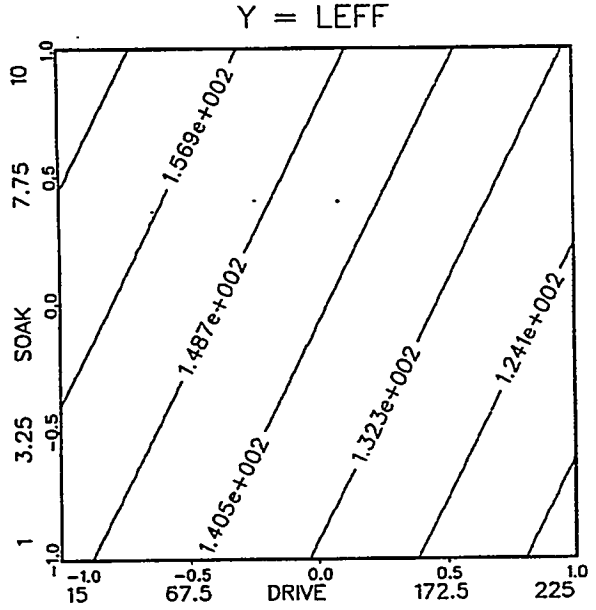

Figure 2. Sample of an experiment that examined the effect of seven different diffusion and surface preparation parameters on bulk lifetime using a statistical experimental design. *Soak* and *Drive* refer to inert and oxygen soak times (minutes) of $POCl_3$ diffusion process, respectively. Contours are the effective diffusion length (L_{eff}) in μm.

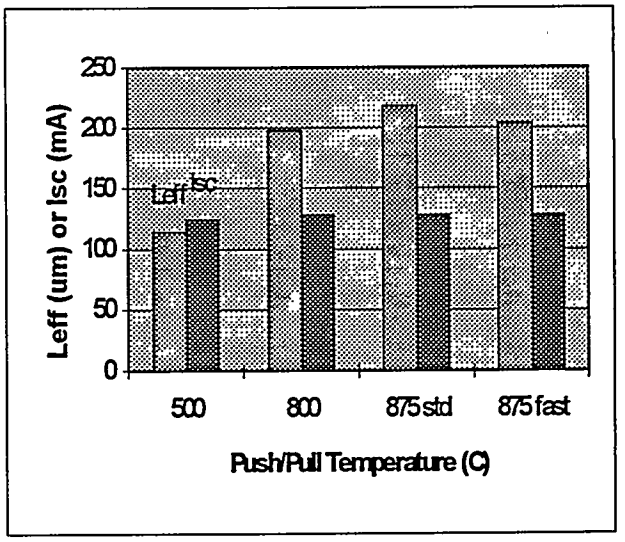

Figure 3. Effect of push/pull temperature on effective diffusion length and on I_{sc} of 4-cm^2 planar cells. *Std.* (standard) and *fast* refer to speed of wafer insertion.

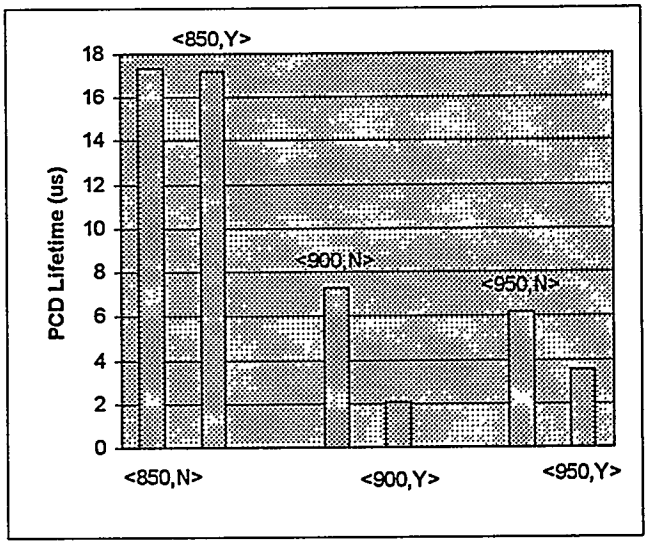

Figure 4. PCD lifetime of phosphorus-diffused SSI-Cz samples as a function of diffusion temperature and of an 800°C pre-diffusion oxidation (*Yes* or *No*).

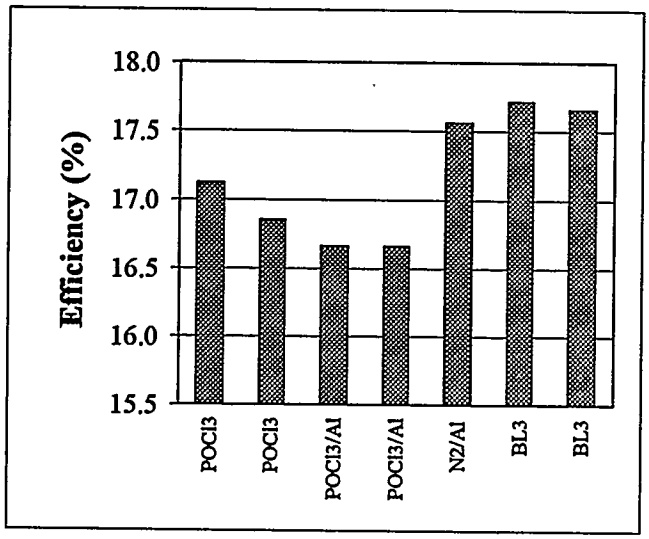

Figure 5. Efficiency of cells fabricated with various gettering sequences (phosphorus, phosphorus and aluminum, or aluminum only) and without the gettering sequence ("BL3").

3.0 ADVANCED DEVICE DEVELOPMENT

The two most important material parameters required for designing an optimized device are the bulk resistivity and bulk lifetime. The material evaluation task found a bulk lifetime between 50 and 100 μs (diffusion length between 400 and 600 μm). Complete cells using SSI Cz material were also analyzed in detail to determine distribution of recombination. The analysis used the spectral analysis technique described by Basore [13]. In an early experiment (*SSI-19*), cells were fabricated with two different thicknesses in order to facilitate analysis of the cell performance. Detailed analysis of the spectral and current-voltage data for these cells found a bulk lifetime around 36 μs (Fig. 6 and Table 2). The open-circuit voltage of these cells was limited by recombination in the base -- *approximately 80% of base recombination at open circuit was at the back surface for the thin (170 μm) cell*! The discrepancy between the bulk lifetime estimated from PCD measurements and from analysis of spectral data in complete cells is believed to be due to limitations in the spectral analysis method for materials with very long diffusion lengths [14]. The important point to note, however, is that these cells are largely limited by recombination at the back surface rather than in the bulk. Hence, performance improvements need to address improved passivation of the surfaces.

Although some work was performed on emitter passivation early in the project, the baseline PDFL cell sequence already uses a well-passivated emitter with low recombination losses. Hence, most of the work examined two high-efficiency cell concepts: thin cells with back-surface fields and emitter wrap-through cells. Back-surface field (BSF) cells have special structures on the rear surface to reduce back-surface recombination losses. This project examined both aluminum-alloyed and boron-diffused BSF's. Other low-recombination back-surface structures that might be of interest, but which the present project could not examine in detail, include thermal oxide passivation, passivation with a floating n^+ diffusion, amorphous silicon or polysilicon heterojunctions, and passivation with SiO_2 or Si_3N_4 deposited by low-temperature plasma-enhanced chemical vapor deposition. Some work in this task was also performed at Siemens Solar Industries with commercial cell fabrication processes, which was reported in a separate publication (see Appendix 3 [8]).

The emitter wrap-through (EWT) cell uses laser-drilled holes to wrap the emitter from the front surface through the holes to the back surface. The advantages of this approach include the following: (1) collection of carriers from the back surface to improve the internal collection efficiency of materials with short diffusion lengths; (2) performance advantages of back-contact cells due to no grid obscuration; and (3) module assembly advantages of back-contact cells [15].

3.1 Aluminum-Alloyed BSF Cells

Aluminum alloys are performed in the PDFL with evaporated aluminum films and furnace anneals. The furnace anneal typically uses an oxygen ambient during part of the furnace cycle to grow a thin oxide for passivation of the emitter. The aluminum alloy is performed after the phosphorus diffusion. The process is described more fully in [7], and full process details for a particular aluminum-BSF experiment are provided in Appendix 1.

An experiment (*SSI-56*) was performed to optimize the aluminum alloy process. The experiment examined several factors associated with aluminum alloys (aluminum thickness, alloy temperature, and alloy time), and used a statistically based, experimental design that included interaction terms.

This experiment considered long alloy times (up to 12 hours) and high alloy temperatures (up to 1000°C) because some high-efficiency laboratory cells use long, high-temperature alloys [16]. Aluminum thickness is believed to be an important parameter because the thickness of the aluminum-doped BSF is directly related to the initial thickness of the aluminum in the alloy process [17]. Representative results of the experiment are presented in Fig. 7.

All three factors (aluminum thickness, alloy time, and alloy temperature) were statistically significant, including all three linear terms and the interaction term associated with alloy time and temperature. The best cell performance used short, high-temperature (1000°C) alloys (Fig. 7). The excellent cell performance for cells processed at such high temperatures 1000°C suggests that aluminum alloys are quite benign on material properties, unlike phosphorus diffusions and oxidations where material degradation could be observed at temperatures as low as 900°C and 800°C, respectively.

There are two possible explanations for the wide process latitude of aluminum alloys compared to phosphorus diffusions and oxidations. The first hypothesis concerns metallic impurities. Aluminum alloys are believed to be extremely good sinks for gettering impurities, while oxidations do not have a sink for impurities and phosphorus diffusions have a limited capacity [18]. The second hypothesis concerns oxygen precipitation. Oxygen precipitates and their agglomerate precursors are very active recombination centers. Phosphorus diffusions and oxidations are believed to inject silicon self-interstitials that accelerate oxygen precipitation, while aluminum alloys are believed to inject vacancies that do not accelerate, and might even help inhibit, oxygen precipitation [19]. Further support for the second hypothesis is the observation that low-oxygen-content silicon, which should not be affected by oxygen precipitation, is more tolerant of high oxidation and phosphorus-diffusion temperatures than high-oxygen-content silicon.

The results of *SSI-56* and similar process optimization experiments were used to define a process for large-area (42 cm^2) cells with aluminum-alloyed BSF's. Experiments *SSI-51*, *SSI-57*, and *SSI-64* fabricated large-area, aluminum-alloyed cells with efficiencies up to 17.6% (Tables 3-5, Fig. 8). The repeatability of the process is demonstrated in the large number of cells with efficiencies above 17%. Experiment *SSI-57* also used very thin (220-μm) substrates. Unlike *SSI-56*, there was little difference in *SSI-57* cell performance between cells alloyed at 875°C and at 1000°C. The performance of the large-area cells was also very similar to typical wafer-average results for similarly processed moderate-area (4-cm^2) cells, which indictes that areal nonuniformities have only a small effect on large-area cell performance. The process for moderate-area cells is more process intensive due to an additional photolithography level to define the eight 4-cm^2 cells on the wafer. The best moderate-area cell performance was 18.3% for an aluminum-alloyed BSF cell (V_{oc} of 634 mV, J_{sc} of 35.9 mA/cm^2, and FF of 0.803).

The recombination properties of the aluminum-alloyed BSF's were estimated from the cells. There was little difference in performance between thick and thin cells with the aluminum-alloyed BSF, so the back-surface recombination velocity S must be approximately equal to the diffusion velocity. The diffusion velocity is equal to the minority-carrier diffusivity divided by the cell thickness (D/W), and is approximately 1500 and 1000 cm/s for 200- and 300-μm thick SSI-Cz cells, respectively. Analysis of the *SSI-57* cells found bulk lifetimes around 15 μs and S values around 2000 cm/s. As previously described, S may also be estimated from measured J_{oe}'s. J_{oe}'s are

difficult to measure for aluminum-alloyed junctions due to the difficulty in completely removing the metallic aluminum silicide. Nevertheless, measurements indicate a J_{oe} over 1 pA/cm^2, which corresponds to S values over about 1000 cm/s. Hence, the various device and material measurements collectively suggest S values on the order of 1000 cm/s for our aluminum-alloyed BSF's.

A collaborative experiment (*SSI-43*) was also performed with SSI to characterize aluminum alloys performed at SSI. This experiment used commercially available c-Si Cz and FZ wafers with various resistivities (0.4, 1, and 2 Ωcm), performed the aluminum alloy using an aluminum paste and fire sequence at SSI, and performed the rest of the device processing in the PDFL. The estimated S values from analysis of the spectral data were between 200 and 700 cm/s, which is an improvement over aluminum-alloyed junctions using evaporated aluminum and furnace anneals. The paste-aluminum process is expected to produce superior BSF's due to the thicker aluminum layer, and our measured range for S agrees with previously published results [17].

3.2 Boron-Diffused BSF Cells

The aluminum-BSF performance was not sufficient to improve the performance of thin cells. Boron-doped BSF's are expected to have lower recombination losses compared to aluminum-doped BSF's due to the higher doping concentrations achievable with boron. For example, J_{oe}'s of boron diffusions measured in the PDFL correspond to recombination velocities much less than 1000 cm/s (Fig. 9).

Two types of boron doping processes were considered. In the first process, a borosilicate glass (BSG) is deposited by atmospheric-pressure chemical vapor deposition (APCVD) on the back surface of the wafer, and the boron is driven into the silicon during the phosphorus diffusion. This "B/P-codiffusion" process requires only a single high-temperature furnace step to simultaneously diffuse both the phosphorus emitter and the boron BSF, although the diffusion temperature needs to be relatively high (>900°C) in order to obtain sufficient boron doping. The second process uses relatively low temperatures (<900°C) by alloying boron-doped aluminum. In the "B/Al-alloy" process, boron dopes silicon at boron's high solid solubility during the regrowth of silicon from the silicon-aluminum eutectic layer.

The first experiment (*SSI-43*) examined boron-doped BSF cells using the B/P-codiffusion process. This experiment used two diffusion temperatures: 875°C and 950°C. The high diffusion temperature is of interest because it should yield a more optimal boron-doped BSF, but is also suspected of degrading bulk lifetime (see Material Evaluation). The cell performance was limited by poor V_{oc} and I_{sc} due to poor diffusion lengths (Table 6); the effective diffusion lengths were less than 150 μm. Analysis of the spectral data found S values around 350 and 1300 cm/s for the 950°C and 875°C BSF's, respectively. Note that there are large uncertainties associated with these S values due to the short bulk diffusion lengths. Nevertheless, the 950°C diffusion produced a superior BSF as expected.

Additional experiments (*SSI-51* and *SSI-68*) fabricated large-area, boron-doped BSF cells with the B/P- codiffusion process. The cell performance was again limited by poor V_{oc} and I_{sc} due to poor diffusion lengths (Tables 3 and 7). *SSI-68* cells have a gridded back contact. The gridded back contact should improve the BSF due to surface passivation. The gridded contact also allows for rear spectral measurements, which is useful for analyzing base recombination properties S [20].

Analysis of the rear spectral data yielded inconclusive results, with S values between 100 and 1000 cm/s.

Several experiments (*SSI-53, -53a, and -54)* examined PCD lifetime of boron diffusions in SSI Cz material. *SSI-54* found acceptable PCD lifetimes (>15 μs) after either a boron diffusion, a phosphorus diffusion, or codiffusion of boron and phosphorus. However, separate high-temperature steps to diffuse the boron and phosphorus independently degraded the PCD lifetime to less than 10 μs. Most of our boron-doped BSF experiments used the B/P-codiffusion process, so the degradation in lifetime in the cell lots is not understood.

Two methods for doping aluminum with boron were considered for the B/Al-alloy process. In the first process, an aluminum film is evaporated over a BSG film and the Si-BSG-Al structure is then alloyed in a furnace. Mandelkorn *et al.* use a very similar process, and report additional passivation of the BSF in this particular process due to a heterojunction with the heavily doped, silicon-silicon dioxide matrix left after the eutectic freezeout [21]. Experiment *SSI-61* examined this process using a statistically based, experimental design. The factors included diborane flow rate during BSG deposition (0 and 0.5 slm), oxide thickness (10 and 100 nm), aluminum thickness (1 and 10 μm), alloy temperature (800 and 1000°C), and alloy time (0.5 and 12 hours). All the factors except oxide thickness were statistically significant (Fig. 10). Boron doping improved the factor-average efficiency by 0.9% absolute and the factor-average V_{oc} by 12 mV. While the trend with boron doping was promising, all the cells have lower performance compared to cells that have aluminum-alloyed BSF's without the intervening oxide layer. A subsequent experiment (*SSI-63*) used the optimized B/Al-alloy process from *SSI-61* to fabricate large-area cells. The performance of these cells was limited by poor diffusion lengths (Table 8).

The second B/Al-alloy process used evaporated boron-doped aluminum films. Boron-doped (3% by weight) aluminum material was thermally evaporated. The problem with this approach is that stoichiometry control is very difficult in evaporation of alloys due to large variations in evaporation rates. Analysis of B/Al evaporated films found only a thin layer of boron at the interface with the substrate, so it is doubtful that this method achieved sufficient boron doping levels. Experiment *SSI-64* fabricated BSF cells using the evaporated Al/B films, and found little difference between cells using pure aluminum and boron-doped aluminum (Table 5). Little difference in cell performance would be expected due to the poor boron incorporation in the evaporated boron-doped aluminum films.

3.3 Emitter Wrap-Through (EWT) Cells

A parallel project is developing a high-efficiency EWT cell using FZ material. The basic process was described in Ref. 15, except that the n-type contact is on the front surface rather than both contacts on the back surface. A bifacial-contact configuration avoids shunt issues associated with the interdigitated contacts in the back-contact configuration. Experiment *LAPERF12* fabricated bifacial-contact EWT cells using SSI Cz material. There were two splits in this experiment; half the cells have holes to electrically connect the front and back n^+ diffusions (EWT cell), while the n^+ diffusion on the back surface is left floating for surface passivation in other half of the cells (PERF cells). The process of Ref. 15 was modified to minimize the number of high-temperature furnace steps. Appendix 2 contains a full description of the process.

The results were quite credible for such an advanced device structure, with the best EWT cell achieving an efficiency of 15.7% (Table 9). The poor FF's was primarily due to high series resistance; the present process uses only sintered-aluminum contacts to the p-type substrate and requires a fairly low bulk resistivity (<1 Ωcm) to minimize base resistance losses. The EWT cells have higher current compared to the PERF cells, which is expected due to the enhanced collection of carriers from the rear junction (Fig. 11). Another advantage of EWT cells is the excellent collection efficiency for rear illumination (Fig. 12), which is useful for modules using bifacial illumination.

3.4 Summary

- Efficiencies of 18.3% and 17.6% were demonstrated for moderate- and large-area cells with aluminum-alloyed BSF's, respectively. 21-out-of-23 large-area cells had efficiencies above 17%, and the overall average for the large-area, aluminum-alloyed cells was 17.25 ± 0.25%. Cell performance was limited by recombination at the back surface due to the relatively high S values of aluminum-alloyed BSF's using evaporated aluminum films.
- Back-surface recombination velocity of around 350 cm/s was demonstrated with a boron-doped BSF using a B/P codiffusion process. Cell performance was limited by degradation of bulk lifetime, which is only partially related to the higher diffusion temperatures. Average large-area boron-doped BSF cell performance was 14.1 ± 1.1%.
- A low-temperature process (Al/B-alloy) to form boron-doped BSF's was investigated. Improved methods for doping aluminum with boron are still required.
- Bifacial-contact EWT cell was demonstrated with an efficiency of 15.7% using SSI Cz material.

Table 2. Comparison of measured and modeled data for an experiment that fabricated cells with two substrate thicknesses. The model fit used a bulk resistivity of 1 Ωcm, a bulk lifetime of 36 μs, and a back-surface recombination velocity of 10,000 cm/s. These particular cells had a very thin aluminum-alloyed back-surface field. The model calculations used a numerical device simulator (PC-1D).

Cell ID (Thickness)	Parameter	Eff %	V_{oc} volts	FF	J_{sc} mA/cm^2
19-4D	Measured	16.9	0.613	0.795	34.6
(350 μm)	Modeled	17.1	0.615	0.805	34.6
19-2C	Measured	16.2	0.605	0.794	33.8
(170 μm)	Modeled	16.4	0.605	0.804	33.7

Table 3. Results from *SSI-51*, which fabricated aluminum- and boron-doped BSF, 42-cm^2 cells on thick and thin SSI-Cz. Material E has a bulk resistivity and thickness of 1.5 Ωcm and 225 μm, respectively, while material F has a bulk resistivity and thickness of 1.2 Ωcm and 290 μm, respectively.

Cell ID	Split Descr	V_{oc} volts	I_{sc} amps	FF	Eff %
SSI-51-2	E,Al	0.614	1.489	0.797	17.4
SSI-51-11	E,Al	0.615	1.479	0.803	17.4
SSI-51-12	E,Al	0.617	1.490	0.806	17.6
SSI-51-3	E,B	0.589	1.342	0.784	14.8
SSI-51-4	E,B	0.587	1.332	0.780	14.5
SSI-51-13	E,B	0.587	1.339	0.781	14.6
SSI-51-8	F,Al	0.615	1.470	0.801	17.3
SSI-51-17	F,Al	0.613	1.461	0.803	17.1
SSI-51-18	F,Al	0.621	1.463	0.800	17.0
SSI-51-9	F,B	0.591	1.305	0.779	14.3
SSI-51-10	F,B	0.583	1.267	0.773	13.6
SSI-51-19	F,B	0.590	1.315	0.771	14.2
SSI-51-20	F,B	0.585	1.262	0.760	13.4
Average	E,Al	0.615	1.486	0.802	17.5
	E,B	0.587	1.338	0.782	14.6
	F,Al	0.616	1.465	0.801	17.1
	F,B	0.587	1.287	0.771	13.9

Table 4. Results from *SSI-57*, which fabricated aluminum-alloyed 42-cm^2 BSF cells on thin (220-μm) SSI-Cz material.

Cell Name	Al-Alloy Temp (°C)	Eff %	V_{oc} volts	I_{sc} amps	FF
SSI-57-3	1000	17.6	0.612	1.490	0.800
SSI-57-11	1000	17.5	0.617	1.496	0.805
SSI-57-1	875	17.3	0.616	1.476	0.805
SSI-57-2	875	17.5	0.617	1.483	0.798
SSI-57-10	875	17.3	0.614	1.462	0.807
SSI-57-19	875	16.7	0.606	1.443	0.799
	Average	17.3	0.614	1.475	0.802
	StDev	0.3	0.004	0.02	0.004

Table 5. Results from *SSI-64*, which fabricated Al- and B/Al-alloyed BSF, large-area cells on SSI-Cz material. B/Al-alloy process used evaporated films of boron-doped aluminum. This experiment used material with a bulk resistivity of 1.15 Ωcm, and *Thick* and *thin* refer to substrate thicknesses of 320 and 220 μm, respectively.

Cell ID	Thickness	Alloy Type	Eff %	V_{oc} volts	I_{sc} amps	FF
SSI-64-9	thick	Al	17.5	0.621	1.467	0.804
SSI-64-13	thick	Al	17.3	0.620	1.459	0.802
SSI-64-19	thick	Al	17.0	0.615	1.454	0.800
SSI-64-4	thick	Al/B	17.5	0.622	1.461	0.805
SSI-64-10	thick	Al/B	17.6	0.621	1.475	0.805
SSI-64-20	thick	Al/B	17.2	0.617	1.468	0.801
SSI-64-2	thin	Al/B	15.9	0.617	1.452	0.743
SSI-64-8	thin	Al/B	17.0	0.618	1.439	0.804
SSI-64-12	thin	Al/B	17.3	0.618	1.460	0.804
SSI-64-18	thin	Al/B	17.0	0.615	1.447	0.803
	Average		17.3	0.618	1.459	0.803
	<thick,Al>		17.2	0.619	1.460	0.802
	<thick,Al/B>		17.4	0.620	1.468	0.803
	<thin,Al/B>		17.1	0.617	1.448	0.804

Table 6. Summary of results for experiment *SSI-43* -- boron-doped BSF cells. The data is average of several 4-cm^2 cells from each wafer, with the number of cells in the average provided in the last column.

Wafer I.D.	Diffusion Temp. (°C)	V_{oc} mV	I_{sc} mA	FF	Eff %	Number Cells
W1	950	594	124.0	0.789	14.53	8
W9	875	602	134.7	0.798	16.18	8
W10	875	601	134.1	0.799	16.09	5

Table 7. Results from *SSI-68*, which fabricated large-area, boron-doped BSF cells on 2-Ωcm FZ and SSI-Cz material using a B/P-codiffusion process. *Dual* and *Single* refer to oxide passivation of BSF -- *dual* used an additional oxidation for passivation. Data is normalized to a solar-weighted reflectance of 5% to facilitate comparison of different splits.

Cell Name	Material	Split	Eff %	V_{oc} volts	J_{sc} mA/cm^2	Fill Factor	L_{eff} μm
SSI-68-2	FZ	Dual	11.9	0.590	32.4	0.621	190.5
SSI-68-10	FZ	Dual	14.2	0.591	33.2	0.724	195.2
SSI-68-19	FZ	Dual	14.1	0.586	32.1	0.749	185.7
SSI-68-4	FZ	Single	15.5	0.601	36.6	0.704	328.2
SSI-68-9	FZ	Single	16.1	0.603	35.8	0.747	360.3
SSI-68-14	FZ	Single	15.6	0.600	36.6	0.708	392.3
SSI-68-17	FZ	Single	16.3	0.597	35.6	0.766	360.3
SSI-68-7	SSI	Dual	13.8	0.590	30.5	0.766	117.0
SSI-68-12	SSI	Dual	14.1	0.596	31.8	0.747	152.7
SSI-68-8	SSI	Single	11.5	0.592	31.2	0.624	156.3
SSI-68-11	SSI	Single	14.3	0.591	32.3	0.747	170.4
SSI-68-20	SSI	Single	16.5	0.607	35.3	0.767	184.4
		<FZ>	14.8	0.595	34.6	0.717	287.5
		<SSI>	14.0	0.595	32.2	0.730	156.2
		<FZ,Single>	15.9	0.600	36.1	0.731	360.3
		<FZ,Dual>	13.4	0.589	32.6	0.698	190.5
		<SSI,Single>	14.1	0.596	32.9	0.713	170.4
		<SSI,Dual>	14.0	0.593	31.1	0.756	134.9

Table 8. Results of *SSI-63*, which fabricated Al- and B/Al-alloyed BSF, large-area cells using SSI Cz material. The cells have a bulk resistivity of 1.2 Ωcm, and *thick* and *thin* refer to substrate thicknesses of 310 and 215 μm, respectively.

Cell Name	Split Description	Efficiency %	V_{oc} Volts	I_{sc} Amps	Fill Factor
SSI-63-3	Al,thick	15.9	0.609	1.399	0.783
SSI-63-9	Al,thick	15.7	0.605	1.367	0.797
SSI-63-19	Al,thick	15.6	0.605	1.383	0.784
SSI-63-1	Al,thin	16.4	0.613	1.411	0.797
SSI-63-7	Al,thin	16.0	0.607	1.404	0.788
SSI-63-10	Al/B,thick	15.4	0.604	1.361	0.790
SSI-63-14	Al/B,thick	15.6	0.607	1.361	0.792
SSI-63-20	Al/B,thick	15.6	0.606	1.367	0.790
SSI-63-8	Al/B,thin	15.2	0.605	1.364	0.772
SSI-63-12	Al/B,thin	15.9	0.609	1.383	0.793
SSI-63-18	Al/B,thin	15.5	0.607	1.365	0.785
Entire Population	Average	15.7	0.607	1.379	0.788
	Std Dev	0.3	0.003	0.018	0.007
Split Averages	<Al,thin>	16.2	0.610	1.407	0.792
	<Al,thick>	15.7	0.606	1.383	0.788
	<Al/B,thin>	15.5	0.607	1.371	0.783
	<Al/B,thick>	15.5	0.605	1.363	0.791
Factor Averages	<thin>	15.8	0.608	1.385	0.787
	<thick>	15.6	0.606	1.373	0.789
	<Al>	15.9	0.608	1.393	0.790
	<Al/B>	15.5	0.606	1.367	0.787

Table 9. Results from *LAPERF11*, large-area EWT and PERF cells using SSI-Cz material. *H* and *L* refer to the phosphorus-diffusion process -- heavy (*H*) diffusion has a sheet resistance around 30 Ω/□ and light (*L*) diffusion has a sheet resistance around 80 Ω/□.

Cell Name	Split Descr	Eff %	V_{oc} volts	I_{sc} amps	Fill Factor
LAPERF 11 - 5	EWT,H	14.8	0.619	1.358	0.739
LAPERF 11 - 8	EWT,H	14.5	0.619	1.358	0.726
LAPERF 11 - 13	EWT,H	13.1	0.615	1.362	0.658
LAPERF 11 - 3	EWT,L	15.7	0.613	1.466	0.731
LAPERF 11 - 7	EWT,L	13.0	0.609	1.424	0.630
LAPERF 11 - 4	PERF,H	13.0	0.622	1.282	0.683
LAPERF 11 - 10	PERF,H	14.6	0.620	1.288	0.769
LAPERF 11 - 15	PERF,H	14.1	0.618	1.294	0.739
LAPERF 11 - 9	PERF,L	15.3	0.611	1.394	0.755
LAPERF 11 - 12	PERF,L	15.1	0.615	1.399	0.737
Entire Population	Average	14.3	0.616	1.362	0.717
	Std Dev	1.0	0.004	0.061	0.045
Split Averages	<EWT H>	14.1	0.618	1.359	0.707
	<EWT,L>	14.3	0.611	1.445	0.680
	<PERF,H>	13.9	0.620	1.288	0.730
	<PERF,L>	15.2	0.613	1.396	0.746
Factor Averages	<EWT>	14.2	0.615	1.394	0.697
	<PERF>	14.4	0.617	1.331	0.737
	<L>	14.0	0.619	1.324	0.719
	<H>	14.8	0.612	1.421	0.713

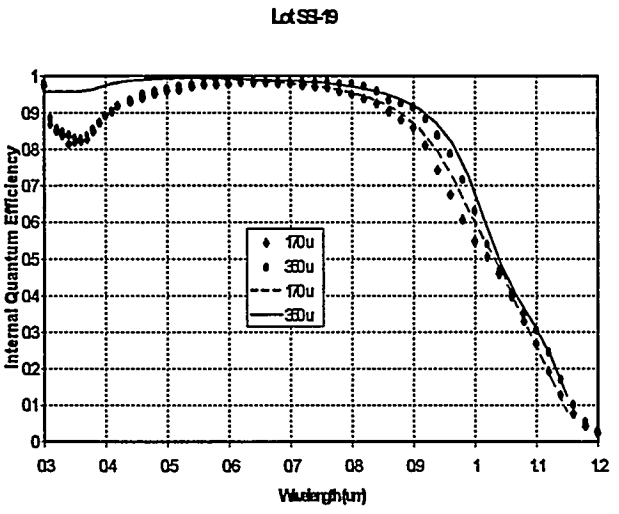

Figure 6. Example of model fit (lines) and measured data (points) of internal quantum efficiency data for high-efficiency cells using photovoltaic-grade silicon. See Table 2 for details of model.

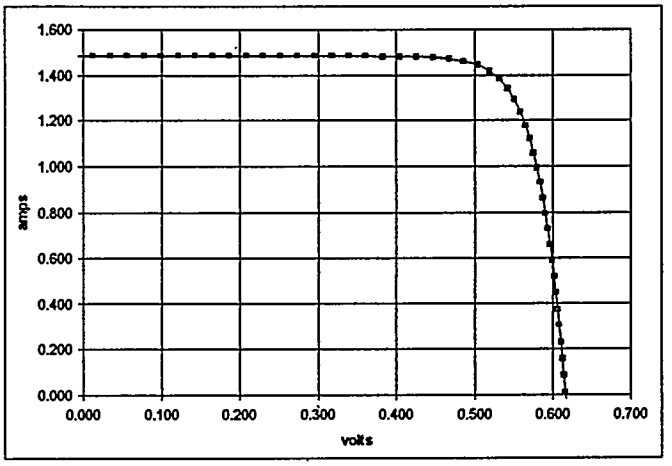

Figure 8. One-sun current-voltage plot of a 42-cm^2, 220-μm thick, 17.6%-efficient, aluminum-alloyed BSF cell using SSI Cz silicon.

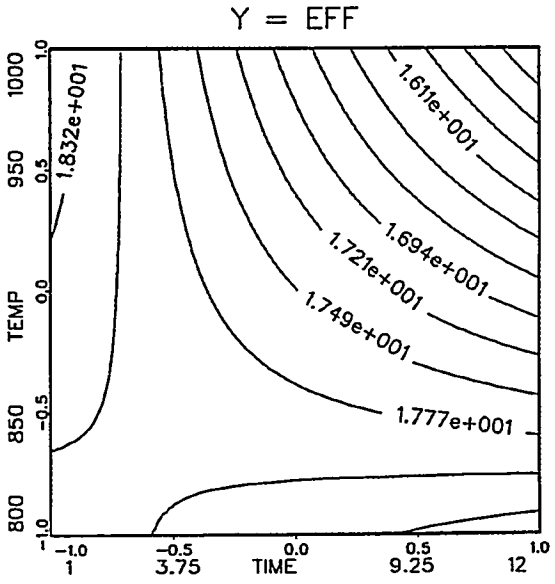

Figure 7. Representative response surface from experiment *SSI-56*. The contours are cell efficiency in %, *time* and *temp* are alloy time (hours) and temperature (°C), and aluminum thickness is 1 μm.

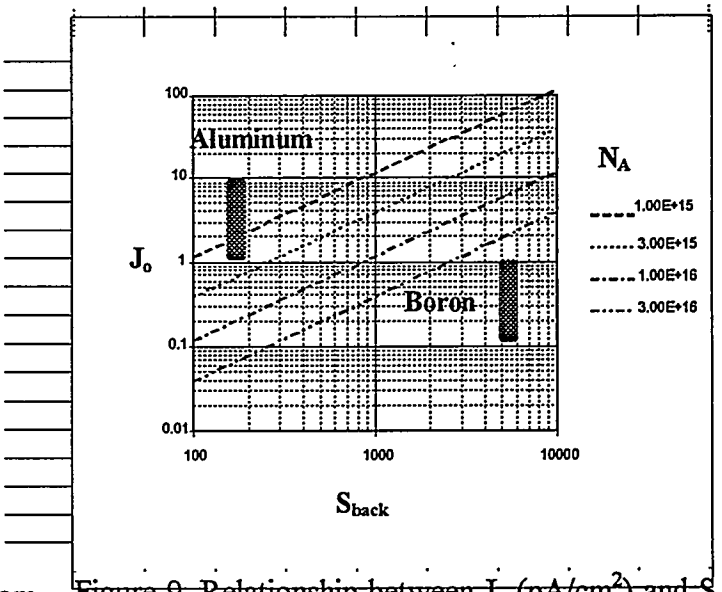

Figure 9. Relationship between J_o (pA/cm^2) and S (cm/s) as a function of bulk resistivity (N_A -- cm^{-3}). The shaded bars show the range of J_{oe} values obtained for aluminum-alloyed and boron-diffused junctions in the PDFL.

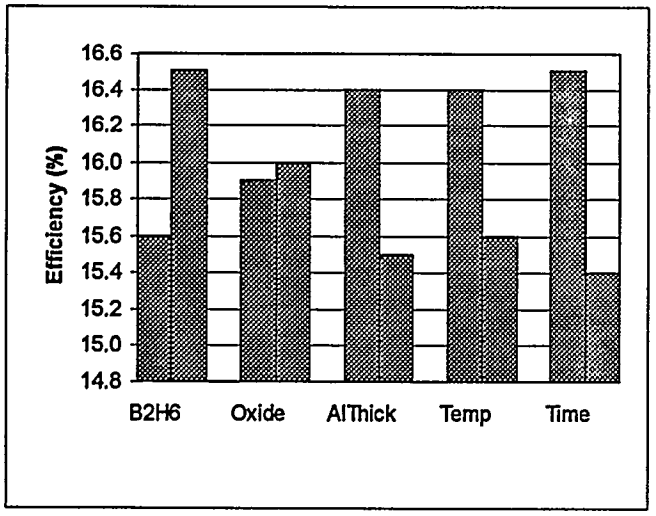

Figure 10. Factor-average efficiency from a main-effects experiment (*SSI-61*) that examined B/Al-alloy process using APCVD BSG and evaporated aluminum films. See text for low and high values associated with each factor.

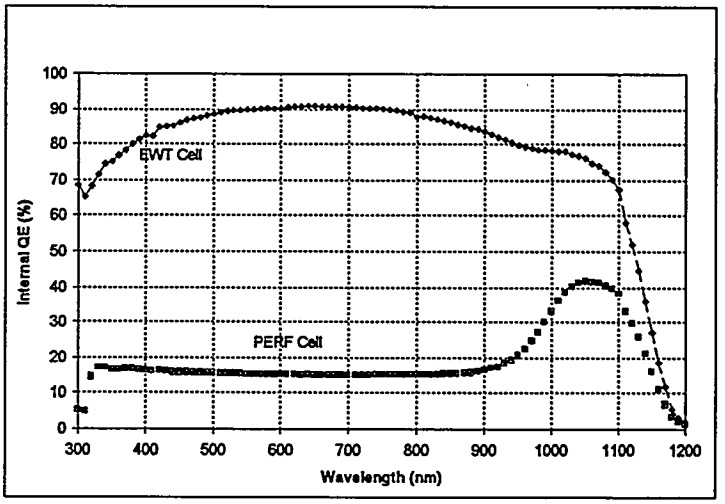

Figure 12. Internal quantum efficiency spectra illuminated from the **rear** surface of EWT and PERF cells from *LAPERF11*.

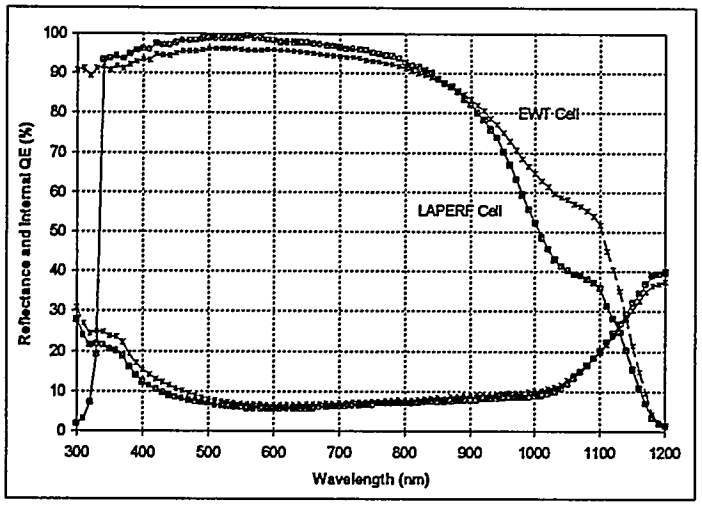

Figure 11. Internal quantum efficiency spectra of EWT and PERF cells from *LAPERF11*.

4.0 STABILITY OF CZ-SILICON SOLAR CELLS

Some early publications described a photon degradation phenomenon in Cz-silicon solar cells [22]. While not discussed much publicly, the phenomenon has been known by c-Si module and cell manufacturers for perhaps 15 years. The instability appears primarily as a decrease in short-circuit current in the first two to four hours of exposure, after which the cell is stable. Investigations by SSI and others indicated that the degradation is primarily in bulk diffusion length. The origin of the instability has never been fully determined.

In this chapter, some preliminary investigations on instabilities in Cz-silicon solar cells are reported. The studies included both commercial modules and cells, and high-efficiency laboratory cells.

4.1 Commercial Cz-Silicon Modules and Cells

A series of well-controlled tests was performed at Sandia in March of 1994 on four previously unexposed M55 modules supplied by SSI. These outdoor module tests confirmed the presence of the phenomenon and quantified the magnitude of the effect in the 2 to 5 percent range. The tests were performed on two modules simultaneously, both covered prior to the solar exposure; one module was previously unexposed while the other module was previously exposed to a stable condition. Modules were normal to the sun (tracking), and corrections for the small influence of changing solar spectrum during the four-hour test were also applied. Temperature variations during the tests were compensated for by translating I_{sc} measurements to a common temperature using measured temperature coefficients, and slight changes in solar irradiance were compensated for by normalizing the measured I_{sc} to 1000 W/m^2 using a silicon reference cell. Figures 13-16 illustrate typical measures results for the SSI M55 modules.

The transient nature of the phenomenon is clearly evident. For clarification, the observed transient is not due to a temperature transient -- which typically lasts only around 15 minutes, while the photodegradation lasted for about 2 hours. Similarly, the degradation is not due to changes in the reference module. Two previously exposed modules (s/n 674907 and s/n 674931) were tested with the same test configuration as the unexposed modules of Fig. 13-15; this test shows no degradation since both modules had been previously exposed to reach a steady-state condition (Fig. 16).

These tests demonstrated that there is photodegradation in Cz-silicon modules, that the degradation occurs primarily in I_{sc}, that the degradation rapidly ceases, and that the degradation reduces module performance in the 2 to 5 percent range. The module measurements do not indicate whether the degradation is entirely due to changes in the cells, or if there are possible changes in the optical transmittance of the module construction (e.g., EVA encapsulation). Hence, additional tests were performed on commercial Cz-silicon cells supplied by SSI.

A production sample of ten 104-cm^2 cells was provided by SSI in January of 1995 for comprehensive characterization. Three of these cells were used in an outdoor photodegradation test. The spectral response, light IV, and dark IV characteristics of the cells were measured prior to solar exposure. Then, the three cells were placed on a soft insulated mat, covered with a low-iron glass sheet, and exposed to full sunshine for about 6 hours. Spectral response, light IV, and dark IV measurements were then repeated. The spectral response measurements indicated a small but measurable decrease in the red response (diffusion length), and the light IV measurements

indicated a slight loss in I_{sc}. But the loss observed in I_{sc} was very small (0.8%) and did not fully explain the magnitude of the loss confirmed at the module level. Table 10 presents a summary of the commercial Cz cells' performance parameters before and after solar exposure along with the control cells that were not exposed.

Table 10. SSI commercial cell performance before and after a 6-hour solar exposure.

Cell ID	I_{sc} (A)	V_{oc} (V)	I_{mp} (A)	V_{mp} (A)	FF
Before					
1 (Control)	3.445	0.5981	3.179	0.4825	0.744
5 (Control)	3.485	0.6032	3.201	0.4880	0.743
2 (Before)	3.477	0.6024	3.174	0.4849	0.735
3 (Before)	3.450	0.6015	3.157	0.4830	0.735
4 (Before)	3.491	0.6038	3.194	0.4884	0.740
Avg. 2-4	3.473	0.6026	3.175	0.4854	0.737
Std Dev 2-4	0.021	0.0012	0.019	0.0027	0.003
After					
1 (Control)	3.459	0.5968	3.185	0.4781	0.738
5 (Control)	3.496	0.6021	3.199	0.4844	0.736
2 (After)	3.456	0.5982	3.156	0.4778	0.729
3 (After)	3.455	0.5983	3.163	0.4777	0.731
4 (After)	3.465	0.5998	3.168	0.4812	0.734
Avg. 2-4	3.459	0.5988	3.162	0.4789	0.731
Std Dev. 2-4	0.0055	0.0009	0.0060	0.0020	0.003
2-4 Δ (%)	-0.76	-0.63	-0.46	-1.35	-0.72

Additional tests of EVA encapsulant are planned in order to rule out a change in its optical transmittance as a contributor to the module-level degradation observed. Test coupons laminated using the SSI EVA formulation and manufacturing process parameters will be required.

4.2 Laboratory Cells and Processes

The PDFL has fabricated high-efficiency c-Si cells on a variety of c-Si substrates. These cells include a range of resistivities (0.4 to 8 Ωcm) and a range of oxygen concentrations (low-oxygen FZ and HEM, high-oxygen Cz from SSI and from various vendors, and high-oxygen multicrystalline-silicon from Solarex). A set of these cells was used as reference cells for initial screening measurements in the PDFL. These reference cells have been exposed to the equivalent of at least 10 hours of simulated solar radiation. These reference cells were recalibrated in the PDML, and the new calibrations were compared with old calibrations to look for degradation (Fig. 17).

The cells (SSI and 1-Ωcm Cz) with both high oxygen and high boron concentrations exhibited degradation, while the materials with low oxygen concentrations (FZ and HEM) and materials with low boron concentrations (8-Ωcm Cz) exhibited no degradation. Module measurements have also found little degradation in c-Si modules using low-oxygen-content HEM silicon [7]. The degradation was evident in both I_{sc} and V_{oc} for the high-efficiency cells.

Analysis of the degraded cells found that the degradation was entirely due to degradation in the diffusion length. For a 0.8-Ωcm SSI-Cz silicon cell, the bulk diffusion length decreased from 191 to 125 μm (Fig. 18). All the cells returned to their original performance with a 30-minute 200°C forming gas anneal, so the phenomenon is reversible. The exception to the high-oxygen-boron rule was the Solarex cells. The lack of degradation in the Solarex cells is believed to be due to a lower starting bulk lifetime, so that changes due to photoactivated recombination centers have less effect.

One possible explanation for the photodegradation is iron-boron (Fe-B) pairs. Fe is an ionized interstitial atom (Fe_i^+) in the silicon lattice that binds ("pairs") with boron acceptors (B^-) at room temperature. The FeB pairs have a lower recombination cross section compared to interstitial ionized Fe atoms. Disassociation of FeB pairs would decrease the diffusion length due to the higher recombination activity of ionized interstitial Fe atoms. A recent study of photodegradation in Cz silicon found recombination behavior that is consistent with FeB pairs [4].

The common element in photodegradation in various c-Si materials is both high oxygen and high boron content, so it seems likely that oxygen and boron must be involved. A second possible explanation for photodegradation concerns oxygen thermal donors. Oxygen thermal donors are an oxygen-related species that are donors and are created in high-oxygen-content silicon around 400°C. As a donor, oxygen thermal donors should be positively charged and might therefore exhibit long-range interactions with negatively charged, ionized boron acceptors similar to ionized interstitial Fe atoms.

Experiment *CzStbl-2* examined the effect of oxygen thermal donors on Cz cell stability. Cells were fabricated on 1-Ωcm Cz silicon. Half of the cells received a 6-hour, 450°C, forming gas anneal to create oxygen thermal donors. The bulk resistivity of coprocessed 8-Ωcm Cz wafers increased to 13 Ωcm due to compensation by oxygen thermal donors, which indicated that approximately $1 \bullet 10^{15}$ cm^{-3} oxygen thermal donors were created by the anneal. The cells were then exposed to simulated one-sun solar illumination at 25°C, and were tested every 2 minutes during the exposure.

There was only a small difference in the total degradation observed between cells with and without oxygen thermal donors (Fig. 19). However, there is a clear difference in the degradation rate. Because the absolute difference is small, further measurements are needed to improve statistical confidence. The bulk diffusion length decreased by about 10 and 20% for the cell with thermal donors and the baseline cell, respectively.

At the request of Richard King of SSI, PCD measurements were used to look for photodegradation (experiment *SSI-69*). Samples from various points in the SSI process were sent to Sandia for PCD measurements. The PCD measurements were performed both before and after exposure to 1-hour of natural sunlight. There was no degradation evident in the PCD data. PCD lifetime measurements frequently have large variances, so large changes in lifetime or large sample

sizes would be required before the resolution of PCD measurements could observe the photodegradation.

4.3 Summary

- Photodegradation due to exposure to solar radiation was observed in commercial c-Si cells and modules, and in laboratory c-Si cells. The degradation occurs only during the first few hours of exposure, and then the output stabilizes. The degradation reduces the power output by 2 to 5%.
- The photodegradation in c-Si modules is primarily in I_{sc}. The magnitude of photodegradation observed in commercial c-Si cells is much less than observed in modules, so effects other than cell degradation might be involved.
- The photodegradation observed in laboratory cells is due to degradation in bulk diffusion length, and is observed primarily in c-Si materials with high oxygen and high boron concentrations.
- Preliminary investigations suggest that oxygen thermal donors might be involved in the photodegradation.

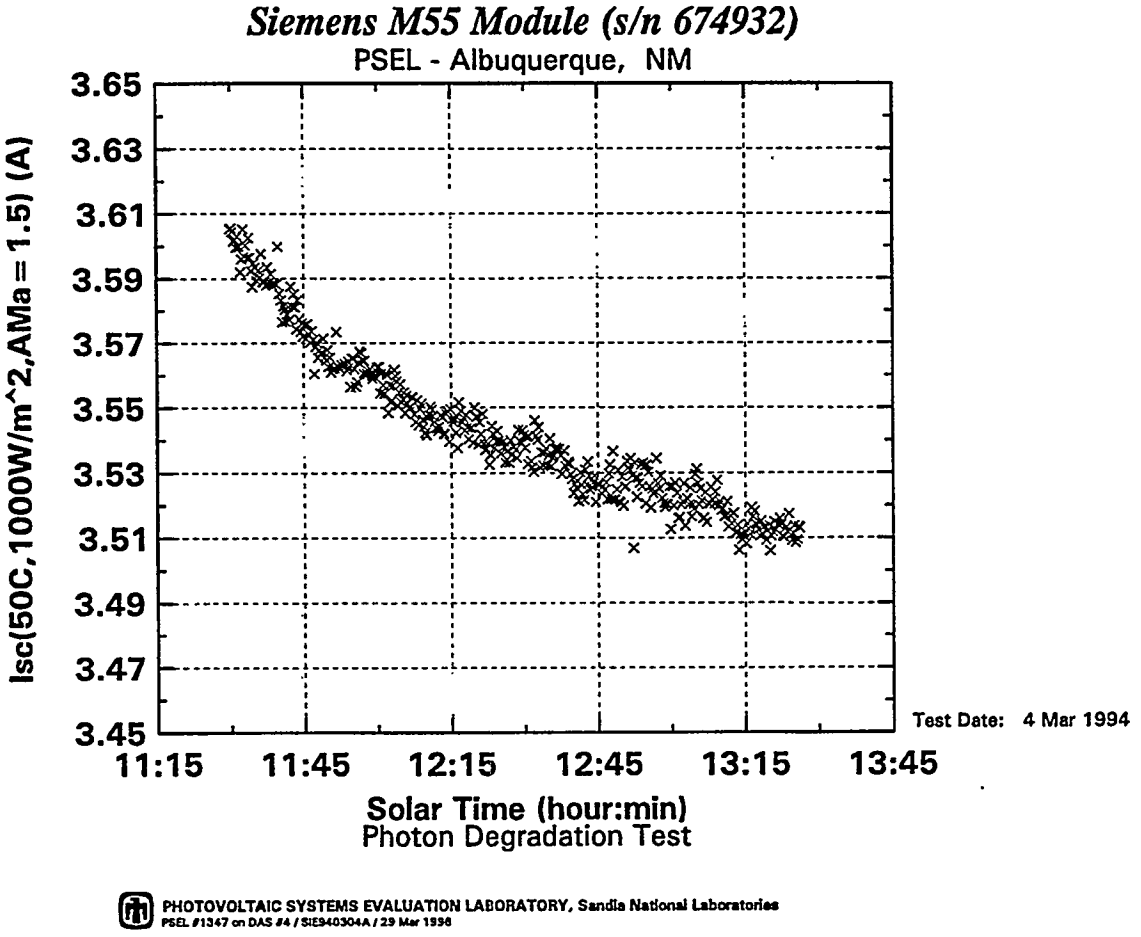

Figure 13. Normalized I_{sc} of previously unexposed SSI M55 module (s/n 674932) as a function of time from initial exposure.

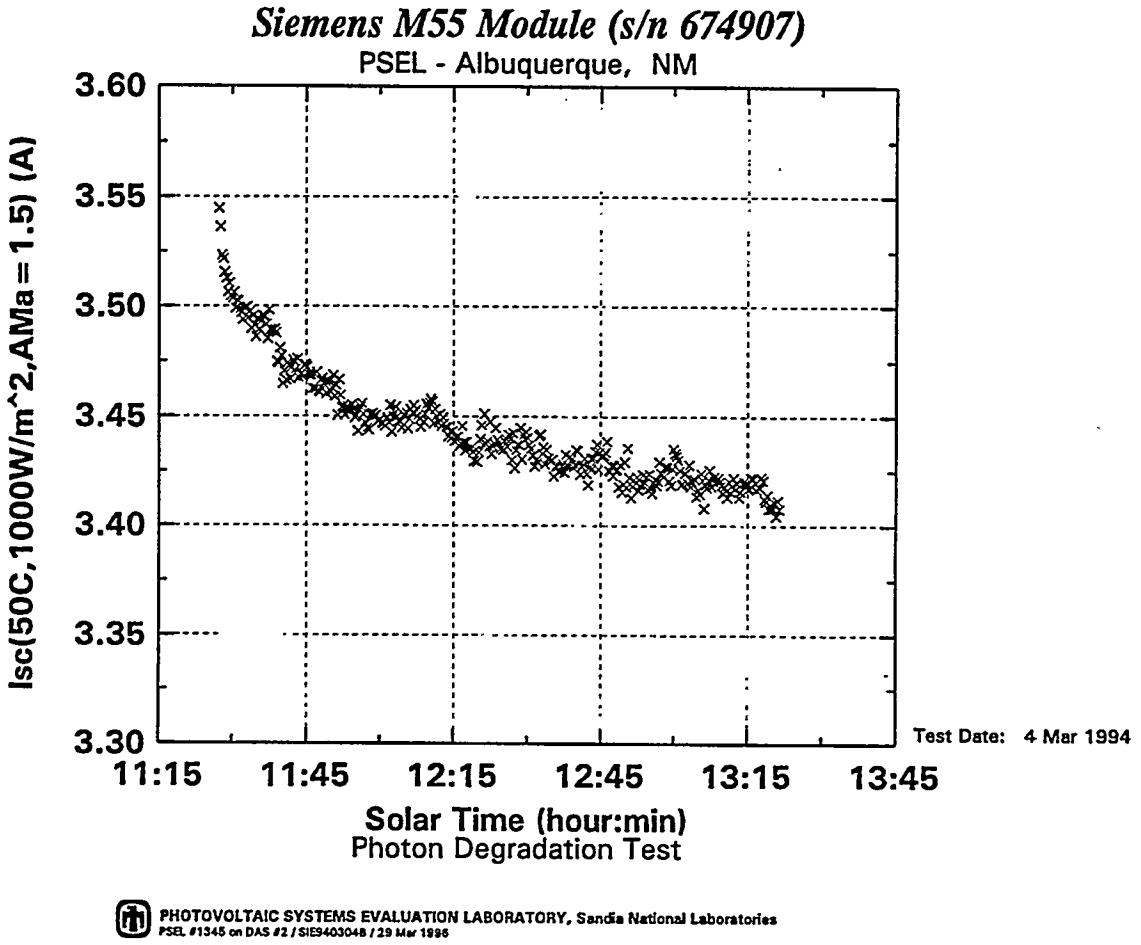

Figure 14. Normalized I_{sc} of previously unexposed SSI M55 module (s/n 674907) as a function of time from initial exposure.

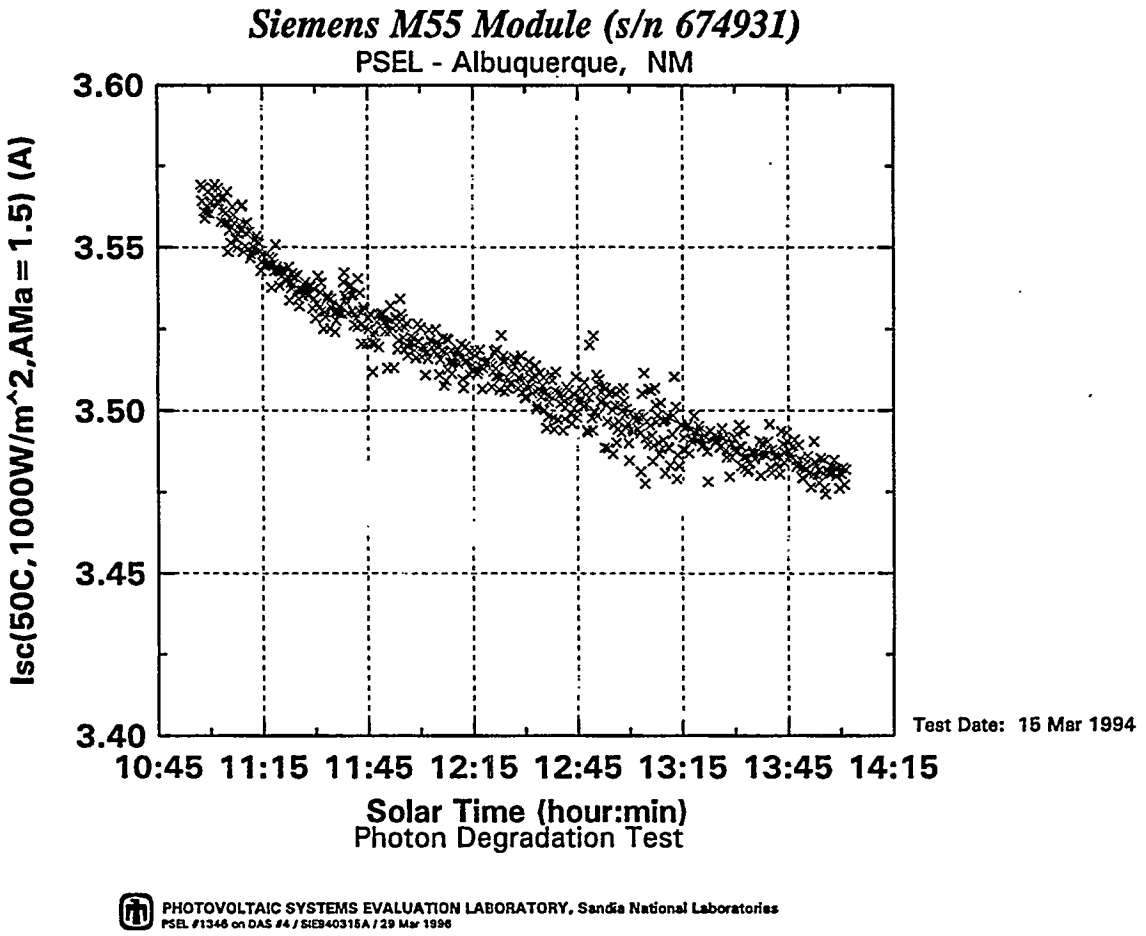

Figure 15. Normalized I_{sc} of previously unexposed SSI M55 module (s/n 674931) as a function of time from initial exposure.

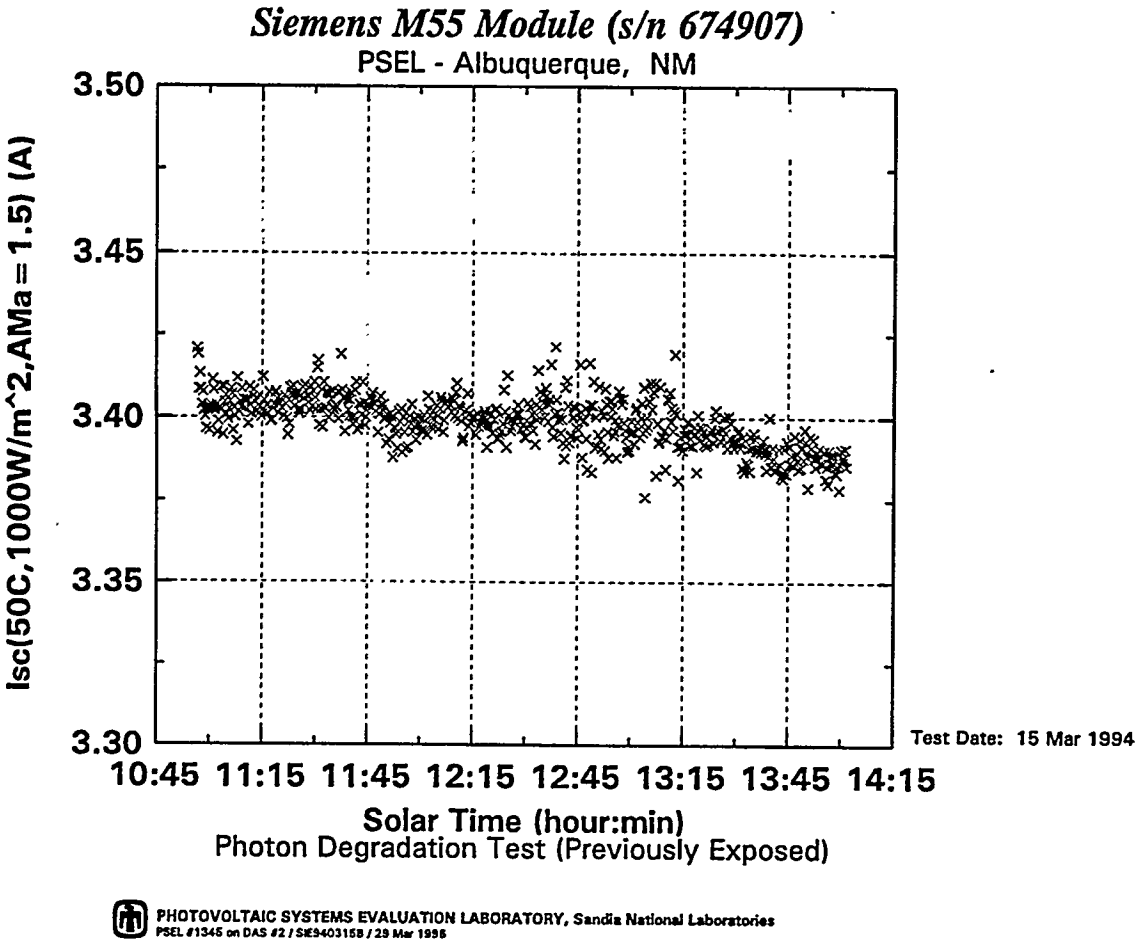

Figure 16. Normalized I_{sc} of previously exposed SSI M55 module (s/n 674907) as function of time.

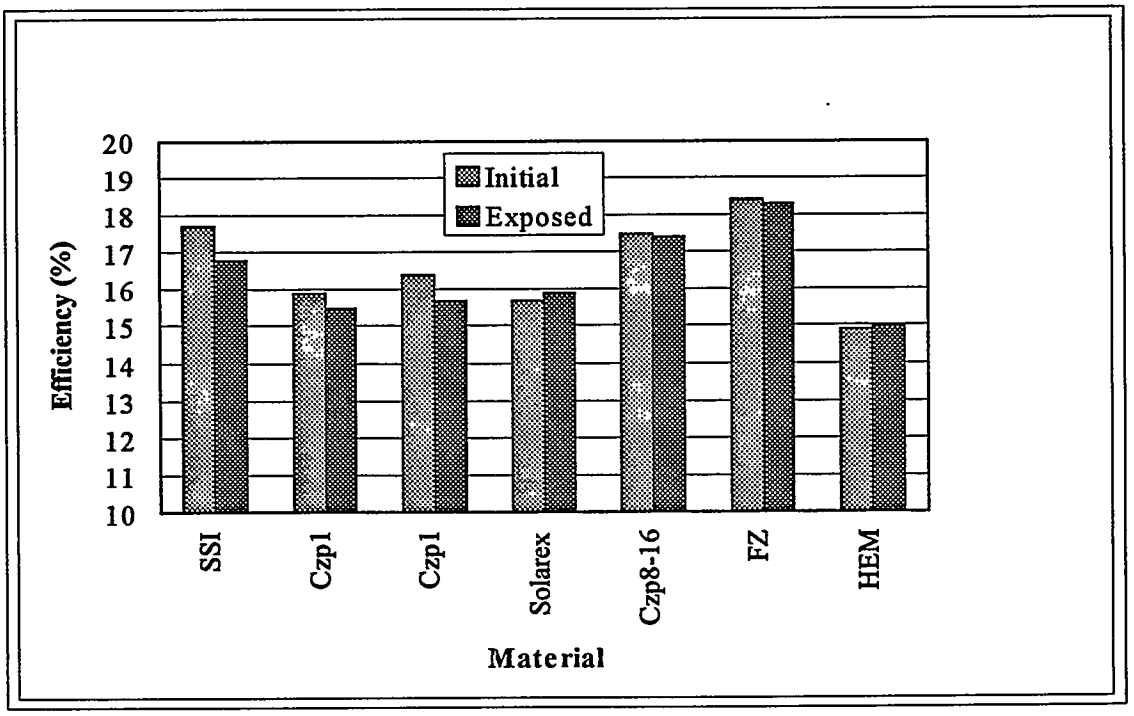

Figure 17. PDFL reference cell calibrations both before and after exposure to at least 10 hours of simulated solar radiation. Data is the average of 8 or 9 moderate-area cells, except for the "Czp8-16" cells the average is for only two cells.

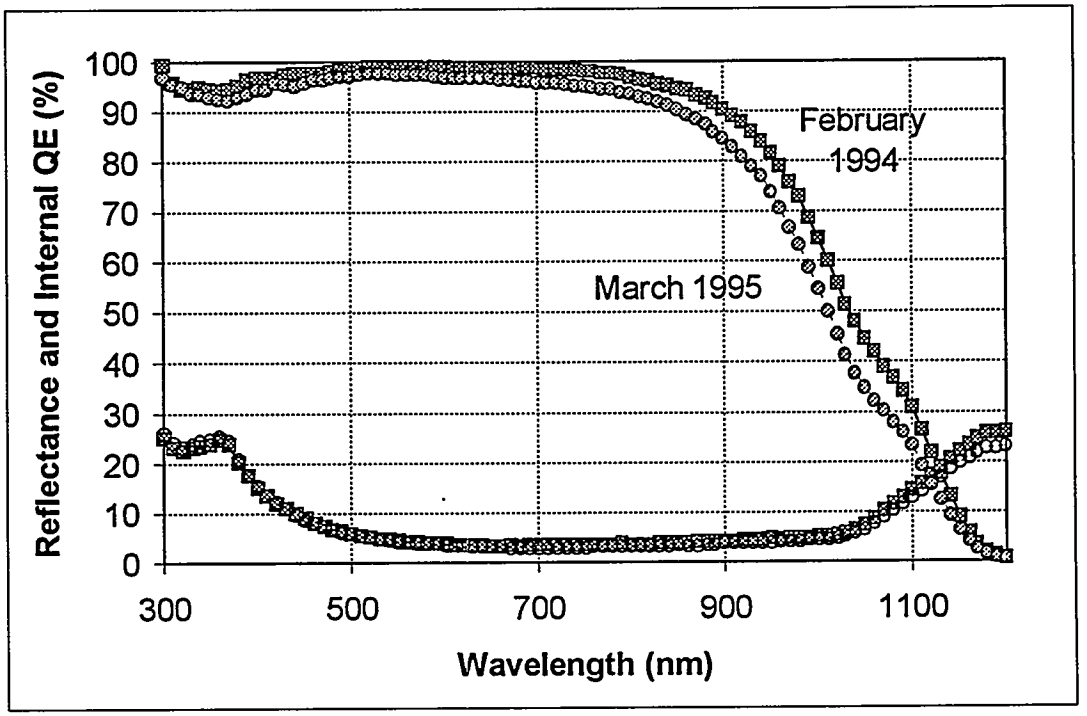

Figure 18. Internal quantum efficiency spectral of SSI-Cz cell before and after exposure. The bulk diffusion length degraded from 191 to 125 μm.

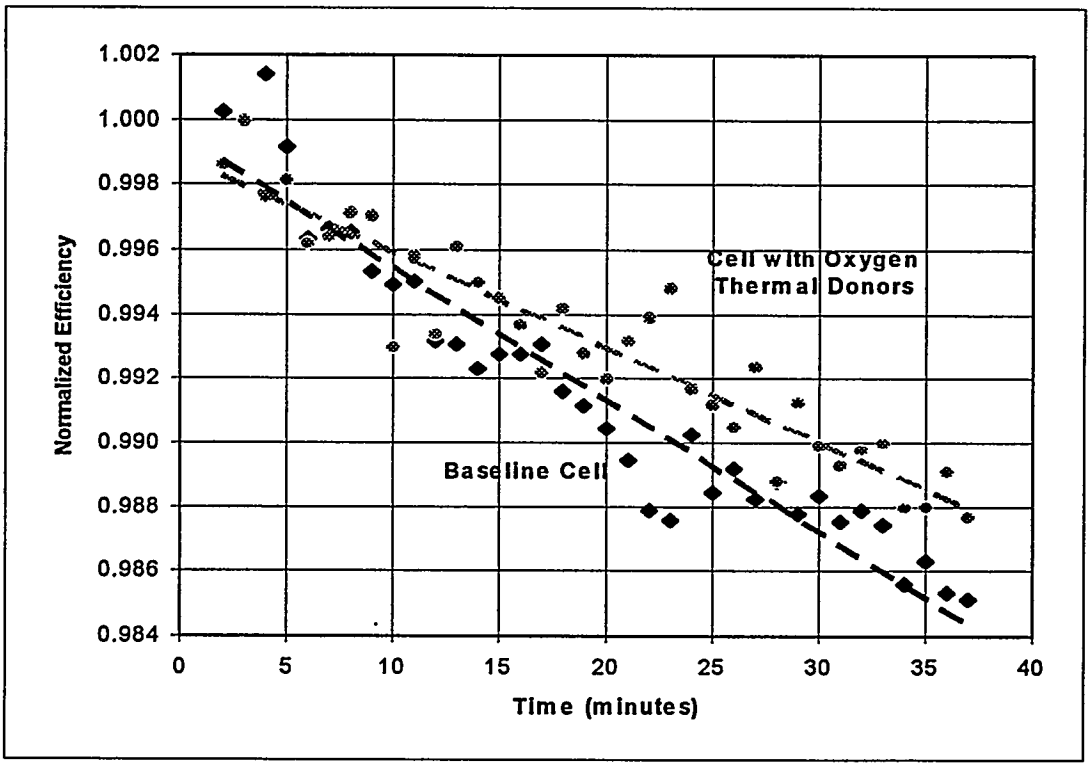

Figure 19. Normalized efficiency of 1-Ωcm Cz cells with and without oxygen thermal donors as a function of exposure time. The lines are linear least-squares fit of the data.

5.0 CONCLUSIONS

The ultimate performance potential of photovoltaic-grade Cz silicon was projected based on the material evaluation and advanced device development tasks in this project. Two types of devices were considered: thin BSF cells and EWT cells. The calculations used a bulk lifetime of 75 μs, a bulk resistivity of 1 Ωcm, a series resistance of 0.5 Ωcm^2, a well-passivated emitter ($N_s=3\bullet10^{19}$ cm^{-3}, sheet resistance of 108 Ω/□, junction depth of 550 nm, and surface recombination velocity of 5000 cm/s), a solar-weighted extrinsic reflectance of 5%, an internal back-surface reflectance of 90%, and an internal front-surface reflectance of 92%. These values are considered appropriate, if aggressive, targets for advanced c-Si cells. PC1D was used for the calculations (Fig. 20). Efficiencies of 20% are projected for thin cells with excellent BSF's (S<300 cm/s), or for EWT cells for nearly all the thicknesses considered. Because the best BSF demonstrated to date only has an S around 300 cm/s, the EWT cell has about 0.5% absolute higher efficiency potential compared to thin BSF cells. The superior projected performance of the EWT cell is due to (1) a high V_{oc} that is roughly equivalent to a BSF cell with an S of 100 cm/s, and (2) a J_{sc} that is higher than any of the BSF cells.

This study found that material quality is clearly sufficient, and that substantial performance improvements are still possible with photovoltaic-grade Cz silicon cells compared to typical commercial cells or to the cells demonstrated in this project. Furthermore, many advanced device structures can be implemented with manufacturable processes. Recommendations for future work therefore include:

- Continued development of a boron-doped BSF and/or other advanced back-surface structures using manufacturable processes.
- Continued development of an EWT cell.
- Continued investigation of photodegradation in c-Si cells.

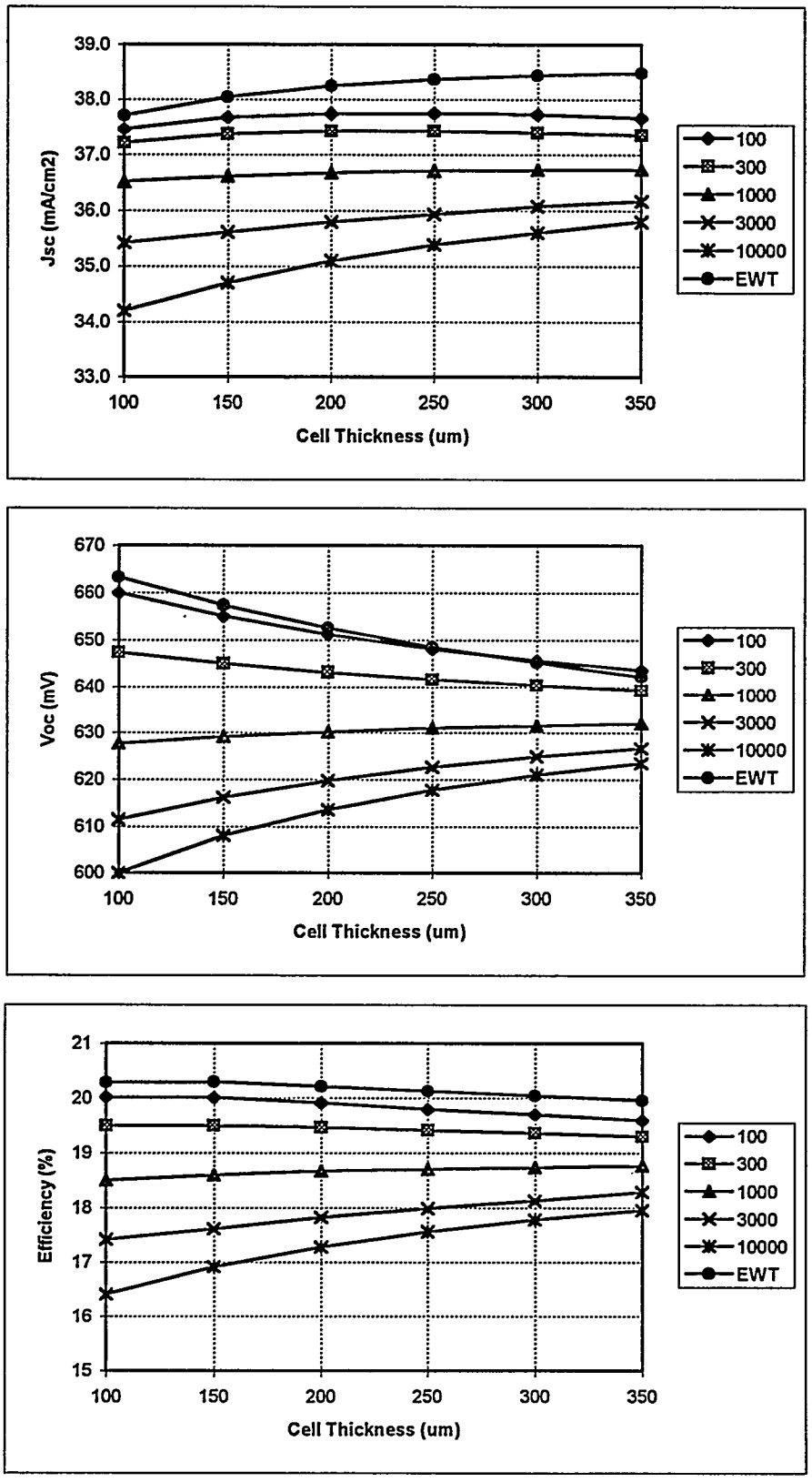

Figure 20. Projected performance of optimized cells using photovoltaic-grade Cz silicon. Legend is back-surface recombination velocity in cm/s.

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APPENDIX 1. PDFL runsheet ("SSI-57") with process details for experiment that produced 17.6%-efficient, large-area cell using SSI-Cz silicon substrates.

Lot ID: SSI-57 Optimized Al-BSF SSI-Cz cells.

Requester: JMG James M. Gee (SMTS) 4-7812
Approved: EB 21-FEB-1995 08:54:54.00
Finished: JMG 15-MAR-1995 17:00:12.00
Samples: 1-20

Lot Materials:

Wafer4R.CZn1-10 Samples: 5,15
 100-mm (4-in) round silicon wafer
  Exsil CZ n-type (100) 1-10 ohm-cm
Wafer4R.CZp8-16 Samples: 6,16
 100-mm (4-in) round silicon wafer
  SEH CZ p-type (100) 8-16 ohm-cm 625 um
Xtal10.Siemens Samples: 1-4,7-14,17-20
 10-cm crystalline silicon
  CZ silicon grown by Siemens Solar
 JMG: Please use slices from Group I.

Lot References: SSI-51

Purpose: (JMG, 02/13/95) Investigate aluminum-alloyed BSF cells on Cz material from SSI. This lot investigates two factors: Al-alloy sequence and gettering sequence. The two Al-alloy sequences correspond to our baseline sequence (875C) and to the optimal sequence from our recent Al-alloy factorial experiment (SSI-56, 1000C alloy). Gettering is included because we routinely observe longer lifetimes in PCD-lifetime lots (20-30 us) than we observe in SSI cell lots (10-20 us). The PCD-lifetime lots diffuse phosphorus on both surfaces, which might improve the gettering efficiency of the POCl3 diffusion.

Experiment: (JMG, 02/13/95) This lot fabricates 16 large-area n+pp+ BSF cells, which are distributed into four 4-cell splits. The splits correspond to two factors: BSF process (baseline and 1000C) and gettering (Y and N). Gettering refers to diffusing phosphorus on both surfaces, and then removing the n+ diffusion from the back surface prior to evaporating the Al for the alloy.

The splits are as follows:

Wafer	Split Description
1,8,14,18	n+pp+ cells, 875, gettered
2,10,12,19	n+pp+ cells, 875, not gettered
3,7,11,20	n+pp+ cells, 1000, gettered
4,9,13,17	n+pp+ cells, 1000, not gettered
5,6,15,16	Cz controls

Summary: (JMG, 03/15/95)

Table 1. Summary of PDML one-sun IV data.

Cell Name	Split Descr	Eff %	Voc volts	Isc amps	FF	Jo pA/cm2
SSI-57-3	1000,G	17.6	0.612	1.490	0.800	1.55
SSI-57-11	1000,G	17.5	0.617	1.496	0.805	1.32
SSI-57-1	875,G	17.3	0.616	1.476	0.805	1.34
SSI-57-2	875,NG	17.5	0.617	1.483	0.798	1.28
SSI-57-10	875,NG	17.3	0.614	1.462	0.807	1.43
SSI-57-19	875,NG	16.7	0.606	1.443	0.799	1.89
	Average	17.3	0.614	1.475	0.802	1.47
	StDev	0.3	0.004	0.020	0.004	0.23

Table 2. Summary of IQE analysis.

Cell Name	Split Descr	Rb %	Job pA/cm2	L um	S cm/s	<R> %
SSI-57-3	1000,G	82.4	1.60	229.8	1780	4.5
SSI-57-11	1000,G	82.5	1.90	190.4	2010	5.6
SSI-57-1	875,G	81.8	2.02	177.3	2010	4.3
SSI-57-2	875,NG	82.6	1.84	194.8	1840	4.2
SSI-57-10	875,NG	83.0	1.77	194.9	1370	4.3
SSI-57-19	875,NG	82.6	1.75	201.9	1590	4.5
	Average	82.5	1.81	198.2	1767	4.6
	StDev	0.4	0.14	17.5	250	0.5

This is our first lot to process thin, large-area, SSI-Cz cells. (Thin, large-area, BSF cells are a task in our SSI CRADA.) The average thickness for these cells was 205 um. There was considerable breakage, with only 6 out of 16 cells completed processing. Three wafers were broken during liftoff, three wafers were broken in the two Al evaporations, 2 wafers were broken in separate chemical steps, and one wafer was broken during transport to the PDPL; the runsheet did not specify where the last wafer was broken.

The cell performance for the completed cells was very good. The best cell (prior to degradation) achieved an efficiency of 17.6%, which matches our previous best large-area cell for SSI-Cz material. The average for the six completed cells was 17.3%. Cell 19 is cracked and is missing a chipped edge, which accounts for its low performance. Although the statistics are obviously very weak due to the poor yield, there was clearly very little difference in cell performance between the factors. I expected the 1000C-alloyed cells to have better performance based on the factorial study of SSI-56, so the present results are a little disappointing.

The diffusion lengths from the IQE analysis (Table 2) indicate a bulk lifetime around 15 us, which agrees with the PCD lifetime measurement after the POCl3 diffusion on textured, n+pn+, SSI-Cz samples. PC-1D modelling with the IQE parameters of Table 2 matched the measured one-sun parameters and measured IQE curve very well. (See attached plot.) The IQE and PC-1D models both show that considerable recombination occurs at the back surface at both short circuit and open circuit. The efficiency can be improved by approximately 0.5% absolute by reducing the rear surface recombination velocity to our best value of about 500 cm/s. The efficiency can further be improved by about another 0.5% absolute by improving the bulk lifetime to 30 us, which is the best lifetime we have observed in planar SSI-Cz PCD controls.

```
EB    1. Laser.Groove  Ver: 8   Samples: 1-4,7-14,17-20   (1:41+100:00)
          Groove pulse rate (Hz): 3000
          Groove cutting speed (mm/s): 2
          Groove cutting axes: X
          Groove cutting pulse energy (mJ): max
          Hole drilling pulse rate (Hz): 3000
          Hole drilling time (ms): 100
          Lot scribing time (#wafers*(min/wafer)): 100
          Alignment (0-chuck, #wafers-pattern): 0
          CADD pattern file name w/o extension: MultiRnd
          CADD layer: 4
          Side of wafer to cut: front
         Started: 21-FEB-1995 08:55:52.00

BLS   2. Laser.Label  Ver: 2   Samples: 1-4,7-14,17-20   (0:26+100:00)
          Pulse Rate: 3000
          Cutting Speed: 5
          Laser Current: 20
          Cutting Angles: X-Y
          CADD layer (wafer): Wafer-#
          CADD layer (lot): 57
         Started: 21-FEB-1995 10:32:46.00

BLS   3. Label.Scribe  Ver: 4   Samples: 5,6,15,16   (0:07+1000:00)
         Started: 21-FEB-1995 10:34:38.00

BLS   4. Clean.Degrease  Ver: 6   Samples: 1-4,7-14,17-20   (0:15+100:00)
          Prepare fresh chemicals: No
          Time in acetone (min): 5
          Time in propanol (min): 5
         Started: 21-FEB-1995 11:03:14.00

BLS   5. Etch.HF  Ver: 5   Samples: 1-4,7-14,17-20   (0:06+0:15)
          Side of wafer(s) to monitor for HPO: timed
          Etch time (min) ["+" means after HPO]: 1
         Started: 21-FEB-1995 11:49:16.00

BLS   6. Etch.Polish  Ver: 6   Samples: 1-4,7-14,17-20   (0:10+0:30)
         Number of process batches required: 2
          Nitric:HF mixture ratio: 15:1
```

```
          Time in solution (minutes): 2
         Started: 21-FEB-1995 11:57:26.00

         BLS:  Added 24 ml of HF before and after etch.

BLS   7. Etch.KOH  Ver: 8   Samples: 1-4,7-14,17-20   (1:05+0:30)
          H2O:KOH mixture ratio: 2:1
          Temperature of solution (C): 70
          Time in solution (minutes): 60
         Started: 21-FEB-1995 12:26:22.00

BLS   8. Etch.Polish  Ver: 6   Samples: 1-4,7-14,17-20   (0:10+0:30)
         Number of process batches required: 2
          Nitric:HF mixture ratio: 15:1
          Time in solution (minutes): 2
         Started: 21-FEB-1995 13:29:26.00

         BLS:  Added 24 ml of HF before and after etch.

BLS   9. Clean.Estek  Ver: 2   Samples: 1-4,7-14,17-20   (0:07+100:00)
          Program number: 1
         Started: 21-FEB-1995 13:35:28.00

BLS  10. Measure.BulkRho  Ver: 2   Samples: 1,8,14,18   (0:13+100:00)
          Side of wafer to measure: Front
          Number of points: 5
         Started: 21-FEB-1995 13:44:54.00

         BLS:  Wafer       Mean      StdDev
                No.     (ohms/sq)     (%)
                 1        64.60      2.763
                 8        65.19      2.281
                14        62.69      .5322
                18        61.81      2.454

BLS  11. Etch.HF  Ver: 5   Samples: 1-20   (0:06+0:15)
          Side of wafer(s) to monitor for HPO: timed
          Etch time (min) ["+" means after HPO]: 1
         Started: 21-FEB-1995 13:53:50.00

BLS  12. Etch.IsoEtch  Ver: 4   Samples: 1-20   (0:15+0:30)
          Nitric:HF mixture ratio: 100:1
          Time in solution (minutes): 10
         Started: 21-FEB-1995 13:58:28.00

BLS  13. Etch.HFDip  Ver: 6   Samples: 1-20   (0:06+0:15)
          H2O:HF mixture ratio: 50:1
          Etch time (seconds): 60
         Started: 21-FEB-1995 14:11:54.00

BLS  14. Clean.Estek  Ver: 2   Samples: 1-20   (0:07+1:00)
          Program number: 1
         Started: 21-FEB-1995 14:25:28.00
```

```
BLS  15. Deposit.CVDundop  Ver: 7   Samples: 1-20   (1:07+100:00)
         Number of process batches required: 3
          Time of deposition (min): 2.5
          Surface receiving deposition: Back
          Expected film thickness (nm): 350
         Started: 21-FEB-1995 14:33:18.00

         BLS:    Run      Wafer     Thickness   R.I.
                 No.       No.       (nm)
                3752    control     381.17     1.434
                3753      1-7       394.15     1.436
                3754      8-14      373.63     1.437
                3755     15-20      374.90     1.434

BLS  16. Etch.Texture2  Ver: 3   Samples: 1-4,7-14,17-20   (0:30+100:00)
          Mixture ratio (H2O:KOH:IPA): 125:2:5
          Temperature of solution: 70
          Time in solution (min): 15
         Started: 21-FEB-1995 15:03:20.00

         BLS:  Wafer 12 broke and will not continue with lot.

BLS  17. Etch.HF  Ver: 5   (0:06+0:15)
         Samples: 1,3,6-8,11,14,16,18,20
          Side of wafer(s) to monitor for HPO: backs
          Etch time (min) ["+" means after HPO]: +1
         Started: 22-FEB-1995 06:58:06.00

         BLS:  Wafers etched HPO in 2 minutes plus 1 minute after HPO.

BLS  18. Clean.HCl  Ver: 5   Samples: 1-20   (0:15+0:30)
          Temperature of solution (C): 50
          Time in solution (min): 5
         Started: 22-FEB-1995 07:08:56.00

BLS  19. Etch.IsoEtch  Ver: 4   Samples: 1-20   (0:06+1:00)
          Nitric:HF mixture ratio: 100:1
          Time in solution (minutes): 0.5
         Started: 22-FEB-1995 07:19:12.00

BLS  20. Etch.HFDip  Ver: 6   Samples: 1-20   (0:06+0:15)
          H2O:HF mixture ratio: 50:1
          Etch time (seconds): 30
         Started: 22-FEB-1995 07:27:20.00

BLS  21. Clean.Estek  Ver: 2   Samples: 1-20   (0:07+1:00)
          Program number: 1
         Started: 22-FEB-1995 07:32:38.00

BLS  22. Furnace.PCL1  Ver: 6   Samples: 1-20   (3:38+100:00)
          Temperature (C): 875
          POCl3 deposition time (min): 6
          First N2 soak time (min): 7
          O2 soak time (min): 120
```

```
          Final N2 soak time (min): 15
          Wafer orientation: FaceFace
         Started: 22-FEB-1995 07:40:14.00

BLS  23. Measure.Lifetime  Ver: 5   Samples: 1,8,14,18   (0:18+100:00)
          Number of locations: 8
          Pattern: BL2
          Location spacing (mm): 0
          Data to record: Mean/Std
          Light bias level (%): 80
         Started: 22-FEB-1995 11:04:46.00

         BLS:  Wafer      Mean      StdDev      Sweep      Points w/RMS error
               No.        (us)       (us)       (us)          > 10 %
                 1       15.66      0.67         20             none
                 8       16.83      1.11         20             none
                14       17.60      1.10         20             none
                18       16.70      2.43         50             none

BLS  24. Etch.HF  Ver: 5   (0:06+0:15)
         Samples: 1,3,6-8,11,14,16,18,20
          Side of wafer(s) to monitor for HPO: 6,16Both
          Etch time (min) ["+" means after HPO]: +1
         Started: 22-FEB-1995 11:27:58.00

         BLS:  Wafers etched HPO in 2 minutes and 30 seconds plus 1
         minute after HPO.

BLS  25. Clean.Estek  Ver: 2   (0:07+1:00)
         Samples: 1,3,6-8,11,14,16,18,20
          Program number: 1
         Started: 22-FEB-1995 11:34:04.00

BLS  26. Deposit.CVDundop  Ver: 7   (0:45+100:00)
         Samples: 1,3,6-8,11,14,16,18,20
         Number of process batches required: 2
          Time of deposition (min): 2.5
          Surface receiving deposition: Front
          Expected film thickness (nm): 350
         Started: 22-FEB-1995 11:38:48.00
         BLS:   Run       Wafer      Thickness  R.I.
                No.         No.        (nm)
               3756      control      357.19    1.440
               3757      1,3,6-8      365.04    1.442
               3758  11,14,16,18,20   363.86    1.435

BLS  27. Etch.KOH  Ver: 8   (0:07+0:30)
         Samples: 1,3,6-8,11,14,16,18,20
          H2O:KOH mixture ratio: 2:1
          Temperature of solution (C): 70
          Time in solution (minutes): 2
         Started: 22-FEB-1995 13:33:38.00
         JMG: The purpose of this step is to remove the phosphorus
         diffusion from the back surface.
```

```
BLS  28. Clean.Estek  Ver: 2   (0:07+100:00)
         Samples: 1,3,6-8,11,14,16,18,20
          Program number: 1
         Started: 22-FEB-1995 13:38:54.00

BLS  29. Measure.HotProbe  Ver: 4   Samples: 6,16   (0:07+100:00)
          Side of wafer to measure: Back
         Started: 22-FEB-1995 13:47:56.00
         JMG: Wafers should be p-type.
         BLS:  Both measured as p-type.

BLS  30. Etch.HF  Ver: 5   Samples: 1-20   (0:06+0:15)
          Side of wafer(s) to monitor for HPO: 5,15back
          Etch time (min) ["+" means after HPO]: +1
         Started: 22-FEB-1995 14:07:10.00

         BLS:  Wafers etched HPO in 7 minutes plus 1 minute after HPO.

BLS  31. Clean.HCl  Ver: 5   Samples: 1-20   (0:15+0:30)
          Temperature of solution (C): 50
          Time in solution (min): 5
         Started: 22-FEB-1995 14:18:10.00

         BLS:  Wafer 18 broke and will not be continued with lot.

BLS  32. Etch.HFDip  Ver: 6   Samples: 1-20   (0:06+0:15)
          H2O:HF mixture ratio: 50:1
          Etch time (seconds): 30
         Started: 22-FEB-1995 14:28:00.00

BLS  33. Clean.Estek  Ver: 2   Samples: 1-20   (0:07+1:00)
          Program number: 1
         Started: 22-FEB-1995 14:32:52.00

JWT  34. Deposit.Aluminum  Ver: 1   Samples: 1-4,7-14,17-20   (1:16+100:00)
          Desired metal thickness (nm): 1000
          Side of wafer for deposition: Back
          Shadow mask: None
         Started: 22-FEB-1995 15:02:52.00
         JWT- Sheet rho 29.6 milli-ohms, thickness 114nm, 3.40 u-ohms-cm.
         Wafer #19 broke on planetary.

BLS  35. Furnace.ALY2  Ver: 2   (1:55+100:00)
         Samples: 1,2,5,6,8,10,12,14,18,19
          Alloy temperature (degrees C): 875
          Push Ambient: O2
          1st alloy time (minutes): 30
          1st alloy ambient: O2
          2nd alloy time (minutes): 15
          2nd alloy ambient: Ar
          Tube number: 3
         Started: 23-FEB-1995 09:10:10.00
```

```
BLS  36. Furnace.ALY2  Ver: 2   (2:11+100:00)
         Samples: 3,4,7,9,11,13,15-17,20
          Alloy temperature (degrees C): 1000
          Push Ambient: O2
          1st alloy time (minutes): 1
          1st alloy ambient: O2
          2nd alloy time (minutes): 15
          2nd alloy ambient: Ar
          Tube number: 3
         Started: 23-FEB-1995 09:10:56.00

BLS  37. Measure.OxThick  Ver: 3   Samples: 5,6,15,16   (0:09+100:00)
          Expected film thickness (nm): 10,18
          Side of wafer to measure: Front
         Started: 23-FEB-1995 10:22:40.00

         BLS:  Wafer  OxThickness
                No.       (nm)
                 5       11.958
                 6       12.237
                15       24.290
                16       24.359

BLS  38. Photo.HMDS  Ver: 2   Samples: 1-4,7-14,17-20   (0:35+100:00)
         Started: 23-FEB-1995 10:31:58.00

EB   39. Photo.Spin-on  Ver: 11   Samples: 1-4,7-14,17-20   (1:32+24:00)
          Side of wafer to coat: Front
         Started: 24-FEB-1995 06:21:58.00

EB   40. Photo.Expose  Ver: 5   Samples: 1-4,7-14,17-20   (0:37+24:00)
          Mask set identifier: LA2
          Mask-set level: Metal
          Surface to expose: front
         Started: 24-FEB-1995 10:50:50.00
         EB:  Use a 15-second exposure.

EB   41. Photo.Reversal  Ver: 6   Samples: 1-4,7-14,17-20   (2:16+100:00)
         Started: 24-FEB-1995 13:03:04.00
         EB:  Use a 45-second flood exposure.

EB   42. Photo.Inspect  Ver: 1   Samples: 1-4,7-14,17-20   (0:37+100:00)
         Started: 27-FEB-1995 14:30:26.00

JWT  43. Etch.BOE  Ver: 6   Samples: 1-20   (0:05+0:15)
          Side of wafer(s) to monitor for HPO: 5,15frnt
          Etch time (min) [after HPO, if given]: +0.5
         Started: 28-FEB-1995 15:29:00.00
         EB:  Etch time was 30 sec + 30 sec overetch.

JWT  44. Clean.Estek  Ver: 2   Samples: 1-20   (0:07+0:30)
          Program number: 1
         Started: 28-FEB-1995 15:35:58.00
```

```
JWT  45. Deposit.TiPdAg  Ver: 1   Samples: 1-4,7-14,17-20   (3:16+100:00)
          Titanium metal thickness (nm): 100
          Palladium metal thickness (nm): 50
          Silver metal thickness (um): 3
          Side of wafer for deposition: Front
         Started: 28-FEB-1995 15:52:08.00
         JWT- Sheet rho 8.50 milli-ohms, thickness 2.4um, 2.04 u-ohms-cm.

JWT  46. Deposit.Aluminum  Ver: 1   Samples: 1-4,7-14,17-20   (1:16+100:00)
          Desired metal thickness (nm): 500
          Side of wafer for deposition: Back
          Shadow mask: None
         Started:  1-MAR-1995 08:14:10.00
         Sheet ,rho 55.9 milli-ohms, thickness 57nm, 3.21 u-ohms-cm.
         Broke wafer 7 and 20.

BLS  47. Photo.Liftoff  Ver: 4   Samples: 1-4,7-14,17-20   (1:30+100:00)
         Started:  1-MAR-1995 13:36:28.00

         BLS:  Wafer 3,4, and 17 broke during lift-off.  They will not be
         contiued with lot.

BLS  48. Photo.Inspect  Ver: 1   Samples: 1-4,7-14,17-20   (0:15+100:00)
         Started:  1-MAR-1995 14:34:28.00

BLS  49. Furnace.FGA1  Ver: 4   Samples: 1-4,7-14,17-20   (0:59+100:00)
          Forming-gas anneal time (min): 30
          Forming-gas anneal temperature: 400
         Started:  1-MAR-1995 14:44:12.00

BLS  50. Plate.AgPltLa2  Ver: 1   Samples: 1-4,7-14,17-20   (4:00+100:00)
         Number of process batches required: 4
         Started:  2-MAR-1995 06:39:06.00

         BLS:  Wafer 13 broke in box.  It will not be contiued with lot.

JWT  51. Deposit.AR  Ver: 5   Samples: 1-4,7-14,17-20   (3:30+100:00)
          Material: TiO/AlO
          Thickness (nm): 38/70
          Side to coat: Front
         Started:  2-MAR-1995 10:41:40.00

EB   52. Laser.Groove  Ver: 8   Samples: 1-4,7-14,17-20   (2:30+100:00)
          Groove pulse rate (Hz): 5000
          Groove cutting speed (mm/s): 5
          Groove cutting axes: y-only
          Groove cutting pulse energy (mJ): MAX
          Hole drilling pulse rate (Hz): 3000
          Hole drilling time (ms): 100
          Lot scribing time (#wafers*(min/wafer)): 90
          Alignment (0-chuck, #wafers-pattern): 16
          CADD pattern file name w/o extension: LA1Isolt
          CADD layer: 4
          Side of wafer to cut: front
```

```
          Started:  6-MAR-1995 12:52:28.00

EB    53. Laser.Groove  Ver: 8   Samples: 1-4,7-14,17-20   (1:31+100:00)
           Groove pulse rate (Hz): 10000
           Groove cutting speed (mm/s): 5
           Groove cutting axes: y-only
           Groove cutting pulse energy (mJ): MAX
           Hole drilling pulse rate (Hz): 3000
           Hole drilling time (ms): 100
           Lot scribing time (#wafers*(min/wafer)): 90
           Alignment (0-chuck, #wafers-pattern): 0
           CADD pattern file name w/o extension: LA1Isolt
           CADD layer: 5
           Side of wafer to cut: back
          Started:  6-MAR-1995 12:52:40.00

BLS   54. Notify.PDML  Ver: 1   Samples: 1-4,7-14,17-20   (0:05+100:00)
          Started:  6-MAR-1995 13:37:58.00

BLS   55. Measure.SheetRho  Ver: 6   Samples: 5,6,15,16   (0:05+100:00)
           Side of wafer to measure: Both
           Number of points: 5
          Started:  6-MAR-1995 13:38:32.00

          BLS:  Wafer     Mean      StdDev          Wafer     Mean     StdDev
                 No.   (ohms/sq)     (%)             No.   (ohms/sq)   (%)
                  5F      31.88     1.686            5B      32.64    1.748
                  6F      76.72     1.072            6B      157.3    2.846
                 15F      42.63     .8292           15B      45.33    .6692
                 16F      81.31     1.848           16B      132.3    1.313

BLS   56. Measure.HotProbe  Ver: 4   Samples: 5,6,15,16   (0:09+100:00)
           Side of wafer to measure: Both
          Started:  6-MAR-1995 14:00:34.00

          BLS:  Wafers 5 and 15 both sides measured as n-type.  Wafers 6
          and 16 front measured as n-type and back measured as p-type.

BLS   57. Measure.PDML  Ver: 1   Samples: 1-4,7-14,17-20   (0:10+1000:00)
          Started:  6-MAR-1995 14:13:56.00

TOTAL RUN TIME REQUIRED (hours)> 43.6

-- Processing Splits Analysis --

 Split  1: 1,8,14,18  Xtal10.Siemens
 Split  2: 2,10,12,19  Xtal10.Siemens
 Split  3: 3,7,11,20  Xtal10.Siemens
 Split  4: 4,9,13,17  Xtal10.Siemens
 Split  5: 5  Wafer4R.CZn1-10
 Split  6: 6  Wafer4R.CZp8-16
 Split  7: 15  Wafer4R.CZn1-10
 Split  8: 16  Wafer4R.CZp8-16
```

	Split:	1	2	3	4	5	6	7	8
1.	Laser.Groove	*	*	*	*				
2.	Laser.Label	*	*	*	*				
3.	Label.Scribe					*	*	*	*
4.	Clean.Degrease	*	*	*	*				
5.	Etch.HF	*	*	*	*				
6.	Etch.Polish	*	*	*	*				
7.	Etch.KOH	*	*	*	*				
8.	Etch.Polish	*	*	*	*				
9.	Clean.Estek	*	*	*	*				
10.	Measure.BulkRho	*							
11.	Etch.HF	*	*	*	*	*	*	*	*
12.	Etch.IsoEtch	*	*	*	*	*	*	*	*
13.	Etch.HFDip	*	*	*	*	*	*	*	*
14.	Clean.Estek	*	*	*	*	*	*	*	*
15.	Deposit.CVDundop	*	*	*	*	*	*	*	*
16.	Etch.Texture2	*	*	*	*				
17.	Etch.HF	*		*			*		*
18.	Clean.HCl	*	*	*	*	*	*	*	*
19.	Etch.IsoEtch	*	*	*	*	*	*	*	*
20.	Etch.HFDip	*	*	*	*	*	*	*	*
21.	Clean.Estek	*	*	*	*	*	*	*	*
22.	Furnace.PCL1	*	*	*	*	*	*	*	*
23.	Measure.Lifetime	*							
24.	Etch.HF	*		*			*		*
25.	Clean.Estek	*		*			*		*
26.	Deposit.CVDundop	*		*			*		*
27.	Etch.KOH	*		*			*		*
28.	Clean.Estek	*		*			*		*
29.	Measure.HotProbe						*		*
30.	Etch.HF	*	*	*	*	*	*	*	*
31.	Clean.HCl	*	*	*	*	*	*	*	*
32.	Etch.HFDip	*	*	*	*	*	*	*	*
33.	Clean.Estek	*	*	*	*	*	*	*	*
34.	Deposit.Aluminum	*	*	*	*				
35.	Furnace.ALY2	*	*			*	*		
36.	Furnace.ALY2			*	*			*	*
37.	Measure.OxThick					*	*	*	*
38.	Photo.HMDS	*	*	*	*				
39.	Photo.Spin-on	*	*	*	*				
40.	Photo.Expose	*	*	*	*				
41.	Photo.Reversal	*	*	*	*				
42.	Photo.Inspect	*	*	*	*				
43.	Etch.BOE	*	*	*	*	*	*	*	*
44.	Clean.Estek	*	*	*	*	*	*	*	*
45.	Deposit.TiPdAg	*	*	*	*				
46.	Deposit.Aluminum	*	*	*	*				
47.	Photo.Liftoff	*	*	*	*				
48.	Photo.Inspect	*	*	*	*				
49.	Furnace.FGA1	*	*	*	*				
50.	Plate.AgPltLa2	*	*	*	*				
51.	Deposit.AR	*	*	*	*				
52.	Laser.Groove	*	*	*	*				
53.	Laser.Groove	*	*	*	*				

```
 54. Notify.PDML          *  *  *  *
 55. Measure.SheetRho                  *  *  *  *
 56. Measure.HotProbe                  *  *  *  *
 57. Measure.PDML         *  *  *  *

-- Post-Approval Modifications --

MOD_TIME                  MOD_ID   INITIALS   STP      PROC_GRP   PROC_ID
21-FEB-1995 08:56:26.00   Parms    EB              2   Laser      Label

----  End Runsheet  ----
```

APPENDIX 2. PDFL runsheet ("LAPERF11") with process details for experiment that produced 15.7%-efficient, large-area EWT cell using SSI-Cz silicon substrates.

Lot ID: LAPERF11 LAPERF/EWT cells w/ SSI Cz.

Requester: JMG James M. Gee (SMTS) 4-7812
Approved: EB 9-FEB-1996 09:38:56.00
Finished: JMG 21-MAR-1996 17:21:28.00
Samples: 1-15

Lot Materials:

Wafer4R.CZp8-16 Samples: 1,6,11
100-mm (4-in) round silicon wafer
SEH CZ p-type (100) 8-16 ohm-cm 625 um
Xtal10.Siemens Samples: 2-5,7-10,12-15
10-cm crystalline silicon
CZ silicon grown by Siemens Solar
JMG: Please use material from Group C.

Lot References: LAPERF10

Purpose: (JMG, 01/30/96) This lot is part of our project to develop a large-area 18%-efficient emitter wrap-through (EWT) cell, and part of the SSI CRADA project. This lot fabricates PERF (passivated emitter and rear floating) and EWT cells on SSI-Cz material.

Experiment: (JMG, 01/30/96) This lot examines two factors -- diffusion and cell type. The diffusion includes a heavy and a light diffusion, and cell type include PERF and EWT. The KOH-etch-mask oxide is replaced with a fresh CVD oxide. The fresh oxide will hopefully cover any KOH-etched defects. The 800C dry oxidations prior to CVD steps were removed in order to minimize the number of temperature excursions for the SSI Cz material.

The splits are as follows:

Wafers	Diffusion	Cell
2,9,12	Light	PERF
3,7,14	Light	EWT
4,10,15	Heavy	PERF
5,8,13	Heavy	EWT
1,6,11	Controls	

Summary: (JMG, 03/21/96) The attached spreadsheet contains a summary of the IV measurements. Also attached are plots of the data. This lot fabricated our best EWT cells to date, with the best cell achieving an efficiency of 15.7% (no corrections included). The improved performance is due to significantly

reduced shunt conductance. As an example, the reduction in performance of W7 is only around 0.2% absolute due to the shunt conductance of 25 ohms. The series resistance was a much larger limitation to the FF. The series resistance's were between 1.1 and 3.0 ohm*cm2, which reduced the efficiency by between 1.0 and 2.5% absolute, respectively. The higher series resistance might be due to the p-type substrate contact; this lot used material with a higher bulk resistivity compared to past lots. LAPERF12 is fabricating EWT and LAPERF cells on low-resistivity substrates to test this hypothesis.

LBIC scans of the back surface was still able to find shunts, which could be associated with either photodefects or deep pits. (See attached LBIC scans and photomicrographs.) A particularly interesting plot compares the IQE of EWT and LAPERF cell; the EWT cell has enhanced collection in the red due to collection at the rear junction.

EB 1. Etch.HF-Timed Ver: 2 Samples: 2-5,7-10,12-15 (0:05+0:15)
Etch time (minutes): 1
Started: 9-FEB-1996 09:50:20.00

EB 2. Etch.Polish Ver: 6 Samples: 2-5,7-10,12-15 (0:13+0:30)
Nitric:HF mixture ratio: 15:1
Time in solution (minutes): 8
Started: 9-FEB-1996 09:50:32.00
EB: Etched an additional 8 minutes (after multiround grooving) trying to get samples shiny. They are much better. Backs have marks that look like scratchesto the naked eye but not under the microscope. W15 had to be restarted because of a chip at one edge when I broke it out. I noticed that there is some silicon dust on the plexiglass block where the wafers are placed for breaking out. I put a piece of paper over the surface of the block to see if that will help.

EB 3. Clean.Estek Ver: 2 Samples: 2-5,7-10,12-15 (0:07+100:00)
Program number: 1
Started: 9-FEB-1996 09:50:50.00

EB 4. Laser.Groove Ver: 8 Samples: 2-5,7-10,12-15 (0:24+100:00)
Groove pulse rate (Hz): 10000
Groove cutting speed (mm/s): 5
Groove cutting axes: X
Groove cutting pulse energy (mJ): Max
Hole drilling pulse rate (Hz): 3000
Hole drilling time (ms): 150
Lot scribing time (#wafers*(min/wafer)): 24
Alignment (0-chuck, #wafers-pattern): 0
CADD pattern file name w/o extension: MultiRnd
CADD layer: 4
Side of wafer to cut: front
Started: 9-FEB-1996 09:55:30.00

EB 5. Laser.Label Ver: 2 Samples: 2-5,7-10,12-15 (0:22+100:00)
Pulse Rate: 10000
Cutting Speed: 5
Laser Current: 20
Cutting Angles: X-Y
CADD layer (wafer): Wafer-#
CADD layer (lot): 61
Started: 12-FEB-1996 07:36:02.00

EB 6. Laser.Groove Ver: 8 Samples: 2,4,9,10,12,15 (0:12+100:00)
Groove pulse rate (Hz): 15000
Groove cutting speed (mm/s): 5
Groove cutting axes: X-Y
Groove cutting pulse energy (mJ): Max
Hole drilling pulse rate (Hz): 3000
Hole drilling time (ms): 150
Lot scribing time (#wafers*(min/wafer)): 12
Alignment (0-chuck, #wafers-pattern): 0
CADD pattern file name w/o extension: LAPERHEX
CADD layer: 2
Side of wafer to cut: back
Started: 12-FEB-1996 08:05:48.00
JMG: This step scribes alignment targets for PERF cells. Please be sure the wafer flats are flush against the jig to ensure good front-to-back alignment.

EB 7. Laser.Groove Ver: 8 Samples: 2,4,9,10,12,15 (0:12+100:00)
Groove pulse rate (Hz): 15000
Groove cutting speed (mm/s): 5
Groove cutting axes: X-Y
Groove cutting pulse energy (mJ): Max
Hole drilling pulse rate (Hz): 3000
Hole drilling time (ms): 150
Lot scribing time (#wafers*(min/wafer)): 12
Alignment (0-chuck, #wafers-pattern): 0
CADD pattern file name w/o extension: LAPERHEX
CADD layer: 1
Side of wafer to cut: front
Started: 12-FEB-1996 08:29:32.00
JMG: This step scribes alignment targets for PERF cells. Please be sure the wafer flats are flush against the jig to ensure good front-to-back alignment.

BLS 8. Label.Scribe Ver: 4 Samples: 1,6,11 (0:06+1000:00)
Started: 12-FEB-1996 08:52:04.00

BLS 9. Measure.BulkRho Ver: 2 Samples: 2,9,12 (0:11+100:00)
Side of wafer to measure: Front
Number of points: 5
Started: 12-FEB-1996 08:54:38.00

BLS:	Wafer No.	Mean (ohms/sq)	StdDev (%)	Thickness (um)	BulkRho (ohms-cm)
	2	27.30	1.371	287	0.78

9	26.18	1.178	302	0.79
12	26.46	1.930	300	0.79

```
BLS  10. Etch.HF-HPO  Ver: 1   Samples: 1-15   (0:05+0:15)
          Wafer number to be monitored for HPO: 2
          Wafer side to be monitored for HPO: both
          Overetch time after HPO (minutes): 1
         Started: 12-FEB-1996 09:06:06.00

         BLS:  Wafers etched HPO in 15 seconds plus 1 minute after HPO.

BLS  11. Etch.IsoEtch  Ver: 4   Samples: 1-15   (0:15+0:30)
          Nitric:HF mixture ratio: 100:1
          Time in solution (minutes): 10
         Started: 12-FEB-1996 09:09:54.00

BLS  12. Etch.HFDip  Ver: 6   Samples: 1-15   (0:06+0:15)
          H2O:HF mixture ratio: 50:1
          Etch time (seconds): 60
         Started: 12-FEB-1996 09:22:32.00

BLS  13. Clean.Estek  Ver: 2   Samples: 1-15   (0:07+1:00)
          Program number: 1
         Started: 12-FEB-1996 09:26:02.00

BLS  14. Deposit.CVDundop  Ver: 7   (0:21+100:00)
         Samples: 1,3,5,7,8,13,14
          Time of deposition (min): 4
          Surface receiving deposition: Back
          Expected film thickness (nm): 500+
         Started: 12-FEB-1996 09:34:42.00

         BLS:  Run       Wafer       OxThickness   R.I.     Deposit time
               No.         No.           (nm)                   (min)
              4309      control         527.97     1.561        4.2
              4310  1,3,5,7,8,13,14     514.34     1.544        4.2

BLS  15. Clean.HCl  Ver: 5   (0:15+0:30)
         Samples: 1,3,5,7,8,13,14
          Temperature of solution (C): 50
          Time in solution (min): 5
         Started: 12-FEB-1996 09:49:14.00

BLS  16. Clean.Estek  Ver: 2   (0:07+1:00)
         Samples: 1,3,5,7,8,13,14
          Program number: 1
         Started: 12-FEB-1996 09:56:50.00

BLS  17. Deposit.CVDundop  Ver: 7   (0:21+100:00)
         Samples: 1,3,5,7,8,13,14
          Time of deposition (min): 4.2
          Surface receiving deposition: Front
          Expected film thickness (nm): 500+
         Started: 12-FEB-1996 10:09:20.00
```

BLS:	Run No.	Wafer No.	OxThickness (nm)	R.I.
	4311	1,3,5,7,8,13,14	511.43	1.565

BLS 18. Clean.HCl Ver: 5 (0:15+0:30)
Samples: 1,3,5,7,8,13,14
Temperature of solution (C): 50
Time in solution (min): 5
Started: 12-FEB-1996 10:22:28.00

BLS 19. Etch.HFDip Ver: 6 (0:06+0:15)
Samples: 1,3,5,7,8,13,14
H2O:HF mixture ratio: 50:1
Etch time (seconds): 30
Started: 12-FEB-1996 10:34:04.00

BLS 20. Clean.Estek Ver: 2 (0:07+1:00)
Samples: 1,3,5,7,8,13,14
Program number: 1
Started: 12-FEB-1996 10:40:06.00

BLS 21. Furnace.DRY1 Ver: 5 (1:32+100:00)
Samples: 1,3,5,7,8,13,14
Oxidation temperature (C): 800
Oxidation time (min): 30
In-situ inert anneal time (min): 15
Tube number: 3
Started: 12-FEB-1996 10:54:36.00

EB 22. Laser.Groove Ver: 8 Samples: 3,5,7,8,13,14 (1:00+100:00)
Groove pulse rate (Hz): 15000
Groove cutting speed (mm/s): 5
Groove cutting axes: X-Y
Groove cutting pulse energy (mJ): Max
Hole drilling pulse rate (Hz): 3000
Hole drilling time (ms): 150
Lot scribing time (#wafers*(min/wafer)): 60
Alignment (0-chuck, #wafers-pattern): 0
CADD pattern file name w/o extension: LAPERHEX
CADD layer: 7
Side of wafer to cut: back
Started: 12-FEB-1996 12:56:46.00
JMG: This step scribes alignment targets and vias. It is very important that the samples are flush against the jig since this will determine the front-to-back alignment.

BLS 23. Laser.Groove Ver: 8 Samples: 3,5,7,8,13,14 (0:12+100:00)
Groove pulse rate (Hz): 15000
Groove cutting speed (mm/s): 5
Groove cutting axes: x-y
Groove cutting pulse energy (mJ): max
Hole drilling pulse rate (Hz): 3000
Hole drilling time (ms): 100

```
          Lot scribing time (#wafers*(min/wafer)): 12
          Alignment (0-chuck, #wafers-pattern): 0
          CADD pattern file name w/o extension: LAPERHEX
          CADD layer: 1
          Side of wafer to cut: front
         Started: 13-FEB-1996 06:59:34.00

BLS  24. Etch.KOH  Ver: 8    (0:35+0:30)
         Samples: 1,3,5,7,8,13,14
          H2O:KOH mixture ratio: 2:1
          Temperature of solution (C): 70
          Time in solution (minutes): 30
         Started: 13-FEB-1996 07:37:50.00

BLS  25. Etch.HF-HPO  Ver: 1   Samples: 1-15   (0:05+0:15)
          Wafer number to be monitored for HPO: 1
          Wafer side to be monitored for HPO: both
          Overetch time after HPO (minutes): 1
         Started: 13-FEB-1996 08:12:10.00

         BLS:  Wafers etched HPO in 6 minutes and 45 seconds plus 1
         minute after HPO.

BLS  26. Clean.HCl  Ver: 5   Samples: 1-15   (0:15+0:30)
          Temperature of solution (C): 50
          Time in solution (min): 5
         Started: 13-FEB-1996 08:22:26.00

BLS  27. Etch.HFDip  Ver: 6   Samples: 1-15   (0:06+0:15)
          H2O:HF mixture ratio: 50:1
          Etch time (seconds): 30
         Started: 13-FEB-1996 08:35:14.00

BLS  28. Clean.Estek  Ver: 2   Samples: 1-15   (0:07+1:00)
          Program number: 1
         Started: 13-FEB-1996 08:39:06.00

BLS  29. Deposit.CVDundop  Ver: 7   Samples: 1-15   (1:00+100:00)
         Number of process batches required: 3
          Time of deposition (min): 2.5
          Surface receiving deposition: Back
          Expected film thickness (nm): 300
         Started: 13-FEB-1996 08:41:50.00

         BLS:  Run        Wafer      OxThickness   R.I.
               No.         No.          (nm)
              4312       control        326.42     1.567
              4313        1-7           348.71     1.435
              4314        8-15          (no control)

BLS  30. Clean.HCl  Ver: 5   Samples: 1-15   (0:15+0:30)
          Temperature of solution (C): 50
          Time in solution (min): 5
         Started: 13-FEB-1996 11:08:26.00
```

```
BLS  31. Etch.HFDip  Ver: 6   Samples: 1-15   (0:06+0:15)
          H2O:HF mixture ratio: 50:1
          Etch time (seconds): 30
         Started: 13-FEB-1996 11:15:56.00

BLS  32. Clean.Estek  Ver: 2   Samples: 1-15   (0:07+1:00)
          Program number: 1
         Started: 13-FEB-1996 11:18:58.00

BLS  33. Furnace.DRY1  Ver: 5   Samples: 1-15   (1:32+100:00)
          Oxidation temperature (C): 800
          Oxidation time (min): 30
          In-situ inert anneal time (min): 15
          Tube number: 3
         Started: 13-FEB-1996 11:33:46.00

EB   34. Photo.HMDS  Ver: 2   Samples: 2-5,7-10,12-15   (0:35+100:00)
         Started: 13-FEB-1996 12:39:42.00

EB   35. Photo.Spin-on  Ver: 11   Samples: 2-5,7-10,12-15   (1:24+24:00)
          Side of wafer to coat: Back
         Started: 13-FEB-1996 13:12:08.00
         EB:  Wafers 3, 5, 7, 8, 13, and 14 have holes.  Use tape to
         protect fronts on these wafers.

         EB:  W7, 12, and 14 had to be reworked because of photoresist
         sticking to the mask.

EB   36. Photo.Align  Ver: 6   Samples: 2-5,7-10,12-15   (0:41+24:00)
          Mask set identifier: LAPhWT
          Mask set level: p-
          Surface to expose: back
          Alignment target: laser
         Started: 13-FEB-1996 14:32:10.00

EB   37. Photo.Develop  Ver: 9   Samples: 2-5,7-10,12-15   (0:45+100:00)
         Started: 16-FEB-1996 07:58:08.00

EB   38. Photo.Inspect  Ver: 1   Samples: 2-5,7-10,12-15   (0:15+100:00)
         Started: 16-FEB-1996 08:23:22.00
         EB:  W14 had large area where photoresist did not stick.  Will
         discard rather than rework again.

EB   39. Etch.BOE-HPO  Ver: 1   Samples: 1-5,7-10,12-15   (0:10+0:15)
          Wafer to monitor to HPO: 1
          Side to monitor for HPO: back
          Overetch time (after HPO): 1
         Started: 16-FEB-1996 09:16:16.00
         EB:  Etch time was 3 min + 1 min overetch.  I accidentally put
         W6 and 11 in this etch for the first 50 sec.  I have added a
         comment to step 60 for the overetch time to be 2 min instead of
         1.
```

```
EB   40. Clean.Estek  Ver: 2   Samples: 1-5,7-10,12-15   (0:07+100:00)
          Program number: 1
         Started: 16-FEB-1996 10:25:42.00

EB   41. Photo.Inspect  Ver: 1   Samples: 2-5,7-10,12-15   (0:15+100:00)
         Started: 16-FEB-1996 10:28:42.00

EB   42. Photo.PRStrip  Ver: 4   Samples: 2-5,7-10,12-15   (0:20+100:00)
          Time in 1st acetone bath (min): 10
          Time in 2nd acetone bath (min): 5
          Time in propanol bath (min): 5
         Started: 16-FEB-1996 10:41:00.00

EB   43. Etch.IsoEtch  Ver: 4   Samples: 1-15   (0:06+1:00)
          Nitric:HF mixture ratio: 100:1
          Time in solution (minutes): 0.5
         Started: 16-FEB-1996 10:54:10.00

EB   44. Clean.Estek  Ver: 2   Samples: 1-15   (0:07+100:00)
          Program number: 1
         Started: 16-FEB-1996 10:56:18.00

EB   45. Etch.Texture2  Ver: 4   Samples: 2-5,7-10,12-15   (0:30+100:00)
          Mixture ratio (H2O:KOH:IPA): 125:2:5
          Temperature of solution: 70
          Time in solution (min): 15
         Started: 16-FEB-1996 11:03:26.00
         EB:  Texture is not great on this lot.  The solution was about
         due to be changed.

EB   46. Clean.HCl  Ver: 5   Samples: 1-15   (0:15+0:30)
          Temperature of solution (C): 50
          Time in solution (min): 5
         Started: 16-FEB-1996 11:35:40.00

EB   47. Etch.IsoEtch  Ver: 4   Samples: 1-15   (0:06+1:00)
          Nitric:HF mixture ratio: 100:1
          Time in solution (minutes): 0.5
         Started: 16-FEB-1996 11:45:16.00

EB   48. Etch.HFDip  Ver: 6   Samples: 1-15   (0:06+0:15)
          H2O:HF mixture ratio: 50:1
          Etch time (seconds): 30
         Started: 16-FEB-1996 11:47:54.00

EB   49. Clean.Estek  Ver: 2   Samples: 1-15   (0:07+1:00)
          Program number: 1
         Started: 16-FEB-1996 11:51:52.00

EB   50. Furnace.PCL1  Ver: 6   (4:58+100:00)
         Samples: 1-3,6,7,9,12,14
          Temperature (C): 900
          POCl3 deposition time (min): 8
          First N2 soak time (min): 1
```

```
          O2 soak time (min): 200
          Final N2 soak time (min): 15
          Wafer orientation: FaceFace
         Started: 16-FEB-1996 12:04:28.00
         EB:  O2 soak was 2 hours instead of 200 minutes (operator error!)

BLS  51. Furnace.PCL1  Ver: 6   (5:11+100:00)
         Samples: 4,5,8,10,11,13,15
          Temperature (C): 900
          POCl3 deposition time (min): 8
          First N2 soak time (min): 15
          O2 soak time (min): 200
          Final N2 soak time (min): 15
          Wafer orientation: FaceFace
         Started: 19-FEB-1996 06:51:24.00

EB   52. Measure.Ellipse  Ver: 9   Samples: 1,6,11   (0:08+100:00)
          Expected index of refraction: 1.462
          Expected film thickness (nm): 100
          Side of wafer to measure: front
         Started: 19-FEB-1996 12:46:26.00
         EB:  Wafer   Ox Th (nm)   R.I.
                1       86.56     1.4754
                6       86.93     1.4768
               11      122.26     1.4717

EB   53. Photo.HMDS  Ver: 2   Samples: 2-5,7-10,12-15   (0:35+100:00)
         Started: 19-FEB-1996 12:52:36.00

EB   54. Photo.Spin-on  Ver: 11   Samples: 2-5,7-10,12-15   (1:24+24:00)
          Side of wafer to coat: front
         Started: 19-FEB-1996 13:38:44.00
         EB:  Use tape to protect backs of Wafers 3, 5, 7, 8, 13, 14.

EB   55. Photo.Align  Ver: 6   Samples: 2-5,7-10,12-15   (0:41+24:00)
          Mask set identifier: LA2
          Mask set level: metal
          Surface to expose: front
          Alignment target: laser
         Started: 20-FEB-1996 07:23:04.00

EB   56. Photo.Spin-on  Ver: 11   Samples: 2-5,7-10,12-15   (1:24+24:00)
          Side of wafer to coat: Back
         Started: 20-FEB-1996 08:06:56.00
         EB:  Use tape to protect fronts of Wafers 3, 5, 7, 8, 13, 14.

         EB:  W10 has a circular defect on the front side which happened
         on the spinner.  It stuck to the spinner chuck for some reason.

EB   57. Photo.Align  Ver: 6   Samples: 2-5,7-10,12-15   (0:41+24:00)
          Mask set identifier: LAPhWT
          Mask set level: p+
          Surface to expose: back
          Alignment target: mask
```

Started: 20-FEB-1996 09:32:36.00

EB 58. Photo.Reversal Ver: 6 Samples: 2-5,7-10,12-15 (2:08+100:00)
Started: 20-FEB-1996 09:58:56.00
EB: Flood-expose both sides.

BLS 59. Photo.Inspect Ver: 1 Samples: 2-5,7-10,12-15 (0:08+100:00)
Started: 20-FEB-1996 13:22:12.00

BLS 60. Etch.BOE-HPO Ver: 1 Samples: 1-15 (0:10+0:15)
Wafer to monitor to HPO: 6,11
Side to monitor for HPO: both
Overetch time (after HPO): 2
Started: 20-FEB-1996 13:37:24.00
JMG: Please note the overetch time is 2 MINUTES!! The time was increased because the etch control wafers were accidentally exposed to 50 seconds of BOE in a prior step.

BLS: Wafers etched HPO in 2 minutes and 15 seconds plus 2 minutes after HPO.

BLS 61. Clean.Estek Ver: 2 Samples: 1-15 (0:07+1:00)
Program number: 1
Started: 20-FEB-1996 13:51:50.00

JWT 62. Deposit.MetlEvap Ver: 3 Samples: 2-5,7-10,12-15 (3:00+100:00)
Metal thicknesses (um): .2/.2/2
Side of wafer: Back!!!!
Type of metals (3 max): AlTiAg
Define shadow mask: None
Started: 20-FEB-1996 13:55:40.00
JWT- Sheet rho 6.96 milli-ohms, thickness 3.1um, 2.20 u-ohms-cm.

JWT 63. Deposit.TiPdAg Ver: 1 Samples: 2-5,7-10,12-15 (2:18+100:00)
Titanium metal thickness (nm): 100
Palladium metal thickness (nm): 100
Silver metal thickness (um): 1
Side of wafer for deposition: Front
Started: 20-FEB-1996 15:15:42.00
JWT- Sheet rho 8.80 milli-ohms, thickness 1.7um, 1.52 u-ohms-cm.

BLS 64. Photo.Liftoff Ver: 4 Samples: 2-5,7-10,12-15 (1:10+100:00)
Started: 21-FEB-1996 06:39:56.00
EB: Both sides need lift-off.

BLS 65. Photo.Inspect Ver: 1 Samples: 2-5,7-10,12-15 (0:11+100:00)
Started: 21-FEB-1996 07:51:40.00

BLS 66. Notify.PDML Ver: 1 Samples: 2-5,7-10,12-15 (0:05+100:00)
Started: 21-FEB-1996 07:52:14.00

BLS 67. Furnace.FGA1 Ver: 4 Samples: 2-5,7-10,12-15 (1:04+100:00)
Forming-gas anneal time (min): 30
Forming-gas anneal temperature: 400

Started: 21-FEB-1996 07:55:52.00

BLS 68. Plate.AgPltLa2 Ver: 1 Samples: 2-5,7-10,12-15 (3:00+100:00)
Number of process batches required: 3
Started: 21-FEB-1996 09:08:26.00

BLS: Wafers 3,4,5 and 8 have curls of silver on some of their gridline. Continued lot per WKS.

BLS 69. Laser.Groove Ver: 8 Samples: 2-5,7-10,12-15 (1:12+100:00)
Groove pulse rate (Hz): 12000
Groove cutting speed (mm/s): 5
Groove cutting axes: y-only
Groove cutting pulse energy (mJ): MAX
Hole drilling pulse rate (Hz): 3000
Hole drilling time (ms): 100
Lot scribing time (#wafers*(min/wafer)): 24
Alignment (0-chuck, #wafers-pattern): 12
CADD pattern file name w/o extension: LAPER
CADD layer: 6
Side of wafer to cut: back
Started: 22-FEB-1996 10:18:00.00
EB: Must align to pattern on each wafer. Check the depth of the cut on the first sample. It should go only half-way through.

BLS 70. Measure.SheetRho Ver: 6 Samples: 1,6,11 (0:06+100:00)
Side of wafer to measure: Both
Number of points: 5
Started: 22-FEB-1996 13:55:24.00

BLS:

Wafer No.	Mean (ohms/sq)	StdDev (%)	Wafer No.	Mean (ohms/sq)	StdDev (%)
1F	119.2	2.374	1B	71.64	4.701
6F	117.0	2.964	6B	140.8	.1214
11F	27.90	.9465	11B	144.9	.2826

BLS 71. Measure.HotProbe Ver: 4 Samples: 1,6,11 (0:08+100:00)
Side of wafer to measure: Both
Started: 22-FEB-1996 13:55:38.00

BLS:

Wafer	Measured	Wafer	Measured
1F	n-type	1B	n-type
6F	n-type	6B	p-type
11F	n-type	11B	p-type

BLS 72. Measure.PDML Ver: 1 Samples: 2-5,7-10,12-15 (0:10+1000:00)
Started: 22-FEB-1996 13:55:48.00

TOTAL RUN TIME REQUIRED (hours)> 46.6

-- Processing Splits Analysis --

Split 1: 1 Wafer4R.CZp8-16
Split 2: 2,9,12 Xtal10.Siemens

```
Split  3: 3,7,14  Xtal10.Siemens
Split  4: 4,10,15  Xtal10.Siemens
Split  5: 5,8,13  Xtal10.Siemens
Split  6: 6  Wafer4R.CZp8-16
Split  7: 11  Wafer4R.CZp8-16
```

Split:	1	2	3	4	5	6	7
1. Etch.HF-Timed		*	*	*	*		
2. Etch.Polish		*	*	*	*		
3. Clean.Estek		*	*	*	*		
4. Laser.Groove		*	*	*	*		
5. Laser.Label		*	*	*	*		
6. Laser.Groove		*		*			
7. Laser.Groove		*		*			
8. Label.Scribe	*					*	*
9. Measure.BulkRho		*					
10. Etch.HF-HPO	*	*	*	*	*	*	*
11. Etch.IsoEtch	*	*	*	*	*	*	*
12. Etch.HFDip	*	*	*	*	*	*	*
13. Clean.Estek	*	*	*	*	*	*	*
14. Deposit.CVDundop	*		*		*		
15. Clean.HCl	*		*		*		
16. Clean.Estek	*		*		*		
17. Deposit.CVDundop	*		*		*		
18. Clean.HCl	*		*		*		
19. Etch.HFDip	*		*		*		
20. Clean.Estek	*		*		*		
21. Furnace.DRY1	*		*		*		
22. Laser.Groove			*		*		
23. Laser.Groove			*		*		
24. Etch.KOH	*		*		*		
25. Etch.HF-HPO	*	*	*	*	*	*	*
26. Clean.HCl	*	*	*	*	*	*	*
27. Etch.HFDip	*	*	*	*	*	*	*
28. Clean.Estek	*	*	*	*	*	*	*
29. Deposit.CVDundop	*	*	*	*	*	*	*
30. Clean.HCl	*	*	*	*	*	*	*
31. Etch.HFDip	*	*	*	*	*	*	*
32. Clean.Estek	*	*	*	*	*	*	*
33. Furnace.DRY1	*	*	*	*	*	*	*
34. Photo.HMDS		*	*	*	*		
35. Photo.Spin-on		*	*	*	*		
36. Photo.Align		*	*	*	*		
37. Photo.Develop		*	*	*	*		
38. Photo.Inspect		*	*	*	*		
39. Etch.BOE-HPO	*	*	*	*	*		
40. Clean.Estek	*	*	*	*	*		
41. Photo.Inspect		*	*	*	*		
42. Photo.PRStrip		*	*	*	*		
43. Etch.IsoEtch	*	*	*	*	*	*	*
44. Clean.Estek	*	*	*	*	*	*	*
45. Etch.Texture2		*	*	*	*		
46. Clean.HCl	*	*	*	*	*	*	*
47. Etch.IsoEtch	*	*	*	*	*	*	*

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 48. Etch.HFDip          *  *  *  *  *  *  *
 49. Clean.Estek         *  *  *  *  *  *  *
 50. Furnace.PCL1        *  *  *        *
 51. Furnace.PCL1                 *  *     *
 52. Measure.Ellipse     *                 *  *
 53. Photo.HMDS             *  *  *  *
 54. Photo.Spin-on          *  *  *  *
 55. Photo.Align            *  *  *  *
 56. Photo.Spin-on          *  *  *  *
 57. Photo.Align            *  *  *  *
 58. Photo.Reversal         *  *  *  *
 59. Photo.Inspect          *  *  *  *
 60. Etch.BOE-HPO        *  *  *  *  *  *  *
 61. Clean.Estek         *  *  *  *  *  *  *
 62. Deposit.MetlEvap       *  *  *  *
 63. Deposit.TiPdAg         *  *  *  *
 64. Photo.Liftoff          *  *  *  *
 65. Photo.Inspect          *  *  *  *
 66. Notify.PDML            *  *  *  *
 67. Furnace.FGA1           *  *  *  *
 68. Plate.AgPltLa2         *  *  *  *
 69. Laser.Groove           *  *  *  *
 70. Measure.SheetRho    *                 *  *
 71. Measure.HotProbe    *                 *  *
 72. Measure.PDML           *  *  *  *

-- Post-Approval Modifications --

MOD_TIME                  MOD_ID   INITIALS   STP      PROC_GRP   PROC_ID
16-FEB-1996 10:39:12.00   Parms    EB            60   Etch       BOE-HPO
12-FEB-1996 07:36:32.00   Delete   EB             8   Etch       Polish
12-FEB-1996 07:35:10.00   Delete   EB             5   Laser      Label
12-FEB-1996 07:35:00.00   Insert   EB             5   Laser      Label
 9-FEB-1996 09:55:10.00   Insert   EB             8   Etch       Polish

----  End Runsheet  ----
□
```

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