Hardware Design and Implementation of the Closed-Orbit Feedback System at APS*

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Abstract. The Advanced Photon Source (APS) storage ring will utilize a closed-orbit feedback system in order to produce a more stable beam. The specified orbit measurement resolution is 25 microns for global feedback and 1 micron for local feedback. The system will sample at 4 kHz and provide a correction bandwidth of 100 Hz. At this bandwidth, standard rf BPMs will provide a resolution of 0.7 micron, while specialized miniature BPMs positioned on either side of the insertion devices for local feedback will provide a resolution of 0.2 micron (1). The measured BPM noise floor for standard BPMs is 0.06 micron per root hertz mA. Such a system has been designed, simulated, and tested on a small scale (2). This paper covers the actual hardware design and layout of the entire closed-loop system. This includes commercial hardware components, in addition to many components designed and built in-house. The paper will investigate the large-scale workings of all these devices, as well as an overall view of each piece of hardware used.

INTRODUCTION

The Advanced Photon Source (APS) is a third-generation synchrotron light source. It is characterized by a low positron beam emittance, and hence a high-brightness x-ray beam. It is of vital importance to sustain transverse stability of the positron beam. This can be done using a closed-loop feedback system. The system at APS incorporates both global and local correction systems (2) to achieve its goal. The system has available 360 rf beam position monitors (rf BPMs), two photon position monitors for each x-ray beamline (up to 70 beamlines), and 318 dipole corrector magnets. An example of the ring with BPMs and corrector magnets is shown in Fig. 1. Miniature rf BPMs are located on each side of each insertion device (wiggler or undulator) in order to increase measurement resolution for the local feedback around these devices.

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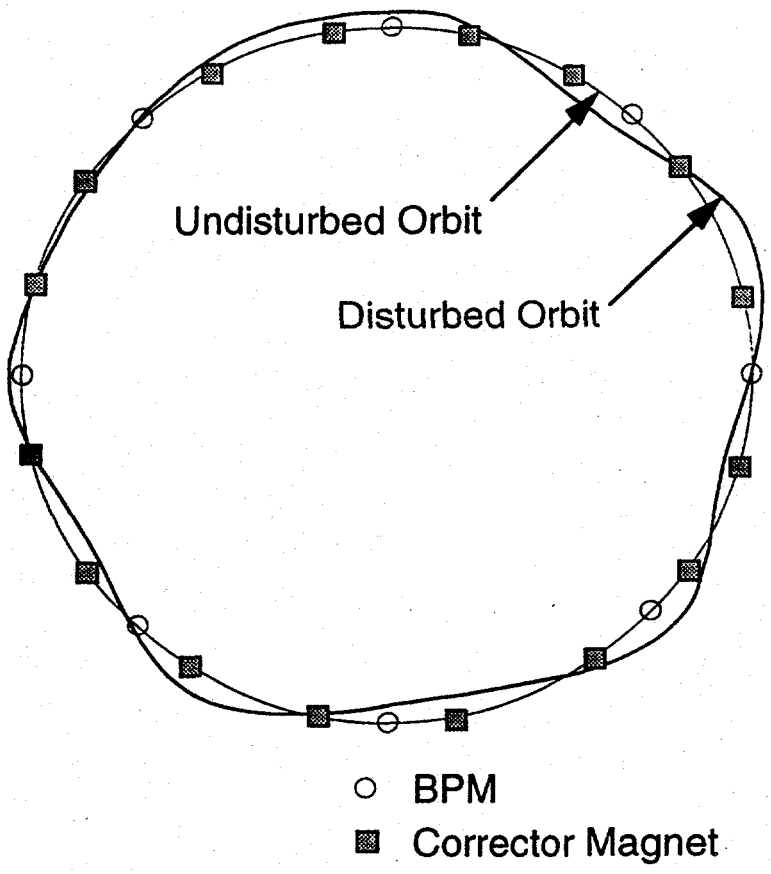

FIGURE 1. BPMs and corrector magnets for global beam position feedback.

The closed-orbit correction system as a whole is comprised of 20 VME crates covering 40 sectors (1104-m circumference). Each sector contains one bending magnet (for x-ray extraction) and one insertion device (either wiggler or undulator), leaving each feedback crate to cover two sectors. The design of each crate is the same thus producing an evenly distributed computing system. A diagram of a two-sectored controlled feedback system is shown in Fig. 2. Note that the two sectors are always an odd sector followed by an even sector. Figure 3 shows the layout of the feedback front panel. Figure 4 displays an aerial view of the crate. The front panel is located at the top the figure. An explanation of the various boards shown in Figs. 3 and 4 follows.

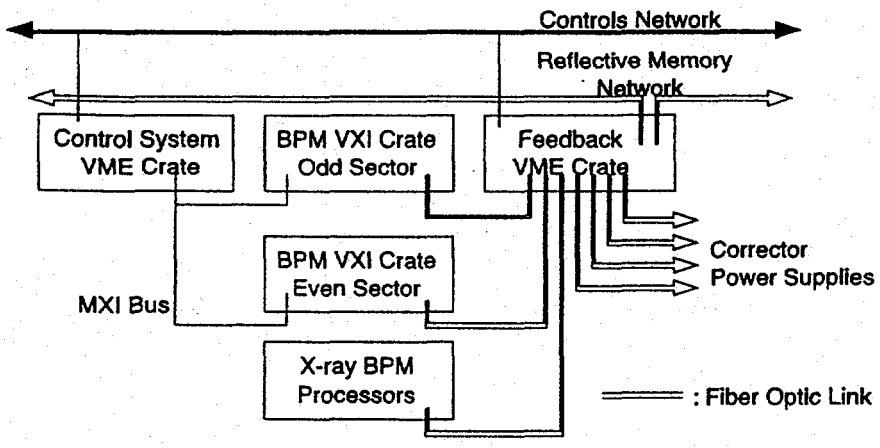

FIGURE 2. Hardware configuration of the beam position feedback system.

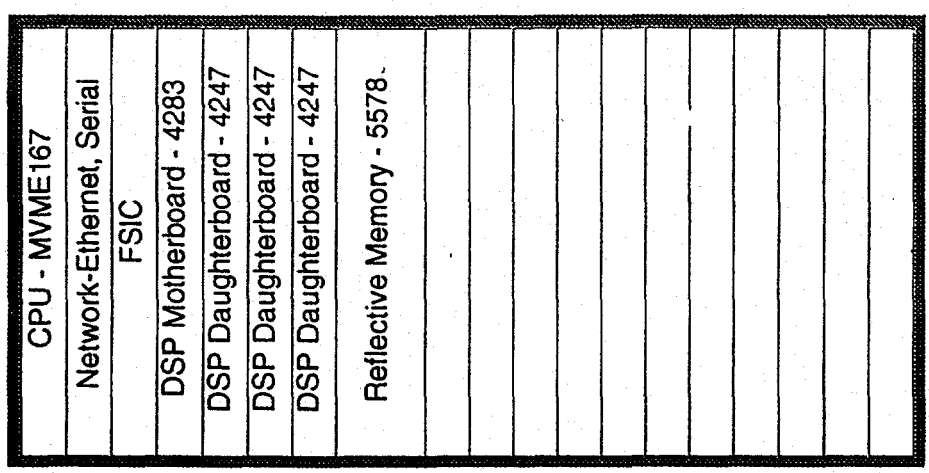

FIGURE 3. The front side of an orbit feedback crate.

FEEDBACK HARDWARE COMPONENTS

The entire system runs on a 4-kHz clock brought into the front panel of the feedback system interface controller (FSIC) (see Fig. 3). One feedback loop is thus comprised of 250 μs: the data acquisition (from the memory scanner interfaces (MSIs) and reflective memory boards) takes 50 μs, the calculation of the corrector strength by the various digital signal processors (DSPs) takes 100 μs, and the passing of the data to the power supply interface and moving of the magnets takes another 100 μs.

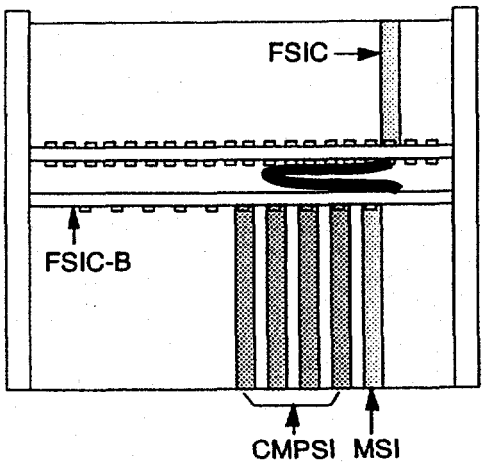

FIGURE 4. The feedback interface boards FSIC, FSIC-B, MSI, and CMPSI installed in the feedback crate (aerial view).

Each piece of hardware, whether commercially produced or manufactured and tested in house, plays a vital role in the closed-orbit feedback system. These will be covered now.

Hardware Components

MS, MSI, FSIC, and FSIC-B

Data can be acquired from either the memory scanner (MS) or the x-ray photon monitors. Currently information is only gathered from the MS as the x-ray BPM interface is not yet complete. The MS sits in a nearby VXI crate and obtains beam position data from the signal conditioning and digitizing units (SCDUs). The MS passes information at the rate of 200 Mbits/s over a fiber-optic cable to the MSI (see Fig. 4). The MSI has two channels: one for the odd sector and one for the even sector. This information is passed through the feedback system interface controller backplane (FSIC-B) (see Fig. 4) and through the FSIC (see Figs. 3 and 4) to the DSP motherboard. Each MSI is capable of handling transverse horizontal and vertical data from eight SCDUs. Since there are eighteen SCDUs in two sectors, two MSIs will usually be needed for each feedback crate.

Reflective Memory

The reflective memory is a high-speed, daisy-chained data transmission device and storage vessel for all beam position values. Each of the 20 feedback crates has one double-wide slot VME reflective memory. These commercially available boards form a network for high-speed communications between the feedback crates. APS uses the VMIC model 5578 boards which have a data transfer rate of 26 Mbytes/s in the non-redundant mode and 13 Mbytes/s in the redundant mode. Figure 5 shows a typical daisy-chained reflective memory network. Each node contains one reflective memory board.

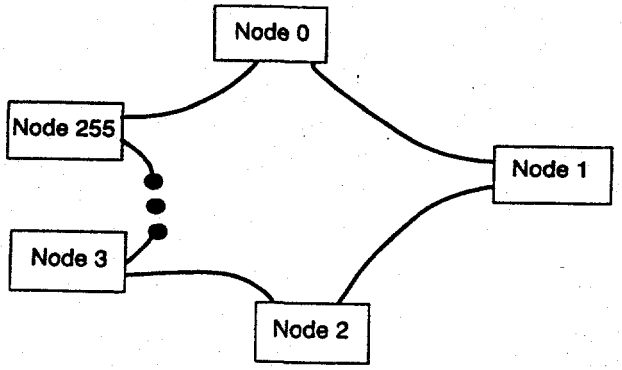

FIGURE 5. Example reflective memory network with 256 nodes.

DSP Motherboards and Daughterboards

The DSP motherboards and daughterboards are the heart of the feedback system. Each is based on the Texas Instruments' TMS320C30 floating point DSP. The motherboard has one of these processors while each daughterboard has two processors. The motherboard is capable of a peak processing power of 40 Mflops and contains 8 Mbytes of dynamic random-access memory (DRAM). This DRAM is mapped onto the VME bus and is the only way for the main CPU (the MVME167) to talk to the motherboard. The daughterboards connect to the motherboard or to each other depending on their location (see Fig. 3), and thus must use the DRAM on the motherboard for communication as well.

The DSP C30s act as the embedded controller for the entire feedback system. They handle the code for both the local and global feedback correction systems. They work on a polling system. At the end of every loop the DSPs check certain registers on the motherboard DRAM to see if they have received new instructions from the MVME167.

CPU and Ethernet Connection

The CPU (an MVME167) is a Motorola 68040-based processor running a real-time operating system called VxWorks. This processor is connected to the rest of the accelerator control system through a fiber-optic Ethernet link. The CPU can monitor status and operation of the feedback crate and send commands to the DSPs through the DRAM on each DSP motherboard.

CMPSI

The corrector magnet power supply interface (CMPSI) is the last piece of the puzzle. It is designed to take information from the DSP through the FSIC and FSIC-B and pass it over fiber-optic cables to the power supply interface which is located in another rack. The FSIC communicates with the power supply interface by sending a serial data train consisting of one start bit, 16 data bits, and 1 stop bit. For each corrector, a clock line is also run, thus making the communication synchronous. The transmission speed is 500 kHz, and therefore, it takes a minimum of 36 μsec to send data to the corrector power supplies. Each CMPSI can handle 8 channels in parallel (both data and clock included). For a complete two-sector setup using global feedback, two bending magnets, and two insertion devices, a total of four CMPSIs will be necessary for a single feedback crate.

CONCLUSION

The design and prototype of the hardware for the feedback system is completed with the exception of the x-ray BPM interface. The commercial boards have all been purchased with the exception of some of the DSP daughterboards. All in-house production boards are in various phases of ordering, assembly, and testing and should be finished by the end of September 1996. The initial local feedback system (in one sector) is being commissioned now. We hope to test the global feedback system by the end of September 1996.

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