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# AC-DC CONVERTER FIRING ERROR DETECTION

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ALTERNATING GRADIENT SYNCHROTRON DEPARTMENT

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# AC-DC CONVERTER FIRING ERROR DETECTION

by O. L. Gould

## 1.0 ABSTRACT

Extracting specific harmonics from the rectifier output signal of a 6, 12, or 24 pulse ac-dc converter allows the detection of SCR firing angle errors or complete misfires. A bandpass filter provides the input signal to a frequency-to-voltage converter. Comparing the output of the frequency-to-voltage converter to a reference voltage level provides an indication of the magnitude of the harmonics in the ac-dc converter output signal.

## 2.0 INTRODUCTION

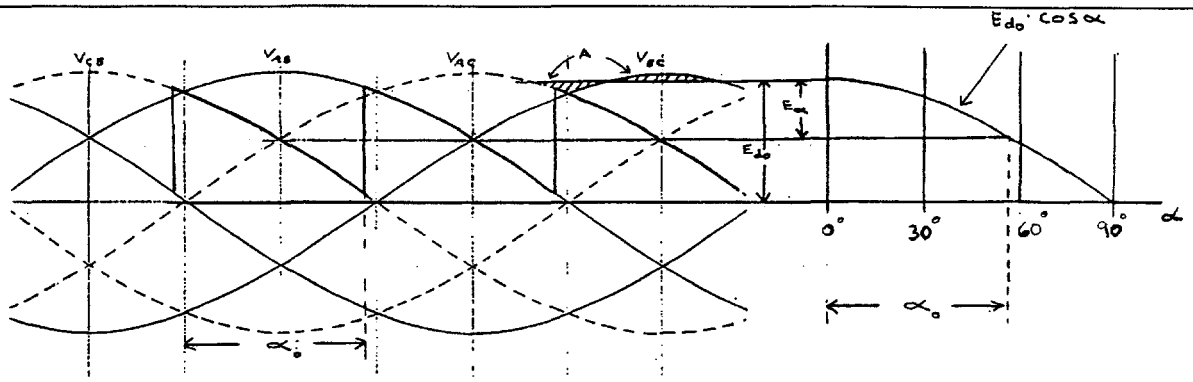
Each of the twelve Booster Main Magnet Power Supply modules consist of two three-phase, full-wave rectifier bridges in series to provide a 560 VDC maximum output. The harmonic contents of the twelve-pulse ac-dc converter output are multiples of the 60 Hz ac power input, with a predominant 720 Hz signal greater than 14 dB in magnitude above the closest harmonic components at maximum output. The 720 Hz harmonic is typically greater than 20 dB below the 500 VDC output signal under normal operation.

However, SCR firing angle errors cause normally suppressed sub-harmonics to become significant in magnitude. This condition produces large errors in the output voltage and current of the ac-dc converter. The current regulation circuit of the power supply system must then compensate for the errors in the ac-dc converter output current. The consequence of these conditions can be further damage to the power supply module with the error or undue stress on the power supply system leading to a system failure. Detection of firing angle errors allows for the expeditious determination of a problem and subsequent shutdown of the power system to prevent further damage. The Ripple Detector circuit provides fast and precise determination of SCR firing problems of an ac-dc converter.

## 3.0 PRINCIPLE

The SCR firing control for a twelve-pulse ac-dc converter produces a fundamental 720 Hz voltage ripple on the output dc signal with sub-harmonic components of much lower magnitude. The SCR firing sequence of each six-pulse bridge rectifier requires each SCR to conduct for 60 degrees in series with an adjoining SCR. Specific pairs of SCRs are conducting simultaneously for 30 degrees once within a 60 Hz cycle. The absence of an SCR conducting will cause a drop in the dc level for 60 degrees within the 60 Hz cycle. Therefore, a large 60 Hz signal component will appear in the voltage ripple signal. Detecting this 60 Hz signal is an indication of a malfunction within the ac-dc converter. The 60 Hz signal varies in magnitude with the phase-back of the SCR firing signal. Hence, the phase shift of the firing angle determines the magnitude

of the 60 Hz component in both the rectify and invert modes. A 120 Hz frequency component is also commonly present in the output of the ac-dc converter under error conditions. The detection of these harmonic components provide an indication of the performance of the ac-dc converter. Figure 1 provides a graphical representation of the ac-dc converter principle.




The above diagram represents the operation of a 6-pulse ac-dc converter. The same principle holds for 12 and 24 pulse ac-dc converters. The two areas marked 'A' are equal areas. Note the maximum dc voltage output Edo of the ac-dc converter is a boundary to these areas. The dc voltage output of the ac-dc converter is reduced as a function of the phase control angle $\alpha$ as shown on the right-side of the diagram.

Figure 1. Graphical representation of the ac-dc converter principle.

The following equations determine the desired sensitivity of the Ripple Detector circuit.

| | |
|---|---|
| $q := 12$ | Number of firing pulses in one 60 Hz cycle. |
| $\alpha := 0..\frac{\pi}{2}$ rad | Phase control angle of the SCRs for the rectify mode. The invert mode requires $\alpha$ to vary from $\pi/2$ to $\pi$ radians. |
| $Em := 566$ volt | Peak value of the ac line-to-line voltage. |
| $Edo := Em\cdot\left(\frac{q}{\pi}\cdot\sin\left(\frac{\pi}{q}\right)\right)$ volt | Maximum dc output of the ac-dc converter. |
| $E_{\alpha} := Edo\cdot(1-\cos(\alpha))$ volt | Amount of voltage reduction of the ac-dc converter as a function of the phase control angle of the SCRs. |
| $Vcmin := .75$ volt | Minimum reference voltage value of the comparator at the output of the band-pass filter of the Ripple Detector circuit. It is found empirically based on Eq and the voltage functions of the Proton run. Pulses with a longer risetime and falltime will allow the Ripple Detector circuit to achieve greater sensitivity. |
| $E_q := Edo\cdot\cos(\alpha)$ volt | Output dc voltage of the ac-dc converter. |
| $Vcomp := \frac{Efault_{\alpha}}{120}$ volt | Minimum amount of voltage reduction detectable due to an error. This equation determines the level of sensitivity of the Ripple Detector circuit. This equation is further explained below. |

$$Efault_{\alpha} := E_q - Edo \cdot \cos\left(\alpha + \beta_{\alpha}\right) \quad volt$$

The minimum detectable phase lag of the firing pulse is therefore

$$\beta_{\alpha} := \operatorname{acos}\left(\frac{E_q}{Edo}\right) - \operatorname{acos}\left[\frac{\left(E_q - Efault_{\alpha}\right)}{Edo}\right] \quad rad$$

For $E_q := 500$ volt and $Vcomp := Vcmin$,

$$\beta_{\alpha} = -.282 \text{ rad}$$

These equations are valid for q not equal to one.

Vcmin is established to determine a lower limit on possible detection. The value of Vcmin is a function of Eq, the rate at which the ac-dc converter is pulsed, and the typical risetime (falltime) of the pulse. The above equations determine the level of the reference voltage, Vcomp, of the comparator at the output of the bandpass filter by choosing a value for βα (depending on the level of sensitivity required) and calculating Efaultα, given Eq, and solving for Vcomp. For example, if the Booster Main Magnet Power Supply's level of sensitivity is chosen to be .641 rad at Eq = 500 VDC then,

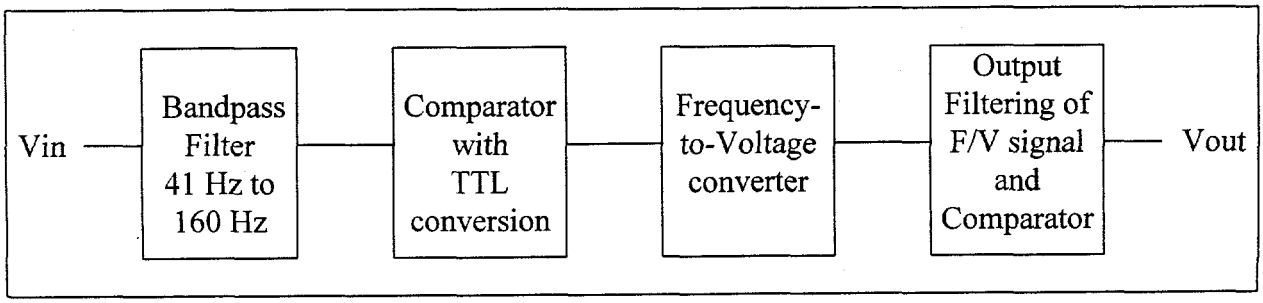
$$Efault_{\alpha} := 250 \text{ volt}$$

$$Vcomp := \frac{Efault_{\alpha}}{120} \quad volt$$

hence, Vcomp = 2.08 VDC. The factor of 120 in the comparator voltage (Vcomp) equation, arises from the current transformer ratio (100) used to detect Eq, the transients produced by the bandpass filter and the approximation of the Booster voltage function under a fault condition where an SCR is misfiring or the phase control angle is lagging. All other types of fault conditions produce a greater fault voltage, therefore the Vcomp equation is a relative lower limit for the detection of a fault. (Vcmin is the absolute lower limit for the detection of a fault.)

## 4.0 CIRCUIT DESCRIPTION

The block diagram below summarizes the Ripple Detector circuit scheme.



## 4.1 FILTER DESIGN

A typical pulse for a power module of the Booster Main Magnet Power Supply is shown in Figure 3.

The main magnet cycle for the Booster machine typically varies from 1 Hz to 7.5 Hz. The cycle rate is important to the filter design because the filter is a high order bandpass filter and produces large transients that increase with decreasing risetimes of pulses. The transient response of the Proton run's voltage pulses interferes with the detection of the 60 Hz component due to the greater rate of pulsing and the shorter risetime of the pulses. A method of minimizing the interference caused by transients is described in the following section.

A bandpass Butterworth filter design with three highpass poles and zeros, and two lowpass poles extracts the desired frequency components. The reason for a high order filter is to eliminate the large low frequency component and the natural ripple components of the ac-dc converter output signal.

The low frequency component is 20 dB above the 720 Hz ripple component when the ac-dc converter is operating at maximum output. The bandwidth of the filter is 119 Hz, with 3 dB frequencies at 41 Hz and 160 Hz (shown in Figure 2).

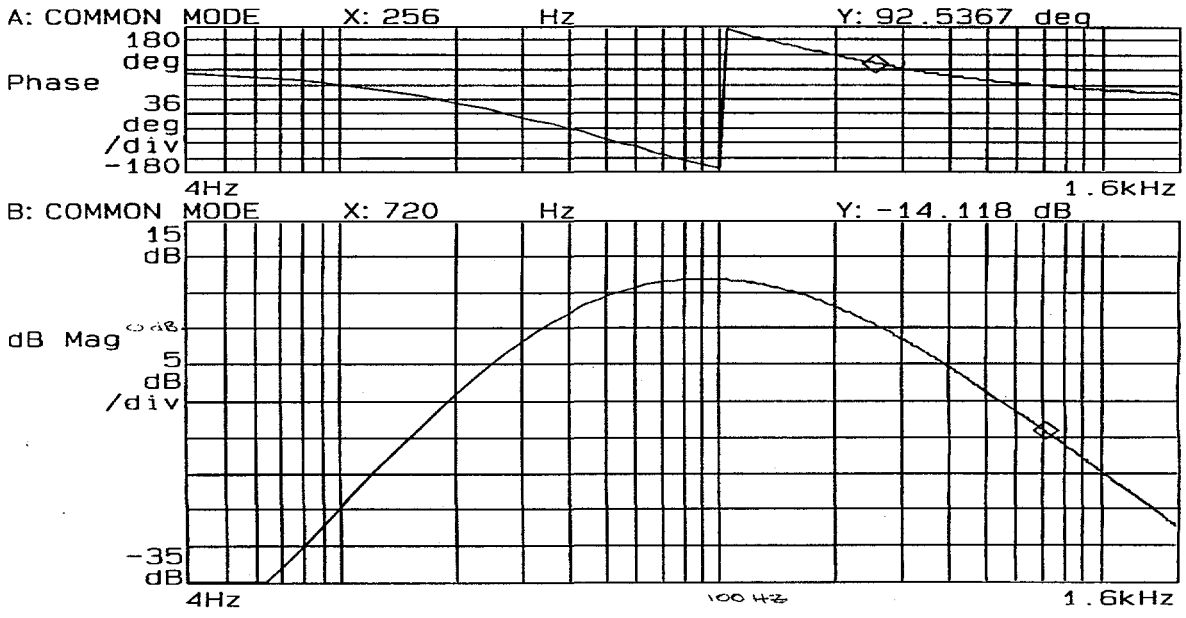



Figure 2. Bandpass filter transfer function.

These filter design frequencies provided maximum attenuation of the 7.5 Hz and the 720 Hz frequency components while allowing the 60 Hz and the 120 Hz components to pass and be detected. The output of the filter provides the necessary information to determine whether the rectifier is operating properly.

The magnet pulse shown in Figure 3 has a bandpass filter output (inverted) as shown in Figure 4. The filter output signal is the input to a comparator that determines the sensitivity of detection. The comparator reference voltage is Vcomp.

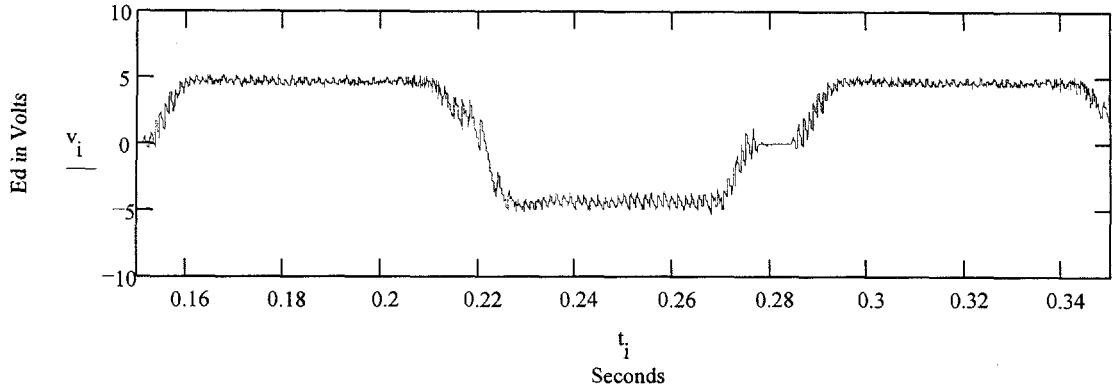



Figure 3. Typical Booster main magnet pulse (100:1 ratio).

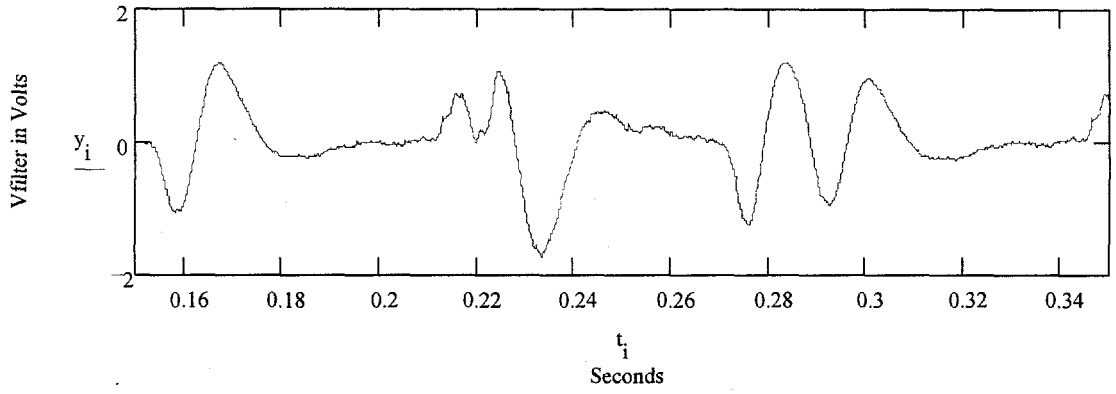



Figure 4. Typical output signal of the bandpass filter.

## 4.2 DETECTION STAGE DESIGN

The comparator that determines the sensitivity of detection normalizes the amplitude of the filter output signal to TTL levels (see Figure 5). A frequency-to-voltage (F/V) converter provides an output dc voltage level relative to the input frequency of the comparator output signal. Therefore, the magnitude of the transient does not affect the final outcome of the circuit, since the leading edges of the TTL pulses provide the triggering of the F/V converter. The frequency-to-voltage

converter's input comparator receives the TTL pulses. The comparator provides a stable input to a one-shot timer. The one-shot timer triggers an electronic switch. This switch controls the rate at which a current source at the input to an amplifier charges a capacitor at the output of the amplifier (integrator). Therefore, a linear relationship exists between the input frequency of the pulses and the output voltage. The one-shot timer's capacitor determines the frequency range of operation (0 Hz to 70 Hz). The output voltage range (0 V to 10 V) is determined by the integrator circuit of the amplifier and the power supply voltage of the amplifier. The F/V converter performance is further discussed in section 5.1.

The output of the F/V converter is compared to the voltage reference level of another comparator. The output of this comparator sends a signal to the PLC to shut off the power supply if the F/V converter's dc voltage output is greater than the voltage reference level of the comparator.

Although the circuit is designed to minimize the effects of the transient signal, the input signal to the filter should be no greater than 10 Volts peak and 20 Hz maximum to further avoid interference from the transients produced by the filter response.

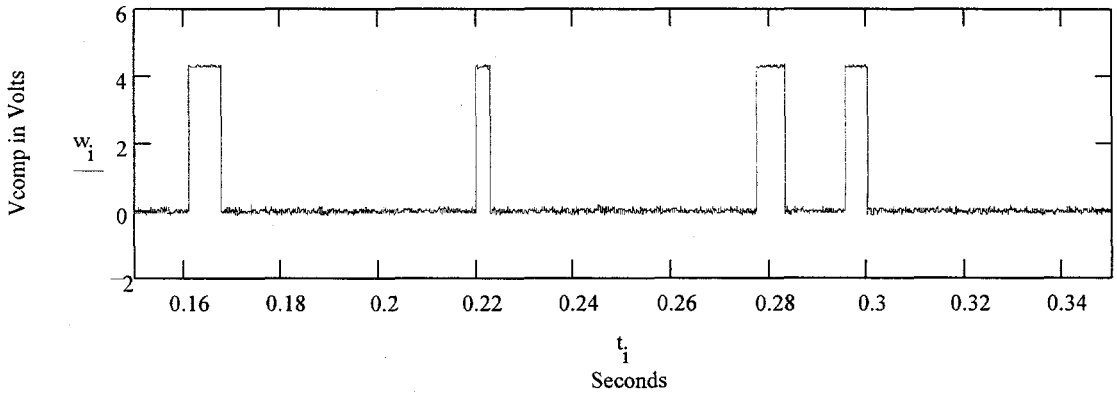



Figure 5. Typical output signal of the comparator under normal conditions.

## 5.0 PERFORMANCE

The filter response produces peak amplitudes at a minimum time interval of 25 ms under normal operating conditions. The threshold level of the comparator at the output of the filter determines the sensitivity of detection. As the threshold setting decreases, the comparator detects smaller amplitudes. The reference level is typically set between 750 mV to 1 V to detect errors.

The reference level of the output comparator is set at 8.5 VDC, which corresponds to a 54 Hz input signal to the frequency-to-voltage converter. Any frequencies above 54 Hz will cause a change of state at the output of the Ripple Detector circuit.

## 5.1 FREQUENCY-TO-VOLTAGE CONVERTER

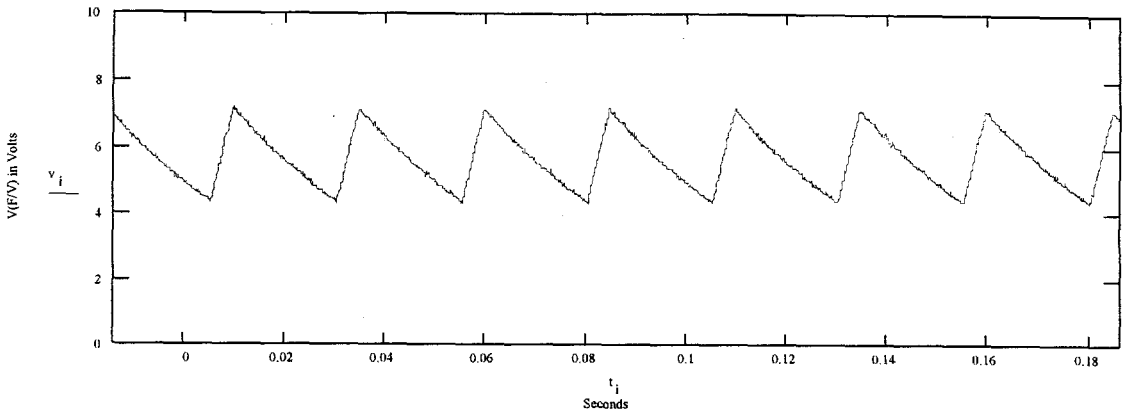



Figure 6. Frequency-to-voltage converter output with a 40 Hz input signal.

The F/V converter produces a large ripple voltage (as shown above in Figure 6). This creates the possibility of a false error indication. A sample-hold circuit, described below, is used to reduce the voltage ripple by 15 dB. An active filter is also used at the output of the sample-hold circuit to buffer the signal and further reduce the ripple voltage. However, the dynamic range of the frequency-to-voltage converter is reduced from (0 Hz to 70 Hz) to (10 Hz to 65 Hz) due to the sample-hold circuit and the active filter at the output of the F/V converter.

The performance of the Ripple Detector circuit is not affected by the reduction in the dynamic range, since the 60 Hz frequency level of the F/V converter is within the dynamic range. Any frequencies above 65 Hz will produce the same dc voltage output.

## 5.2 SAMPLE-HOLD CIRCUIT

The timing pulses for the sample-hold circuit is an internal signal from the one-shot timer output of the F/V converter (shown in Figure 7). This signal is normalized by a comparator before gating an FET transistor (see figure 8). This signal was chosen because it provides a reliable gate pulse. The FET transistor is used as an electronic switch to sample the F/V converter's output.

The risetime and falltime of the one-shot timer signal allows the gate time to be varied based on the reference level of the comparator. Hence, the magnitude of the F/V voltage ripple is controlled by the width of the comparator output pulses. Ideally, no F/V converter voltage ripple is desired; however, the shorter the gate time the greater the sensitivity of the comparator to a variation in the amplitude of the one-shot signal. The worst case would be the comparator output not switching states because the one-shot signal does not cross the comparator input threshold. This is not likely to occur since the one-shot signal is constant. However, a comparator with good high frequency characteristics is used due to the requirement of a short gate pulse. This final output is shown in Figure 9. The ripple voltage is reduced by 15 dB as observed from Figure 6 and Figure 9.

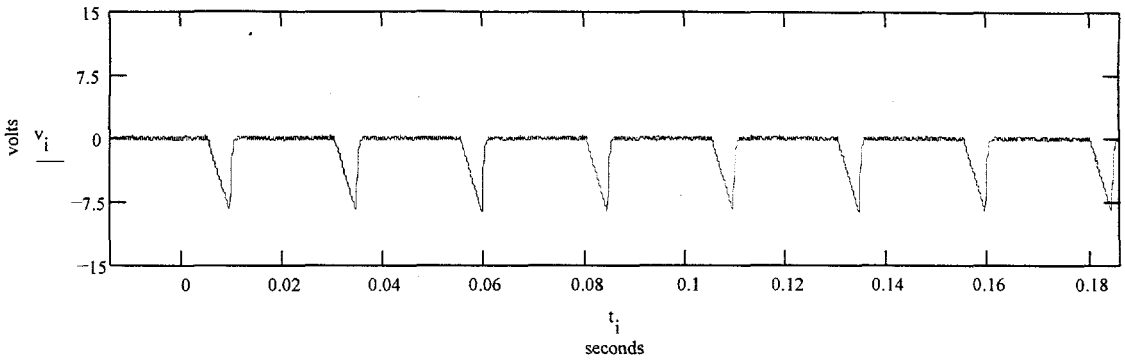



Figure 7. Internal signal from the one-shot timer.

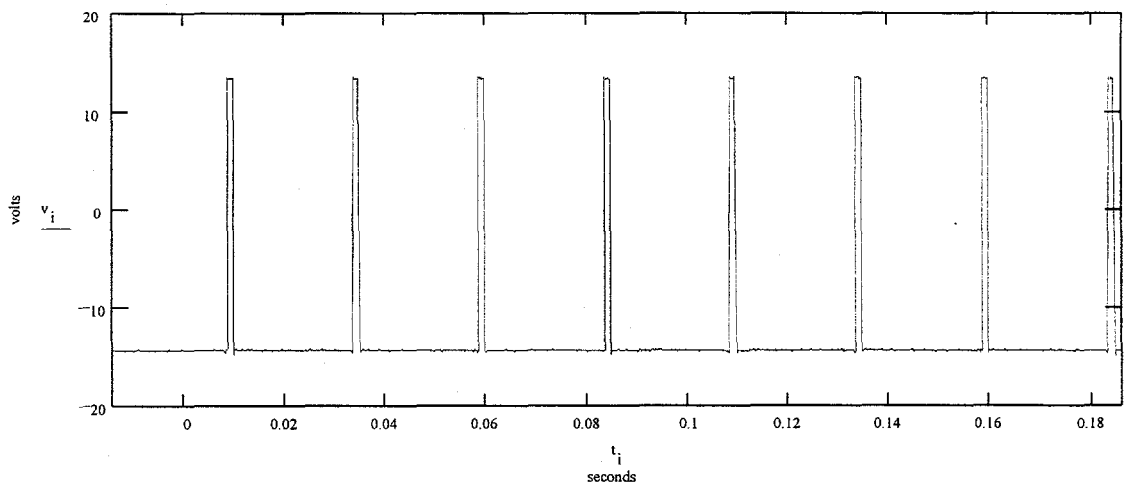



Figure 8. Comparator output with one-shot timer signal as an input. This signal gates the FET transistor.

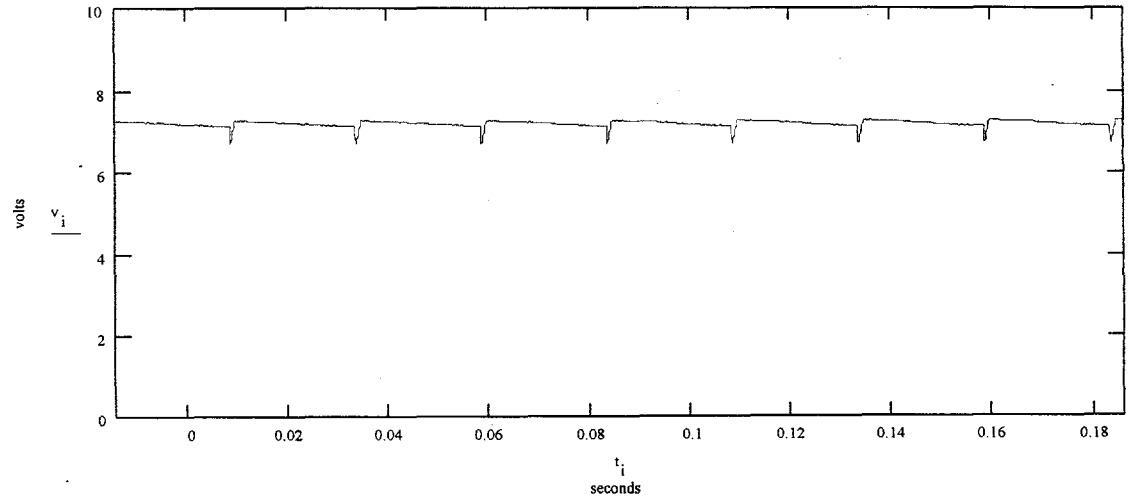



Figure 9. Frequency-to-voltage converter output utilizing the voltage ripple reduction scheme.

The signal in Figure 9 is compared to the reference level of a comparator at the output of the Ripple Detector circuit.

## 6.0 CONCLUSION

The Ripple Detector circuits were tested during a Proton run and a Heavy Ion run for a total time of three months. During this period, the response to actual power supply errors was non-interactive. The performance of the Ripple Detector was reliable and decisive.

The Ripple Detector circuits interacted actively with the Programmable Logic Controller (PLC) units of the Booster Main Magnet Power Supply after testing was successfully completed. The PLC units for the Booster Main Magnet Power Supply are programmed to indicate a fault when they receive a fault state condition continuously for 50 msec. This time period was chosen to avoid tripping on any inadvertent power supply glitches. It is longer than three 60 Hz cycle time periods - which provides adequate time to determine if the power supply is malfunctioning. Higher sensitivity can be obtained if the PLC time period for a fault state is reduced. However, this will be at the expense of nuisance tripouts due to power supply glitches.

The Ripple Detector circuit is a modular unit and can be used in most ac-dc converters with adjustments made to the comparator that determines the sensitivity of the Ripple Detector circuit.

## 7.0 ACKNOWLEDGMENTS

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## 8.0 REFERENCES

1) Johannes Schaefer, Rectifier Circuits: Theory and Design, John Wiley & Sons, NY, 1965.