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GaAs SELF-ALIGNED JFETS WITH CARBON-DOPED P+ REGION

A. G. Baca, P. C. Chang, A. A. Allerman, and T. J. Drummond
Sandia National Laboratories, P. O. Box 5800, Albuquerque, NM 87185-0603

Self-aligned JFETs with a carbon-doped p^+ region have been reported for the first time. For these JFETs, both the channel and p^+ region were grown by metal organic chemical vapor deposition (MOCVD) and are termed epitaxial JFETs in this study. The epitaxial JFETs were compared to ion implanted JFETs of similar channel doping and threshold voltage. Both JFETs were fabricated using the same self-aligned process for doping the source and drain regions of the JFET and for eliminating excess gate capacitance of conventional JFETs. The gate turn-on voltage for the epitaxial JFETs was 1.06 V, about 0.1 V higher than for the implanted JFETs. The reverse breakdown voltage was similar for both JFETs but the reverse gate leakage current of the epitaxial JFETs was 1-3 orders of magnitude less than the implanted JFETs. The epitaxial JFETs also showed higher transconductance and lower knee voltage than the implanted JFETs.

INTRODUCTION

Self-aligned JFETs can give important advantages over MESFETs for wireless technologies that benefit from a single positive power supply. The increased gate turn-on voltage compared to MESFETs allows higher current densities for enhancement-mode (positive threshold voltage) for the JFETs. Digital circuits also benefit from an increase in gate turn-on voltage; direct coupled FET logic (DCFL) circuits have higher noise margin, for example. The use of self-aligned processing eliminates performance degradation due to excess gate capacitance that conventional JFETs suffer compared to MESFETs [1].

Self-aligned JFETs with W gate contacts and ion implanted Zn, Mg, or Cd p^+ regions have been reported [1-3], with JFETs using a Zn or Cd p^+ region having superior performance compared to Mg. Both intersitial Zn and Mg are rapid diffusers at implant activation temperatures, but the Zn implant with co-implanted P creates an excess of group III vacancies which favor Zn incorporation in group III sites and effectively controlled Zn diffusion [4]. Mg implantation profiles were found to be broader than Zn because of channeling due to its lighter mass [4]. Cd behaves similarly to Zn and produces shallower channels [3]. Even though Zn profiles were not appreciably diffused, ion implantation unavoidably introduces broadening of the p-n junction. Epitaxial self-aligned JFETs (p^+ dopant not specified) have also been studied [5], but no direct comparisons have been made to implanted JFETs. In this report, we present initial results for epitaxial self-aligned JFETs with a carbon-doped p^+ region and compare the results with ion implanted JFETs of comparable channel doping and threshold voltage. The use of carbon doping eliminates the need for an undoped spacer reported in the previous epitaxial JFET [5].

FABRICATION

The GaAs wafers were grown by metal organic chemical vapor deposition (MOCVD). The epitaxial layers are as follows: a GaAs buffer of 1.0 μm, a p-backside for channel confinement of GaAs:C (0.2 μm and $2x10^{16}$ cm^{-3}), a GaAs:Si channel (0.1 μm and $3x10^{17}$ cm^{-3}), and a GaAs:C p^+ region (30 nm and $2x10^{19}$ cm^{-3}). This epitaxial structure should give an abrupt pn junction because of the low diffusivity of carbon at implant activation temperatures. In order to study the effect of pn junction broadening due

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to the ion implant, the channel thickness and doping were chosen to be similar to the ion implanted JFET.

The fabrication process is outlined in Figure 1. The W gates are patterned with conventional optical lithography and delineated by reactive ion etching [6]. Non selective wet chemical etching with a H_3PO_4:H_2O_2:H_2O solution (1:4:45) is used to define the p^+ gate region. Self-aligned Si implants (dose of $2x10^{13}$ cm^{-2} for both 40 KeV and 80 KeV) are used to doped the source and drain regions. A rapid thermal anneal of 830 C for 20 sec is used to activate the implants. Ohmic contacts are then patterned and deposited using Ge/Au/Ni/Au and alloyed at 400 C for 15 sec. The JFETs are contacted through SiN vias and Ti/Pt/Au (not shown in Figure 1). This process is very similar to that used in ref 1 with the exception of the epitaxially grown channel.

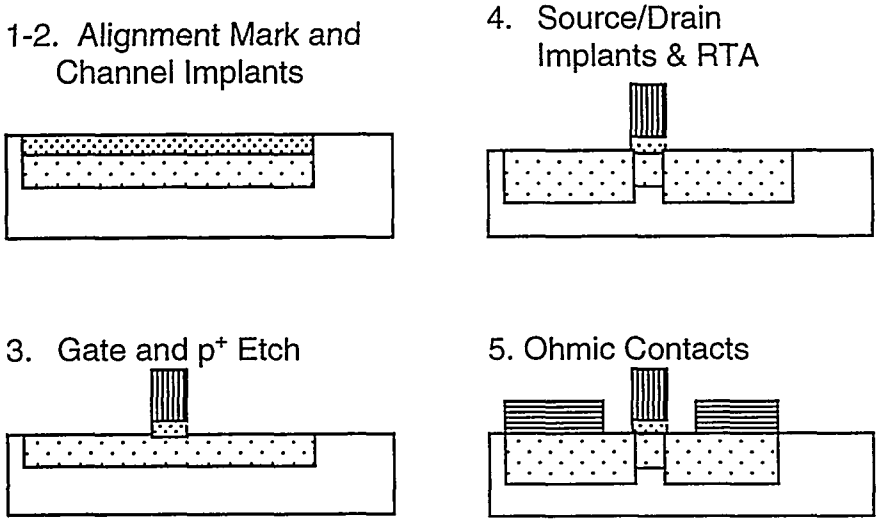

Figure 1. Process sequence for self-aligned JFET fabrication.

RESULTS

The gate diode characteristics for the epitaxial JFETs are shown in Figure 2 and compared to ion implanted JFETs. The reverse breakdown voltage is comparable for both JFETs, but the reverse leakage current is about 1-3 orders of magnitude lower for the epitaxial JFET. Lower reverse leakage is probably indicative of fewer defects in the epitaxial material or less broadening of the pn junction. The forward gate turn-on voltage (defined as the voltage at 1 μA/μm) is higher for the epitaxial JFET by about 0.1 V. Although this difference is small it can be significant in allowing for more current drive for the epitaxial JFET. The gate access resistance is lower for the epitaxial JFET, which is why the currents cross at higher gate voltages.

The drain I-V characteristics for both JFETs are shown in Figures 3 and 4 for 1.0 x 100 μm gate dimensions. The epitaxial JFET is not an optimized structure as its threshold voltage is higher than generally desired. Higher channel doping or a thicker channel can be used to adjust the threshold voltage to the desired value. To facilitate comparison, an implanted JFET with similar threshold voltage and drain current at the onset of gate current was chosen.

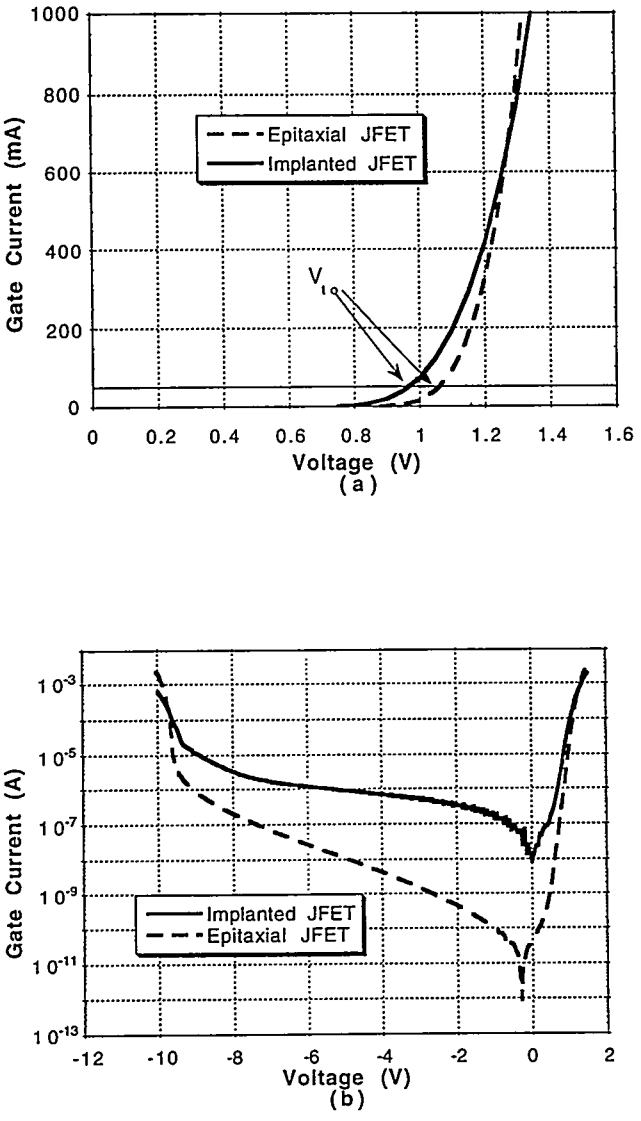

Figure 2. Gate current for Implanted and Epitaxial JFET

The threshold voltage of the epitaxial JFET is approximately 0.25 V higher that the implanted JFET and the currents shown in Figure 3 are approximately comparable for gate voltages 0.25 V apart. However, the epitaxial JFET has lower knee voltages. Likewise, the drain current and transconductance plots of Figure 4 will overlap near threshold if offset by 0.25 V. At higher gate bias, the transconductance of the implanted JFET saturates at about 220 mS/mm, while that of the epitaxial JFET continues to rise.

The carbon doping in the p^+ region of the epitaxial JFET provides an abrupt p-n junction in contrast to the Zn-doped region of the implanted JFET. SIMS data for the implanted JFET shows that the Zn concentration drops from a level of approximately 2×10^{17} cm^{-3} at the p-n junction to 1×10^{16} cm^{-3} over a distance of 700 Å [4]. This residual Zn in the JFET channel no doubt plays a role in limiting the current and the transconductance under high gate bias conditions where the depletion region of the JFET becomes small. A summary of all of the DC parameters is given in Table 1.

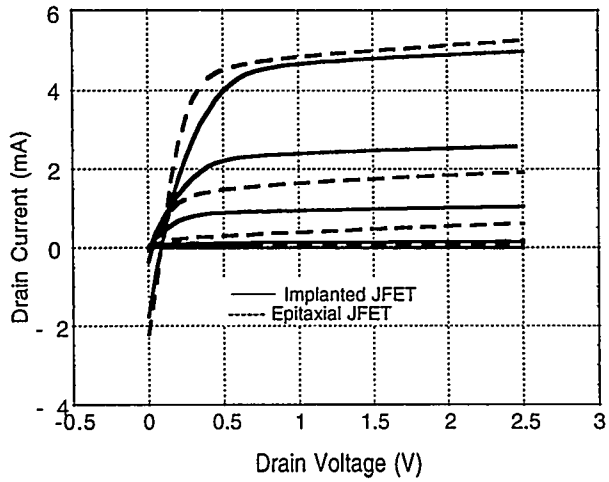

Figure 3. Drain current for implanted and epitaxial JFETs. The gate voltage ranges from 1.5 V to 0 V in -0.25 V increments for the implanted JFET and from 1.25 V to 0 V in -0.25 V increments for the epitaxial JFET.

One issue with the C-doped p^+ region is its stability during the 830 C activation anneal. Two effects may be relevant for these types of samples. The first is that hydrogen can be bonded to the carbon inactivating it as an acceptor. A high temperature anneal can break the C-H bonds leading to greater activation and a lower sheet resistance of the p^+ layer; this should not be detrimental to the JFETs. A second effect is that the carbon atoms may precipitate within the GaAs leading to lower free acceptor levels and higher sheet resistance. This effect would be detrimental to the JFETs as a lower surface acceptor level can result in a rectifying contact with the W gate electrode. In previous work this effect has been shown to lower the gate turn-on voltage of the JFET [2]. In order to examine the

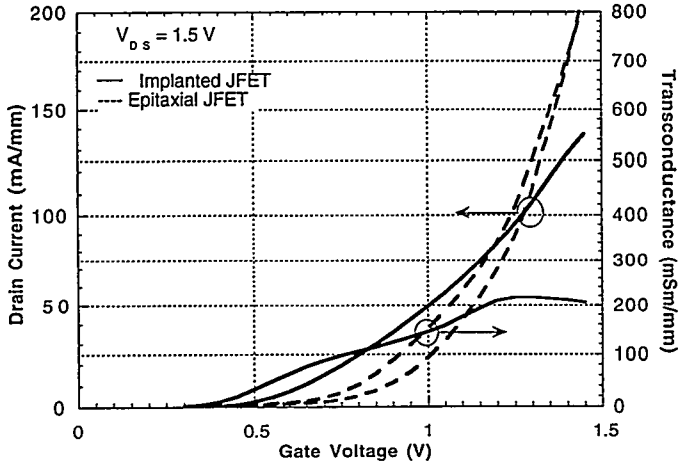

Figure 4. Drain current and transconductance for implanted and epitaxial JFETs.epitaxial JFETs.

effect of high temperature anneals, a 1000 Å layer doped to $2x10^{19}$ cm^{-3} by MOCVD was annealed at various temperatures and the results are shown in Table 2. All anneals up to 800 C result in a reduction in sheet resistance compared to the as-grown values. This observation is consistent with the fact that high gate turn-on voltage was observed in the epitaxial JFETs.

CONCLUSION

Self-aligned epitaxial JFETs with a carbon-doped p^+ region have been fabricated for the first time and compared to ion-implanted JFETs. Enhancement-mode epitaxial JFETs have a greater gate-turn-on voltage, lower reverse gate leakage, and a smaller knee voltage compared to the ion implanted JFETs. These results show promise for digital and microwave applications.

Table 1. A summary of the DC parameters of the epitaxial and implanted JFETs.

Device Parameter	Epitaxial JFET	Implanted JFET
Threshold Voltage (V)	0.75	0.50
Gate Turn-on Voltage	1.06	0.95
Drain-Gate Breakdown Voltage (V)	9	9
Maximum Transconductance (mS/mm)	800	220
Knee Voltage at 4 mA (V)	0.3	0.5

Table 2. Effect of high temperature anneals on a carbon-doped layer with W/p-GaAs contacts.

Anneal Temperature	Sheet Resistance (Ω/square)
As received	581
650 C/20 sec	346
700 C/20 sec	398
750 C/20 sec	367
800 C/20 sec	400

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