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Large Area Silicon Drift Detectors For X-Rays – New Results.

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Abstract

Large area silicon drift detectors, consisting of 8 mm and 12 mm diameter hexagons, were fabricated on 0.35 mm thick high resistivity n-type silicon. An external FET and a low-noise charge sensitive preamplifier were used for testing the prototype detectors. The detector performance was measured in the range –75 to 25 °C using Peltier cooling, and from 0.125 to 6 μs amplifier shaping time. Measured energy resolutions were 159 eV FWHM and 263 eV FWHM for the 0.5 cm^2 and 1 cm^2 detectors, respectively (at 5.9 keV, -75 °C, 6 μs shaping time). The uniformity of the detector response over the entire active area (measured using 560 nm light) was < 0.5 %.

I. Introduction

Development of charge coupled devices (CCD's) for light-signal imaging utilizing extremely low capacitance of the detector and readout circuitry opened up a new chapter in possible nuclear detector designs. This started a vigorous effort to develop silicon drift detectors (SDD's) for high energy physics applications [1,2]. Recently, interest in the development of new structures for x-ray spectroscopy had also begun to appear [3-6]. The beauty of the drift detector design in this regard, is that, unlike traditional planar detectors, it allows for relatively large active area while still maintaining a very low capacitance (60fF) to achieve low noise. In order to take advantage of the low capacitance of the drift detector, the detector must be matched to a low capacitance input transistor. State-of-the-art existing low noise FETs (field effect transistors) for spectroscopy generally have a capacitance much larger than that achievable with the drift detector, and integration techniques add additional stray capacitance. The approach has therefore been to design low noise FETs which can be integrated, or processed, directly on the detector substrate, thereby reducing the overall system capacitance [7-9]. However, the detectors can be effectively characterized using an external FET and low noise preamplifier, which was the technique utilized here. The work presented here concentrates on the design and characterization of the low noise drift detector itself.

SDD Design

A cross sectional view of the SDD is shown in Figure 1. Computer simulations were used to design and optimize the large area SDD structures. Electric field distributions were optimized through calculations using the MEDICI program, a semiconductor device simulation tool available commercially [10], based on the PISCES software developed at Stanford University. Process simulation tools, including SUPREME [10], were used to create a process flow for the detector fabrication. The entrance window side is an optically thin planar p+ contact with a deep vertical etch into the silicon substrate for the high voltage termination of the diode [11]. The back side, with the drift rings, consists of a new structure utilizing alternating p+ and n+ rings surrounding the n+ anode [12]. In this scheme, the n+ electrodes are floating and do not influence charge collection, but are used to reduce the depleted surface area, thereby reducing the surface leakage current. Additional high voltage termination structures, in the form of p+ guard rings surrounding the periphery of the p+/n+ ring side, improve the break down characteristics of the device. Under operating conditions, the entrance window electrode is kept at a fixed potential, while the back side ring electrodes are biased through a resistor ladder connecting all the p+ rings. The detector bulk is fully depleted, producing a drift-valley region within the detector. In order to cause the drift valley to tilt sharply through the detector to the n+ collection anode, the p+ electrodes are biased at monotonically increasing potentials in the radial-direction, which produces a field gradient from the front to the back of the device. The electrode dimensions and optimum form of the electric field, were developed to assure excellent charge collection and shortest carrier drift time [6].

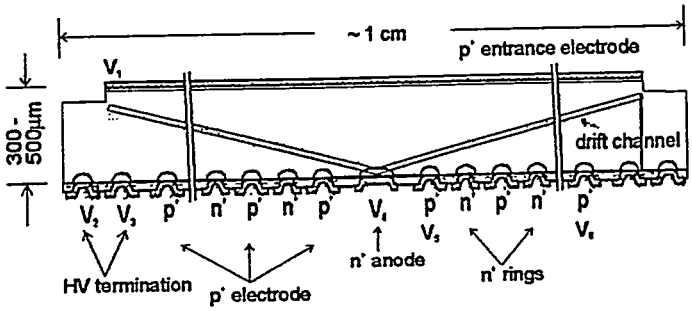

Figure 1: Schematic of the cross-section of the SDD detector illustrating the p^+ entrance electrode, novel alternating p^+/n^+ back side electrodes, n^+ anode (where the charge is collected), and position of the drift channel in the detector.

The silicon drift detectors were fabricated using a modified version of the Stanford University BICMOS process [13], on high resistivity (3000 Ωcm) n-type 0.35 mm thick silicon wafers. Individual detectors were hexagons of 8 mm and 12 mm diameter, 0.5 cm^2 and 1.0 cm^2, respectively. The front side and back side of a typical detector are shown in detail in Figure 2. The hexagonal shape lends itself to easy assembly into larger multi-element arrays, while still maintaining an optimum drift configuration. Monolithic arrays have the advantage of

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minimizing the dead area between the individual detector elements.

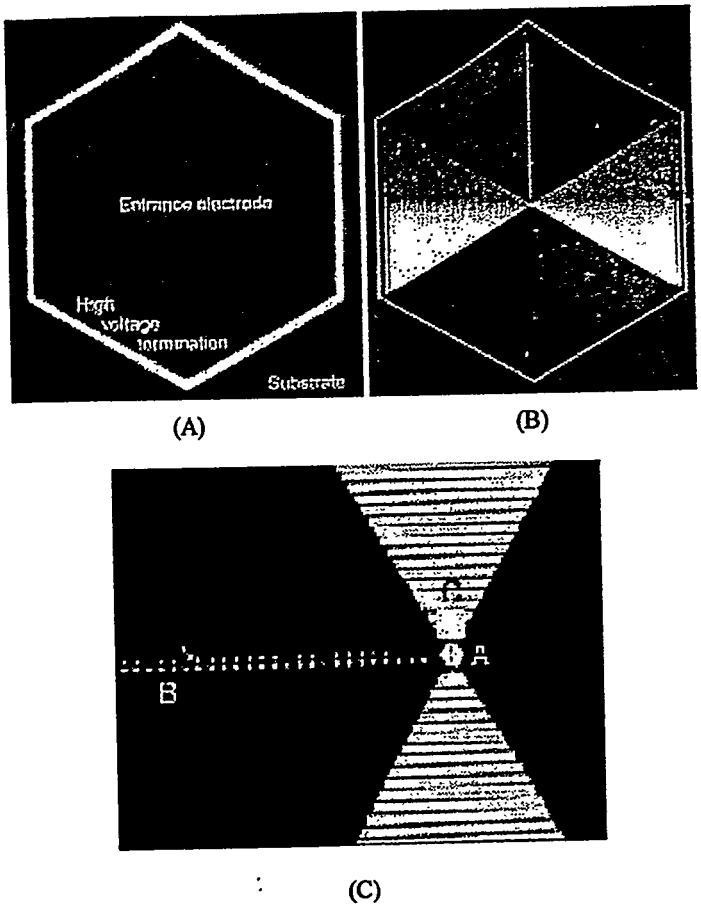

Figure 2. Digitized photograph of the SDD structure; (A) Front entrance window side; (B) Back p+ ring side; (C) Anode region. The p-well resistor ladder structure is marked "B", the biasing electrode for the inner p-well is marked "C", and the small anode located in the center of the detector is marked "A".

II. Experimental

A test fixture was designed and built to accommodate the fabricated SDD structures. The housing included Peltier cooler platforms, heat exchange assemblies and vertical assembly techniques for interconnecting the detector structures with the electronics assuring minimum microphonics and minimum noise. The detectors were coupled to commercially available low noise FETs and a custom-designed low noise preamplifier. Tennelec TC 244 and Canberra 2026X amplifiers and an MCA (Nucleus PCA) were used to measure detector spectra in response to various radioisotope sources. Leakage currents were measured using a Keithley model 487 picoammeter. Although these electronics were not optimal for the low capacitance of the SDD, mainly because of the large capacitance of the interconnections and external input FET, this method was effective for evaluating the prototype structures. The spectral response, energy resolution and uniformity of the detectors were measured as a function of temperature, shaping time and energy.

III. Results

A) Leakage Current

The leakage current was measured on devices of various sizes, up to 1 cm^2, as a function of temperature. The measured leakage current on a typical device is shown in Figure 3.

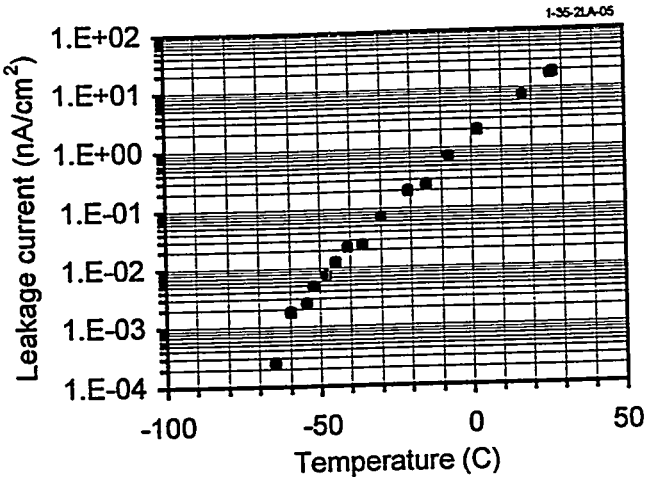

Figure 3: Leakage current as a function of temperature, for a typical SDD prototype at the operating voltage.

B) Electronic Noise

Figure 4 shows the calculated and measured electronic noise as a function of peaking time for a 0.5 cm^2 SDD, at –30 and –75 °C. The noise at lower shaping times is dominated by the system capacitance of 1.5 pF, while that at higher shaping times is dominated by the detector leakage current.

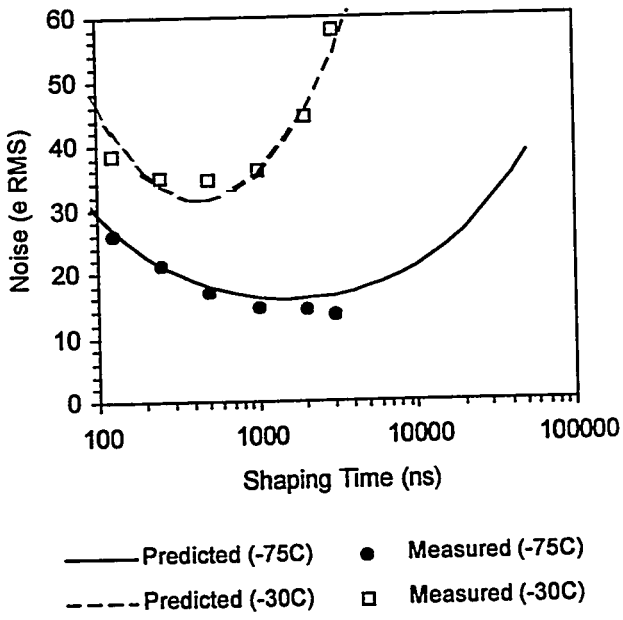

Figure 4. Calculated noise e^- rms as a function of the peaking time for –75°C (solid line) and –30°C (dashed line) operation with external FET and observed leakage current. Also showing measured response at –75°C (solid circles) and –30°C (empty squares). Predicted noise is based on the model described in [6].

C) Spectral Response

An ^{55}Fe spectrum obtained with a 0.5 cm^2 device is shown in Figure 5. An energy resolution of 159 eV FWHM was obtained for the 5.9 keV photopeak, at an amplifier shaping time of 6 μs and temperature of -75 °C achieved via thermoelectric cooling. The electronic noise measured by the pulser method and calibrated with the radioisotope source, was 110 eV FWHM (13 e$^-$ RMS).

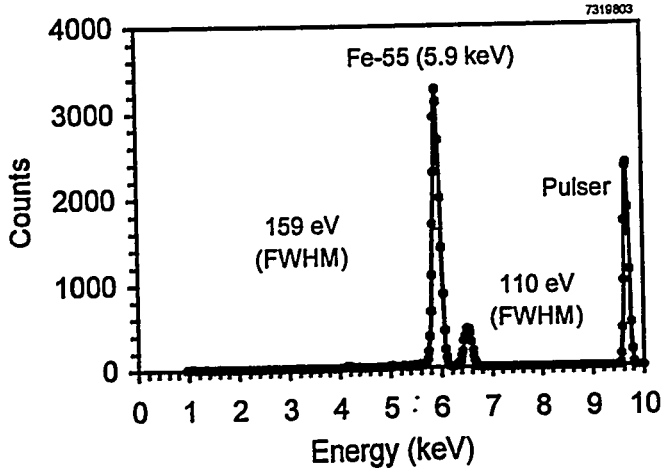

Figure 5. ^{55}Fe spectrum obtained with a 0.5 cm^2 SDD (6 μs shaping time, -75 °C). Data is plotted on a linear scale.

An ^{55}Fe spectrum obtained with a 1 cm^2 SDD is shown in Figure 6. The energy resolution is 263 eV FWHM (at 5.9 keV, 4 μs shaping time, –70 °C) with an electronic noise of 27 e$^-$ RMS. The silicon escape peak is clearly visible, indicating a peak-to-background ratio of ~1000, which demonstrates that the detector has excellent charge collection characteristics. The low noise cutoff is 350 eV.

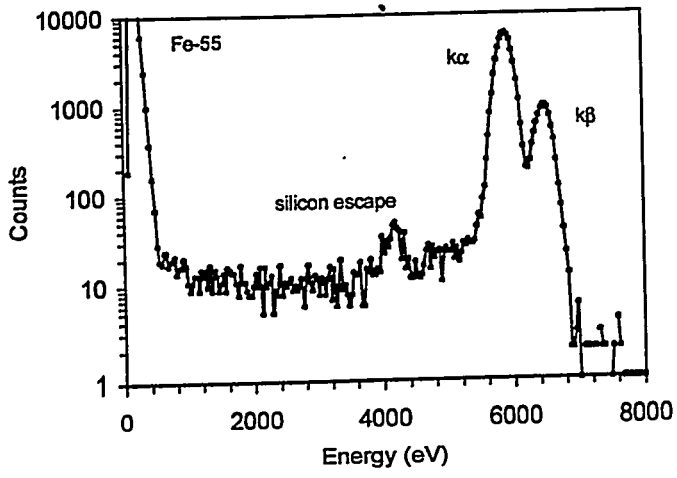

Figure 6: ^{55}Fe spectrum obtained with a 1 cm^2 SDD. The energy resolution is 263 eV FWHM (at 5.9 keV, 4 μs shaping time, –70 °C), with an electronic noise of 27 e$^-$ RMS.

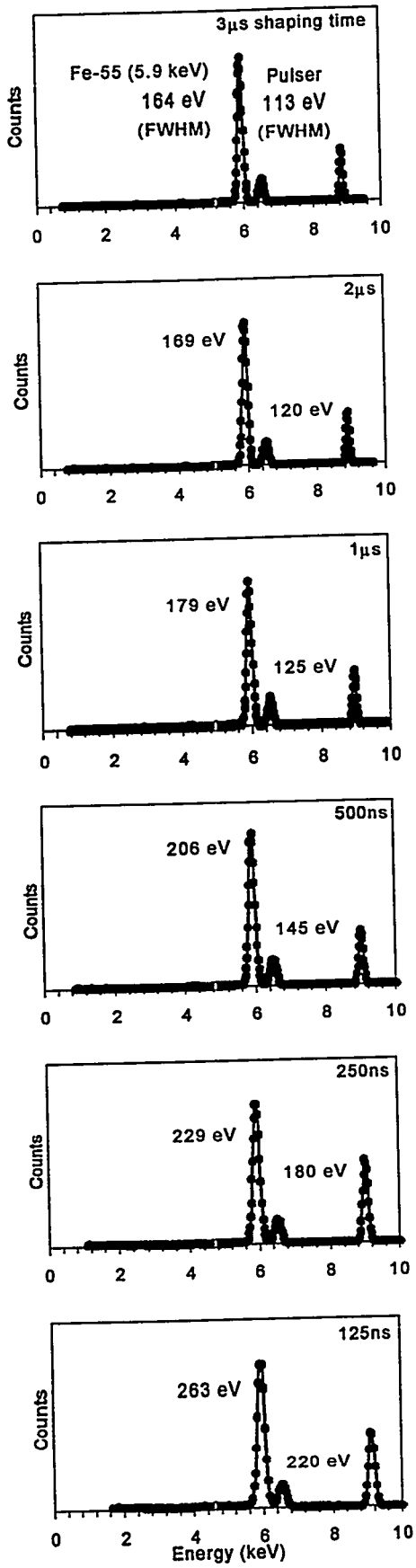

Figure 7: ^{55}Fe spectra obtained at 3μs, 2μs, 1μs, 500ns, 250ns, and 125ns shaping times

^{55}Fe spectra obtained from a 0.5 cm^2 device at –75 °C with shaping times of 3 μs, 2μs, 1μs, 500ns, 250ns, and 125ns are shown in Figure 7. The energy resolution for the 5.9 keV photopeak of ^{55}Fe ranges from 159 eV FWHM at 3 μs to 263 eV FWHM at 125 ns shaping time.

Mars Simulant

To demonstrate the applicability of the large area SDDs in the mapping of the chemical composition of a geological surface, fluorescence measurements on a Mars simulant sample were made. The spectra from the sample (JSC Mars-1, which is spectrally similar to Martian material [14]), is shown in Figure 8, using excitation from an ^{55}Fe source. Note that the Al x-ray line is quite well separated from the Si line as a result of the excellent energy resolution.

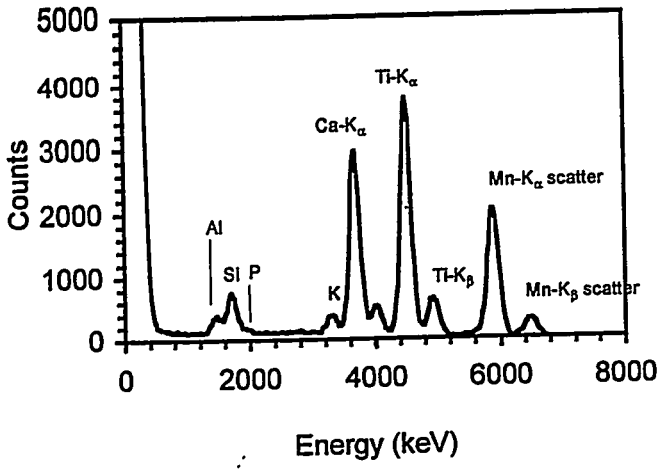

Figure 8: XRF spectrum of JSC Mars-1 sample obtained from a 0.5 cm^2 SDD using an ^{55}Fe excitation source in vacuum, at –75 °C.

D) *Spatial Response*

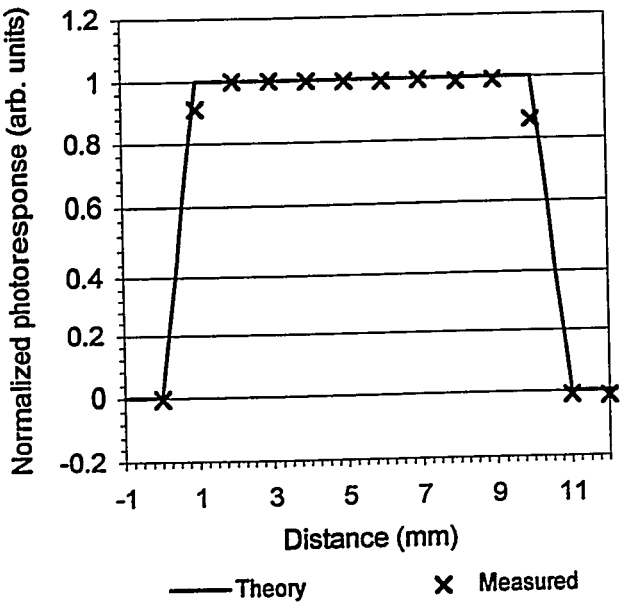

Figure 9: Calculated and measured photoresponse of a 1 cm^2 SDD along the x-axis

The quality of the charge collection over the entire active area of a 1 cm^2 SDD was evaluated by measuring the photoresponse as a function of position on the detector. A 1 mm diameter collimated light beam was scananed in 1 mm increments across the window surface of the detector. The 560 nm light, which penetrates only approximately 1 μm into the silicon, generates charge in the detector near the entrance electrode. Figure 9 shows both the measured photoresponse and the predicted result obtained by convolving the light beam and the detector geometries. The measured response is very uniform over the entire active area, and agrees very well with the predicted response. In fact, the fluctuations over the entire plateau region (from +1 to +10mm in the scan) are less than 0.5%. These results demonstrate that there is excellent electron collection throughout the full detector volume.

IV. Discussion and Conclusions

Large area silicon drift detectors, consisting of 8 mm and 12 mm diameter hexagons, were fabricated on 0.35 mm thick high resistivity n-type silicon.

An external FET and a low-noise charge sensitive preamplifier were used for testing the prototype detectors. The detector performance was measured in the range –75 to 25 °C using Peltier cooling. The leakage current was ~20nA/cm^2 at room temperature, and so in order to obtain the best possible spectral results, the SDD structures were cooled to the lowest temperature possible in our experimental chamber in order to reduce the parallel noise. Leakage current was below 10 pA/cm^2 at –45 °C and dropped to below 1 pA/cm^2 below –60 °C.

Measured energy resolutions were 159 eV FWHM and 263 eV FWHM for the 0.5 cm^2 and 1 cm^2 detectors, respectively (at 5.9 keV, -75 °C, 6 μs shaping time). Corresponding electronic noise was 13 e$^-$ RMS and 27 e$^-$ RMS for the 0.5 cm^2 and 1 cm^2 detectors respectively.

Measurements of energy resolution and noise were made as a function of amplifier shaping time from 0.125 to 6 μs. At the shaping time of 0.125 μs, which corresponds to throughput exceeding 10^6 cps, an energy resolution of 263 eV FWHM was obtained. This type of performance is competitive with state-of-the-art cryogenic Si[Li] detectors operated at similar amplifier time constants.

Measurements of a mars simulant sample were made using an ^{55}Fe x-ray source. The low energy cutoff was approximately 400eV which allowed measurement of the Al K-fluorescence lines. Good separation of the Al and Si K-xray peaks was observed.

The response uniformity (± σ%) defined as the variation in response over the entire active area was < 0.5 % for 560nm light. In addition, future developmental plans for the drift detectors are discussed.

Future plans include integration of the front end FET and lowering of the leakage currents.

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