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MICROSTRUCTURAL EVALUATION OF Sb-ADJUSTED $Al_{0.5}Ga_{0.5}As_{1-y2}Sb_y$ BUFFFER LAYER SYSTEMS FOR IR APPLICATIONS

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Microstructural Evaluation of Sb-adjusted $Al_{0.5}Ga_{0.5}As_{1-y}Sb_y$ BUFFER LAYER Systems for IR Applications

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ABSTRACT

We report on a transmission electron microscopy (TEM) study of Sb-adjusted quaternary $Al_{0.5}Ga_{0.5}As_{1-y}Sb_y$ buffer-layers grown on <001> GaAs substrates. A series of structures were grown by MBE at 470°C that utilize a multilayer grading scheme in which the Sb content of $Al_{0.5}Ga_{0.5}As_{1-y}Sb_y$ is successively increased in a series of 125 nm thick layers. Post growth analysis using conventional bright field and weak beam dark field imaging of these buffer layers in cross-section reveals that the interface misfit dislocations are primarily of the 60° type and are distributed through out the interfaces of the buffer layer. When optimized, we have shown, using plan view and cross-sectional TEM, that this approach can reduce the threading defect density to below the detectability limit of TEM ($<10^5/cm^2$) and preserve growth surface planarity. The Sb-graded approach was used to fabricate two 2.2 μm power converter structures fabricated using InGaAs grown on Sb-based buffer layers on GaAs substrates. A microstructural and electrical characterization was performed on these device structures and the results are contrasted with a sample in which InP was selected as the substrate. Microstructure, defect density and device performance in these not-yet-optimized Sb-based buffer layers compares favorably to equivalent devices fabricated using InP substrates.

INTRODUCTION

The use of buffer layer structures for the creation of lattice-matched surfaces has been explored in the III-V system primarily by using indium-graded $In_xGa_{1-x}As$ alloys to form either continuously graded or step graded structures. Buffer layer structures fabricated using graded $In_xGa_{1-x}As$ steps have shown (e.g. [1]) at least three orders of magnitude reduction in threading dislocation density (to $10^5/cm^2$) when compared to equivalent compositionally-uniform (i.e. single layer) films. An alternative approach to $In_xGa_{1-x}As$ step-based buffer layers that has not been widely explored is the use of Sb-graded alloys. From a lattice parameter perspective, ternary In-grading of the GaAs - InAs (a = 6.0584 Å) pseudobinary is nearly identical to the alloying of GaAs with GaSb (a = 6.095Å) since they both produce the same final relaxed lattice parameter. The mechanism of relaxation and the resultant threading dislocation density in Sb-graded layers is not, to our knowledge, available in the literature. The Sb-graded approach allows greater flexibility in the selection of the group III flux which might be desirable if, for

example, In and/or Ga were replaced with Al to decrease the surface mobility of the metal species to effect an improvement in the growth surface morphology. For this reason, quaternary alloys of $Al_{0.5}Ga_{0.5}As_{1-y}$ Sb_y were grown on GaAs substrates to produce buffer layer structures suitable for the growth of InGaAs high electron mobility transistor (HEMT) structures.

The goal in fabricating buffer layer systems is to produce a heterostructure which is fully relaxed via the presence of interface dislocations but which contains a minimum number of threading defects. The glide of threading dislocations is necessary for the introduction of interface misfit but those threading segments that remain in the active regions of the structure after the growth is completed will degrade device performance and hence must be minimized. To reduce the number of threading defects that remain in the film after growth, their nucleation must be impeded but not eliminated. Those threading dislocations that nucleate must lay down sufficient interface misfit segments to fully relax the structure then, ideally, the threads would be removed either by glide out of the crystal (to the sample edges) or by reaction with other dislocations in the crystal. The rate of glide of a threading dislocation segment is increased by increasing the effective shear stress acting on it and by minimizing the blocking [3] effect caused by dislocation-dislocation strain-field interaction.

The features of graded-layer growth that reduce the density of threading defects (compared to the growth of a compositionally uniform single layer) have been summarized [2]. First, in compositionally graded structures, interface dislocations are not confined to a single interface but instead find a minimum energy position. As the graded-layer structure is grown, the minimum energy position for new dislocations moves further from the substrate/film interface. This is important since threading dislocations gliding in one <110> direction can be impeded by the strain field of interface misfits lying in the orthogonal direction [3]. This blocking effect is reduced by moving the minimum energy position of interface misfit dislocations to positions higher in the film as the buffer layer is grown so that the gliding thread is further removed from misfits that were formed earlier in the growth process. Second, the residual elastic strain that provides the driving force for the glide of threading dislocations is greatest near the free surface of the buffer layer structure (as it is grown) and is greatly enhanced compared to uniform layers. This aids in the movement of threading dislocations to the sample edges since the dislocation velocity is proportional to the elastic stress felt by the defect. Third, threading dislocation nucleation through dislocation reactions occurring near the substrate/film interface (e.g. [4]) are minimized because, compared to a uniform layer, the residual elastic strain deep in the buffer layer is reduced.

EXPERIMENTAL

A series of buffer layer structures were grown in a Varian MOD GEN II MBE on <001>-oriented GaAs substrates at a temperature of 450-500°C. The Al, Ga, and Sb sources were standard 125 cc cells and As was generated in a valved cracker as As_2. The buffer layer fabrication began with a 100-nm-thick homoepitaxial GaAs layer and continued with the growth of eight 125-nm-thick layers that were grown with fixed (and equal) Al:Ga fluxes. Each subsequent layer was grown with an approximately 5% increment in the Sb flux to form a concentration stair-case shown schematically in Fig. 1. The buffer structures were designed to increase the relaxed lattice parameter from that of the GaAs substrate (5.65Å) to match the lattice parameter of the materials in the active device structure (5.84Å corresponding to $In_{0.46}Ga_{0.54}As$). Between each layer, the growth was paused by shuttering the metal sources and the Sb cell temperature was ramped.

When close to the Sb-cell set-point temperature, the metal cell shutters were opened and the next layer was grown. A total of eight layers were grown all with equal Al:Ga fluxes and, at each step, an increased Sb/As ratio. On top of the staircase, a final 1 μm thick spacer layer was grown which formed the template for the growth of the active device layers. Cross-sectional and plan view TEM samples were prepared by mechanical thinning followed by ion milling at 5 keV.

RESULTS

Buffer-Layer Microstructure Characterization

Figure 2 shows a bright field 004 2-beam cross-sectional image of the 8 step stair case structure. The dislocations at the interfaces of each compositional step are revealed by g•b-analysis to be primarily 60°-type. The interface misfit dislocation density at each interface was estimated in this sample by counting the number of end-on dislocations visible when the cross-sectional sample was viewed along the [220] direction in the 004 2-beam condition. As can be seen in Fig. 2, the interface misfit density is maximum at the interface between the fourth and fifth compositional steps (i.e. in the middle of the staircase) and is smallest at the GaAs/buffer layer interface.

In conventional bright field imaging, the contrast due to the strain fields of closely spaced interface dislocations may overlap which makes the interpretation of the image difficult. As seen in Fig. 2, the dislocation density is large and, for this reason, weak beam dark field imaging was used to resolve the misfit dislocation configuration in the buffer layer. Figure 3 shows a g-3g weak beam dark field image formed using the 004 reflection. This image shows that the misfit dislocations are not confined to one interface, but instead thread from one interface to another (indicated, for example, by points A and B) and change line direction from [220] (i.e. lying in the plane of the TEM sample) to $\bar{2}20$ (i.e. lying in the thickness direction). The dislocation line segments that lie in the $\bar{2}20$ direction are revealed by oscillatory contrast such as that indicated at the point labeled C in Fig. 3. The possibility of changing interface position as the equilibrium misfit position changes during growth is one of the requirements for a successful buffer layer structure. Further, it is clear that the dislocations in this buffer layer scheme thread to other interfaces in the buffer where dislocation reactions which eliminate the threading portion may result. This reduces the number of dislocations that thread up through the spacer layer.

The effectiveness of the buffer layer in minimizing the number of threading dislocations that pass from the 8-step staircase buffer through the 1 μm spacer layer and into the active device regions is the critical measure of the success of a buffer layer scheme. In this work, this measurement was made using plan view TEM to estimate the threading defect density at the top surface of the structure. A set of samples were thinned from the backside so that only the top-most 300 nm of the structure remained. The number of threading dislocations that could be seen while crystal was tilted through a range of diffracting conditions were counted. The resulting threading dislocation density was estimated at approximately $10^{5\text{-}6}$ /cm^2 which is equivalent to the dislocation density measured for similar indium-graded $In_xGa_{1-x}As$ structures.

Figure 4 shows, in part (a), a 004 2-beam bright field image and, in part (b), an accompanying selected area diffraction (SAD) pattern taken from one of the steps of the buffer layer compositional stair-case. Compositional modulations that have formed parallel to the (004) growth surface are visible as uniformly spaced bright/dark intensity oscillations in the image. The period of these compositional modulations was determined from the satellite reflections seen

in the SAD pattern of Fig. 4(b) and is 1.8 nm. The contrast in Fig. 4(a) is greatly enhanced by the use of the 004 2-beam imaging conditions which allows elastic strain relaxation near the TEM sample surfaces to artificially enhance [5] the image contrast; the same area imaged using the 220 reflection does not reveal the compositional modulations. An analysis of the SAD satellite reflection intensity and investigation of the effect of the growth flux on the satellite period reveals that the modulations consist of small-scale fluctuations in the As:Sb ratio. While the origin of these composition modulations is presently obscure, they provide insight into the planarity of the growth surface. Observation of the compositional modulations through the thickness of the buffer layer and in the spacer layer reveal that the growth surface remains planar over a lateral scale of 100's of nms thoughout the growth. Although not yet clearly established experimentally, it appears that the use of Al in the metal flux, with its lower surface mobility compared to either In or Ga, plays an important role in preserving the growth surface planarity.

Device Performance

0.55 eV p-on-n InGaAs diodes grown on GaAs substrates with GaAsSb graded layers were characterized by measuring external quantum efficiency versus wavelength, non-illuminated current-versus-voltage (I-V), black body-illuminated low-current I-V, and white-light-illuminated high-current I-V. For all measurements, the device temperature was maintained at 25 C. Two n-on-p device structures were investigated: a conventional thin emitter, thick base device [Fig. 5a] and a thick emitter, thin base device [Fig. 5b]. The former device is sensitive to base diffusion length and back surface recombination velocity, while the later device is sensitive to emitter diffusion length and surface recombination velocity.

Figure 6 plots typical external quantum efficiency versus wavelength for each of the device structures. Thick emitter, thin base devices demonstrate low quantum efficiency (< 20%) over the entire wavelength range with the peak quantum efficiency occurring at long wavelengths (2000 nm). This illustrates both poor surface recombination velocity and emitter diffusion length. Conventional, thin emitter, thick base devices however showed improved performance in the short-wavelength regions, since the junction is closer to the front surface.

Cross-sectional and plan view TEM were used to determine the number density of dislocations that pass through the buffer layer into the active 3 μm-thick InGaAs absorption layer. In the best of the two GaAs-substrate devices, plan view TEM reveals a dislocation density of $9x10^8$ /cm^2 while equivalent devices grown on InP substrates were observed to have a dislocation density of $4x10^8$/cm^2. The low long-wavelength response for both device structures was attributed to the propagation of defects due to the 0.83% lattice mismatch between the final graded layer and the base [Fig. 7]. Analytic 1-D modeling of these device structures yielded surface and back recombination velocities of 10^7 cm/s, and emitter/base diffusion lengths of ~ 2 μm.

Table 1 summarizes average values of the dark current density (J_d), series resistance (R_s), and ideality factor (n) extracted from non-illuminated I-V measurements; open circuit voltage (V_{oc}), short circuit current (I_{sc}) and fill factor (FF) for both a 1200 C blackbody measurement (BB) (view factor ~ 0.2) and a high intensity flash lamp (FL) for both device structures. These results again indicate high values of dark current, low open circuit voltage, and low fill factor are due to the propagation of defects.

Microstructure, defect density and device performance in these not-yet-optimized Sb-based buffer layers compares favorably to equivalent devices fabricated using InP substrates.

SUMMARY

Relaxed Sb-graded AlGaAsSb quaternary buffer layer structures were fabricated that consist of an eight-step staircase that provides a growth surface with a 5.85Å lattice parameter on GaAs substrates. Cross-sectional TEM reveals that both the 1 μm thick spacer layer and the underlying buffer layers remain planar throughout the growth and that the structure is relaxed via the introduction of 60° misfit dislocations at the interfaces of the buffer layer. Thus, the relaxation mechanism of the step graded quaternary AlGaAsSb buffer is similar to that observed for step graded InGaAs buffers. The threading defect density in the active regions of these structures was measured using plan view TEM to be approximately $10^{5\text{-}6}$ /cm^2 which suggests that this approach to buffer layer synthesis is a promising alternative to the use of InGaAs graded layer structures.

ACKNOWLEDGMENTS

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Figure 3: Weak beam dark field image using g-3g and g=$2\bar{2}0$. Features A, B, and C represent examples of dislocations threading from one interface to another, changing line direction, and interacting, respectively.

Figure 4: (a) Bright-field 004 2-beam image showing compositional modulations taken from one of the steps of the buffer layer compositional stair-case. (b) Selected area diffraction pattern showing the satellite reflections oriented in the 004 direction around each of the primary reflections in the 110 zone.

Figure 5: Schematic diagram of a conventional thin emitter, thick base device (a) and a thick emitter, thin base device (b).

Figure 6: Quantum efficiency versus wavelength measurements for each of the 2.2 μm power conversion devices grown on a Sb-step-graded buffer layer.

Figure 7: Cross-sectional TEM image of a InGaAs 2.2 μm power conversion device grown on a Sb-step-graded buffer layer.

	J_d (A/cm^2)	R_s ($m\Omega$)	n	BB V_{oc} (mV)	BB I_{sc} (mA)	BB FF	FL V_{oc} (mV)	FL I_{sc} (mA)	FL FF
Thin emitter , Thick base	8×10^{-3}	10	2	118	152	37	211	1355	37
Thick emitter, thin base	1.5×10^{-2}	10	1.6	50	150	35	115	935	32

Table 1

	$In_{0.46}Ga_{0.54}As$ HEMT
1.0 µm	$Al_{0.5}Ga_{0.5}As_{1-v}Sb_v$
125 nm	$Al_{0.5}Ga_{0.5}As_{1-v}Sb_v$
125 nm	$Al_{0.5}Ga_{0.5}As_{1-v}Sb_v$
125 nm	$Al_{0.5}Ga_{0.5}As_{1-v}Sb_v$
125 nm	$Al_{0.5}Ga_{0.5}As_{1-v}Sb_v$
125 nm	$Al_{0.5}Ga_{0.5}As_{1-v}Sb_v$
125 nm	$Al_{0.5}Ga_{0.5}As_{1-v}Sb_v$
125 nm	$Al_{0.5}Ga_{0.5}As_{1-v}Sb_v$
125 nm	$Al_{0.5}Ga_{0.5}As_{1-v}Sb_v$
100 nm	GaAs
	GaAs Substrate

Figure 1

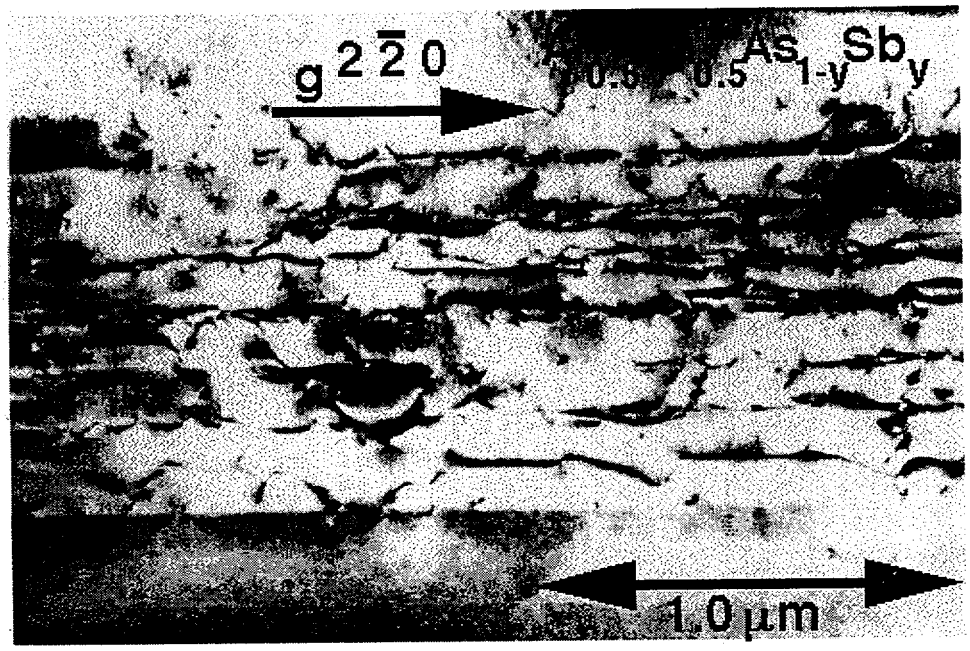


Figure 2

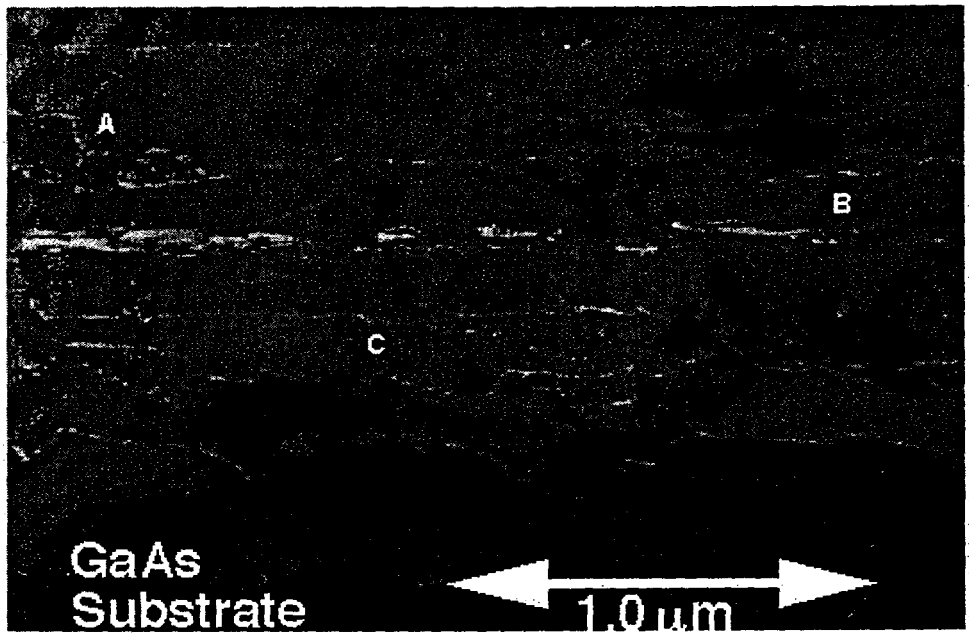


Figure 3

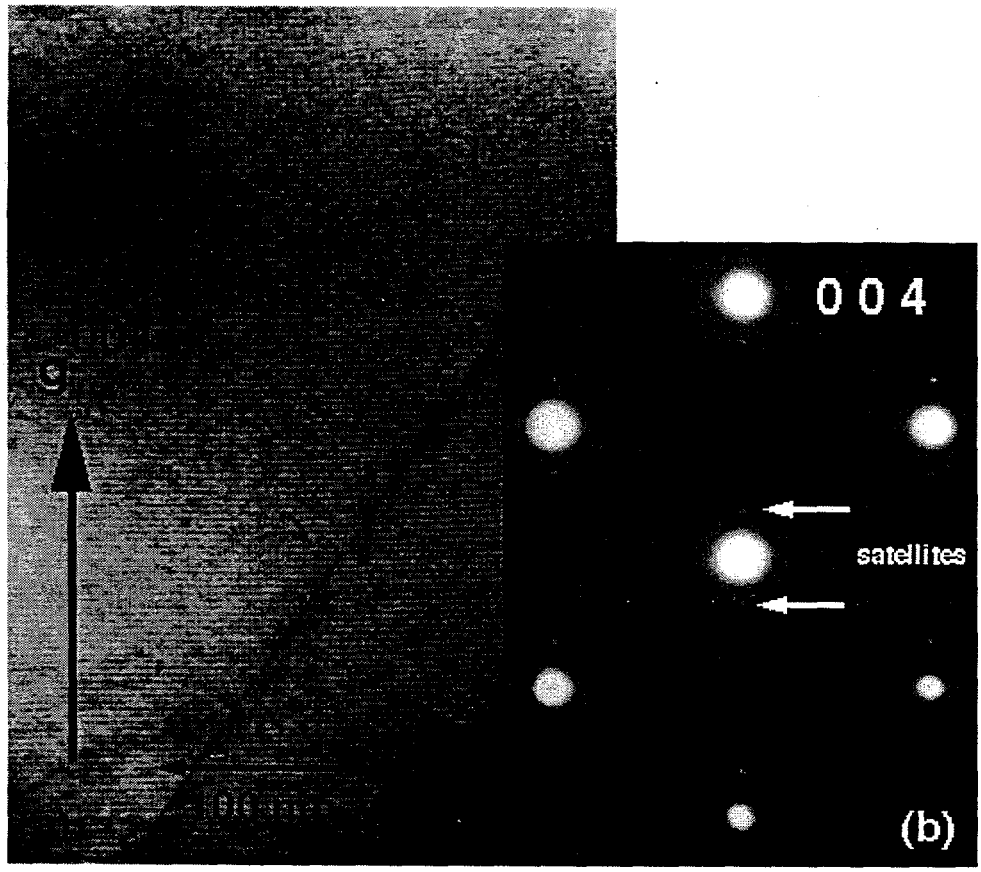
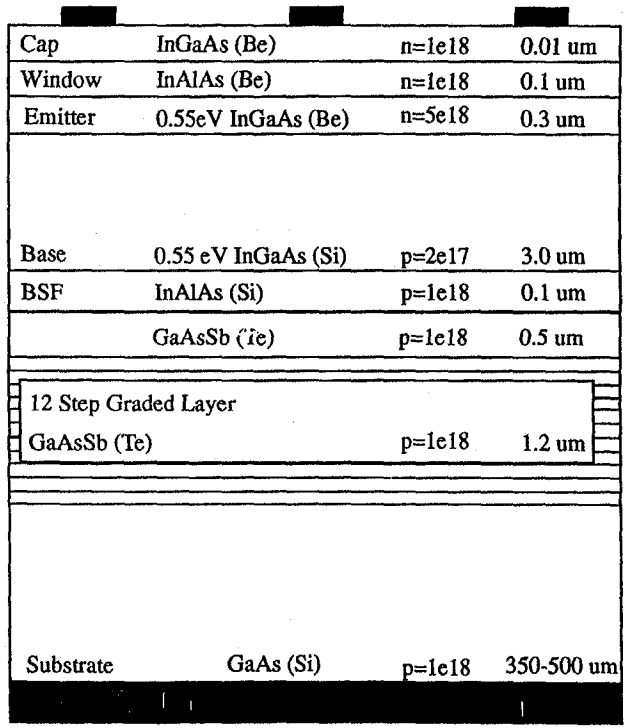
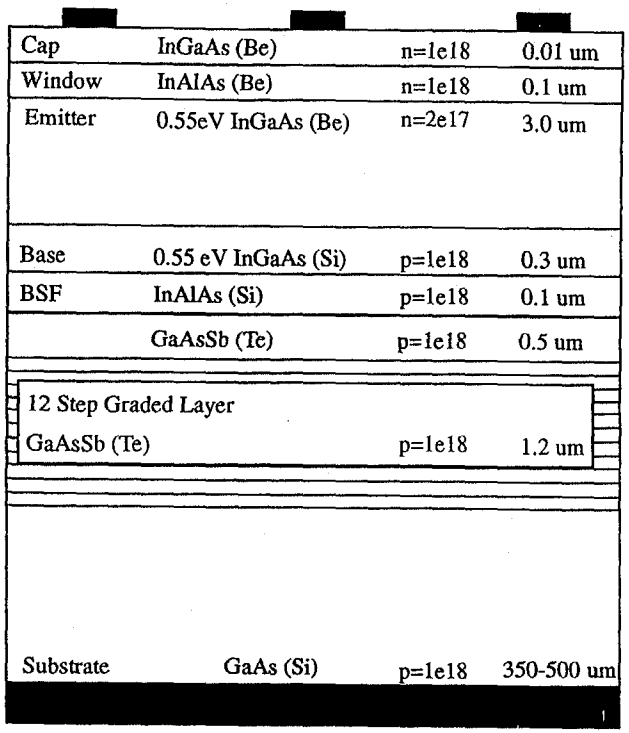


Figure 4

Figure 5


Cap InGaAs (Be) n=1e18 0.01 um
Window InAlAs (Be) n=1e18 0.1 um
Emitter 0.55eV InGaAs (Be) n=5e18 0.3 um
Base 0.55 eV InGaAs (Si) p=2e17 3.0 um
BSF InAlAs (Si) p=1e18 0.1 um
GaAsSb (Te) p=1e18 0.5 um
12 Step Graded Layer
GaAsSb (Te) p=1e18 1.2 um
Substrate GaAs (Si) p=1e18 350-500 um

(a)


Cap InGaAs (Be) n=1e18 0.01 um
Window InAlAs (Be) n=1e18 0.1 um
Emitter 0.55eV InGaAs (Be) n=2e17 3.0 um
Base 0.55 eV InGaAs (Si) p=1e18 0.3 um
BSF InAlAs (Si) p=1e18 0.1 um
GaAsSb (Te) p=1e18 0.5 um
12 Step Graded Layer
GaAsSb (Te) p=1e18 1.2 um
Substrate GaAs (Si) p=1e18 350-500 um

(b)

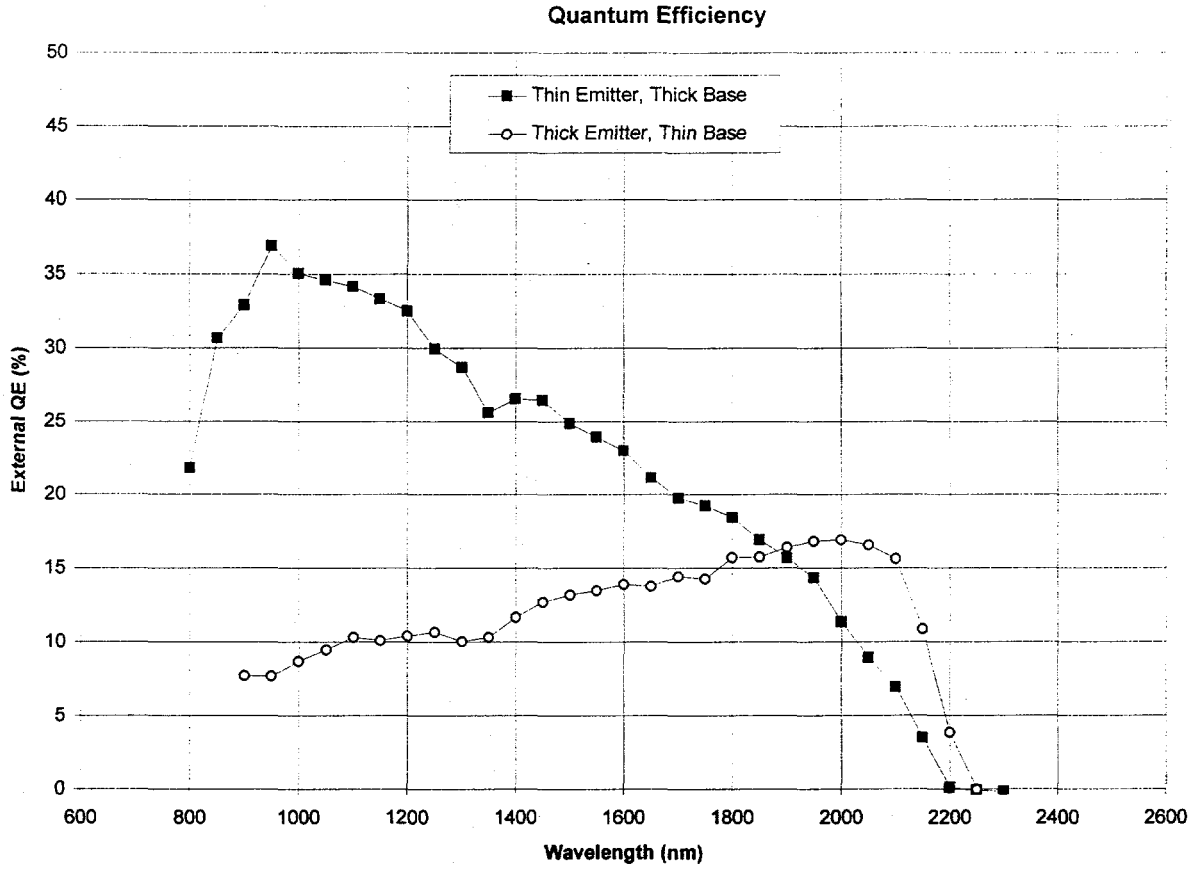

Quantum Efficiency
Thin Emitter, Thick Base
Thick Emitter, Thin Base
External QE (%)
Wavelength (nm)
0
5
10
15
20
25
30
35
40
45
50
600
800
1000
1200
1400
1600
1800
2000
2200
2400
2600

Figure 6

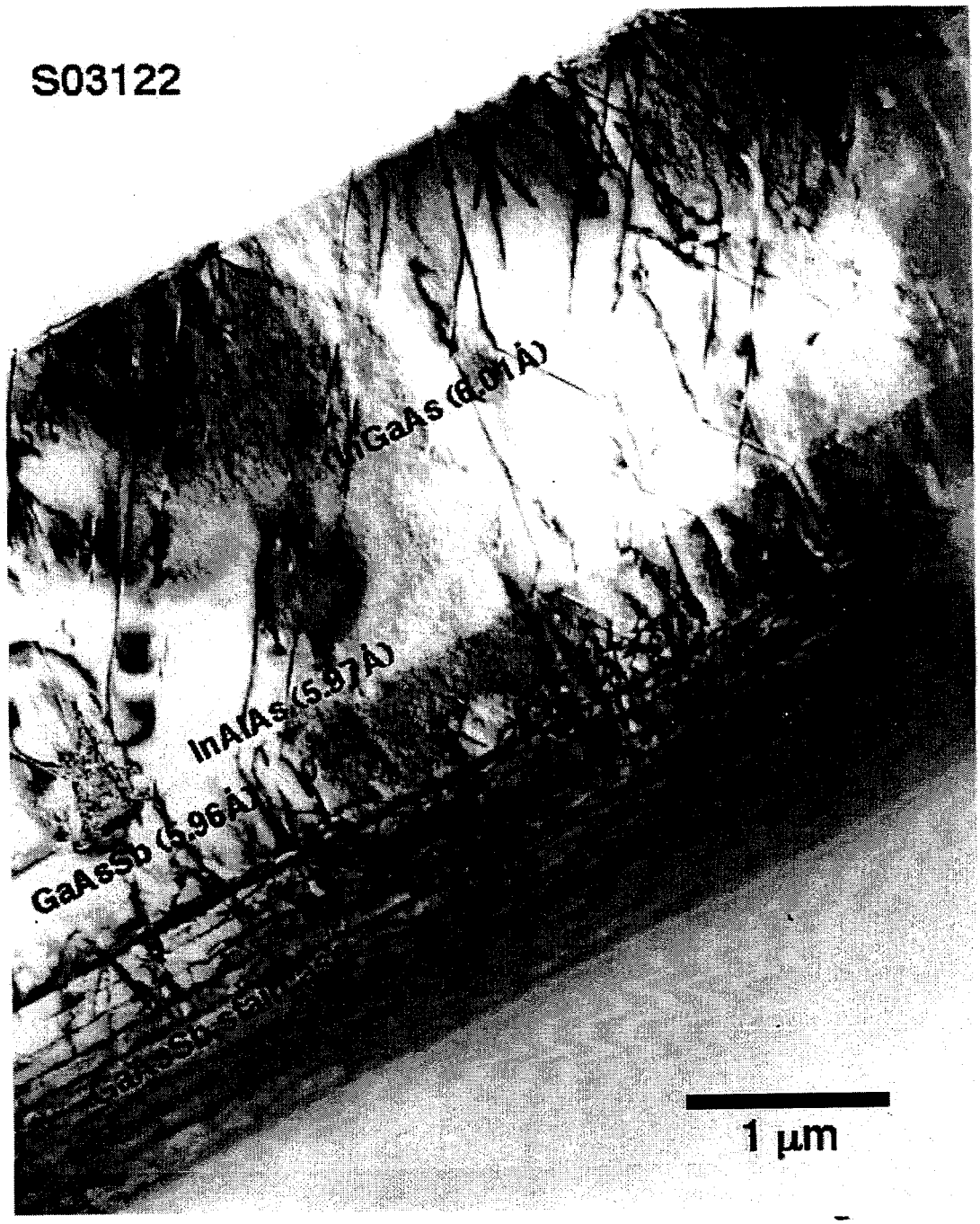


Figure 7