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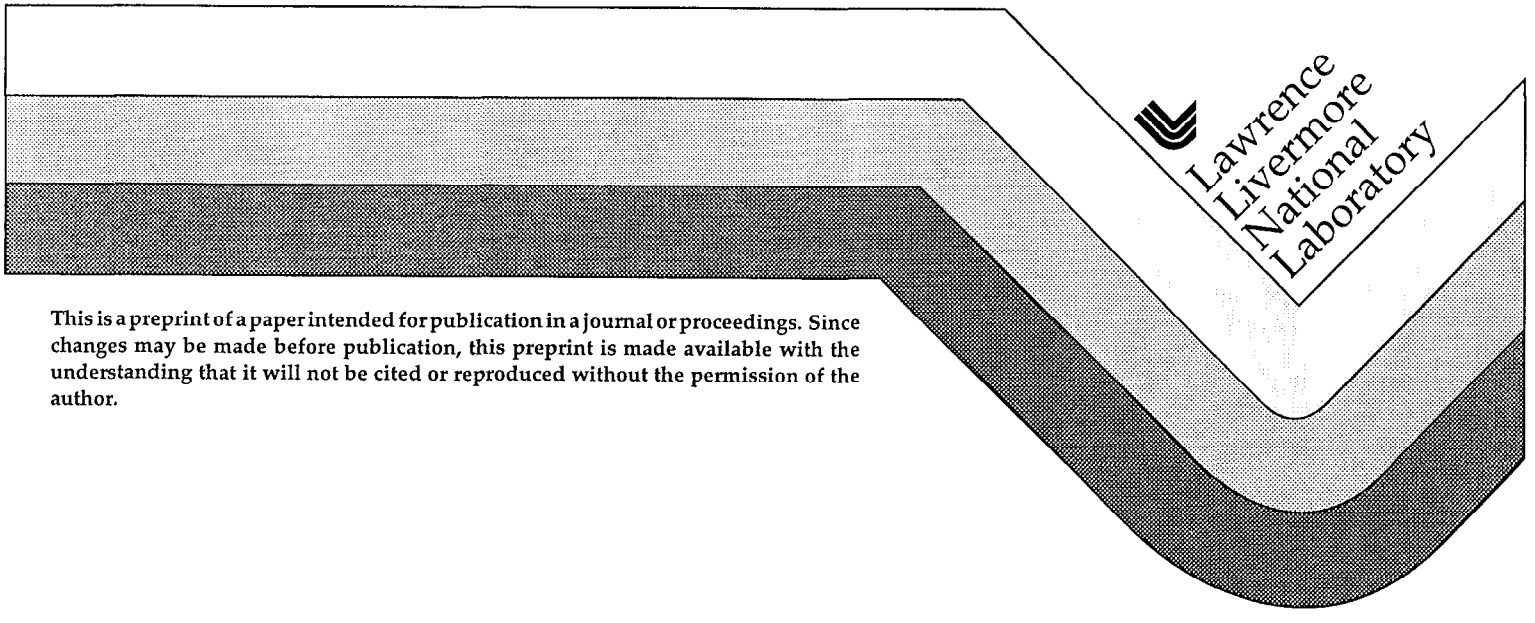

AN ALL SOLID STATE PULSE POWER SOURCE FOR HIGH PRF INDUCTION ACCELERATORS

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ABSTRACT

Researchers at the Lawrence Livermore National Laboratory (LLNL) are developing a flexible, all solid-state pulsed power source that will enable an induction accelerator to produce mulitkiloampere electron beams at a maximum pulse repetition frequency (prf) of 2 MHz. The prototype source consists of three, 15-kV, 4.8-kA solid-state modulators stacked in an induction adder configuration. Each modulator contains over 1300 field-effect transistors (FETs) that quickly connect and disconnect four banks of energy storage capacitors to a magnetic induction core. The FETs are commanded on and off by an optical signal that determines the duration of the accelerating pulse. Further electronic circuitry is provided that resets the magnetic cores in each modulator immediately after the accelerating pulse. The system produces bursts of five or more pulses with an adjustable pulse width that ranges from 200 ns to 2 μs. The pulse duty factor within a burst can be as high as 25% while still allowing time for the induction core to reset. The solid-state modulator described above is called ARM-II and is named for the Advanced Radiographic Machine (ARM)—a powerful radiographic accelerator that will be the principal diagnostic device for the future Advanced Hydrotest Facility (AHF).

BACKGROUND

The Stockpile Stewardship and Stockpile Management Programs were developed to assure the performance, reliability and safety of our nuclear weapons stockpile without the use of nuclear testing. This assurance will be achieved through a combination of computational modeling and non-nuclear experiments. Key among these experiments is an examination of the chemical explosive phase of a stockpiled weapon with its nuclear components removed and replaced with non-nuclear materials. Pulsed radiographs are used in these experiments to diagnose changes in density and material position as the explosive pressures compress the simulant materials into a dense core. If the radiographic information is detailed and accurate enough, it is possible to infer certain safety and performance aspects about the aged weapon for comparison against the original design specifications.

The radiographic machines now in use produce a penetrating flash of x rays from several types of single-pulse electron beam accelerators [1,2]. In each case, the explosive action is imaged for only one moment in time. Unfortunately, the radiographic data needed to replace an underground nuclear test requires enough radiographs be taken from several vantage points to provide a three-dimensional assessment of the explosion at several important moments in time (multipulse tomography). This radiographic capability is beyond all existing facilities to date.

INTRODUCTION

We are developing a concept to produce the radiographic capabilities needed for Stockpile Stewardship. The concept is based on a single linear induction accelerator (LIA) and is shown in Figure 1. The method calls for an accelerator that produces 16-20 MeV, 3-6 kA electron beams in long pulses that may vary from 200 ns to 2 μs. For example, the figure shows how a 200-ns beam is cleaved in half by an electromagnetic "kicker" device that directs the divided beam portions down separate pathways [3]. By repeating the process, the 100-ns beam halves are further chopped into four, 50-ns beams. The four beams are transported along beamlines with different path lengths so as to synchronize their arrival at the firing chamber wall where they are converted into x-ray sources for radiography. The beam chopping produces the needed views but the accelerator must also produce a repeated number of beams to image various moments in time. We are developing an all solid-state power source that will pulse the accelerator at rates beyond a megahertz while magnetically resetting the accelerator cores between pulses. The two power sources shown in Figure 1 are inductive voltage adders that sum the voltage contributions from each of three solid-state modulators. The output voltage from the adders is multiplied by three at the accelerating gap due to the action of three induction cores within the accelerator cell. Details concerning the operation of an induction accelerator and the behavior of a multicore cell can be found in the literature [4,5].

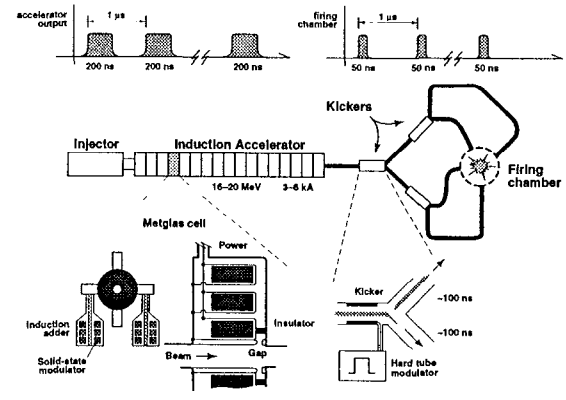

Figure 1. Illustration of an LIA concept for advanced radiography.

The solid-state induction adder is a significant advancement over previous power systems for induction accelerators. For example, the ETA-II induction accelerator at LLNL produces a short burst of 7.5-MeV, 2-kA, 50-ns beams at a maximum prf of 5 kHz [6]. This record-setting pulse rate is accomplished with thyratron switches and magnetic pulse compression technology [7]. By comparison, a solid-state power system will exceed the ETA-II performance by a factor of 400 for prf and a factor of 1000 for a long-burst duty cycle. The solid-state system also produces a variable pulse width and can be used to actively regulate the cell voltage by operating the FETs as amplifier elements, rather than as fast switches.

ARM-II MODULATOR

The network architecture for ARM-II is based on the simple idea of connecting and disconnecting a large capacitor bank to an accelerator cell using solid-state switches. By doing so, the capacitors attempt to keep the gap voltage constant while providing the nonlinear currents needed by the beam and core material. Furthermore, a large capacitor bank stores far more energy than is needed for a high prf burst, so the bank does not require recharging between pulses (as would transmission lines or pulse-forming networks). Figure 2 illustrates the switching actions and idealized waveforms from a simplified ARM-II circuit.

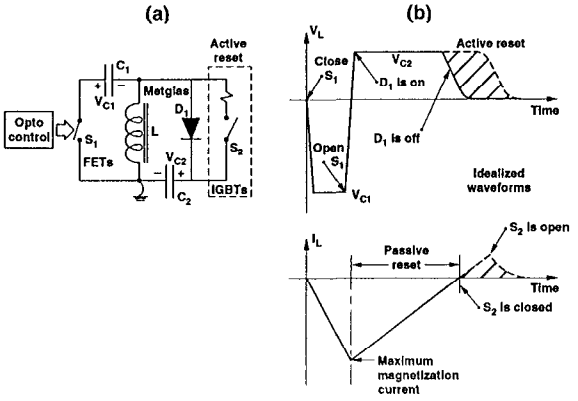

Figure 2. (a) Shows an idealized ARM-II circuit diagram accompanied by (b) voltage and current waveforms. One should note that the closure of S_2 enables the magnetization current to reverse in L.

Two views of a single ARM-II modulator are shown in Figure 3 along with the original design specifications listed in Table 1. The switching and reset circuits are divided into separate modules that attach to the circumference of a central induction core. The switching module contains a stack of 28, 1-kV circuit boards that host 12 FETs in parallel. Each FET is served by a gate-drive circuit that receives control power from a dc/dc converter and on/off commands from an optical fiber. The boards are connected in series by mechanically clamping the boards together using small interface springs as current contacts. The four switching modules per modulator are each connected to a 4-μF, 20-kV capacitor bank.

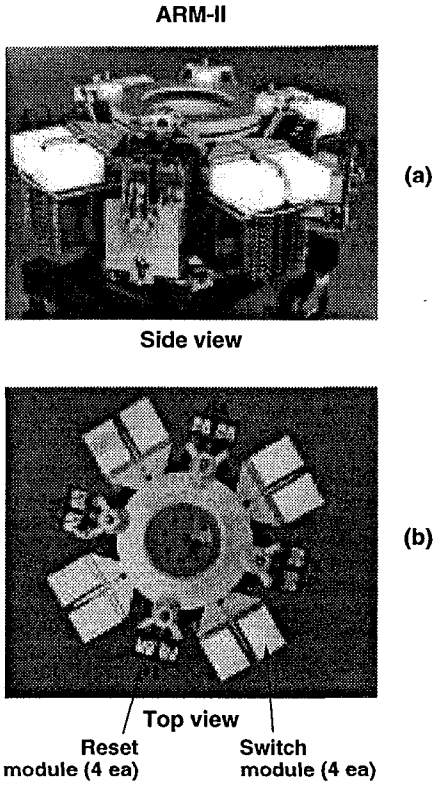

Figure 3 (a,b). Top and side views of a single ARM-II modulator.

Design specifications

Design voltage	15 kV
Maximum current	4.8–6 kA
Pulse range	200 ns–1.5 μs
Maximum prf range	1 MHz–150 kHz
Number of FETs	1,344
Energy stored	2.25 kJ (total)
Core material	2605 SC
Outer diameter	1.22 m
Approximate weight	280 kg

Table 1. Design specifications for the ARM-II modulator.

The goal of the active reset system is to control the magnetic states of the modulator and accelerator cell so that a long burst of pulses can be sustained without saturating the magnetic core material. This is achieved by switching the insulated gate bipolar transistors (IGBTs) on until the volt-second content of the positive reset pulse equals the volt-second content of the negative accelerating pulse. Like the switching system, the reset system is made up of 1-kV circuit boards that are stacked 28 in series and held together by a mechanical clamping method. The four reset modules per modulator each contain two stacks of reset circuit boards that work in parallel to switch a single 4-μF, 10-kV capacitor.

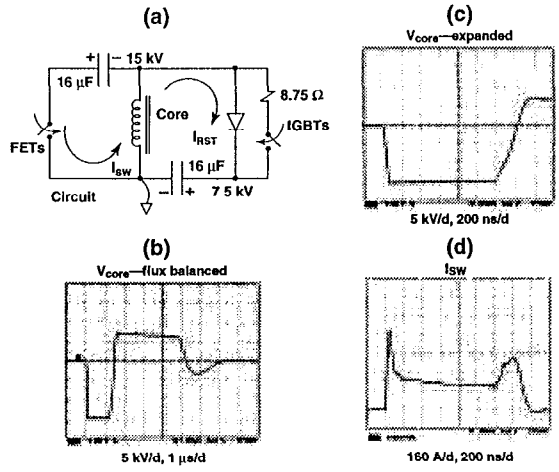

Figure 4. (a) Simple ARM-II circuit diagram showing current pathways and component values. (b) and (c) are voltage measurements across the core. (d) Represents the total FET switch current.

Figure 4 shows the core voltage and switch current from a single ARM-II modulator operating without an external load. Figure 5 shows the same voltage and current information when the modulator is powering a 3-Ω load. One should note that the load resistor is in series with a diode to simulate the loading effect of an electron beam that is present during the acceleration pulse but not during the reset pulse. The ARM-II modulator is the second of three machines scheduled for development within our program. Test results from the ARM-I machine may be found in the literature [8].

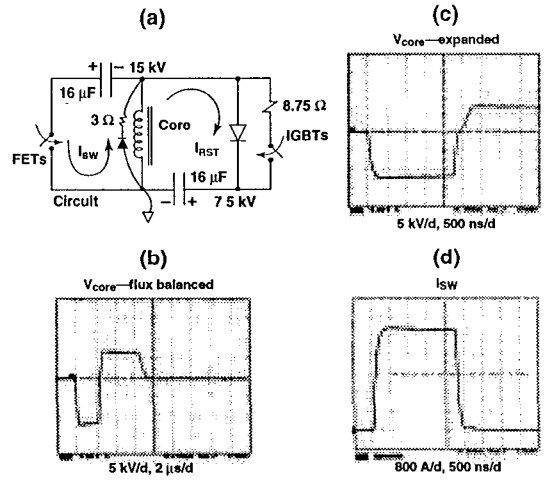

Figure 5. (a) Simple ARM-II circuit diagram showing a diode-coupled load across the core. (b) and (c) are voltage measurements across the core. (d) Represents the total FET switch current.

THREE-STAGE INDUCTION ADDER

The induction adder assembly consists of three ARM-II modulators stacked on top of each other and threaded with a central stalk for voltage summing, as shown in Figure 6. Voltage from each modulator is gathered by the

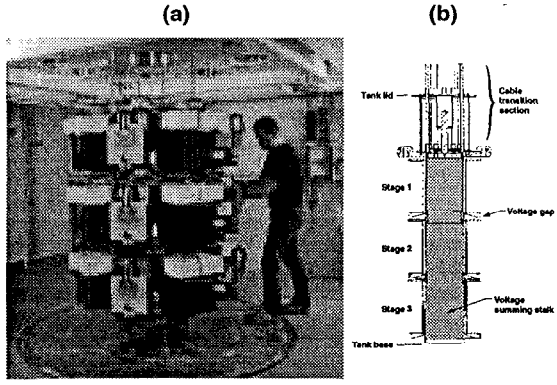

Figure 6. (a) Photograph showing three ARM-II modulators stacked together without service attachments. (b) Mechanical diagram showing that the summing stalk fits within the ARM-II cores and delivers power to the cables.

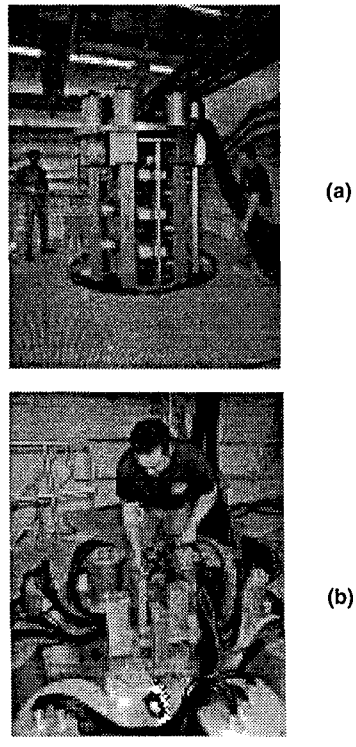

Figure 7. (a) Adder assembly being lowered into an oil tank. (b) Top deck of the adder showing service cables and form load assemblies connected in place of 50-Ω cables.

stalk and delivered to a set of 50-Ω cable connections at the top of the machine. At these connections, we have the option of plugging in cables that can carry the power away to another location or plugging in enough 50-Ω, diode-coupled load assemblies to simulate an electron beam load at the machine. Figure 7(a) is a photograph of the adder assembly being lowered into a tank filled with insulating oil. The large bundle of cables in the picture carries utilities and diagnostic services to the modulators via eight vertical enclosures. Figure 7(b) shows four, 50-Ω load assemblies plugged into the output ports.

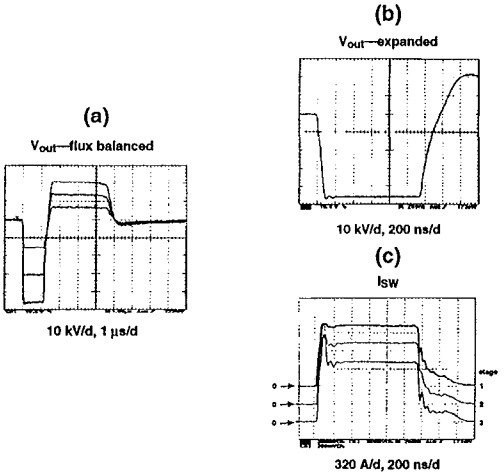

Figure 8. (a) Shows three voltages measured at the stalk as the modulators are changed one at a time. (b) Representative voltage with all three modulators operating. (c) Currents from all three modulators (displaced one division for clarity).

Figure 8 shows the stalk voltage and switch currents when the adder is operating into a 50-Ω load. In this figure, each modulator is activated one at a time to show their independent but equal power contributions. Figure 9 is a short-circuit test of the adder at full power, which illustrates a well coordinated effort by all three modulators to manage an over-current condition for the switching and reset

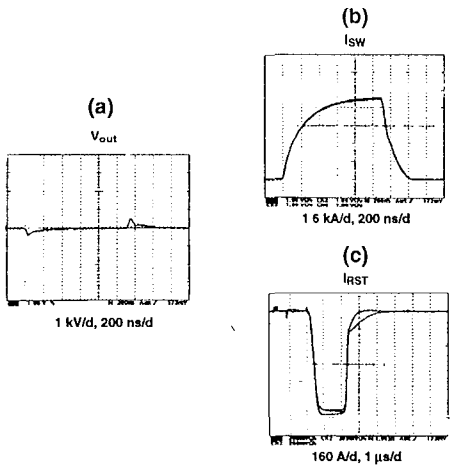

Figure 9. Short circuit tests on the adder showing (a) stalk voltage. (b) FET switch current indicating a peak short-circuit current of 7.2 kA (limited by feedback). (c) Total IGBT current indicating a short-circuit current of 912A (limited by resistor).

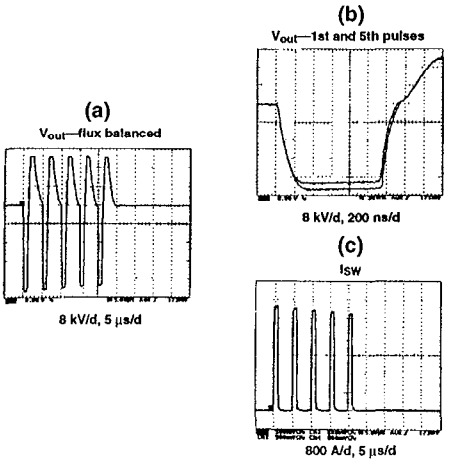

Figure 10. 200-kHz burst data showing (a) five voltage pulses with active reset. (b) Voltage measured at the stalk showing a drop in voltage on the fifth pulse when compared with the first. (c) Burst of FET current pulses indicating a peak value of 4.4 kA.

systems. Figure 10 is a 200-kHz burst of five pulses at full power with the first and fifth pulses overlaid to show the total change in output voltage due to pulsed loading. The figure also illustrates a typical operating condition where the volt-second content of the accelerating and reset pulses are adjusted to be equal (flux balanced). This condition affords each pulse in the burst the maximum available flux swing from each core. Managing the reset condition of the cores is important when pulse flexibility is needed. The pulse schedule in Figure 11 illustrates the pulse-to-pulse agility of the adder and shows that the final long pulse (or long burst) can avoid core saturation by actively controlling the reset conditions of earlier pulses.

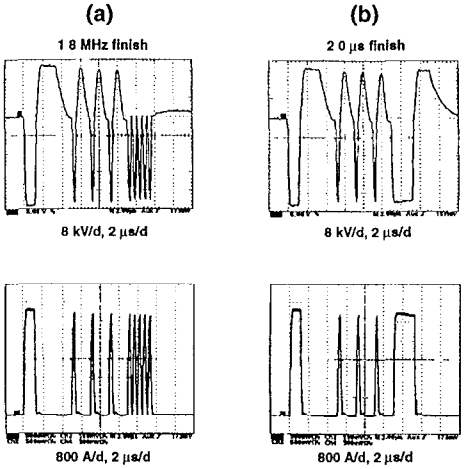

Figure 11. An arbitrary pulse schedule showing (a) stalk voltage and FET current for a pulse train that finishes with five 200-ns pulses at 1.8 MHz. (b) Stalk voltage and FET currents showing a pulse train that finishes with a 2-µs pulse.

OUR NEXT STEP AND AN OUTLOOK TO THE FUTURE

The ARM-II modulators and adder assembly were built to demonstrate that solid-state power electronics is mature enough to produce the pulse power needed for high-current induction accelerators. To reduce our investment risk, we made ARM-II far more durable than fast with the idea that speed and analog waveform control would be topics for future investigations. For example, the five-pulse burst in Figure 12 produces full-power pulses that are nearly triangular due to a slow FET turn-on time. We are developing a new switch board that, according to simulations, will speed up the turn-on time by an order of magnitude.

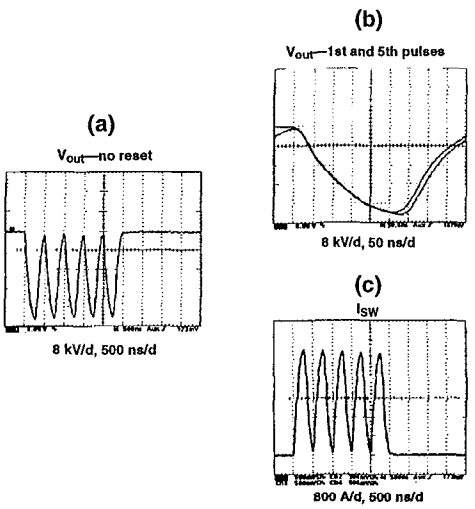

Figure 12. 2-MHz burst data showing (a) five voltage pulses with no reset time. (b) Stalk voltage detail showing the first and fifth pulses. Note the slow rise time. (c) Five current pulses at the maximum prf with a peak current of 4.3 kA.

At present, we are designing and building a double-core, long-pulse accelerator cell that will be powered by the solid-state adder. Our plans include moving the adder-cell combination to the Los Alamos National Laboratory early next calendar year for tests on a long-pulse electron beam facility called THOR. If successful, the tests will demonstrate a complete accelerator pulse power chain using solid-state switching.

We believe that continued rapid growth in the power electronics industry will further expand the applications of solid-state switching to pulse power problems [9]. In the five years since our ARM research began, we have seen the current capacity of power FETs double, with more increases expected. We are also expecting the commercial availability of silicon carbide FETs in the very near future, which will offer dramatic improvements in off-state voltage, on-state resistance, and switching speed.

REFERENCES

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