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Plasma Etching, Texturing, and Passivation of Silicon Solar Cells

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Abstract. We improved a self-aligned emitter etchback technique that requires only a single emitter diffusion and no alignments to form self-aligned, patterned-emitter profiles. Standard commercial screen-printed gridlines mask a plasma-etchback of the emitter. A subsequent PECVD-nitride deposition provides good surface and bulk passivation and an antireflection coating. We used full-size multicrystalline silicon (mc-Si) cells processed in a commercial production line and performed a statistically designed multiparameter experiment to optimize the use of a hydrogenation treatment to increase performance. We obtained an improvement of almost a full percentage point in cell efficiency when the self-aligned emitter etchback was combined with an optimized 3-step PECVD-nitride surface passivation and hydrogenation treatment. We also investigated the inclusion of a plasma-etching process that results in a low-reflectance, textured surface on multicrystalline silicon cells. Preliminary results indicate reflectance can be significantly reduced without etching away the emitter diffusion.

PASSIVATED, PATTERNED EMITTER

The purpose of our work is to improve the performance of standard commercial screen-printed solar cells by incorporating high-efficiency design features without incurring a disproportionate increase in process complexity or cost. Our approach uses plasma processing to replace the heavily doped homogenous emitter and non-passivating antireflection coating (ARC) with a high-performance selectively patterned diffusion covered with a passivating ARC. A slight variation of the plasma step can effectively texture even multicrystalline silicon (mc-Si) surfaces to significantly reduce front surface reflectance.

Plasma-enhanced chemical vapor deposition (PECVD) is now recognized as a performance-enhancing technique that can provide both surface passivation and an effective ARC layer [1]. For some solar-grade silicon materials, it has been observed that the PECVD process results in the improvement of bulk minority-carrier diffusion lengths as well, presumably due to bulk defect passivation [2].

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In order to gain the full benefit from improved emitter surface passivation on cell performance, it is necessary to tailor the emitter doping profile so that the emitter is lightly doped between the gridlines, but heavily doped under them [3]. This is especially true for screen-printed gridlines, which require very heavy doping beneath them for acceptably low contact resistance. This selectively patterned emitter doping profile has historically been obtained by using advanced screen-printed alignment techniques [4] and multiple high-temperature diffusion steps [3]. We have attempted to build on a self-aligned emitter etchback technique described by Spectrolab that requires only a single emitter diffusion and no alignments [5].

Reactive ion etching (RIE) using SF_6 etches back the emitter but leaves the gridlines and emitter regions beneath them unetched. This removes the heavily diffused region and any gettered impurities between gridlines while leaving the heavily doped regions under the metal for reduced contact resistance and recombination. This leaves a low-recombination emitter between gridlines that requires good surface passivation for improved cell performance. Therefore, we follow the etchback with a surface-passivating PECVD-nitride layer. The nitride also provides a good ARC and can be combined with plasma-hydrogenation treatments for bulk defect passivation.

Textured, Low-Reflectance Emitter

Several groups have reported interest in plasma-etching techniques to texture mc-Si cells, because mc-Si cannot benefit sufficiently from the anisotropic etches typically used for single-crystal Si. In contrast to laser or mechanical texturing, plasma-etching textures the entire cell at once, which is necessary for high-throughput. Inomata et al. used Cl_2-based RIE on mc-Si to fabricate a 17.1% efficient cell, showing that plasma-texturing does not result in performance-limiting surface damage [6].

We developed a variation of the SF_6 emitter etchback process, which results in good surface texturing. Use of SF_6 keeps the process compatible with the metal gridlines. This allows the texturing to be done after the metallization step as part of the emitter-etchback process.

EXPERIMENTAL PROCEDURE

The textured, self-aligned selective-emitter (SASE) plasma-etchback and passivation process is shown in Figure 1. The SASE concept uses cells that have received standard production-line processing through the printing and firing of the gridlines. Then the cells undergo reactive ion etching (RIE) to first texture and etch away the most heavily-doped part of the emitters in the regions between the gridlines, increasing the sheet resistance in these areas to 100 ohms/square.

For emitter etchback, we used a new PlasmaTherm 790 reactor. This is a commercial RF dual parallel-plate reactor operating at 13.56 MHz. This equipment is IC industry-standard, programmable, and capable of being configured in a cluster-tool arrangement for high-throughput. Wafers were etched in pure SF_6 at powers between 15 and 45 W and pressures ranging from 100 to 150 mTorr. Gas flow rates were between 14 and 26 sccm.

For texturization, we performed room-temperature RIE in a Technics, PEII-A parallel-plate reactor. We used mixtures of SF_6 with varying amounts of O_2. RF power ranged from 50 to 300 W.

Wafers received a silicon-nitride deposition (PECVD-nitride), using conditions similar to those found to be effective for bulk and surface passivation in String Ribbon™ mc-Si [2]. The plasma-nitride depositions were performed using the PECVD chamber of the PlasmaTherm reactor. Reaction gases for nitride deposition were a 5% mixture of silane in helium, nitrogen, and anhydrous ammonia. The optional H-passivation treatment consists of an exposure to a pure ammonia plasma between 300-400C in the PECVD reactor. We found that less power is required to generate a NH_3-plasma than a H_2-plasma, resulting in less surface damage. Nitride-coated cells then receive a forming gas anneal (FGA) at 300C for 30 minutes. The cells at this point are returned to the production-line for final cell processing, if any.

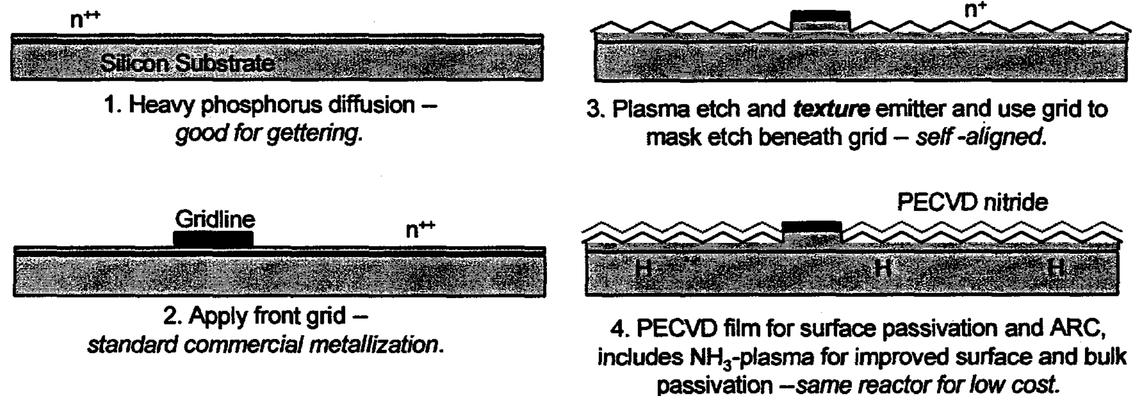

FIGURE 1. Process sequence for textured, self-aligned selective-emitter cells. The emitter etchback can be done after texturization to remove any surface damage the texturing may cause.

Emitter-Passivation Studies

Our previous work showed that we were able to obtain lower J_{oe} values and better surface passivation using a 3-step nitride deposition process compared to a single continuous deposition [7]. The 3-step process starts with deposition of a thin layer of nitride to protect the Si surface, followed by exposure to a NH_3-plasma, and finally the deposition of the remaining nitride required to attain the correct thickness for ARC purposes.

We conducted a statistically designed multifactor experiment to find the 3-step parameters that would minimize J_{oe} on float zone wafers using our previous response surface methodology [7,8]. The results of a quadratic interaction experiment are shown in Fig. 2.

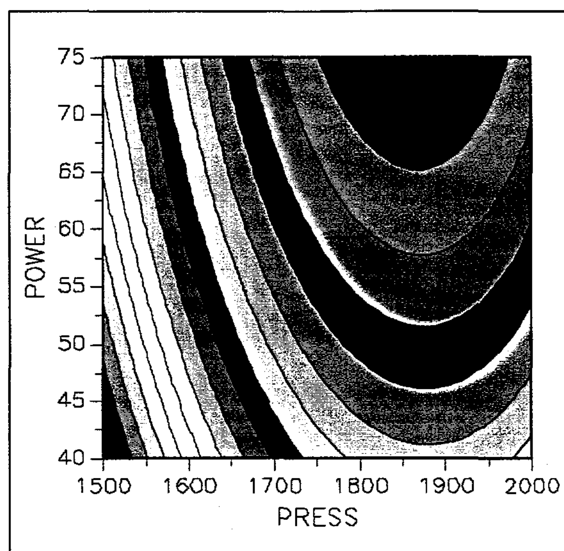

FIGURE 2. Contour plot showing response of J_{oe} to the power (W) and pressure (mT) during NH_3-treatment with a protective-nitride thickness of 10 nm. J_{oe} ranges from 216 in the lower left corner to a minimum of 161 fA/cm^2 near the upper right corner. The duration of the NH_3 hydrogenation was 20 minutes.

SASE Cell Processing

We used the parameters that produced minimum J_{oe} on 130-cm^2 cells processed up through gridline firing on the Solarex production line. We investigated whether shorter NH_3-treatments would retain the benefits of surface passivation. Results of IV testing are shown in Table 1.

TABLE 1. Six SASE sequences were applied to 12 Solarex mc-Si cells (2 cells/sequence) using matched material from the same ingot as the controls. Illuminated cell IV data ± standard deviation are shown normalized to a constant transmittance to account for the additional 1.1% spectral-weighted absorbtance in the nitride.

Eff.	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (%)
90 sec. RIE, **1-step** SiN, FGA			
12.3±0.4	30.5±.0.0	565±4	71.6±1.6
90 sec. RIE, **3-step** SiN, **5 min NH_3**, FGA			
12.9±0.1	30.6±.0.1	573±1	73.5±0.4
90 sec RIE, **3-step** SiN, **10 min NH_3**, FGA			
12.4±0.0	30.3±.0.0	570±0	72.0±0.0
150 sec RIE, **1-step** SiN, FGA			
12.1±0.5	30.1±.0.0	562±7	71.3±2.2
150 sec RIE, **3-step** SiN, **5 min NH_3**, FGA			
12.9±0.2	30.4±.0.3	576±4	73.5±1.4
150 sec RIE, **3-step** SiN, **10 min NH_3**, FGA			
13.0±0.2	30.4±.0.0	577±2	74.0±0.9
Control Cells: No emitter etchback, TiO_2 ARC			
12.6±0.0	30.2±.0.1	569±0	73.5±0.0

The first three groups of cells were not etched back sufficiently, because the etch duration did not account for etching through a thermal oxide that grew on the cells

during gridline firing. These cells do not show consistent improvement over the controls. The second three groups used a longer 150-second RIE-etch that removed the thermal oxide and then etched the emitters from their starting sheet resistance of 50 Ω/sq. to 100 Ω/sq. The 1-step cells show a drop in performance compared to the controls, in agreement with our J_{oe} results that showed poorer passivation by a 1-step nitride. Once the emitter is etched back to 100 Ω/sq., it requires excellent surface passivation to avoid excess surface recombination.

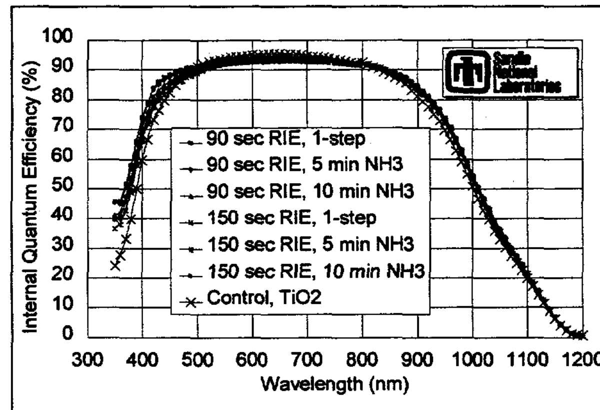

FIGURE 3. IQE for cells described in Table 1.

The 3-step cells show significant improvements, especially in V_{OC}, suggesting longer diffusion lengths from bulk defect passivation. Internal quantum efficiency (IQE) of these cells, showing both improved red and blue response is shown in Fig. 3.

All the nitride passivated cells show similar red and blue response, consistent with their similar J_{SC} values. The J_{SC} is no greater than that of the control cell because the increase in IQE is compensated by parasitic absorbtion in the nitride, which is due to the high refractive index of 2.2 used to minimize reflectance. Another series of SASE cells were processed using a lower refractive index of 2.12 to reduce the spectral-weighted absorbtance to 0.5%. Normalized IV data for the cells are shown in Table 2.

TABLE 2. Three SASE sequences were applied to seven Solarex mc-Si cells using matched material from the same ingot as before. IV data are shown below normalized to the transmittance of the control cells.

Eff. (%)	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (%)
140 sec RIE, **3-step** SiN, **5 min NH$_3$**, FGA			
12.9±0.2	31.1±.0.1	572±3	72.7±0.3
140 sec RIE, **3-step** SiN, **10 min NH$_3$**, FGA			
13.1±0.0	31.4±.0.1	574±0	73.0±0.1
140 sec RIE, **3-step** SiN, **20 min NH$_3$**, FGA			
12.2±0.4	31.2±.0.1	563±5	69.5±1.5
Control Cells: No emitter etchback, TiO_2 ARC			
12.3±0.1	30.8±.0.0	558±2	71.4±0.4

The SASE cells have consistently higher J_{SC} than the controls, because now the increased IQE due to passivation is not lost due to excessive parasitic absorbtion. The cells that received 10 minutes of NH_3-hydrogenation performed the best, exceeding the controls by almost a full percentage point due to the large improvement in V_{OC}.

However, improvement in V_{OC} is reduced for the cells that received a 20-minute NH_3-exposure. These cells also suffered a loss in fill factor due to an increase in diode ideality factor.

RIE-textured Cells

We developed an RIE process that uses SF_6/O_2 mixtures to produce a randomly textured surface on c-Si. Figure 4 shows an SEM of an RIE-textured sample with less than 0.5% specular reflectance at all wavelengths.

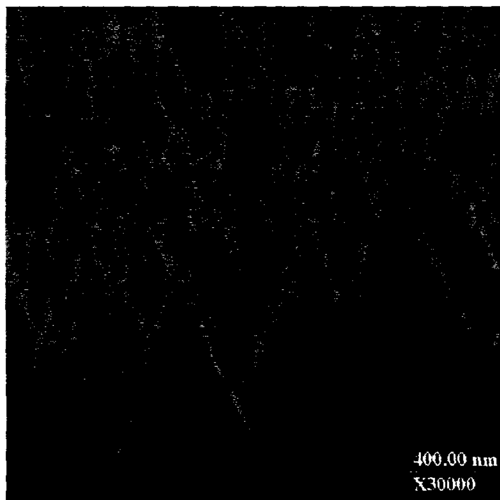

FIGURE 4. SEM of Si surface textured for 30 minutes.

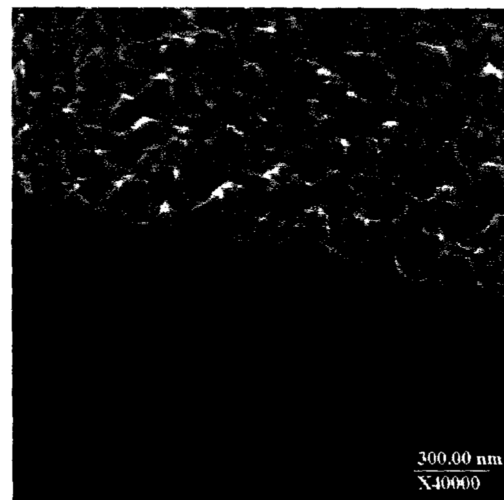

FIGURE 5: Textured Si surface with 0.1 μm feature sizes.

About 6.0 μm of Si was removed from the surface shown in Fig. 4. This process could be applied to the wafers before emitter diffusion, when removal of a few micrometers of Si would not be an issue. The SASE process could then be applied after gridline firing as usual.

We developed a second process that could be applied after emitter diffusion since it removes only 0.1 μm from the surface, increasing the emitter sheet resistance to about 60 Ω/sq. This process requires the Si surface to be prepared in a simple manner using low-cost, low-temperature techniques. An SEM of such a textured surface prepared in this manner near a cleaved wafer edge is shown in Figure 5.

This second process was applied to single-crystal wafers with three different surface preparation conditions. Specular reflectance curves of the three resulting textures are compared to that of bare Si in Fig. 6. We applied this second process to full-size mc-Si wafers with gridlines using preparation conditions 1 and 2. These cells are currently in process at Solarex and could provide an increase of up to a full percentage point in efficiency due to reflectance reduction alone.

CONCLUSIONS

The SASE process has been improved using statistical experiments, more complete emitter etchback, and lower absorbtance nitride films to achieve nearly a full

percentage point efficiency increase over the standard production line process. The use of an optimum-duration, ammonia-plasma hydrogenation treatment is crucial to the increased performance. In addition, plasma texturing has been shown to reduce reflectance significantly while removing only the heavily diffused portion of the emitter region. As a result, texturing could be included as part of the emitter etchback process.

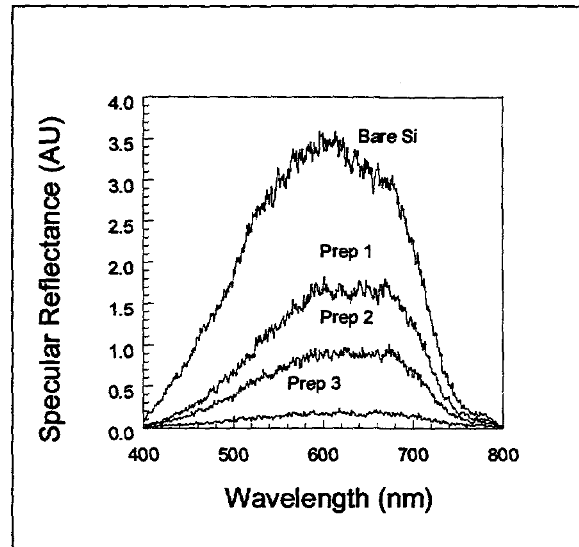

FIGURE 6: Specular reflectance of samples with three different surface preparation conditions that were textured using the second process shown in Figure 5. The reflectance of the textured samples has been reduced by a factor of 2.2, 4.4, and 24, respectively.

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