FERMILAB-SLIDES-25-0198-CMS

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Aug 28, 2025

Precision timing in CMS at the HL-LHC

Current progress on validation and production

Murtaza Safdari

Vertex 2025: 33rd International Workshop on Vertex Detectors

Link to Indico

U.S. DEPARTMENT of ENERGY — Fermi National Accelerator Laboratory is managed by FermiForward for the U.S. Department of Energy Office of Science

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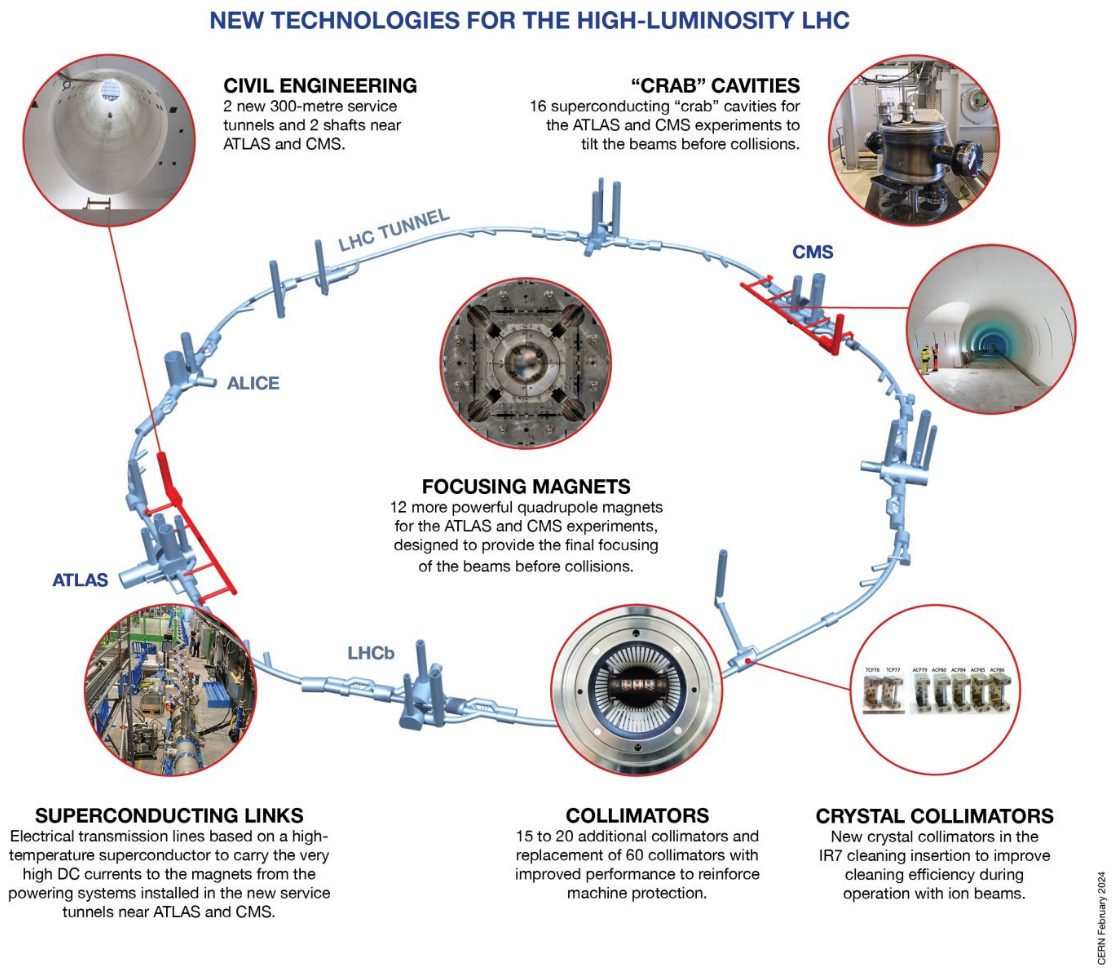
The Need for Precision Timing at the HL-LHC

How do we handle up to 200 interactions per bunch crossing?



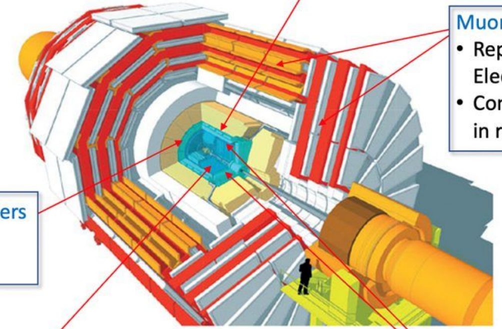
Source

Trigger/HLT/DAQ
- Track information in L1-Trigger
- L1-Trigger: 12.5 μs latency – output 750 kHz
- HLT output 7.5 kHz

Barrel ECAL/HCAL
- Replace FE/BE electronics
- Lower ECAL operating temp. (8 °C)

Muon Systems
- Replace DT & CSC FE/BE Electronics
- Complete Muon coverage in region $1.5<\eta<2.4$

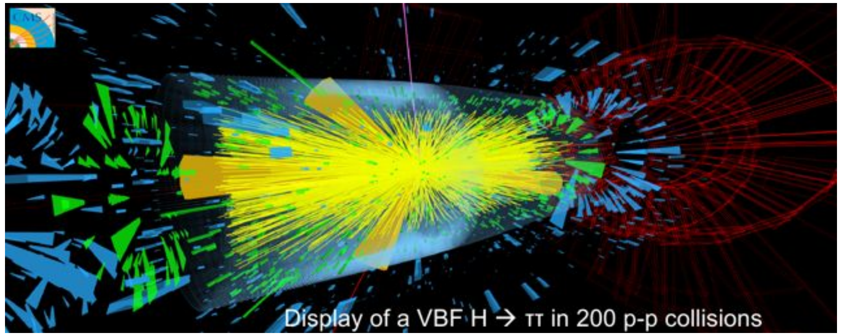
New Endcap Calorimeters
- High granularity
- 3D capable



New Tracker
- Rad. tolerant – high granularity – significant less material
- 40 MHz selective readout (p_T>2 GeV) in Outer Tracker for L1 -Trigger
- Extended coverage to $\eta=4$

New Precision Timing Detector
- Barrel: Crystal +SiPM
- Endcap: Low Gain Avalanche Diodes

Source



Display of a VBF H → ττ in 200 p-p collisions

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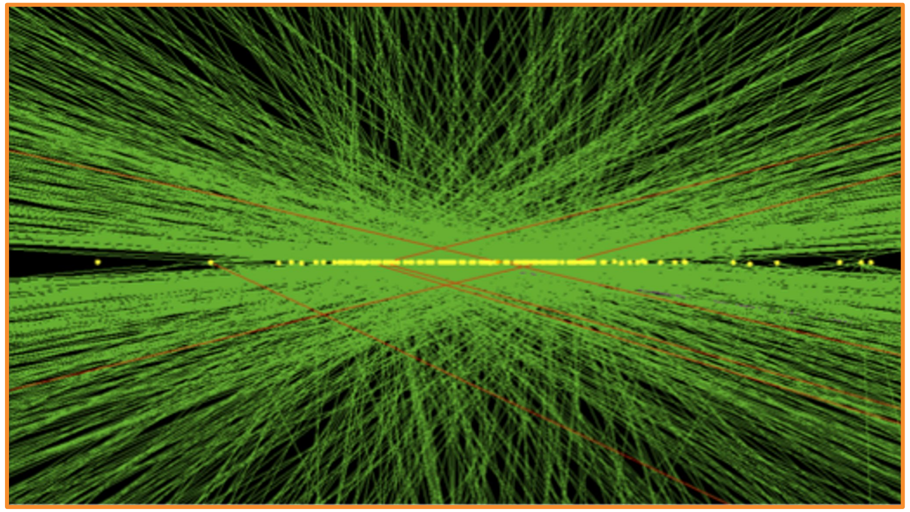
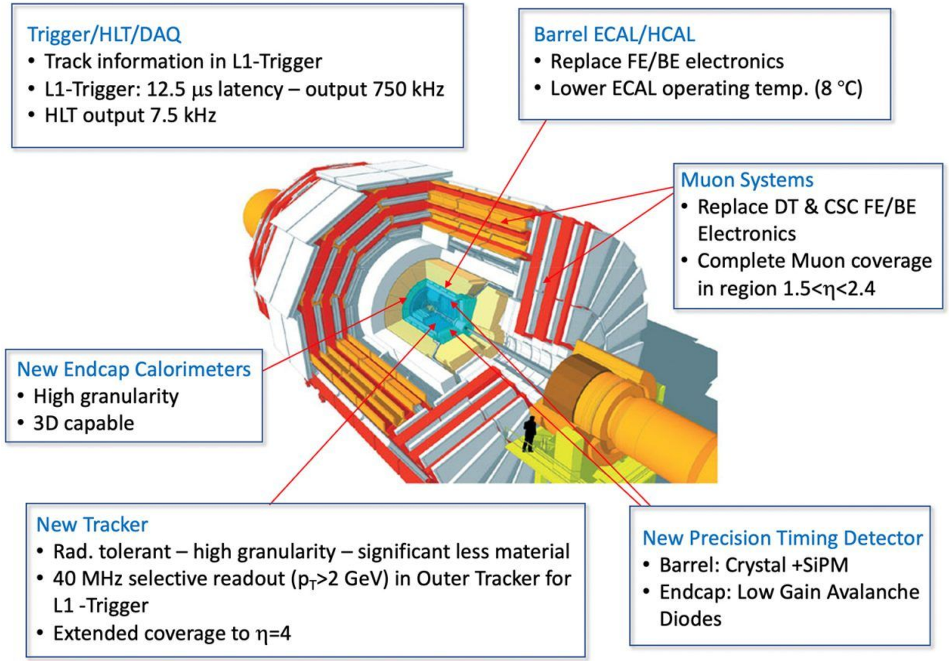


High Luminosity LHC comes with 5x more PU interactions per bunch crossing

Overlapping vertices in space will present limitations for PU track identification



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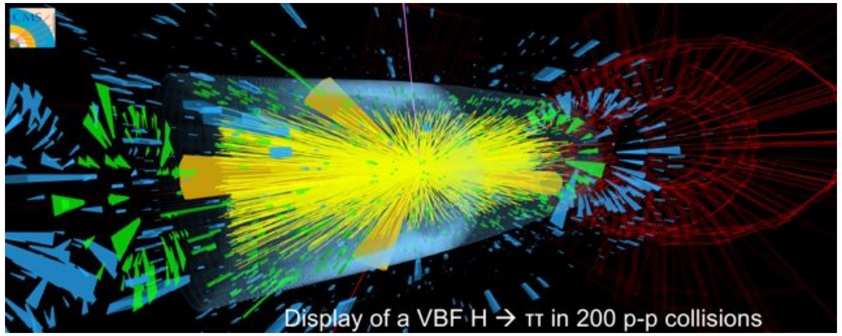

Display of a VBF H → ττ in 200 p-p collisions

Source

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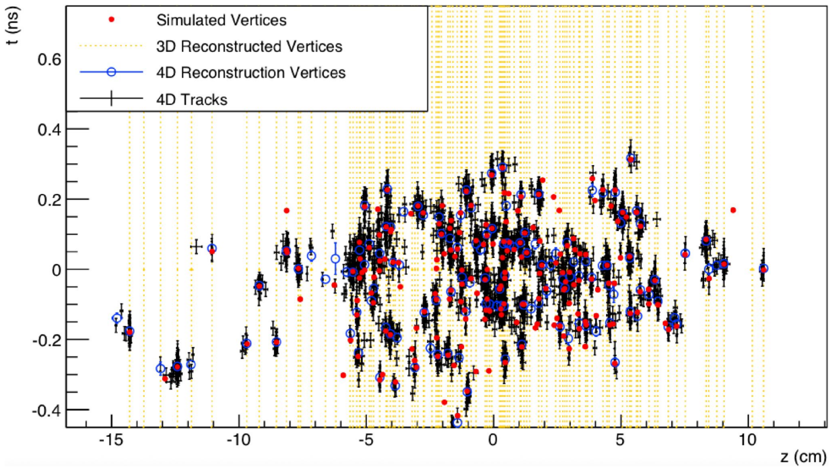
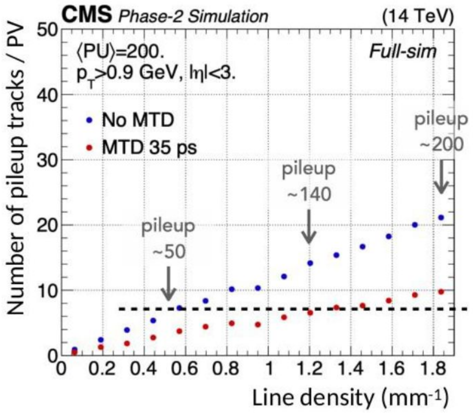
CMS Minimum Ionizing Particle Timing Detector

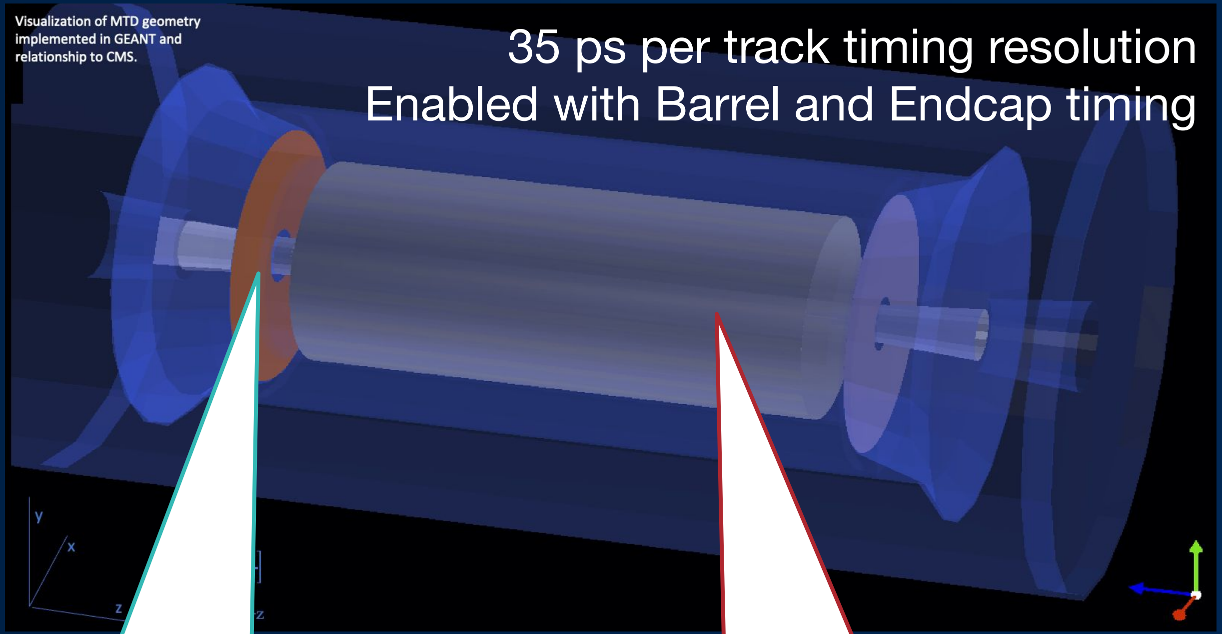
First generation timing detector being deployed at the HL-LHC





The MTD will exploit timing information to reduce pile-up to current LHC level in both the forward and barrel regions.

[CMS-TDR-020](CMS-TDR-020)



Endcap Timing Layer (ETL)

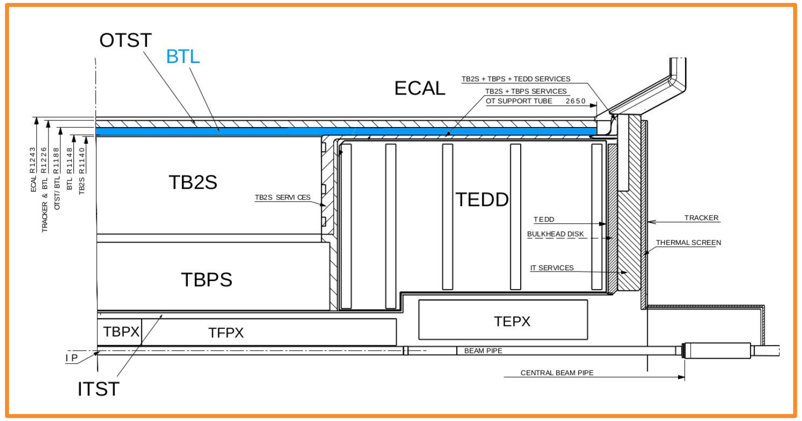
Si with internal gain (LGAD):
- On the CE nose: 1.6 < |η|<3.0
- Radius: 315 < R < 1200 mm
- Position: z = ±3.0 m
- 1.3x1.3 mm^2 pixels
- Area **14 m^2**: 8.5M channels
- Fluence: max **2E15 n_{eq}/cm^2**

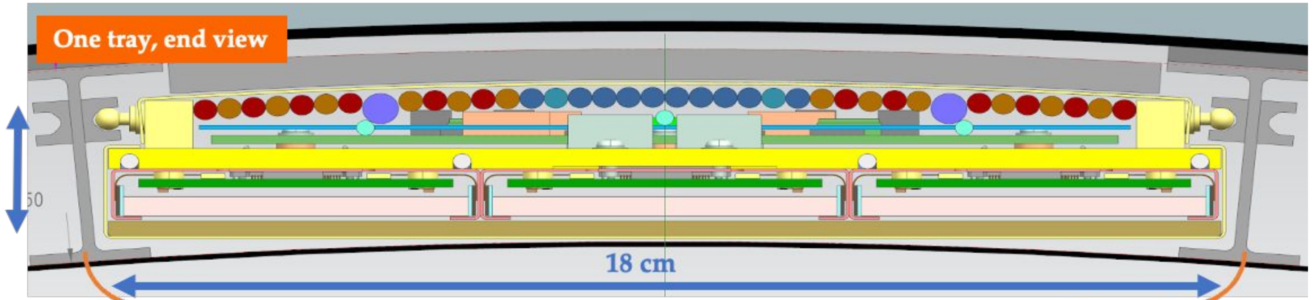
Barrel Timing Layer (BTL)

LYSO:Ce bars + SiPM readout:
- TK/ECAL interface: |η| < 1.45
- Inner radius: 1148 mm
- Thickness: 40 mm
- Length: ±2.6 m along z
- Area **38 m^2**: 332k channels
- Fluence: max **2E14 n_{eq}/cm^2**

CMS Barrel Timing Layer

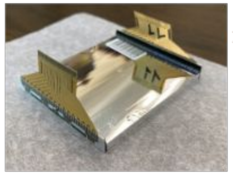
Inner R: 1148 mm, Depth: 40 mm, L: ±2.6 m along z, $|\eta|<1.45$, 38 m^2: ~332k channels





72 trays covering the surface
- total of 10 368 SMs
- total of 331 776 channels

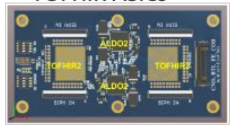
LYSO+SiPM
Sensor Modules

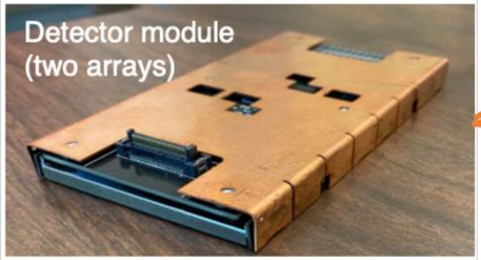


x2

+

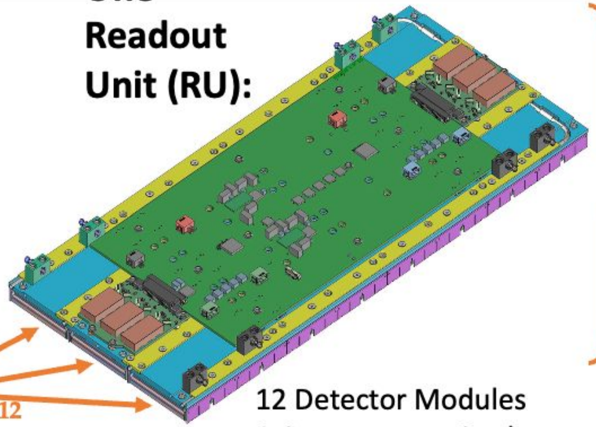
FE Boards housing
TOFHIR ASICs





x12

One Readout Unit (RU):



x6

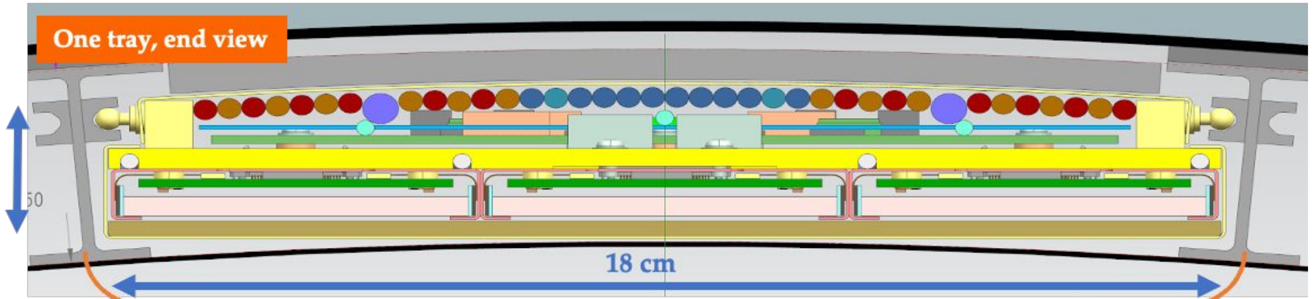
12 Detector Modules
1 Concentrator Card
2 Power Converter Cards

CMS Barrel Timing Layer

Inner R: 1148 mm, Depth: 40 mm, L: ±2.6 m along z, $|\eta|<1.45$, 38 m^2: ~332k channels

ToA for > 0.7 GeV MIPs with **~30 - 60 ps precision**
Thin, large area detector covering central region
Needs to survive **~2x10^{14} n_{eq}/cm^2 irradiation** dose

~10k BTL Modules, each w/ 16 scintillating **LYSO:Ce** bars and two 16-channel SiPM photodetector arrays
Read out with custom **TOFHIR2 ASIC**
Mounted on CO_2 cooled trays and installed on inner surface of BTL Tracker Support Tube



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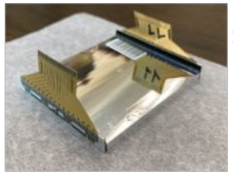
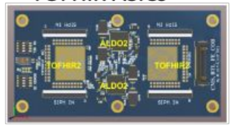
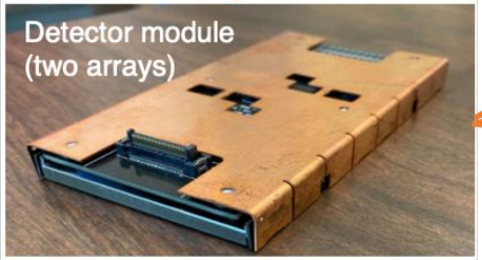


x2 +

FE Boards housing TOFHIR ASICs





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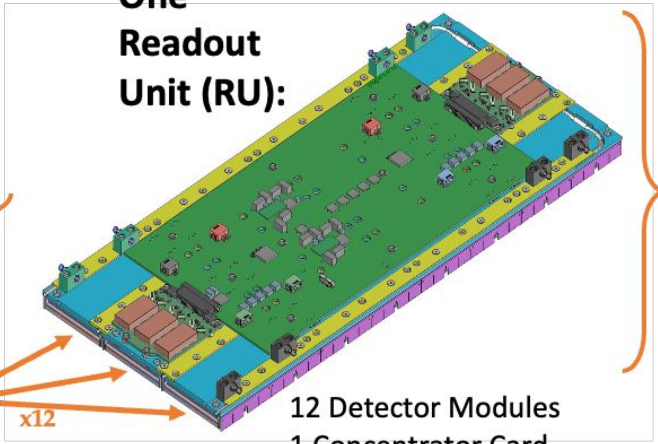

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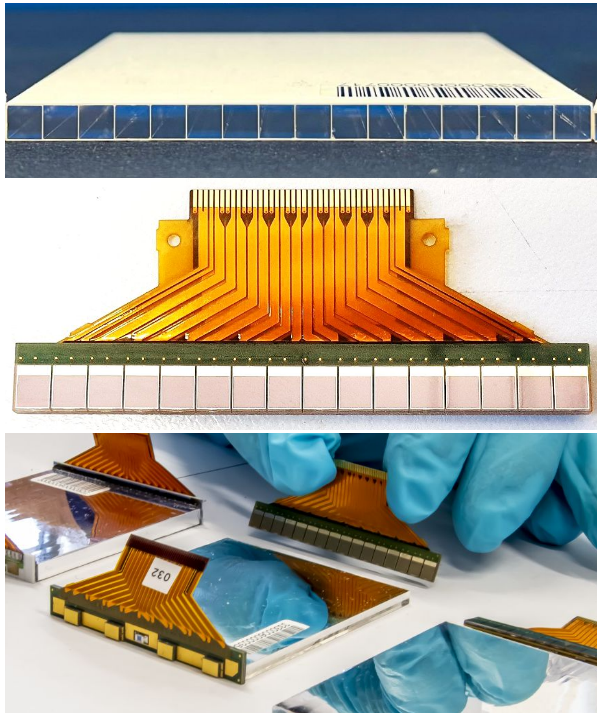
CMS Barrel Timing Layer

Sensor and ASIC

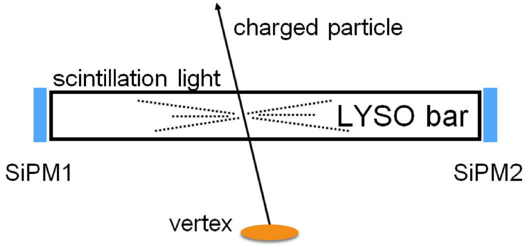


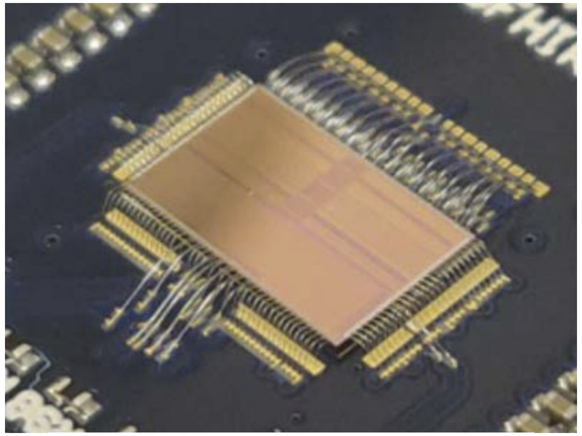
(Lutetium-Yttrium Oxyorthosilicate doped with Cerium) LYSO:Ce crystals as scintillator

- Excellent radiation tolerance
- Bright (40k ph/MeV)
- Fast rise time O(100ps), decay time ~40 ns

Silicon Photomultipliers as photo-sensors

- Compact, insensitive to B fields, fast
- High dynamic range, rad tolerant, good photo detection efficiency

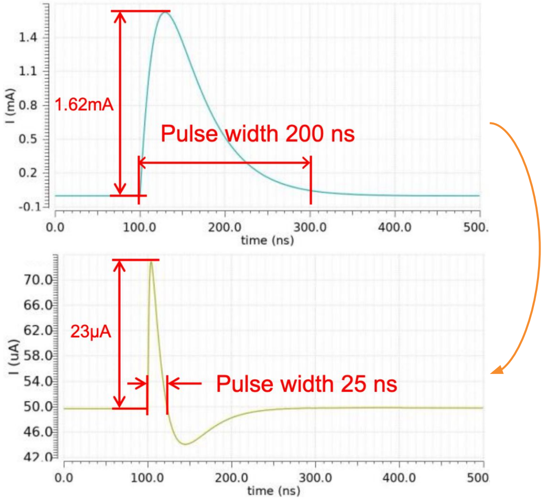




Dedicated readout **TOFHIR2** ASIC, builds upon TOFPET ASIC with significant redesign for HEP in 130nm CMOS withstanding 3 MRad

Key feature is a noise suppression filter

- Inverted and delayed pulse subtraction (**Differential Leading Edge Discriminator**)
- Restores baseline at the rising edge.
- Improves time resolution by about a factor 3 at end of life of the detector.

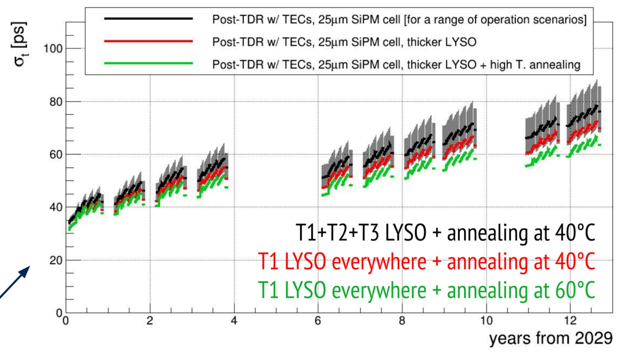


CMS Barrel Timing Layer

Optimize signal amplitude, rise time, dark count rate for timing performance

$$\sigma_t = \sigma_t^{ele} \oplus \sigma_t^{phot} \oplus \sigma_t^{DCR} \oplus \sigma_t^{clock}$$

Electronic Noise term goes as rise-time/SNR
Photostatistics term goes as 1/root(amplitude)
Dark Count Rate term goes as root(DCR)/amplitude



LYSO:Ce bar geometry minimizes SiPM area wrt crystal volume: 3.12 × **3.75** × 54.7 mm^3

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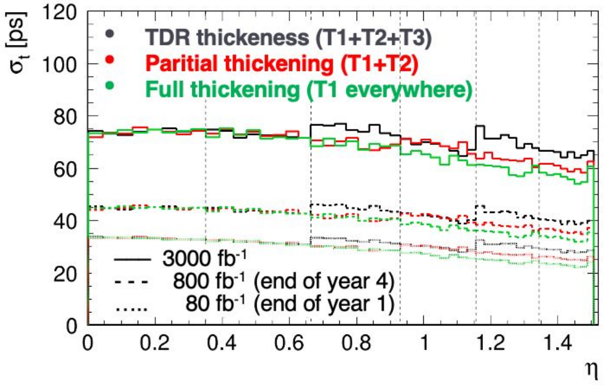

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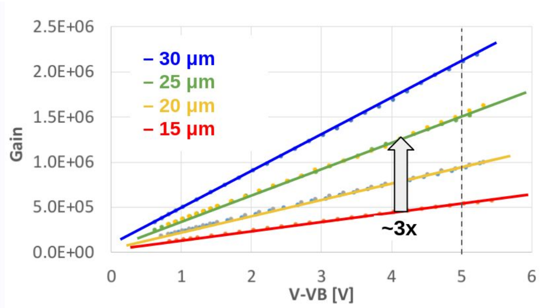

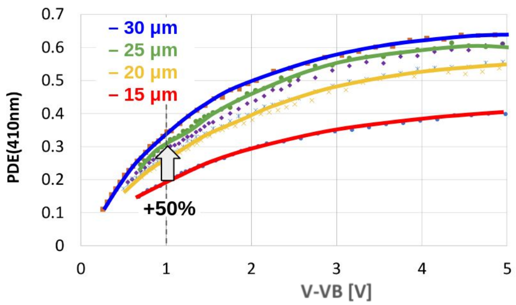

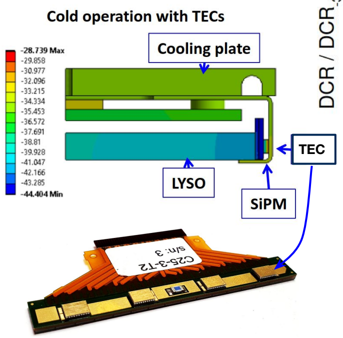

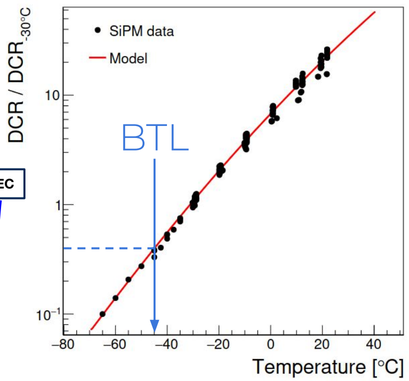

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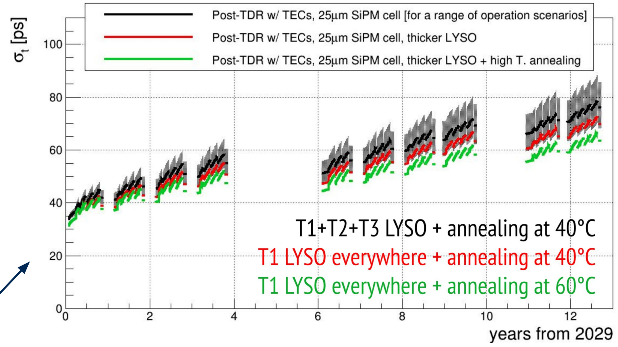
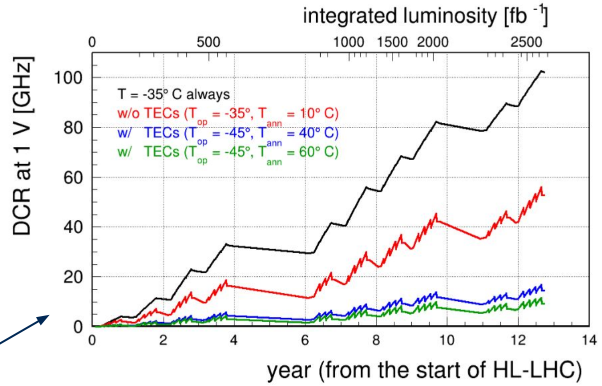
SiPM gain, photodetection efficiency, and speed increased by using **25 µm cell size**

- **Operate at -45 C** (dual-phase CO_2 + Thermoelectric Cooling) to minimize DCR
- High temp **annealing at 60 C** to heal radiation damage over 3 ab^{-1}





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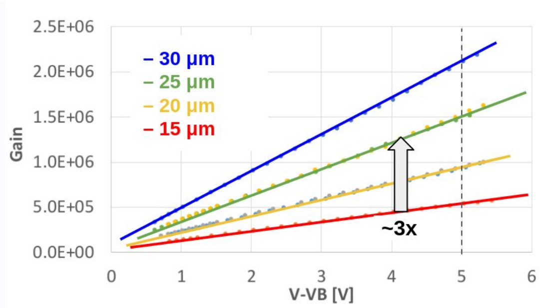

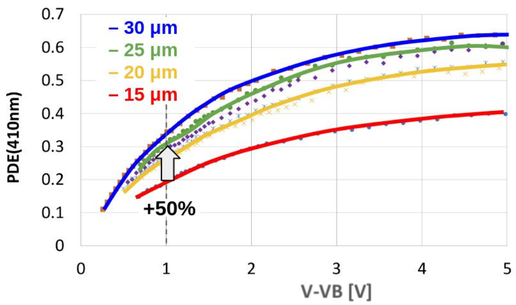

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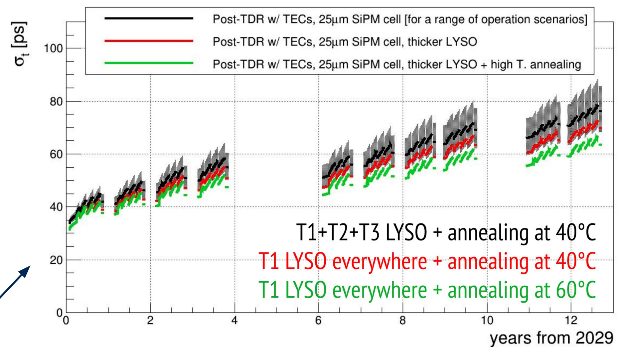

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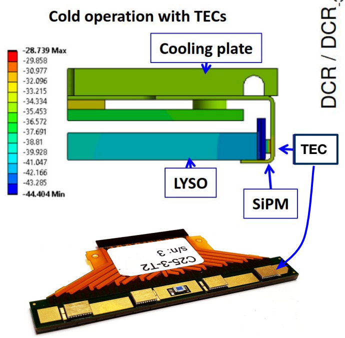
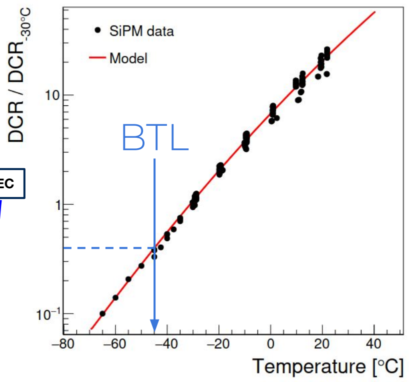
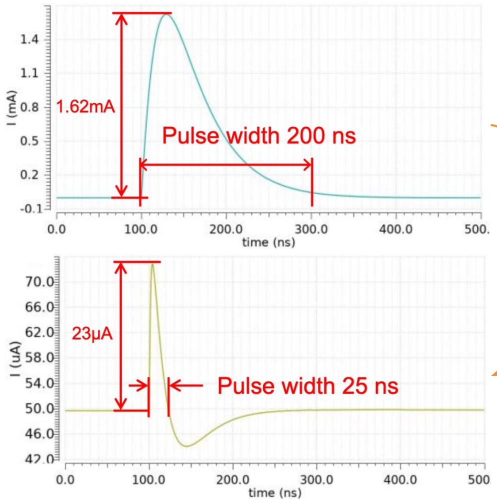




TOFHIR2 Differential Leading Edge Discriminator designed to reduce DCR from SiPM
Increased preamp gain minimizes electronics noise



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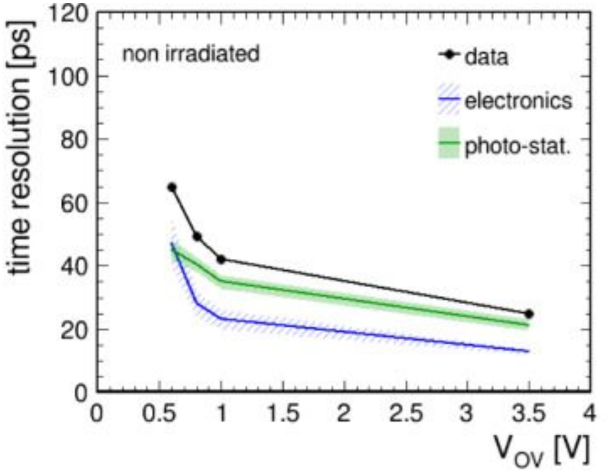
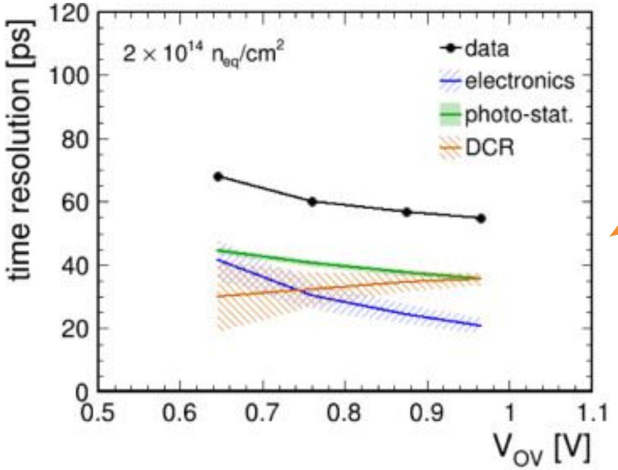
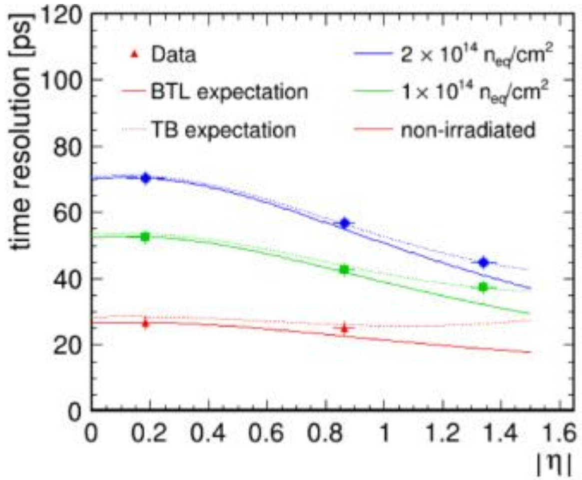
CMS Barrel Timing Layer

Beam Test Validation

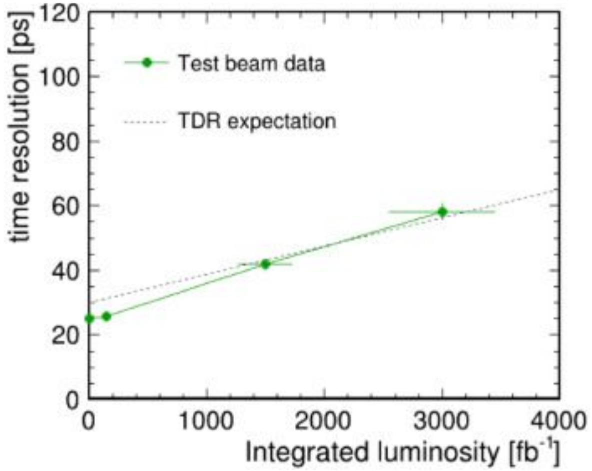




- Test beams with modules before and after irradiation help validate the optimizations to LYSO:Ce, SiPM, and TOPHIR2
- DCR component becomes a significant factor after irritation at end of life levels



- Scans with modules irradiated to different levels to simulate various stages of BTL aging during HL-LHC operations upto 3 ab^{-1}
- **Confirms operational requirement of BTL timing resolution 30-60 ps over the lifetime of the detector**



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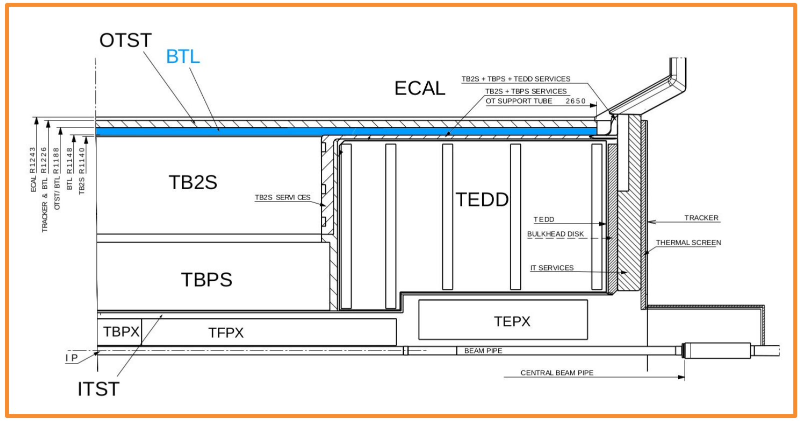

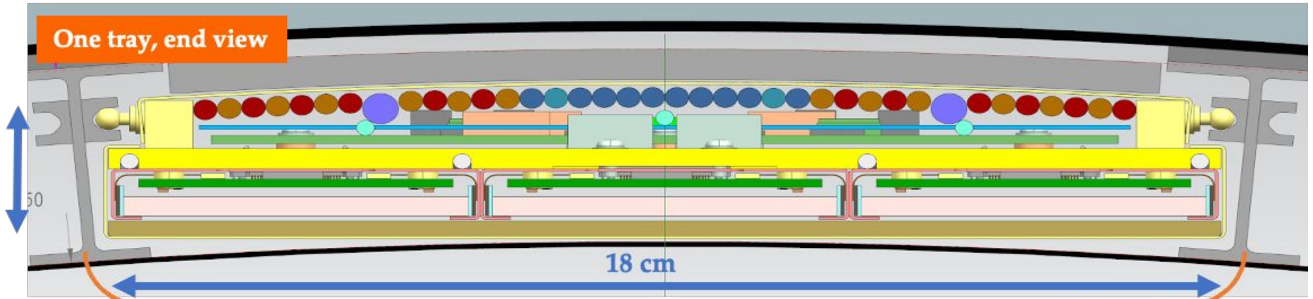

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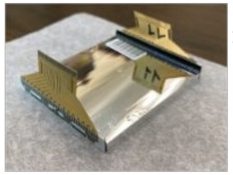
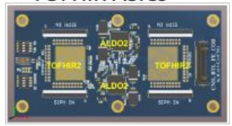
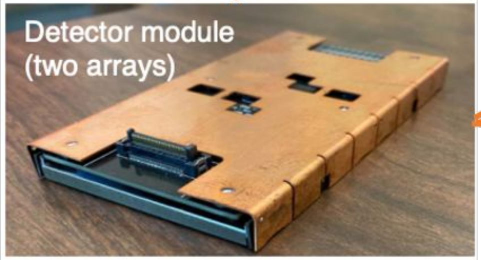
LYSO+SiPM Sensor Modules



x2 +

FE Boards housing TOFHIR ASICs





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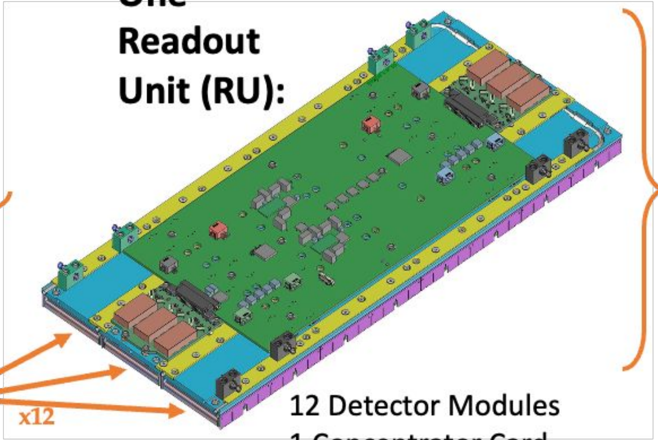
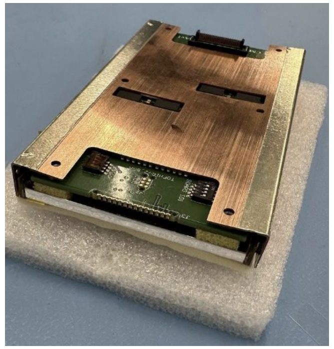


x6

12 Detector Modules
1 Concentrator Card
2 Power Converter Cards

CMS Barrel Timing Layer

Production Underway!



Module and Tray production underway at BTL Assembly Centers in **Caltech, U. Virginia, Milano-Bicocca, Peking U**.

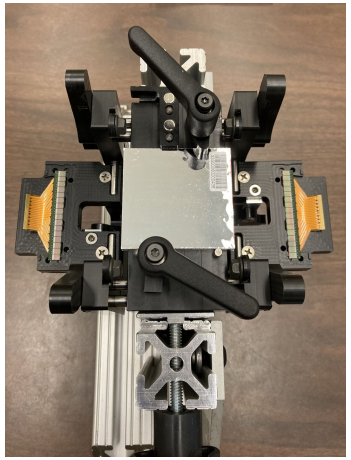
Production kicked off with first tray in March. Targeting 2 Trays / Month / Center assembled & shipped to CERN

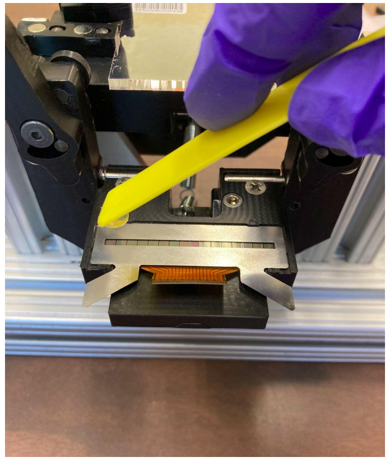
100% of crystals and SiPMs qualified.
80% sensor mod. + 50% of detector mod.
10% of trays assembled and tested.

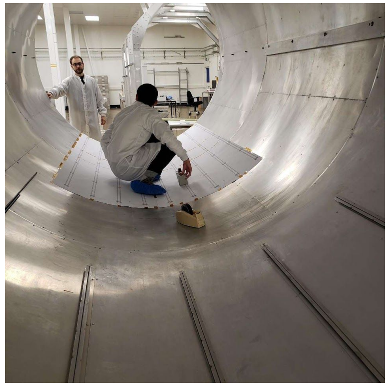
Tray production completion - February 2026

Tray integration in **BTL Tracker Integration Facility at CERN**, with installation in **BTL Tracker Support Tube**, second half of 2025

Commissioning in CMS starting in 2027







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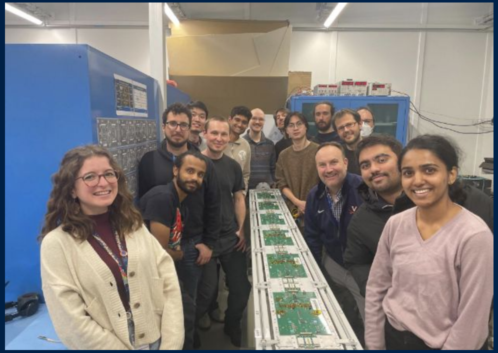
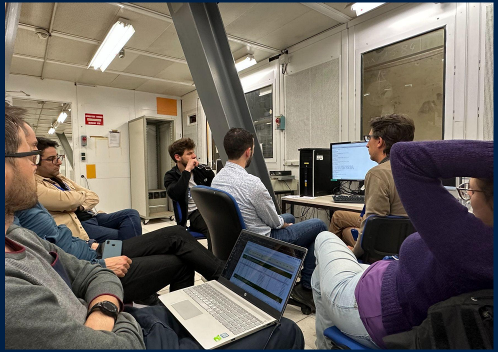
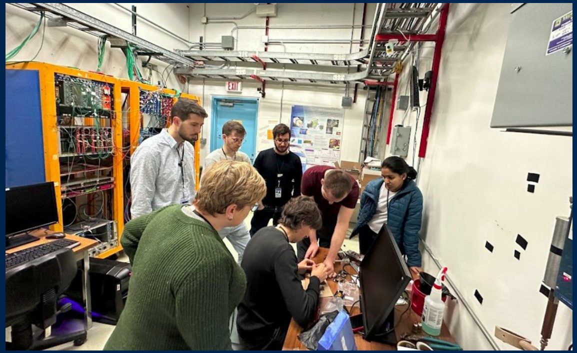
Production Underway!

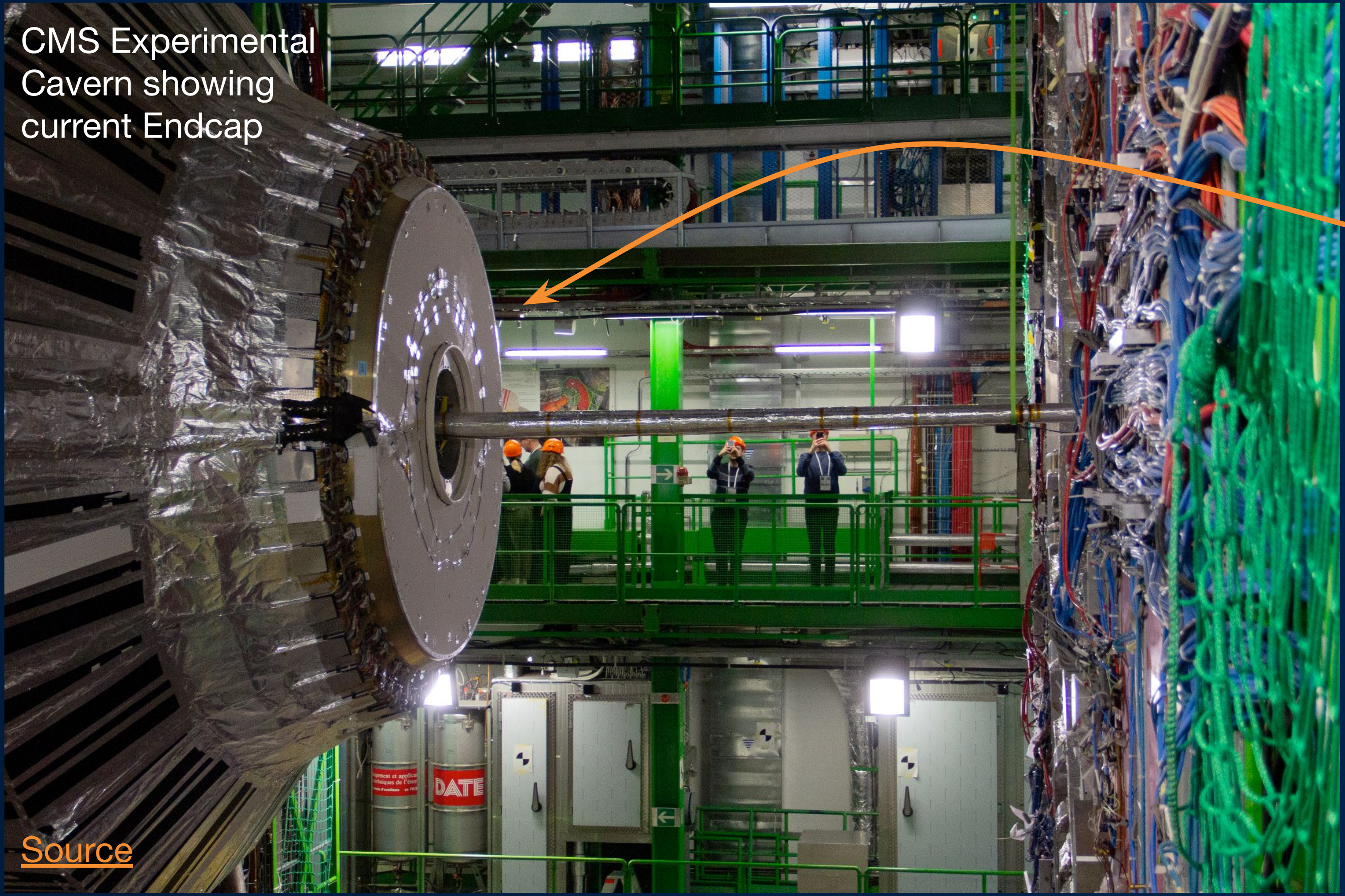


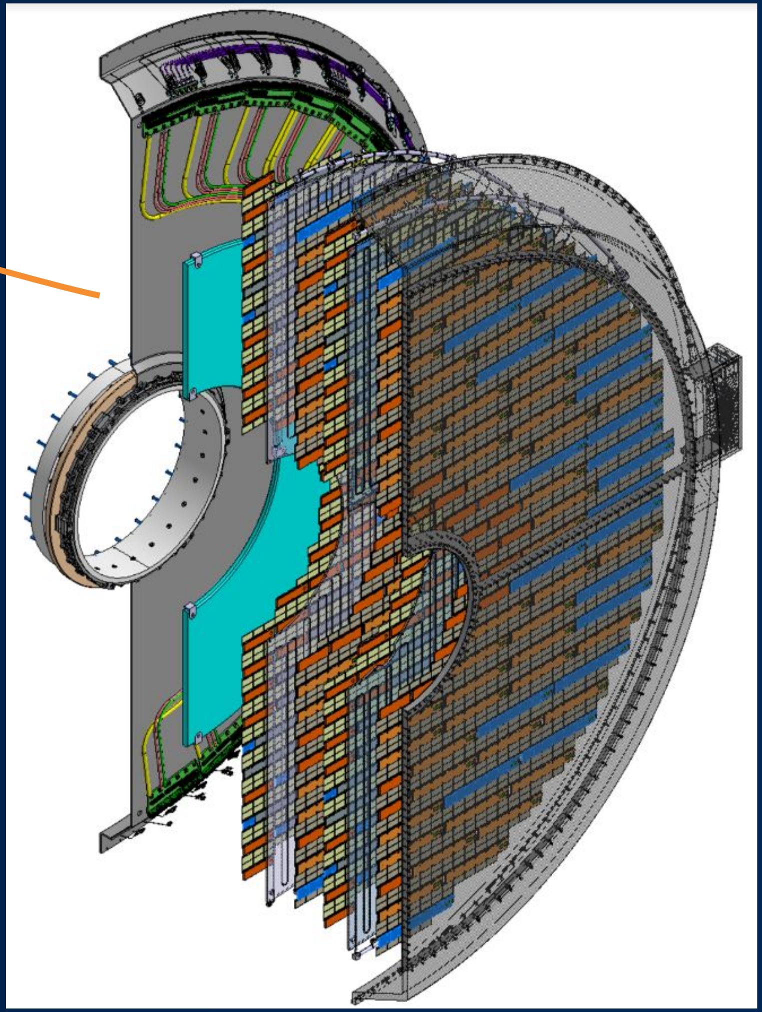




CMS Endcap Timing Layer

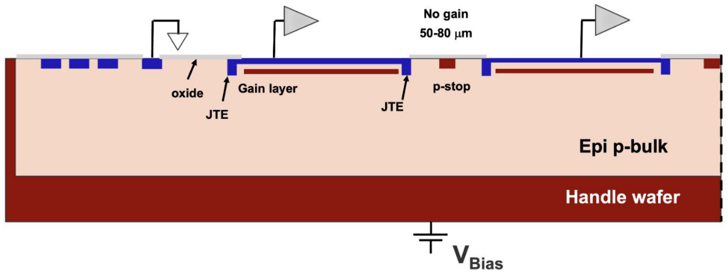
315 < R < 1200 mm, z = ±3.0 m, $1.6 < |\eta| < 3.0$, 1.3mm pixels, 14 m^2: 8.5M channels

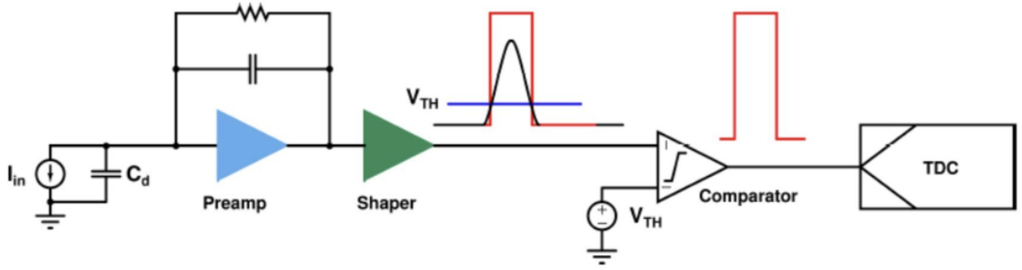




Fundamentals of a Timing Detector

Hybrid Pixel Model - Basics of Time Resolution

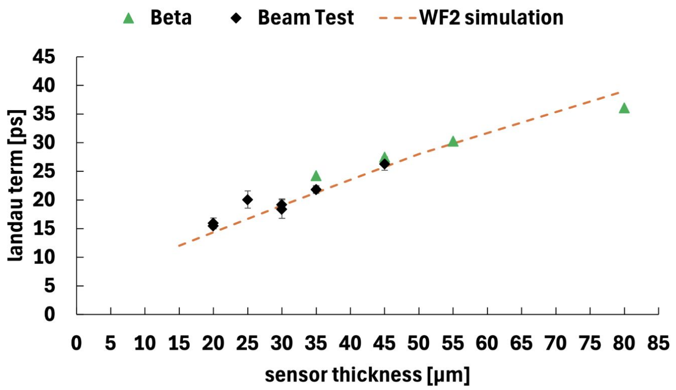


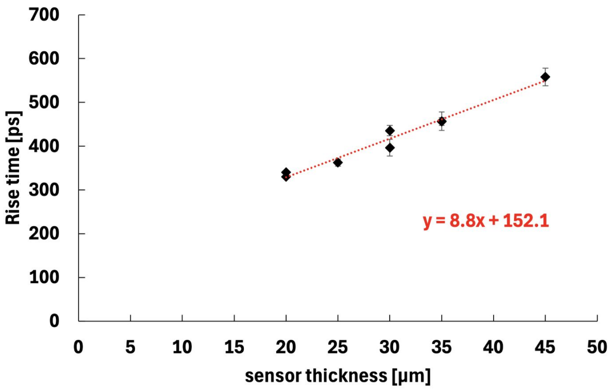


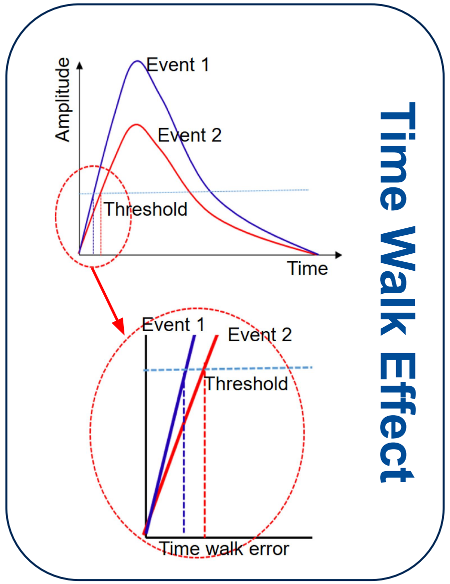
$$\sigma_t^2 = \sigma_{Landau}^2 + \sigma_{timewalk}^2 + \sigma_{jitter}^2 + \sigma_{TDC}^2 + \sigma_{clock}^2$$

$$\frac{t_{rise}}{S / N}$$

V Sola at FAST2025

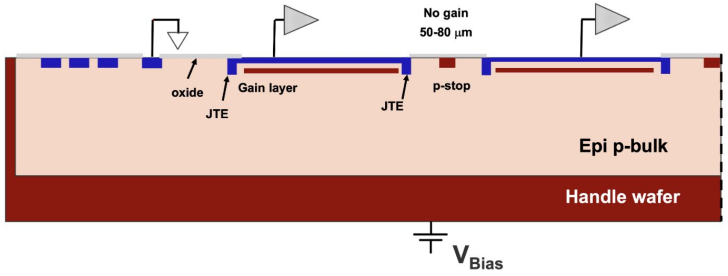






Fundamentals of a Timing Detector

Hybrid Pixel Model - Basics of Time Resolution



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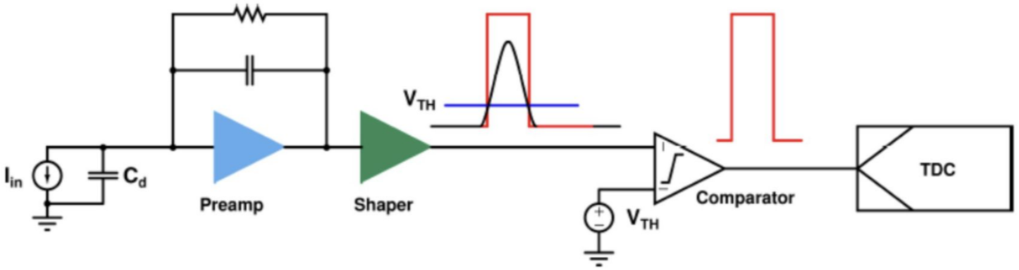
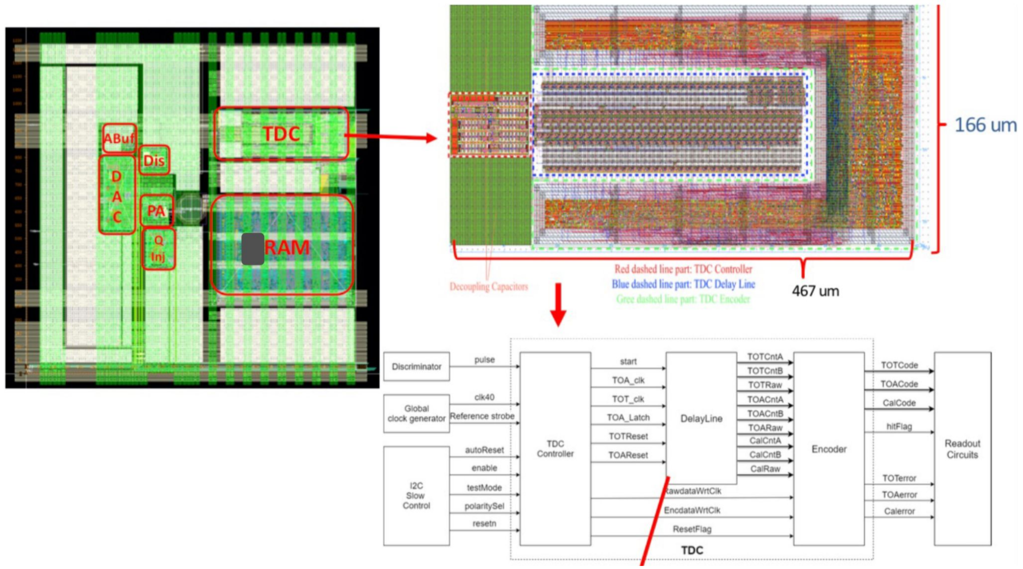
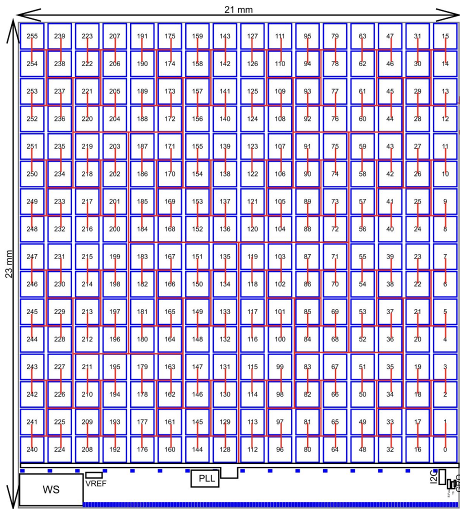
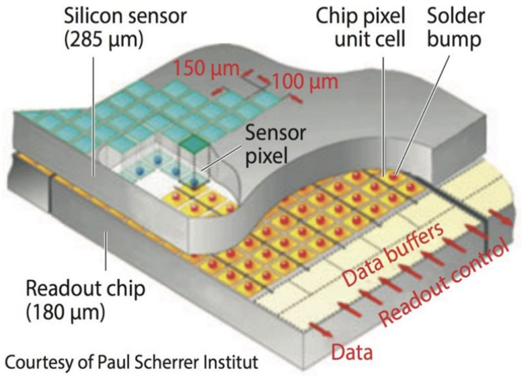


$$\sigma_t^2 = \sigma_{Landau}^2 + \sigma_{timewalk}^2 + \sigma_{jitter}^2 + \sigma_{TDC}^2 + \sigma_{clock}^2$$







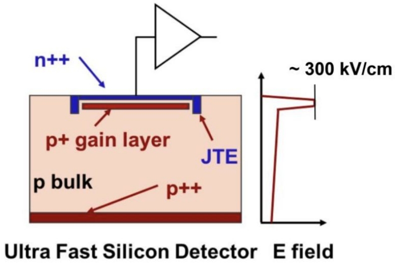
Courtesy of Paul Scherrer Institut

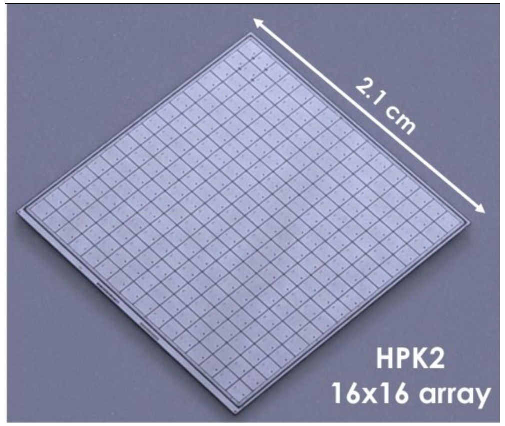
CMS Endcap Timing Layer

Low Gain Avalanche Detectors

Need to withstand 2 x 10^{15} n_{eq}/cm^2 in the innermost region over 3 ab^{-1}, still deliver 8-10 fC for readout at the end of life

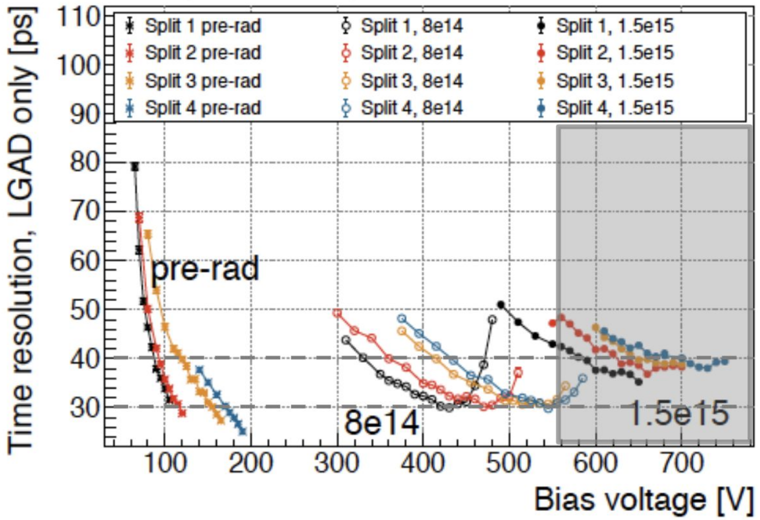
< 30-50 ps contribution from the sensor, limits active depth to 50um with a gain of 10-30 and pad size ~ mm^2 to minimize pad capacitance



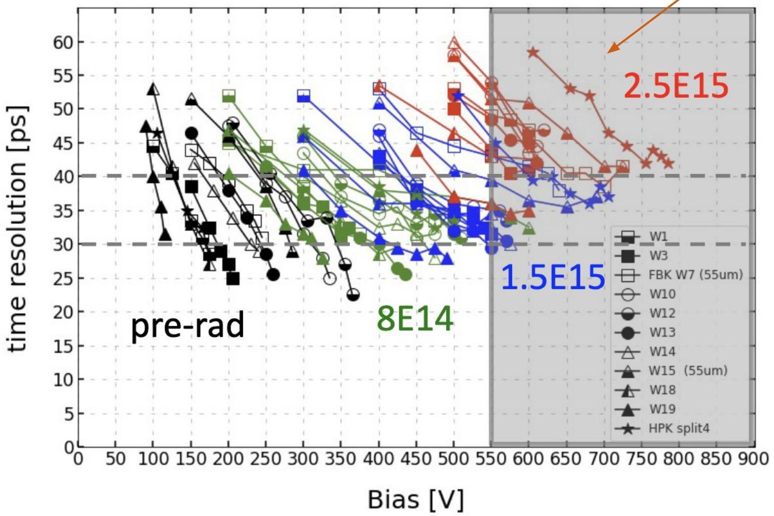


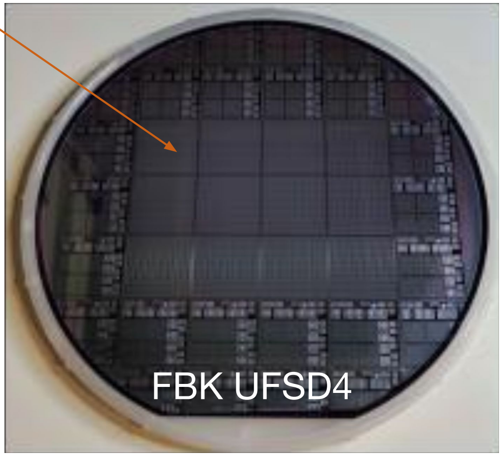
Carbon Co-implants in Gain Volume

HPK2 – Beta source



FBK UFSD3.2 – Beta source



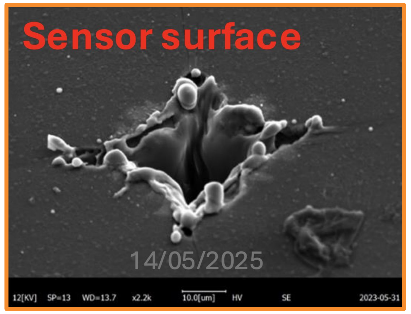


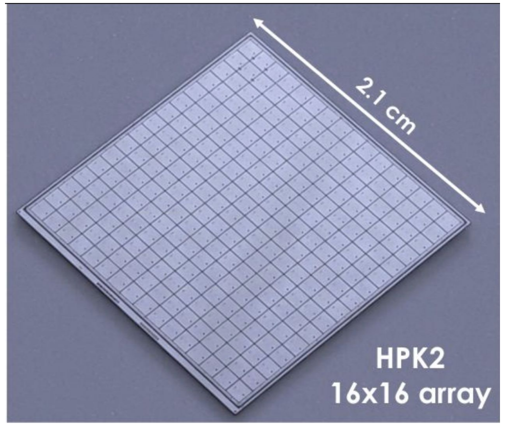
CMS Endcap Timing Layer

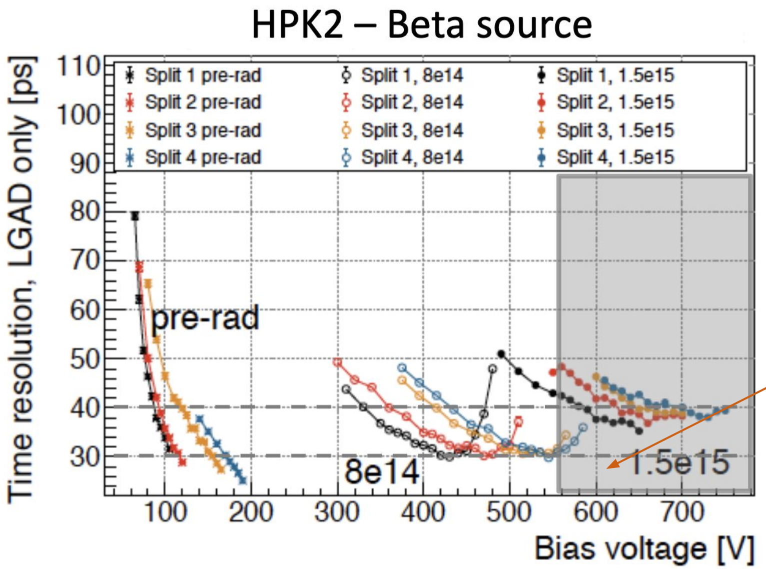
Low Gain Avalanche Detectors

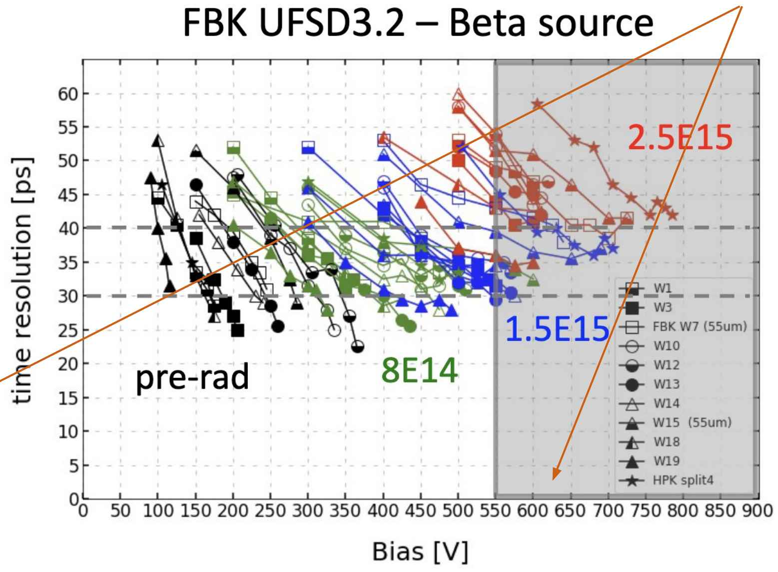
Need to withstand 2 x 10^{15} n_{eq}/cm^2 in the innermost region over 3 ab^{-1}, still deliver 8-10 fC for readout at the end of life

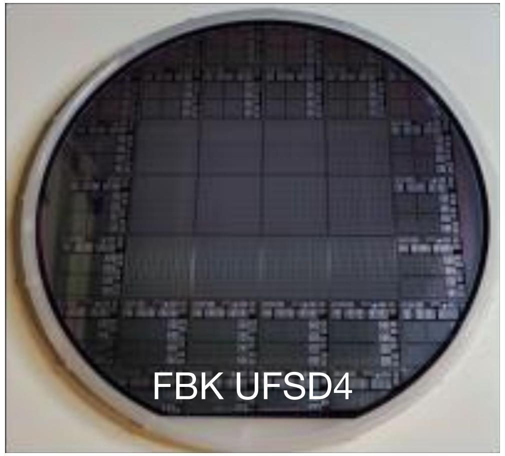
< 30-50 ps contribution from the sensor, limits active depth to 50um with a gain of 10-30 and pad size ~ mm^2 to minimize pad capacitance





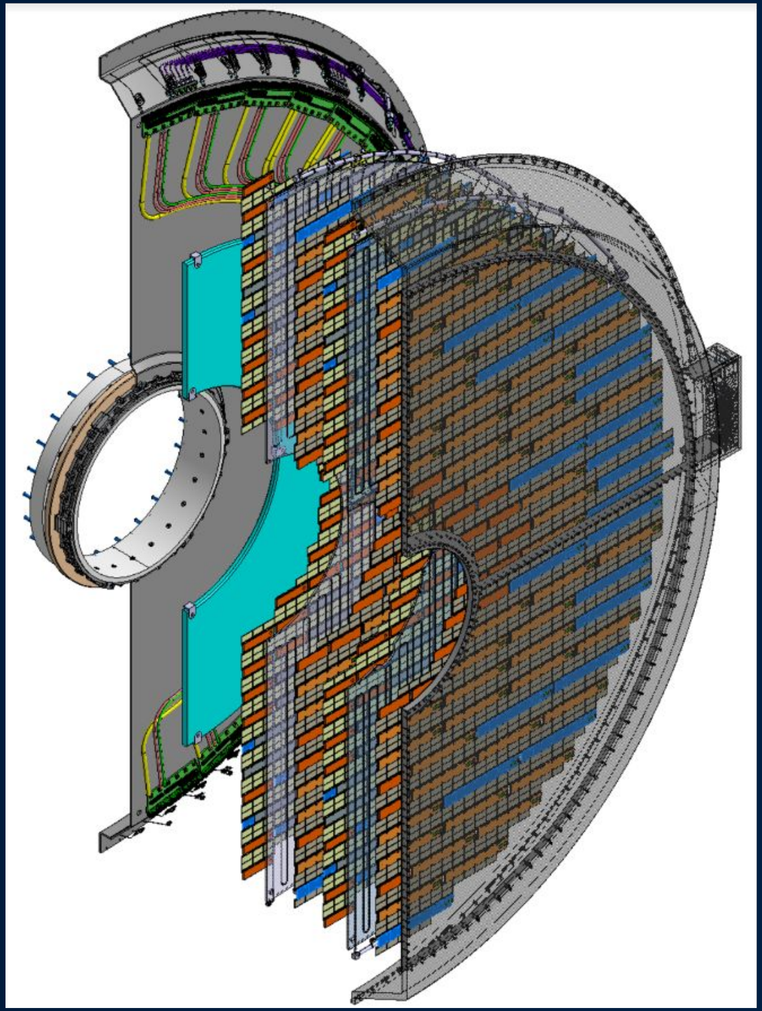


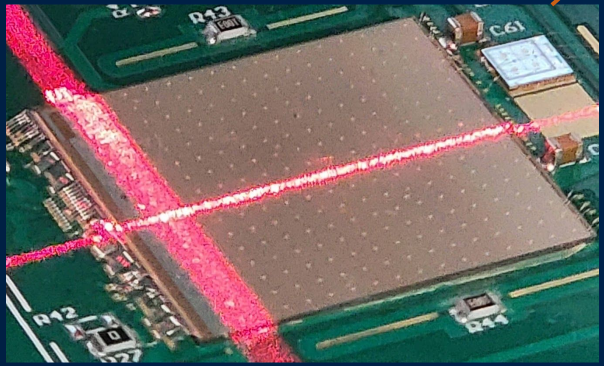




CMS Endcap Timing Layer

~33k chips, 2.3 x 2.1 cm chips, 1.3 mm pixels, 16x16 px





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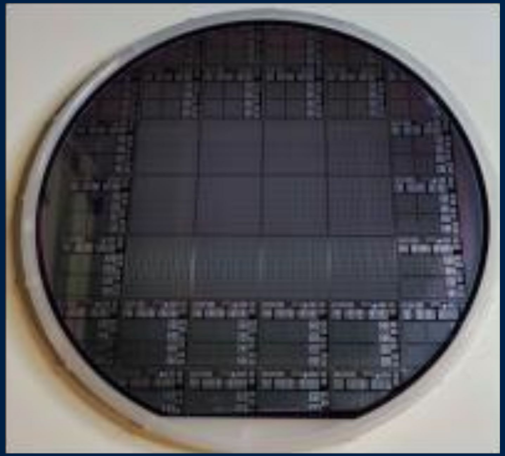
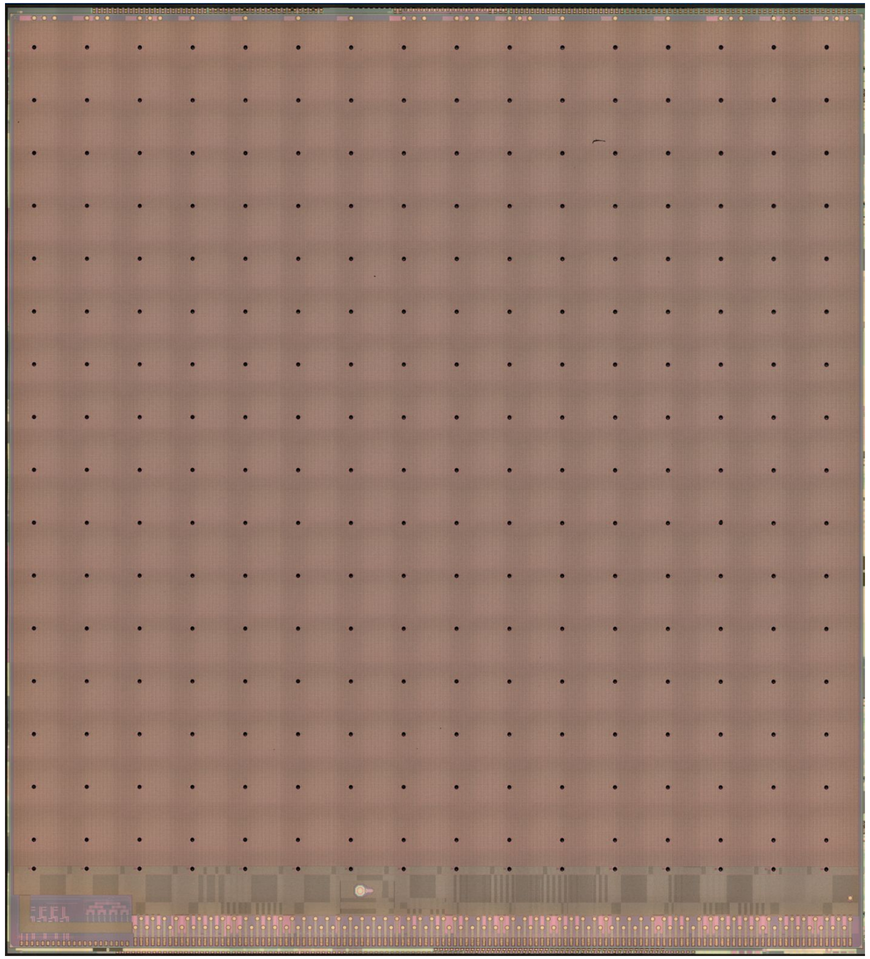


ETL Read Out Chip (ETROC)



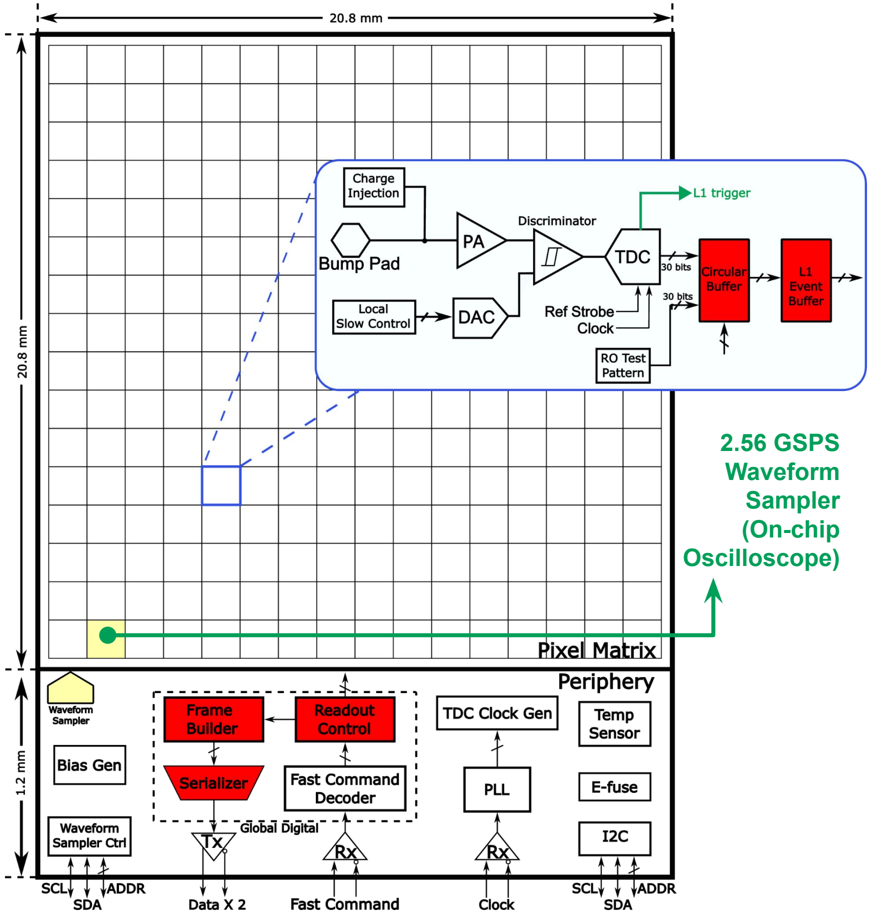
CMS Endcap Timing Layer

2 hits per track, 50 ps res. per hit, 35 ps res. per track

What are the main constraints on this design?

1. Low Noise
   - This is crucial! 30 ps intrinsic (Landau) resolution from LGADs also **limits ASIC contribution < 40 ps**
2. Low Power
   - Thou shall not fry your detector! Cooling capacity limits power consumption to **< 1W per chip, 4 mW per pixel, 240 mW/cm^2**
3. Radiation Hardness
   - Must withstand 100 MRad over the 3 ab^{-1} of HL-LHC
4. Sensitive to small LGAD signals
   - Around 10 fC per MIP towards end of lifetime of LGADs in ETL
5. Synchronized precision timing over ~33k chips, ~8.5M channels...

ETL Read Out Chip (ETROC)



CMS ETL - ETROC2 + LGAD Validation

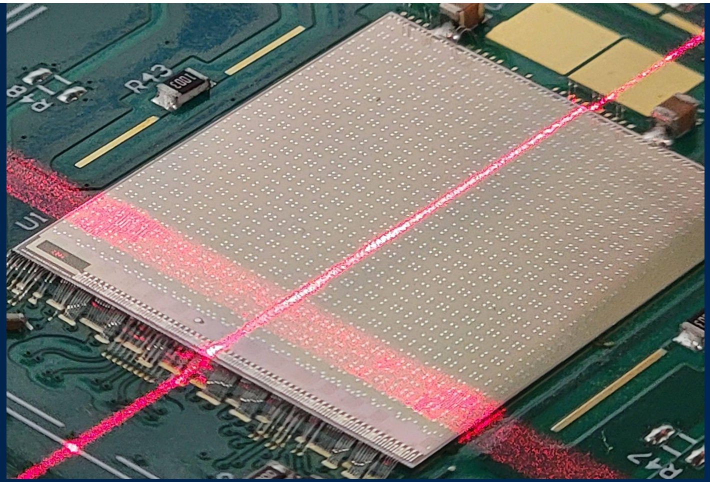
Extensive Characterization Campaign with the full sized ETROC2 chip

Oct 22 | Apr 23 | May 23 | Aug 23 | Sep 23 | Nov 23 | Dec 23 | Jan 24 | Feb 24 | Mar 24 | Apr 24 | May 24 | Jun 24 | Jul 24 | Aug 24 | Sep 24 | Dec 24 | Feb 25 | Mar 25 | Apr 25 | May 25 | Jun 25 | Jul 25 | Sep 25 | Nov 25 | Dec 25

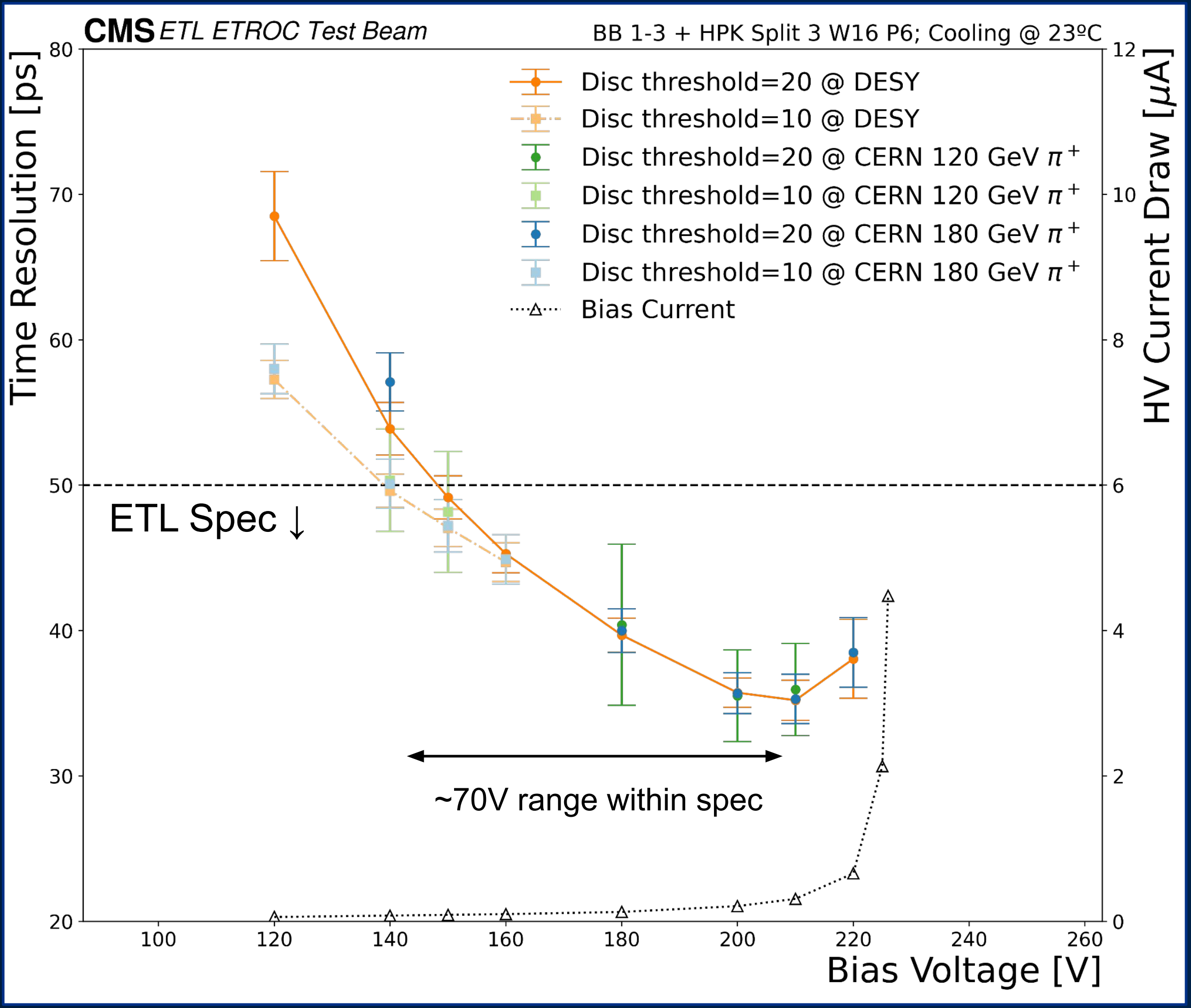
- ETROC2 Submit
- ETROC2 Received
- Software dev. for initial testing and multiboard DAQ
- ETROC2.0 Ext functional testing of bare ETROC2.0 chip, Initial multiboard DAQ.
  At CERN TID Testing, Climate chamb., Wafer probing, Laser testing
- ETROC2.0 CERN TB Hardware comm., σ = 40-50ps observed
- ETROC2.0 Event builder dev for Sync multiboard DAQ
  ETROC2.01 Received
- ETROC2.0 DESY TB Overhauled telescope + new DAQ stack
- ETROC2.01 SEU test, p+
  At CERN TID testing Climate chamber. Wafer probing, Laser testing
- ETROC2.01 DESY TB Added syst. control & cooling
- Firmware improvements & ETROC2 stress testing
- ETROC2.01 DESY+CERN HV Scan HPK Split-3 AIDA Int.
  SEU test, HI
- ETROC2.01 SEU test, p+ -25C Cooling prep,
  At DESY AIDA Integration
- ETROC2.01 DESY TB HV Scan FPK UFSD4
  SEU test, HI
- ETROC2.03 Initial Tests
- ETROC2.01 CERN TB x2 HV Scan BB Yield Test
  ETROC2.03 SEU test, p+
  At CERN TID Testing Climate ch., Laser testing
- ETROC2.03 DESY TB High v Low Power Scan, WS Testing
  At Fermilab Testing with system level firmware and software
- ETROC2.03 SEU test, HI
- ETROC2.03 DESY TB BB Yield Test
  At CERN Wafer probing Climate ch.
- ETROC2.03 DESY TB CERN TB BB Yield Test
  At CERN Wafer probing
  ETROC2.03 SEU test, p+
- ETROC2.02 Initial Tests
- ETROC2.02 CERN TB
- ETROC2.02 DESY TB CERN TB
  At CERN Wafer probing
- *ETROC PRR*
- ETROC2.02 DESY TB

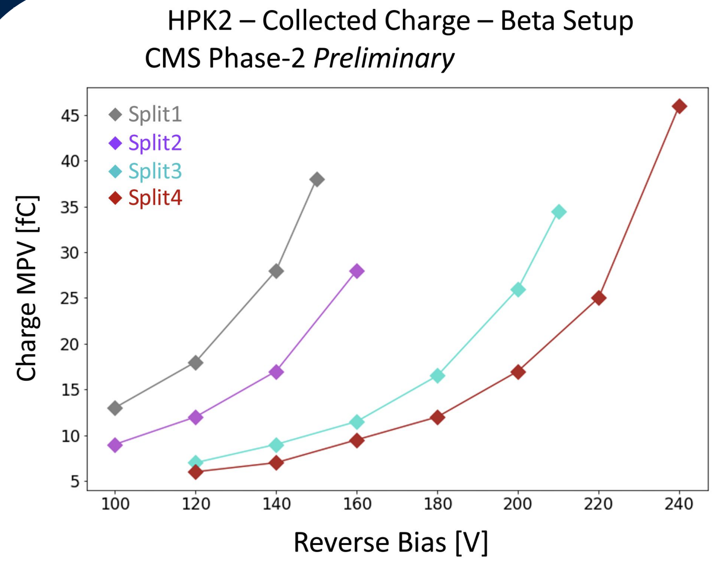
Aggressive heterogeneous campaign to validate the performance of the ETROC2 hybrids

Testing has enabled quick identification and fixes for ASIC and Sensor design for enhanced timing and robust operations



CMS ETL - ETROC2 + LGAD Validation





Sensor under consideration here is HPK2 **Split 3**

Successfully reproduced ~35ps res. *with this board. Results from CERN 120-180 GeV π^+ agree with those from DESY 4 GeV e^- beam*

Total typical chip power consumption is below 800 mW, well within the design constraints on the ETROC

CMS Endcap Timing Layer

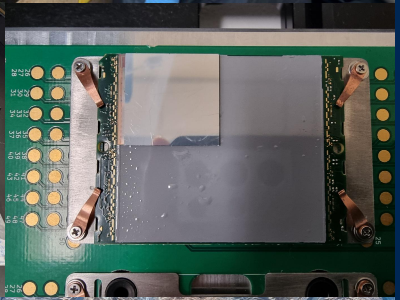
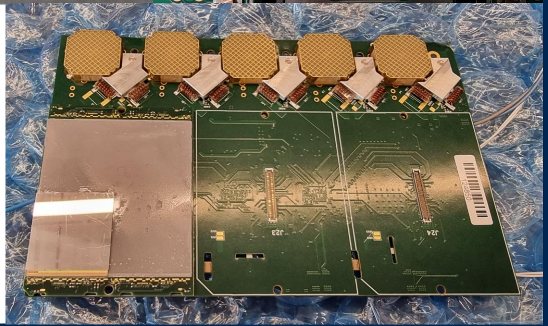
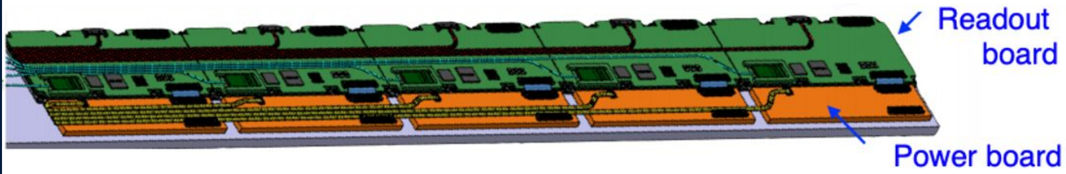
Module production rapidly converging

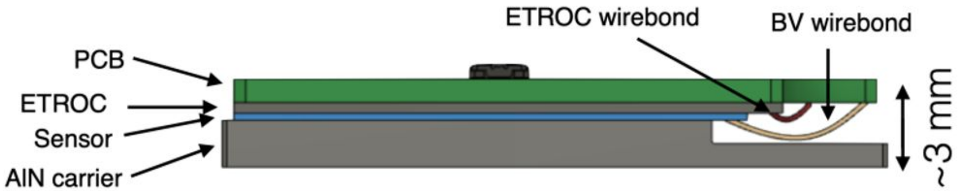
Each ETL module is a 2x2 array of hybrids (LGADs arrays + ETROC) along with a baseplate and PCB for interface with readout

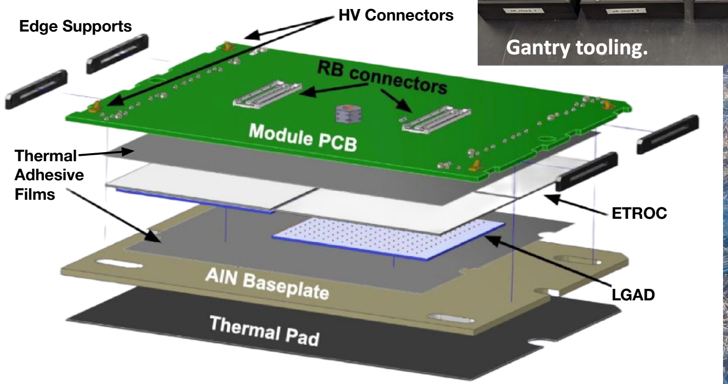
4 ETL assembly sites will produce the 8000 modules required for ETL: Fermilab, Boston University, INFN (Italy) and IFCA (Spain)
- Currently optimizing QA/QC procedures

Demonstrated production at scale (50 modules/week) to understand personnel requirements and identify remaining issues with the assembly procedure.
- Track time of each step as well as QA/QC data such as alignment and number of re-bonds.







CMS Endcap Timing Layer

CMS Minimum Ionizing Particle Timing Detector

First generation timing detector being deployed at the HL-LHC

- CMS MTD is among the very first generation timing detectors being introduced for the LH-LHC era
  - Successful production, assembly, and operations for the CMS MTD and ATLAS HGTD are crucial pathfinding exercises for future 4D trackers
  - Improved PU rejection, and new capabilities for LLP / displaced searches and ToF PID

- The CMS MTD will provide near hermetic precision timing ($|\eta|<3.0$) for tracks using the BTL and ETL
  - Different constraints from radiation hardness, access requirements, instrumented area, etc allow the use of different technologies in each
    - BTL: LYSO:Ce + SiPM
    - ETL: LGADs

- BTL team concluded a successful, multi-faceted campaign of prototyping, optimization, and validation
- BTL production phase has begun in full force, with SM, DM, RU, and tray production and assembly underway
  - Tray assembly on track for early 2026 completion

- ETL team is also nearing the end of a successful characterization campaign
- Sensor procurement tenders are out and ASIC engineering run have commenced

- BTL and ETL on track for timely installation in CMS for Phase-2 upgrade!

CMS ETROC Acknowledgments

- *This work was produced by Fermi Forward Discovery Group, LLC under Contract No. 89243024CSC000002 with the U.S. Department of Energy, Office of Science, Office of High Energy Physics. Publisher acknowledges the U.S. Government license to provide public access under the DOE Public Access Plan DOE Public Access Plan*

- *The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF).*

- *The research leading to these results has received funding from the European Union's Horizon Europe research and innovation programme under grant agreement no. 101057511.*

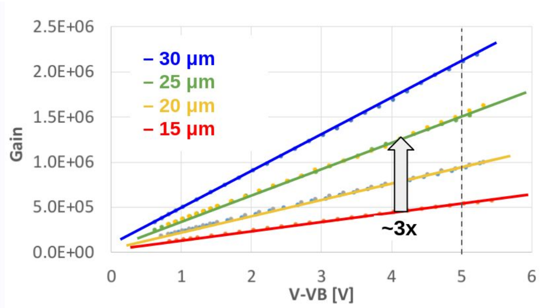
Fermilab

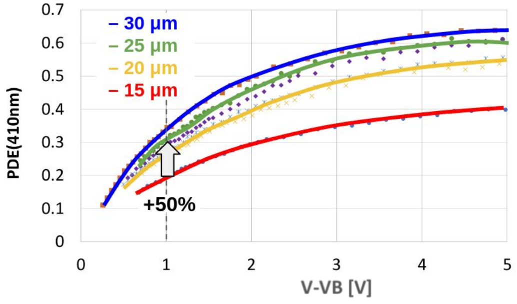
FermiFORWARD

U.S. DEPARTMENT of ENERGY

CMS Barrel Timing Layer

Optimize signal amplitude, rise time, dark count rate for timing performance



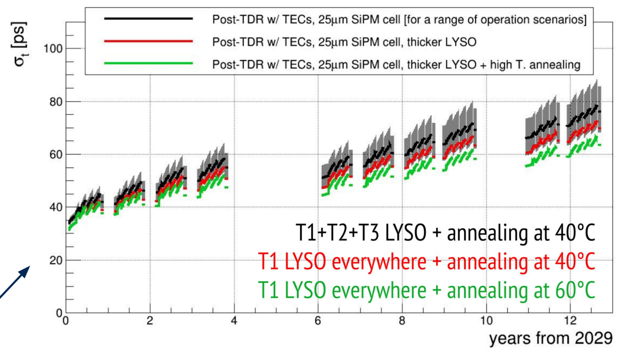


$$\sigma_t = \sigma_t^{ele} \oplus \sigma_t^{phot} \oplus \sigma_t^{DCR} \oplus \sigma_t^{clock}$$

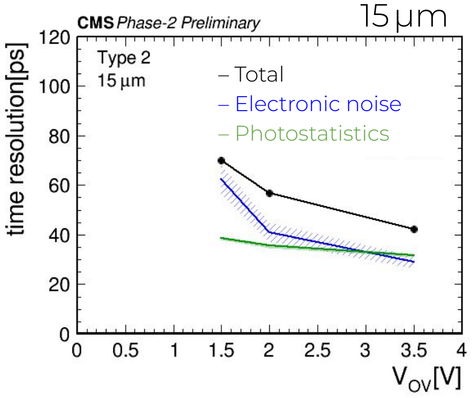
Electronic Noise term goes as rise-time/SNR
Photostatistics term goes as 1/root(amplitude)
Dark Count Rate term goes as root(DCR)/amplitude

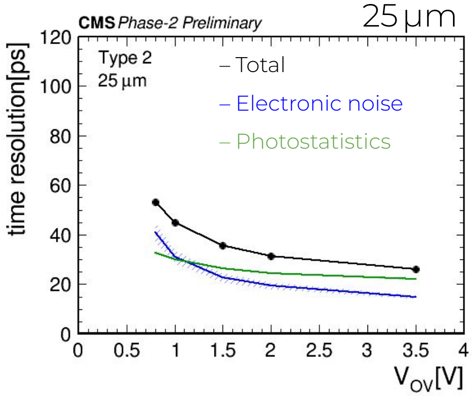
LYSO:Ce bar geometry minimizes SiPM area wrt crystal volume: 3.12 × **3.75** × 54.7 mm^3

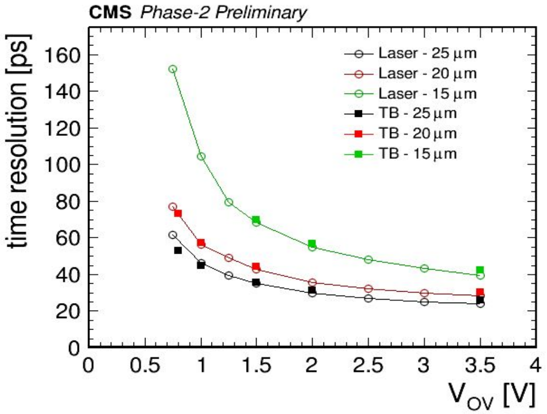
- **Thick** crystals used across the full BTL detector
- Optimized wrapping for improved light collection



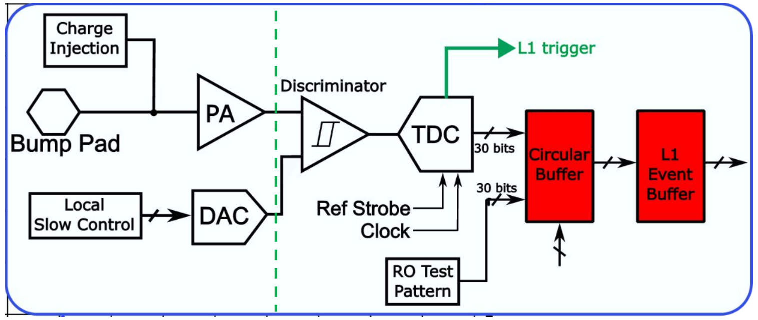
SiPM gain, photodetection efficiency, and speed increased by using **25µm cell size**

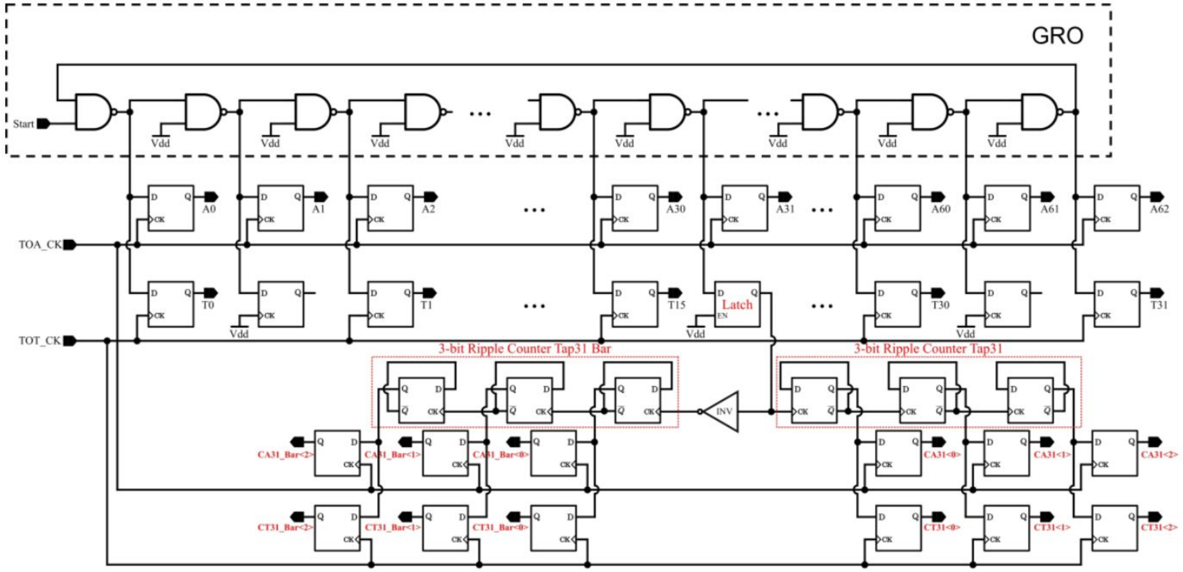


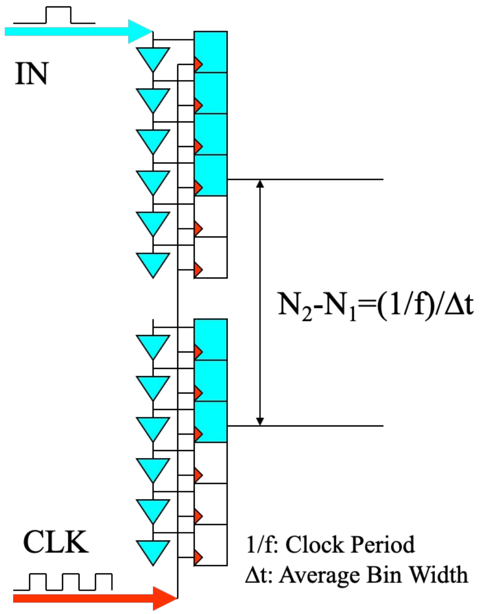




CMS ETROC - TDC Design







Several design features aimed at reducing power compunstion and complexity while retaining good performance

- Delay line based TDC with uncontrolled delay cells
- PVT Effects calibrated with Self-Calibration scheme
- TOA bin size ~ 18ps, TOT bin size ~ 36ps
- Power Consumption limited to 0.1mW at 1% occupancy

CMS ETROC

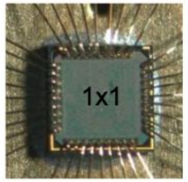
Long Journey to the full sized chip...

Sept 2018 — Dec 2018 — May 2019 — Aug 2019 — March 2020 — May 2020 — July 2021 — Sept 2021 ...

Covid (from Aug 2019)

Project started

ETROC0[1] submitted



Preamp + discriminator

AFE 1.6 - 2.4mW / px

ETROC1[2] submitted

Preamp + discriminator + TDC
4x4 H-tree clock distribution

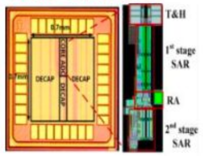
AFE 1.6 - 2.4mW / px
TDC 0.1mW / px

ETROC2: 8x8 → 16x16

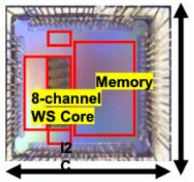
Decision to go for full size full functionality ETROC2,
Delay submission and add few test chips ...

Total of 7 small chips, all successful

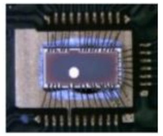
Single channel ADC submitted



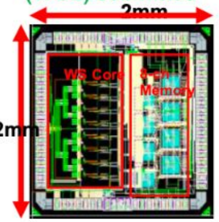
8-channel ADC Waveform Sampler (WS1) submitted



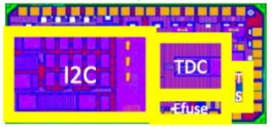
ETROC-PLL mini ASIC submitted



Rad-hard version of Waveform Sampler (WS2) submitted

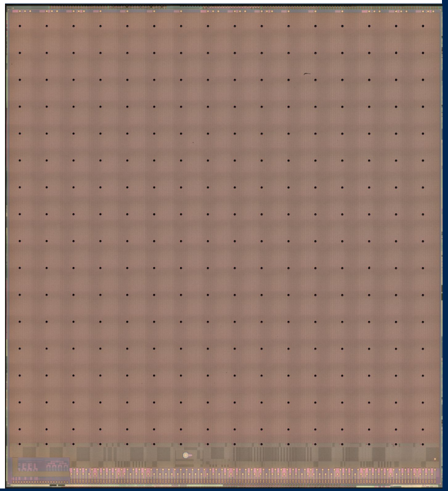


I2C Test chip submitted



All analog blocks have been silicon proven in test chips;
ETROC2 FPGA emulator: has verified digital readout and system interfaces

Design team: FNAL/SMU/LBNL/UCSB
Testing team: FNAL/SMU/UIC/UCSB/Lisbon/IFCA/KUL with students from KSU/KU



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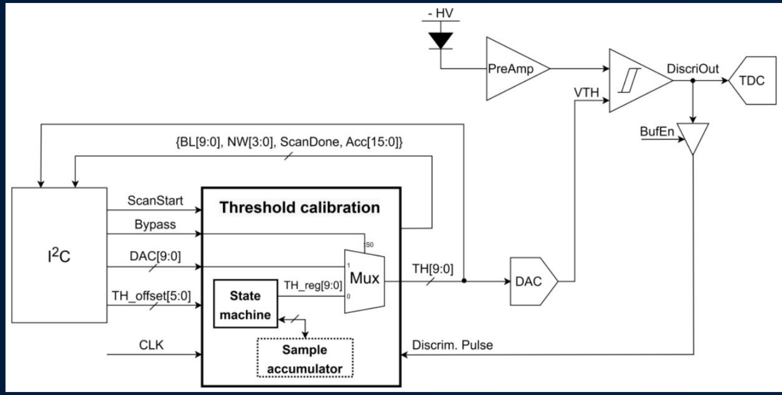
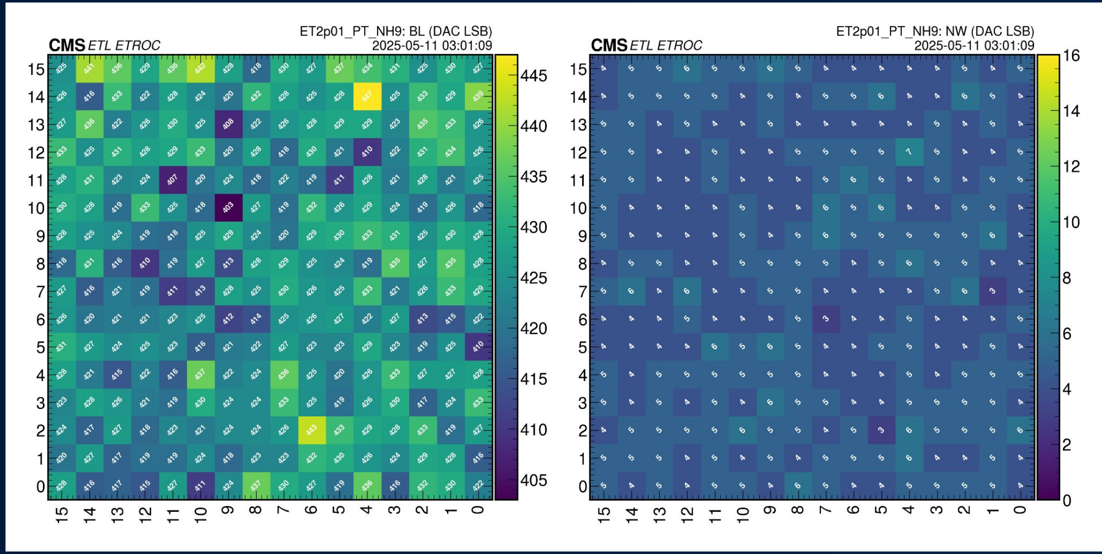
ETROC - Beyond The Timing Precision

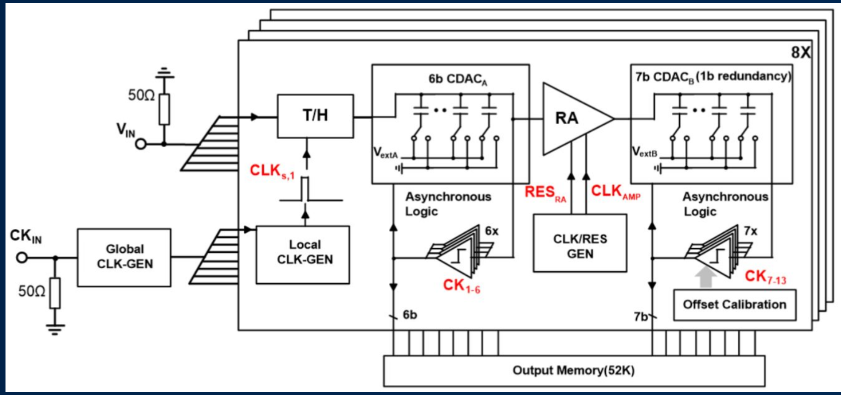
ASIC Design must incorporate features that make the detector operation feasible

Automatic Baseline Calibration

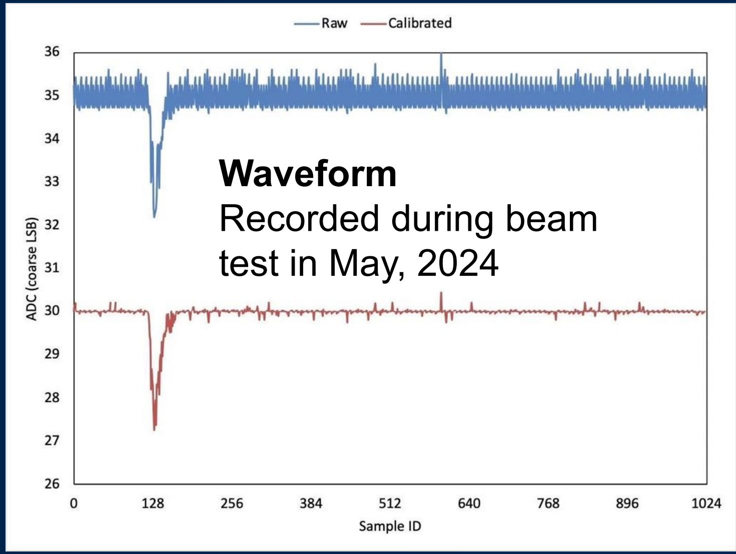




2.56GSps Waveform Sampler

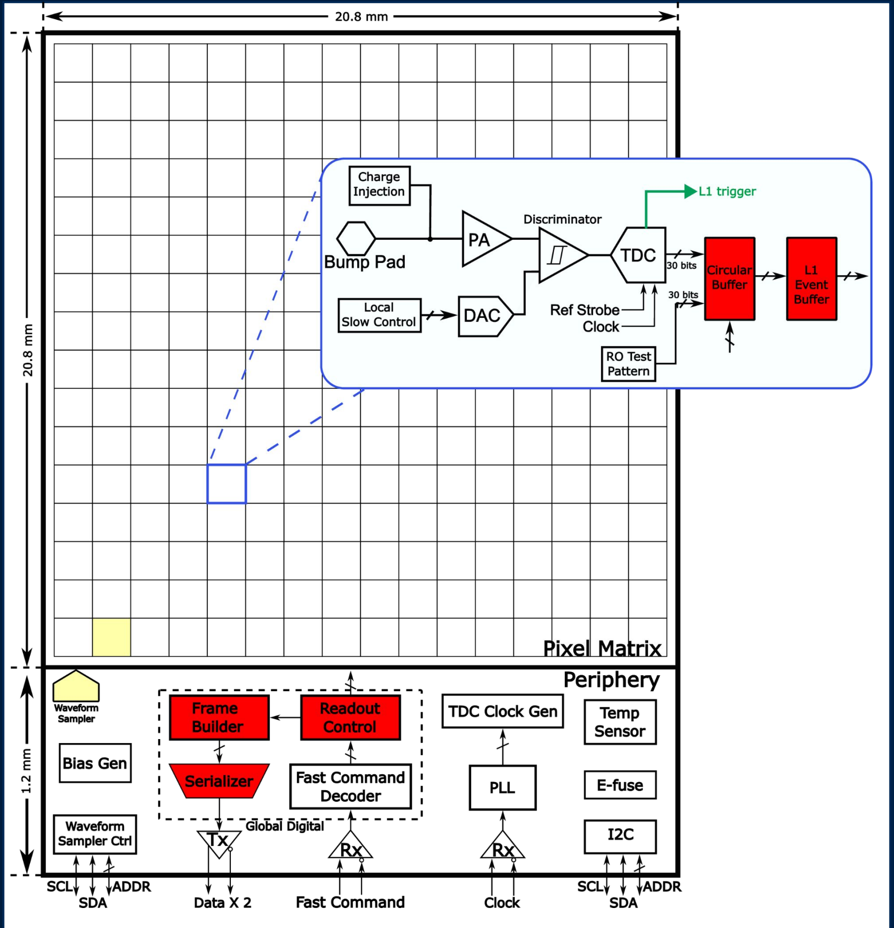


Study LGAD signal shape evolution with TID, etc with 33k oscilloscopes across ETL!



ETROC - Beyond The Timing Precision

ASIC Design must incorporate features that make the detector operation feasible



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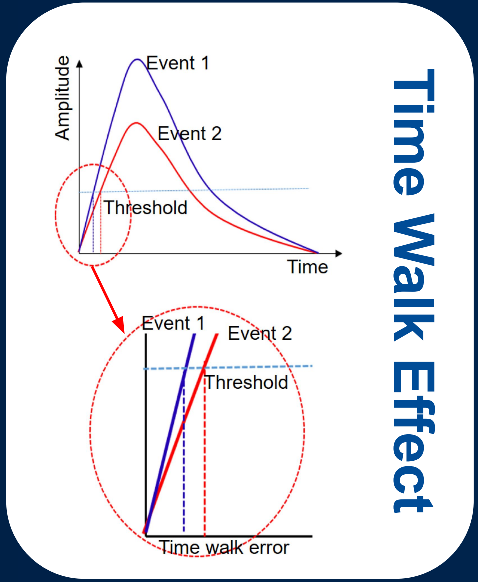

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256 Unique time walk correction parameters?

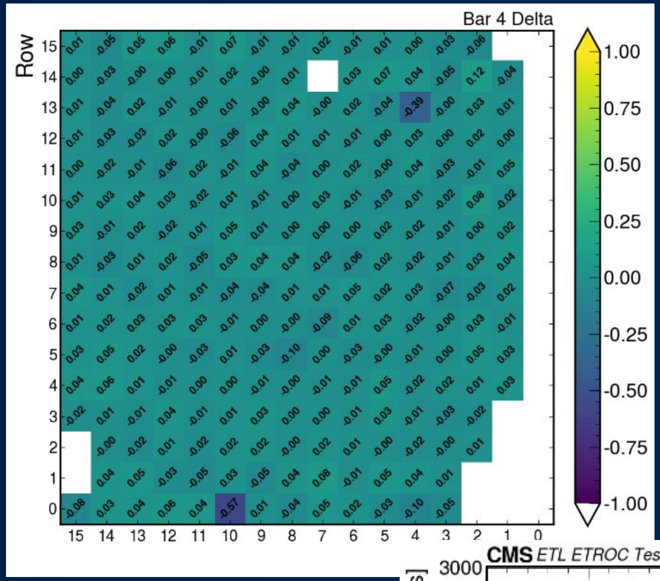
ETROC - Beyond The Timing Precision

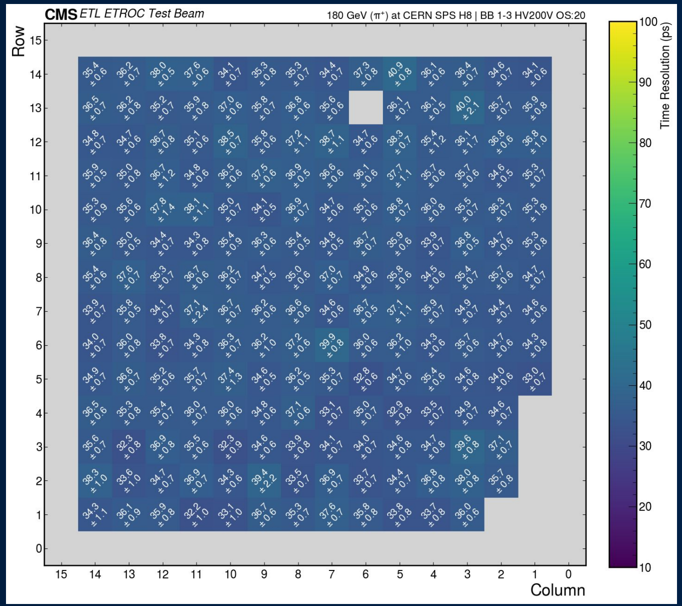
ASIC Design must incorporate features that make the detector operation feasible

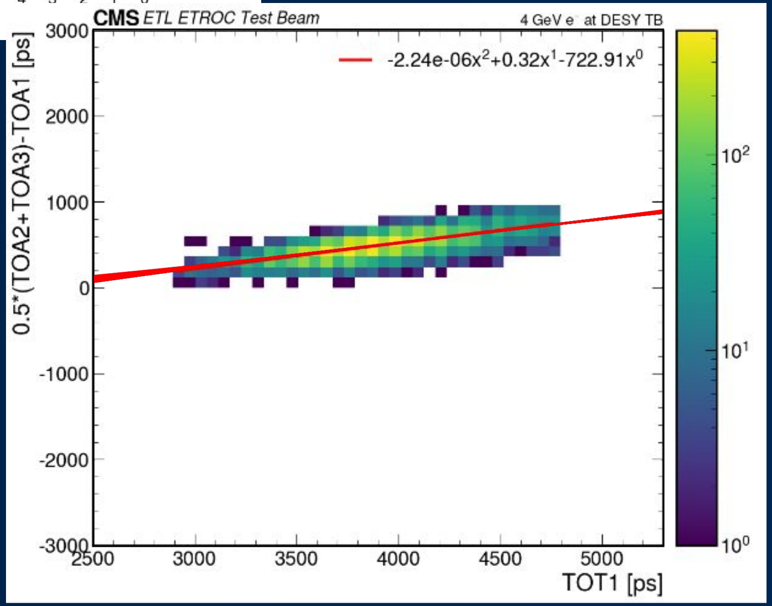
We only need 1 pixel's!

TDC Self-calibration with double strobe method helps eliminate PVT variations across the 16x16 array of pixels

This also means each of the 16x16 pixels is expected to perform identically once the self calibration is applied to each pixel







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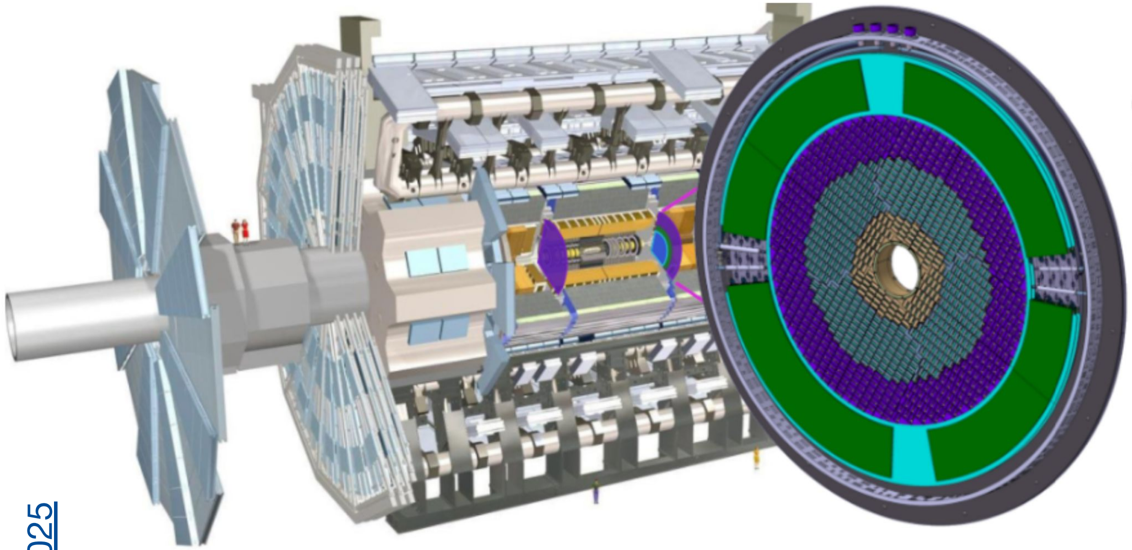
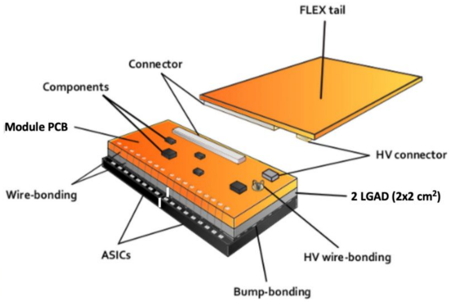
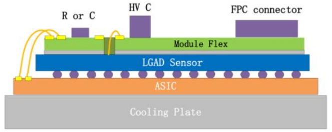
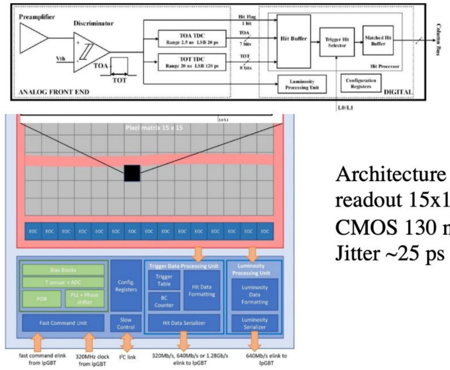
HL-LHC: First generation timing detectors

ATLAS High Granularity Timing Detector









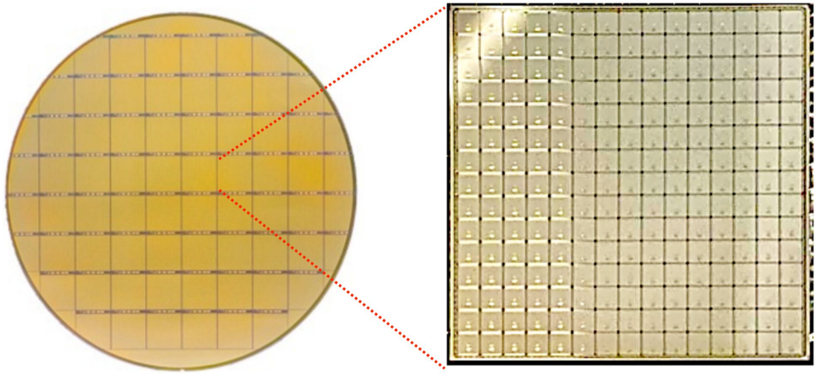
Architecture of the ALTIROC ASIC readout 15x15 pads, 2x2 cm^2, CMOS 130 nm, Jitter ~25 ps

Xiao Yang at VCI2025

2x double-sided layers, based on **Low Gain Avalanche Detectors** (LGADs) and custom ASICs (ALTIROC)

- Target: **30-50 ps per track** (35 - 70 ps per hit),
- **6.4 m²** silicon detector, **3.6M** channels, **1.3 × 1.3 mm²** pixel size, **50 µm** active thickness.

Radiation hardness requirement:
2.0 MGy TID and **2.5E15 n_{eq}/cm^{-2}** @ -30 °C
for **50 ps** and **4 fC**



8-inch LGAD wafer Full size 15*15 LGAD sensor

CMS MTD - Time Walk Correction

Examples from ETL and BTL

Time Walk Effect