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Full Length Article

The ladder and readout cables of intermediate silicon strip detector for sPHENIX

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ABSTRACT

A new silicon-strip-type detector was developed for precise charged-particle tracking in the central rapidity region of heavy ion collisions. A new detector and collaboration at the Relativistic Heavy Ion Collider at Brookhaven National Laboratory is sPHENIX, which is a major upgrade of the PHENIX detector. The intermediate tracker (INTT) is part of the advanced tracking system of the sPHENIX detector complex together with a CMOS monolithic-active-pixel-sensor based silicon-pixel vertex detector, a time-projection chamber, and a micromegas-based detector. The INTT detector is barrel shaped and comprises 56 silicon ladders. Two different types of strip sensors of 78 μm pitch and 320 μm thick are mounted on each half of a silicon ladder. Each strip sensor is segmented into 8 × 2 and 5 × 2 blocks with lengths of 16 and 20 mm. Strips are read out with a silicon strip-readout (FPHX) chip. In order to transmit massive data from the FPHX to the down stream readout electronics card (ROC), a series of long and high speed readout cables were developed. This document focuses on the silicon ladder, the readout cables, and the ROC of the INTT. The radiation hardness is studied for some parts of the INTT devices in the last part of this document, since the INTT employed some materials from the technology frontier of the industry whose radiation hardness is not necessarily well known.

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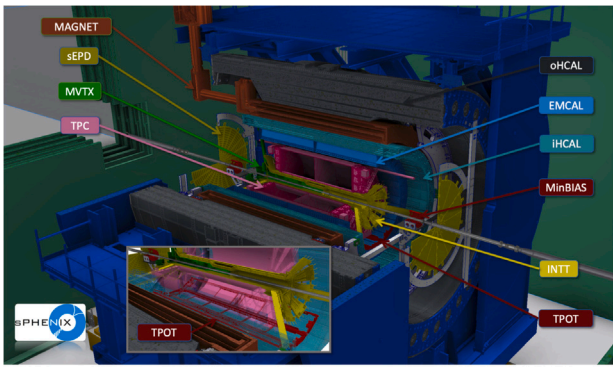

Fig. 1. The mechanical drawing of the sPHENIX detector. The silicon strip intermediate tracker (INTT) is indicated by yellow arrow.

1. Introduction

The sPHENIX detector [1] at the Relativistic Heavy Ion Collider (RHIC) [2] at Brookhaven National Laboratory, USA, is a major upgrade of the PHENIX detector [3], which was decommissioned in 2017. The sPHENIX experiment collects high-statistics proton–proton, proton–nucleus, and nucleus–nucleus data, enabling state-of-the-art studies of jet modification, upsilon suppression, and open heavy-flavor production to probe the microscopic nature of the strongly-coupled quark-gluon plasma. Such measurements are complementary to those of experiments at the Large Hadron Collider (LHC) [4] at CERN, and will also allow a broad range of cold quantum chromodynamic studies [5].

The sPHENIX detector provides precision vertexing, tracking, and electromagnetic and hadronic calorimetry in the central pseudorapidity region $|\eta| < 1.1$ with full azimuthal coverage at the full RHIC collision rate of 15 kHz in Au+Au at $\sqrt{s_{NN}} = 200$ GeV. A comprehensive assessment of these requirements led to the development of the reference design shown in Fig. 1. In its overall layout, sPHENIX follows the typical geometry of modern collider detectors. The tracking system comprises a CMOS monolithic-active-pixel-sensor (MAPS) microvertex detector (MVTX), a silicon-strip intermediate tracker (INTT), and a time-projection chamber (TPC). For calibration, a micromegas based detector (TPOT) [6] partially covers the outside of the TPC acceptance. The calorimeter stack includes a tungsten/scintillating fiber electromagnetic calorimeter (EMCAL) and aluminum/scintillator and steel/scintillator tile hadronic calorimeter (HCAL), divided into inner and outer parts. The inner HCAL sits inside the 1.4 T superconducting solenoid, which was refurbished from the decommissioned BaBar detector [7].

This document describes the details of the INTT silicon ladder, its readout cables, and the readout electronics card.

2. The detector overview for the silicon strip intermediate tracker (INTT)

The barrel-type INTT detector comprises inner and outer layers of INTT silicon ladders. Adjacent ladders are staggered to prevent dead space in azimuthal acceptance. The inner and outer barrels have 24 and 32 ladders, respectively. Details of the INTT barrel are beyond the scope of this document, and a separate paper is under preparation.

The designs of the INTT ladder and its readout are constrained by the specification of the FPHX [8–10] readout chip and the readout card (ROC) of the Forward Vertex (FVTX) detector [11] in PHENIX. Since the INTT reuses the FPHX design and ROCs, the rest of INTT detector was designed to be compatible with these readout chips and electronics. New copies of FPHX chips were produced for the INTT detector, while the ROCs were recycled.

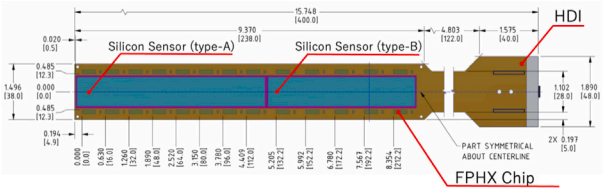

Fig. 2. Schematics of the INTT module and the dimensions of each components, i.e. the silicon sensors, FPHX chips, and the HDI cable. Dimensions are given in inches, while numbers in brackets are in millimeters.

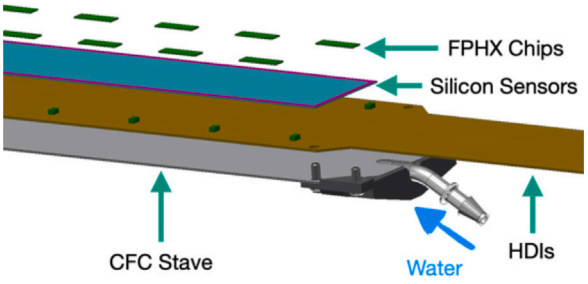

Fig. 3. The stackup of the components of the INTT ladder.

Table 1
The components and total number of channels of the INTT module and ladder. The details of silicon strip sensor type-A and B are discussed in the Section 3.1.

	Component	Quantity
Silicon module	Silicon strip sensor	2 (Type-A & B)
	FPHX Chips	26
	HDI	1
	Total number of channels	3,328
Silicon ladder	Silicon module	2
	Stave	1
	Total number of channels	6,656

Two silicon sensors and 26 FPHX readout chips [9–11] are mounted on a high-density interconnect (HDI) flexible print cable to form an INTT silicon module. The schematics of the silicon module are shown in Fig. 2, which illustrates the layout of the silicon sensors and the FPHX chips with respect to the HDI cable.

These components of the INTT silicon module and the ladder are summarized in Table 1. Two INTT modules are aligned longitudinally and glued to a carbon fiber composite (CFC) support stave to form an INTT silicon ladder. To show the structures of the INTT ladder, the stackup of the components of the ladder is illustrated in Fig. 3. A photo of the INTT ladder is shown in Fig. 4.

Both glue and carbon fiber have high thermal conductivity to diffuse heat generated by the FPHX chips. A water cooling system removes heat from the barrel through a carbon tube integrated within the body of the stave. Fig. 3 also shows the tube attached to the edge of the CFC stave, which is an inlet for cooling water.

The data of a given ladder are read out from both longitudinal ends for each silicon module. Thus, each HDI cable transmits 20.8 Gbit/s of data from half of a ladder on 104 parallel lines with each 200 Mbit/s [11]. The data are further transmitted downstream from the HDI by a bus extender (BEX) cable [13] and a conversion cable (CC).[1] The BEX is a 1.11 meter long flexible print cable (FPC) employing liquid-crystal polymer as a dielectric material to suppress losses in transmission lines. In both ends, the conversion cable comprises three

[1] The illustration of the full readout chain cables is presented in Fig. 14

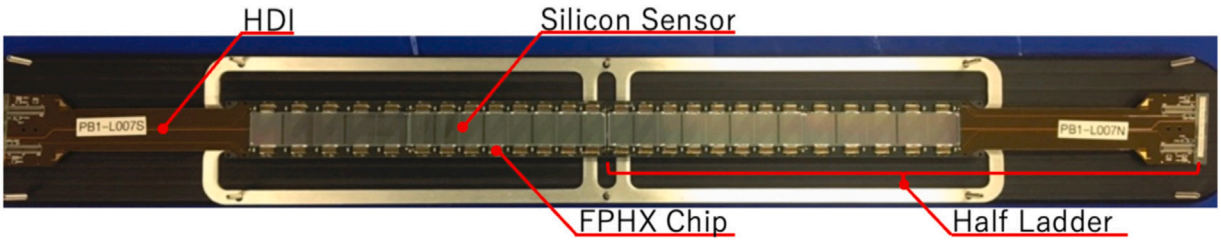

Fig. 4. Photo of the INTT ladder with sensors facing up. Note the center line dividing the two halves of the sensor and the rows of FPHX chips along the sensor edges.

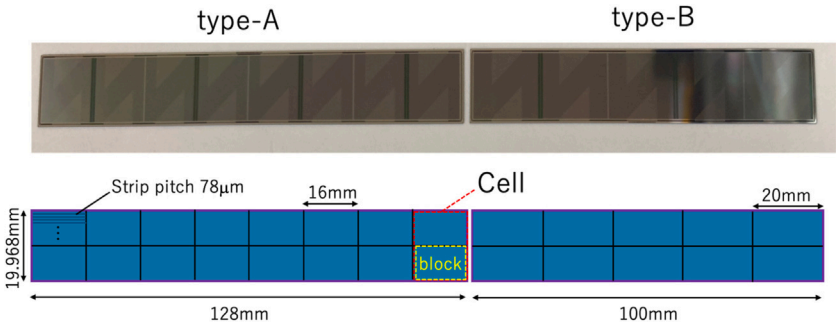

Fig. 5. The photo of type-A and type-B silicon strip sensors (top). The layouts of the cell and the block are defined in the schematic drawing (bottom). The dimensions are presented for the active area of sensors [12]. The strip pitch is not scaled in the drawing.

components: (1) μ-coaxial harness, (2) power and ground cables, and (3) connector print boards. The downstream end of the conversion cable is connected to the read-out card (ROC) which collects data from up to seven half-ladders, and then transmits reformatted data to further downstream electronics via an optical fiber connection. The data of a half ladder are transmitted by two fibers and each of which transmits 2 Gbit/s (4 Gbit/s per ladder). The downstream electronics beyond the ROC and data acquisition system are beyond the scope of this document.

The total length of HDI, BEX, and the conversion cable is 1.65 to 1.75 m, which is about factor of five longer than the signal transmission line of the FVTX. Thus the signal transmission loss is a major technical challenge for the design of each readout cable. The output signal power is fixed by the FPHX design and a receiver of the ROC cannot be changed due to its recycled use. The allowance of the transmission loss was estimated by a circuit simulation based on the output signal amplitude of the FPHX for a given LVDS current, and the $\pm$100 mV mask of the eye diagram of the receiver at the ROC. The input signal models for the simulation imitates the output signal at the LVDS current of 2 mA. The allowance of the entire transmission line was estimated to be approximately $-$12 dB at 500 MHz to prevent the interference with the mask. 500 MHz is the knee frequency assuming a typical 800 ps rise time [14].

3. INTT ladder

This section describes the electrical components and support systems used to read out and power the INTT. The silicon-strip sensors and the FPHX readout chips are described in Section 3.1 and Section 3.2, respectively. The HDI that provides power, bias voltage, and slow-control signals to the sensor is discussed in Section 3.3. The stave support structure is discussed in Section 3.4. The material budget of the ladder in the radial direction is discussed in Section 3.5. Lastly, the dead area of the silicon ladder is evaluated in Section 3.6.

3.1. Silicon sensors

The silicon-strip sensor [12] is single-sided and AC-coupled. The design is a modified version of the PHENIX FVTX silicon mini-strip sensors [11]. The sensors, as well as the FVTX sensors, were fabricated by Hamamatsu Photonics K.K.. There are two types of sensors (type-A and type-B), which are distinguished by the length of strips and number of blocks. Each block is connected to one FPHX readout chip as shown in Figs. 5 and 6. The type-A sensor has an active area of 128 $\times$ 19.968 mm that is segmented into 8 rows and 2 columns of blocks (forming a cell), each of which consisted of 128 strips with 78 μm pitch and 16 mm long. Each strip is oriented in the longitudinal direction and extends to the end of each block. Similarly, the type-B sensor has an active area of 100 $\times$ 19.968 mm that is segmented into 5 rows and 2 columns of blocks, each of which comprises 128 strips in 78 μm pitch and 20 mm long that are also oriented in the longitudinal direction. Fig. 5 shows the photo and layouts of type-A and type-B silicon strip sensors. Table 2 summarizes type-A and -B characteristics.

The small gap between adjacent blocks where the DC pads are laid out on the surface is completely active. The sensors were fabricated with p-implants on a 320 μm thick n-type substrate. The strips are AC-coupled and biased through individual 15 MΩ poly-silicon resistors to a typical operating voltage of 100 V. The aluminum metallization width of the strips is 20 μm, which is wider than the implant width of 10 μm. This provides field-plate protection against micro discharges, which are known to grow with radiation-induced increases in the leakage current. These specifications of the silicon sensor are summarized in Table 3. The strips are also protected by two p-implant guard rings and an n+ region between the guard rings and the sensor edge. These designs follow from the silicon-strip sensors of the FVTX [11].

In Fig. 6, the strips run horizontally (longitudinal direction). The readout lines of each strip are wired perpendicular to the strips orientation using double-metal technology. The other end of the readout lines are connected to readout pads, which transmit data to the FPHX chips using a wire bonding. For a given cell, the strip channels 0 to 127 and 128 to 255 are wired to the readout pads, as shown at the bottom and top, respectively.

Table 2
The characteristics of type-A and type-B silicon strip sensors [12].

Item	Type-A	Type-B	Type-A+B Total
Physical dimensions	130.0 mm × 22.5 mm	102.0 mm × 22.5 mm	232.0 mm × 22.5 mm
Active area dimensions	128 mm × 19.968 mm	100 mm × 19.968 mm	228 mm × 19.968 mm
Active area fraction	87.4%	87.0%	
Active cell dimensions	16 mm × 19.968 mm	20 mm × 19.968 mm	N/A
# of cells	8	5	13
Active block dimensions	16 mm × 9.984 mm	20 mm × 9.984 mm	N/A
# of blocks	16	10	26
Number of blocks per cell	2		
Number of strips per block	128		
Strip pitch	78 μm		
Number of strip channels	2,048	1,280	3,328

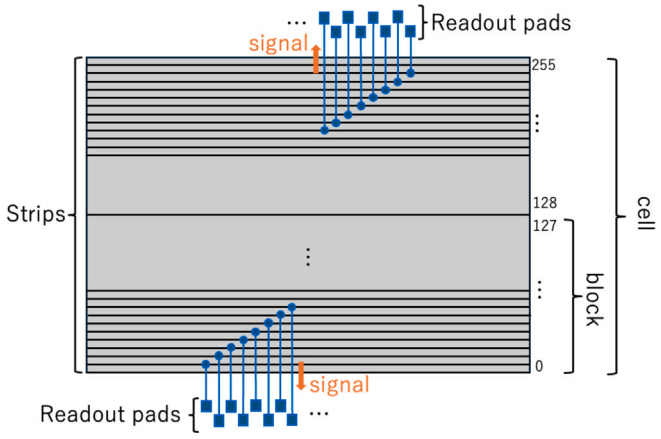

Fig. 6. The schematics of the double metal structured strips and their readout lines [12].

Table 3
Specifications of the silicon strip sensors [12].

Item	Specification
SSD type	AC-SSSD
Nominal operating voltage	100 V
Bias Providing Type	Poly-Si bias
Poly-Si resistance	15 MΩ
Silicon thickness	320 μm
Strip implant width	10 μm
Strip readout aluminum width	20 μm

3.2. FPHX chip

A custom 128-channel front-end ASIC, the FPHX [8–10], was developed at Fermilab for use in the PHENIX FVTX Detector [11]. The size of the chip is 9 × 2 mm. The chip is operated at 2.5 V and consumes power as low as 390 μW per channel. The FPHX is a mixed-mode chip with two major and distinct sections: the analog front-end, and the digital back-end.

The analog section consists of an integration/shaping stage, followed by a 3-bit ADC stage. The FPHX chip integrates and shapes signals from 128 channels and digitizes in parallel. Then it sparsifies data and serially reads out the digitized data.

The back-end is a novel, triggerless, data-push architecture that permits operation without deadtime and high-speed readout with very low latency. It has been designed to process up to four hits within four RHIC beam crossings. Although it takes longer, it can process more than 4 hits from a given crossing.

A fully processed hit is zero suppressed, and contains a 7-bit timestamp in the unit of RHIC radio frequency 9.4 MHz (~ 1/106 ns), a 7-bit channel ID, and a 3-bit ADC value. The data word is output over two

Table 4
Specifications of the FPHX readout chip [8–10].

Item	Specification
Dimensions	9 mm × 2 mm
Operation voltage	2.5 V
Power consumption	390 μW per channel
Number of Channels	128
ADC channels	3 bits
Data Transmission	200 Mbit/s

LVDS serial lines in alternating order at a rate of up to 200 Mbit/s. The default output LVDS current is 1 mA, while it can be tunable up to 8 mA as the trade off of more power consumption. A summary of FPHX specifications [8–10] is given in Table 4.

In addition, to be as self-sufficient as possible, the FPHX chip provides its own internal bias voltages and currents with minimal external support circuitry. For the user to be able to control the internal parameters and biases, a digital slow-control interface is provided on each chip to enable programming. Adjustable parameters include gain, threshold, rise time, fall time, input transistor bias current, channel masking, and several additional fine-tuning parameters [10].

Typical hit rates per FPHX is ≈3–10 kHz in Au+Au collisions at $\sqrt{s_{NN}}$ = 200 GeV. The typical hit-strip cluster is rather compact, as the fraction of cluster size for ≤3 strips is ≈75% and for cluster size equal to 1 is ≈40%.

3.3. High-density interconnects

The HDI is a flexible print circuit board used to read out a half ladder, which comprises two silicon sensors with 26 FPHX chips. The basic layer design of the HDI structure follows from the FVTX [11]. The geometric constraint for the silicon ladder is somewhat less stringent for the INTT than for the FVTX. Thus, the circuit design parameters such as line and space are relaxed from the FVTX, which results in an improved yield rate in the fabricating process.

The HDI was designed by HAYASHI-REPIC Co., Ltd.[15] and fabricated by YAMASHITA MATERIALS CORPORATION [16] in Japan. The width of the HDI is 38 mm in the sensor area and 43 mm at the connector end. The length is 398 mm, which is the longest limit of industry fabrication for the multilayer FPC in an automated manner using dedicated fabrication machines.

The HDI is seven-layered, each layer comprising 9 μm thick electrolytic copper foil, 12.5 to 50 μm thick polyimide (Panasonic FELIOS R-F775) [17], and 15 to 25 μm thick resin glue (Halogen free adhesive sheet SAFG, Nikkan Industries co., ltd.). The total thickness is 418 μm in the sensor area. As discussed in Section 3.5 below, the total thickness of copper layers is 68 μm, and is the greatest contribution to the material budget of the INTT ladder. The top and bottom copper foil layers were

Table 5
Thickness and material of each HDI layer. Regist on the top layer is applied except for pads region for the silicon, the FPHX, and other components.

Layer	Material	Thickness [μm]
	Regist	20
	Copper plated	15
L1	Electrolytic copper foil	9
	Base polyimide	50
L2	Electrolytic copper foil	9
	Glue	25
	Base polyimide	12.5
	Glue	15
L3	Electrolytic copper foil	9
	Base polyimide	50
L4	Electrolytic copper foil	9
	Glue	25
	Base polyimide	12.5
	Glue	15
L5	Electrolytic copper foil	9
	Base polyimide	50
L6	Electrolytic copper foil	9
	Glue	25
	Base polyimide	25
L7	Electrolytic copper foil	9
	Copper plated	15
	Regist	20

plated with 15 μm of copper.[2] The layer structure with thickness and material of each layer is tabulated in Table 5.

The schematic for each layer is shown in Fig. 7. From top to bottom, each layer is for transmitting bias for the type-B silicon sensor (L1), analog ground (L2), signals (L3), DC power for the analog and digital parts of FPHX (L4), signal (L5), digital ground (L6), and for the type-A sensor and signals (L7). There are two thermostats implemented on the L7 to monitor the cooling status of heat generated during operation from the FPHX chips.

There are 122 signal lines per HDI cable: 52 pairs of output data lines, 8 pairs of slow-control and clock LVDS lines, and two dedicated lines to inject calibration pulses to the FPHX. Signal transmission lines are mainly placed in layers 3 and 5 to be shielded from external electromagnetic (EM) fields by keeping these layers between solid-copper layers which are assigned for either analog or digital grounds or the DC power. The line and space are both 60 μm. The characteristic impedance is designed to provide a 100 Ω differential for these LVDS pair lines to ensure matching with the rest of the readout cable chain.

The L7 was originally designed to be a dedicated layer for the bias line to a silicon sensor in the FVTX. In addition to bias lines for the sensors in INTT, some signal lines are implemented around the FPHX region. Ideally these signal lines are to be fit within the signal layers of the L3 or the L5 though, they could not fit as the consequence of the relaxed line & space policy in the INTT (60 & 60 μm) compared to these of FVTX (40 & 40 μm). This is a concern because the back plane of the L7 is not shielded by the solid foil ground nor the power layers, the signal lines are exposed to external EM fields. Therefore, the length of the signal lines were kept as short as possible (centimeter lengthscale) in the L7. Fig. 8 shows a photo of the HDI cables with L1 and L7 face up. Table 6 summarizes the major specifications of the HDI cable.

[2] The copper plate was 15 μm thick for the 1st and 2nd batches of the HDI production. The thickness increased to 25 μm for the 3rd batch in HDI production. The total radiation length of the silicon ladder was increased by 3%.

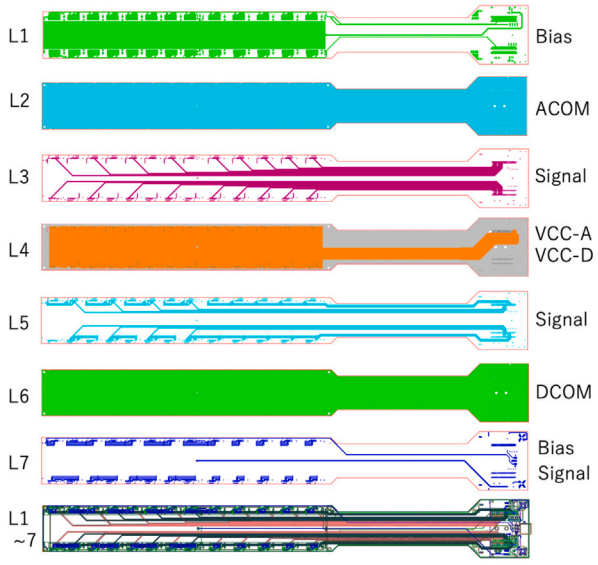

Fig. 7. The schematic of each layer of the HDI. The ACOM and DCOM layers provide analog and digital grounds to FPHX chips, respectively. The 2.5 V power lines for the analog and digital parts of the FPHX chip are electrically isolated from each other within L4. At the bottom (in different colors) is the overlay of line patterns for all seven layers.

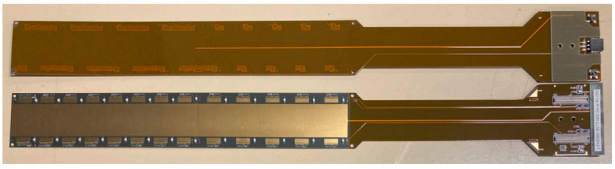

Fig. 8. Photo of the HDI cables with L1 face up (bottom) and L7 face up (top).

Table 6
Specifications of the HDI cable. The characteristic impedance is for the LVDS pair.

Item	Specification
Dimensions	398 mm × 38 mm
Width of connector ends	43 mm
Total thickness (sensor pad region)	418 μm
Conductive material	Copper
Dielectric material	Polymide
Number of layers	7
Number of signal lines	122
Line and space	60 μm & 60 μm
Characteristic impedance	100 Ω

Pairs of connectors for data, LV power for the FPHX, and grounds are implemented in the end of the HDI. The model of data connector is the Hirose Co. DF18C-100DP-0.4V(51) plug, which consists of 100 channels with a 400 μm pitch between conducting pins. Also, there are two bias connectors and a 3-pin thermostat connectors implemented in the end of the HDI.

3.4. Stave

The stave is a mechanical support made mainly of carbon fiber composite (CFC) skins. The stave itself, plus an extension for mechanical attachment is 497 mm long by 38 mm wide. This matches the HDI width around the sensor area and accommodates two silicon modules per stave, forming the INTT silicon ladder. The heat load expected from each half ladder is 64 mW × 26 FPHX chips, or approximately 1.7 W. The total heat load over the entire INTT is ≈186 W for 112 half ladders.

Table 7
Specifications of the CFRP prepreg.

Item	Specification
CFRP prepreg	NT91500-520S [18]
Carbon fiber	XN-90
Resin	25R epoxy
Resin weight fraction	20%
Density	2.19 g/cm^3
Thermal conductivity	500 W/m K
Tensile module	860 GPa
Tensile strength	3430 MPa
Thickness	100 μm

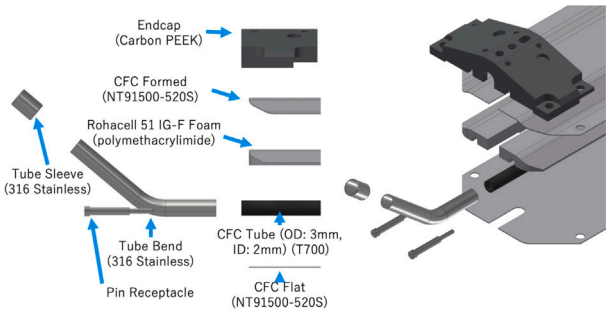

Fig. 9. The mechanical design of the edge of the stave. The HDI is assembled on the bottom flat CFC plate.

The stave is required not only for the rigidity of the support structure, but also for high thermal conductivity to dissipate local heat generated by the FPHX chips. The main component of the stave is a carbon fiber reinforced plastic prepreg (CFRP). The GRANOC prepreg sheet model NT91500-520S of Nippon Graphite Fiber Co. was used, which comprises 25R epoxy and XN-90 carbon fiber with a high thermal conductivity of 500 W/m K, with resin weight fractions of 20% [18]. The thickness of 0.10 mm with density of 2.19 g/cm^3 prepreg provides satisfactory mechanical strength with tensile module and strength of 860 GPa and 3430 MPa, respectively. Table 7 summarizes the specifications of the CFRP prepreg.

Fig. 9 shows the stack up of the stave and the mechanical attachments of its edge. The shells of the stave are CFC plates at the top and bottom are flat and formed, respectively. The formed plate is U-shaped to accommodate the 3 mm diameter cooling tube between two CFC plates with 3 mm thick ROHACELL 110 RIST form [19] that tapers down near the edge forming a structural core. The cooling tube is made of Toreyca T700C carbon fiber prepreg [20] fabricated by Kimuraya Co., Ltd., Japan. The NT91500-520S sheet is unidirectional with high thermal conductivity. To provide omnidirectional rigidity, each CFC plate has three unidirectional sheet layers with high thermal conductivity oriented in longitudinal, transverse, and longitudinal directions. The thickness of the CFC plate is 0.33 mm and the total thickness of the stave is 3.76 mm.

The mechanical attachment of both edges of the stave comprise the end caps, SUS316 cooling-tube extensions, and pairs of pin receptacles manufactured by Mill-Max MFG Co. for grounding. The endcap is made of Ketron CA30 PEEK [21] manufactured by Mitsubishi Chemical Co. The stainless tubes and the cooling tubes were glued using Henkel LOCTITE EA 9396 adhesive [22]. The rest of the stave pieces are assembled using the graphite conductive EP75-1 epoxy adhesive (MasterBond Co.) [23]. Figs. 10 and 11 show the photo and the engineering drawing of the INTT stave. Table 8 summarizes the material list of stave components and specifications.

The staves were fully fabricated by Asuka Co., Ltd., Japan, including the baking process of the CFC plates. To ensure meeting the requirements, the following four tests were applied to staves and to every cooling tube (after the stainless extensions were glued).

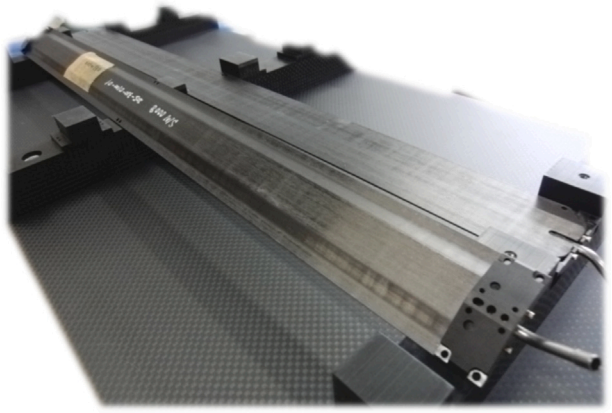

Fig. 10. The photo of the INTT staves.

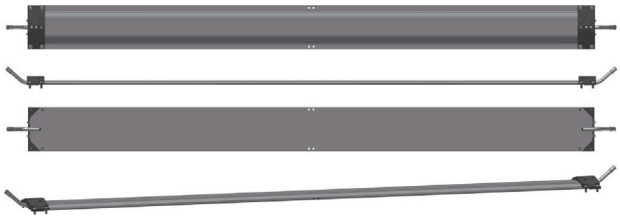

Fig. 11. The INTT stave drawings from four different view angles. The HDI is assembled on the bottom flat CFC plate.

Table 8
The material list of stave components and specifications. The total thickness is at the sensor region.

Item	Model/Specification
Dimensions	497 mm × 38 mm
Total thickness	3.76 mm
Adhesive for stave assembly	MasterBond EP75-1 [23]
Structure core	ROHACELL 110 RIST [19]
End cap	Ketron CA3 PEEK [21]
CFC cooling tube	Toreyca T700C [20]
Cooling tube extension	SUS316
Cooling tube adhesive	Henkel LOCTITE 9396 [22]

1. Burst test : Tube does not burst for 1 h at 60 ± 2 psi
2. Leak test : less than 0.2 ml mbar/min at the initial pressure of ≈10 kPa
3. Heat-cycle test : 40 ↔ 0 °C (one cycle)
4. Flatness < 100 μm of the flat side of the stave and alignment positions are within specified tolerance

Any leak from the cooling tubes can be fatal since it may damage not only the INTT, but also other detectors. Tests 1 and 2 examines the tiny gap between the CFC tube and SUS sleeves are uniformly filled by the glue. The outer diameter of the CFC tube was precisely machined to be 2.936 ± 0.064 mm to make tiny space for the glue in between the inner diameter of the SUS sleeve of 3.0 mm. The staves were assembled with only those cooling tubes that passed the 1 and 2 examinations to keep the yield rate of the stave production reasonably high. The assembled staves were then examined for the above items 3 and 4. The flatness test 4 is also crucial after the heat cycle test 3 because the 320 μm thick silicon sensor can be cracked during the baking process after its assembly on the HDI and the stave.

The overall thermal performance for the ladder was studied using an ANSYS 2019 R3 with the Steady State Thermal module [24]. Shown in Fig. 12 is the simulated results of the ladder with the following boundary conditions; (1) inlet water temperature = 15 °C, (2) flow

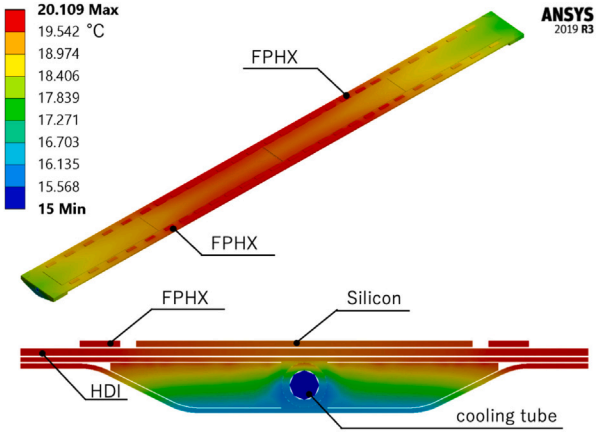

Fig. 12. The simulated results of the thermal conductivity of the ladder. The top figure displays the top surface of the ladder, while the bottom figure shows the cross section of the ladder.

Table 9
The material budget of the silicon ladder. TC-2810 is the thermally conductive glue. The radiation thickness of the HDI listed in the table is for production batches 1 and 2.

Item	Thickness mm	Radiation length X/X_0 %
Silicon Sensor	0.32	0.34
Silver epoxy	0.01	0.02
HDI	0.42	0.43
TC-2810	0.05	0.02
Stave	3.76	0.33
Total	4.56	1.14

rate 0.12 l/m, (3) natural convection at 20 °C room temperature, (4) 3 W total dissipation from the 52 FPHX chips. The chips in the middle of the ladder are hottest due to its shorter spacing between chips, but it is kept near room temperature. The temperature difference between the hottest spot and the cooling water is predicted to be $\Delta T = 5.1$ °C. The actual measurement of ΔT was well reproduced by this ANSYS simulation within 10%.

3.5. Material budget

Table 9 summarizes the material budget of the silicon ladder. The total thickness of the silicon pad area of the ladder is 4.57 mm and its effective radiation length X/X_0 is 1.14%. The largest contributions to the budget is the HDI ($X/X_0 = 0.43\%$), and the silicon and staves with radiation lengths $X/X_0 = 0.34\%$ and $X/X_0 = 0.33\%$, respectively.

The material budget of the HDI is largely governed by the copper layers. As tabulated in Table 5, there are 7 layers of 9 μm thick copper which total 63 μm. Furthermore, both top and bottom surface layers are plated with 15 μm thick copper.[3] While the simple stack up of these copper sheets results in 93 μm, the effective amount of copper in the signal layers is much less than solid ground layers.

Table 10 summarizes the effective copper thickness of each layer, which was estimated based on the residual copper fraction after the etching process of the HDI fabrication. The effective total thickness is estimated to be 44.7 μm, approximately 48% of the 93 μm total stack-up thickness, with corresponding radiation length $X/X_0 = 0.31\%$. The total thickness of polymide and glue layers is 325 μm with X/X_0 of

[3] The thickness of the copper plate was 20 μm only for the last production batch, which increases the radiation length of the third batch HDIs by $X/X_0 = 0.02\%$.

Table 10
The effective thickness of the HDI's copper layers.

Layer	Function	Residual copper fraction %	Effective thickness μm
1	Bias + AGND	71.3	17.1
2	AGND	93.5	8.42
3	Signal	6.5	0.59
4	Power	94.0	8.64
5	Signal	7.2	0.65
6	DGND	93.2	8.38
7	Bias+Signal	4.7	1.12
Total			44.7

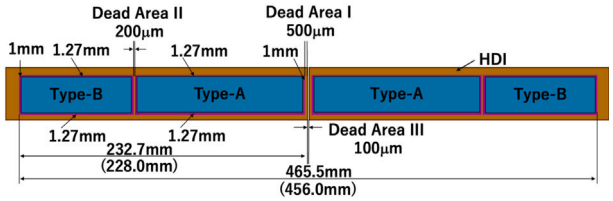

Fig. 13. Dead spaces of the INTT ladder. The number in parentheses is the longitudinal length of the active region of the type-A and B sensors altogether.

0.11%. The total radiation length of the HDI in the silicon pad area is thus 0.43%.

The silicon sensors were glued on the bias pads of the top layer of the HDI using electrically conductive silver epoxy, i.e. Henkel LOCTITE ABLESTIC 2902 adhesive. The average thickness of the epoxy was designed to be 9 μm based on the 50 μm thick glue mask, which has total of 295 glue potting holes with 2 mm diameter each. The radiation length of the silver epoxy was then calculated to be $X/X_0 = 0.02\%$ based on the mixing ratio of the silver powder and the epoxy of 0.21:0.79 [25]. Due to the short radiation length $X_0 = 8.54$ mm of the silver material, the contribution of the silver epoxy to the total material budget can be non-negligible. Without the glue mask, the contribution of the 50 μm thick silver epoxy is as significant as 12% of the total material budget.

To diffuse the heat generated by the FPHX chips, highly thermally conductive epoxy adhesive glue, 3M^{TM} TC-2810 [26], was used to assemble the HDI and the stave. The radiation length for the 50 μm thick the epoxy makes a very small contribution to the total material budget of the silicon ladder, unlike the silver compound one.

3.6. Dead area

Due to the precision limit of the silicon sensor alignment during the assembly process of the silicon sensors on the sensor pads of the HDI, there are small dead spaces between the edge of the type-A sensor and the tip of the HDI (Dead Area I), and also the type-A and type-B sensors (Dead Area II). They are 0.5 and 0.2 mm, respectively, as shown in Fig. 13.

As the result of the dead area in the silicon alignment, the total distance from the boundary of the two half ladders to the large rapidity end of the type-B sensor is 232.7 mm, while the length of the active region of type-A and type-B sensors is 228.0 mm as tabulated in Table 2. This results in 98% coverage of the active region in the longitudinal direction as summarized in Table 11. On the contrary, there is no additional dead space originating from the alignment in the transverse direction. The fraction of the active region in the transverse direction is thus 88.7% as tabulated in Table 12. The resulting fraction of the active area of the half ladder is 87.0% as tabulated in Table 13.

Lastly, there is another 0.1 mm of dead area between two half silicon ladders (Dead Area III in Fig. 13) originating from the alignment precision of the two half silicon modules on the stave. The resulting

Table 11
The dimensions of the dead area and region in the longitudinal direction of the half ladder.

Longitudinal	Physical	Active
Dead Area I	0.5 mm	0 mm
Type-A	130 mm	128 mm
Dead Area II	0.2 mm	0 mm
Type-B	102 mm	100 mm
Total	132.7 mm	228.0 mm
The fraction of longitudinal active length		98.0%

Table 12
The physical and active area of the half ladder.

Transverse	Physical	Active
Type-A & B	22.5 mm	19.968 mm
The fraction of transverse active length		88.7%

Table 13
The physical and active region of the half ladder.

	Physical	Active
Area	5235.75 mm^2	4552.70 mm^2
The fraction of active area		87.0%

physical length between the large rapidity end of the type-B sensors of two half ladders is 465.5 mm, while the total longitudinal length of the active regions of 4 silicon sensors is 456.0 mm. This dead area is relatively minor enough, the fraction of active area still stays as 98.0% in the longitudinal direction for the full ladder.

4. INTT readout cables and front end circuit board

Because the entire INTT barrel must fit within the inner diameter of the TPC detector [1], the signal from the barrel must be transmitted all the way to the outside of the TPC volume. The ROCs from the FVTX detector, which are downstream electronics for signal processing, cannot fit within the inner diameter of the TPC.

As introduced in the detector overview Section 2, raw data of up to 20.8 Gbit/s generated from each half ladder must be transmitted at high-speed to the ROC through a curved cable path for longer than 1 m. Because no commercial cable satisfies the requirements, a novel bus-extender cable was developed based on the FPC. This technology simultaneously satisfies the requirements of high-density signal lines, flexibility, and long cable length. In contrast, the specification of line and space of the bus extender prevented its connector-end design to be compatible with the input connector ports of the existing ROC. Therefore, another 15 to 25 cm conversion cable was developed to interconnect the bus extender to the ROC. Flexibility in three-dimensions for the conversion cable is required to guide the connection smoothly without introducing any stress at the ROC input connector. This is needed to absorb the geometrical mismatch of the downstream end of the bus extender and the corresponding input connector location of the ROC.

The schematics of the INTT silicon ladder and full readout cable chain up to the ROC is depicted in Fig. 14. The data of each half ladder is readout from the opposite side of the full ladder and processed by different ROCs.

4.1. Bus extender cable

Only key features of the bus extender (BEX) are described here, details of the BEX cable are discussed elsewhere [13]. This FPC cable comprises four layers of three flexible-copper-clad laminate (FCCL) as shown in Fig. 15. The top and third layers are for the digital and analog grounds, respectively. The second layer is used for signal lines. The bottom layer has the power supply lines for the FPHX chips. The choice of the four-layer structure, instead of the seven-layer structure of the HDI, is primarily driven by fabrication constraints. The yield rate is a big concern for the BEX. The main driver is the signal layer due to its required microfabrication accuracy over the extraordinary length of 1.11 m. Reducing the number of signal layers was chosen to minimize the risk in the fabrication process. All of the BEX signal lines were thus integrated into a single layer.

Table 14
Key specifications of dielectric materials of LCP (R-F705S) and polyimide (R-F775) employed for the BEX and the HDI, respectively. ϵ_r and $\tan\delta$ are values at 10 GHz for R-F775 and 1 GHz for R-F705S.

Material	LCP (R-F705S)	Polyimide (R-F775)
Dielectric constant ϵ_r	3.3	3.2
Dissipation factor $\tan\delta$	0.002	0.002
Water absorption	0.04%	0.9%

Table 15
Specifications of the BEX cable.

Item	Specification
Dimension	1.11 m × 34 mm
Width (connector region)	43 mm
Total thickness	398 μm
Dielectric material	LCP
Dielectric model	Panasonic FELIOS R-F705S [27]
Dielectric layer thickness	100 μm
Bonding sheet thickness	25 μm
Number of layers	4
Number of signal lines	122
Line and space	130 & 130 μm

The realistic limit of the line and space for the BEX were both found to be 130 μm to achieve a reasonable yield rate of ≈80% in the fabrication factory, which was Printed Denshi Kenkyusho Co., Ltd.. Given the line and space, the thickness of the dielectric material is required to be as thick as 100 μm to match the differential characteristic impedance of 100 Ω.

As mentioned above, the technical challenge is to transmit signals as high frequency of 200 Mbit/s to the electronics nearly 2 meters downstream with minimum insertion loss as possible. Any risk which can depend on environmental conditions should be avoided especially for the BEX due to its extraordinary long length. As the dielectric material, a liquid crystal polymer (LCP) was employed for the BEX, while the polyimide was employed for the HDI, as a popular choice for FPCs in industry. The FELIOS model R-F705S LCP from Panasonic Industry Co., Ltd. [27] was employed because it provides 100 μm thickness. The LCP has been known to be advanced in its low water absorption compared to the conventional polyimide products. It is known fact that the signal transmission loss gets worse once the polyimide absorb moisture and its get worse in higher frequency. The humidity in the experimental hall at RHIC can be increased above 60% during Summer period and thus this is the risk to be avoided for the BEX. Key specifications of dielectric materials of LCP (R-F705S) and polyimide (R-F775) [17] employed for the BEX and the HDI are tabulated in Table 14. Although the dielectric constant ϵ_r and the dissipation factor $\tan\delta$ are similar, the LCP shows an order of magnitude better performance in the water absorption.

For the bonding sheet, a specially optimized model for LCP was employed with thickness of 25 μm chosen for having a low dielectric constant. This was also a crucial choice to achieve decent yield rate in the through-holes plating process [13] by Taiyo Manufacturing Co., Ltd. because the fabrication technology for the LCP is not as well established as for the polymide. Table 15 summarizes the specifications of the BEX cable.

Pairs of DF18C-100DS-0.4V(81) receptacle connectors manufactured by Hirose Electric Co. Ltd. are implemented at both ends of the bus extender as shown in Fig. 16. The space between a pair of DF18

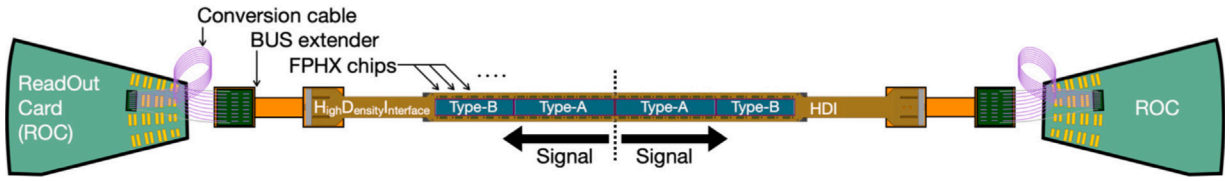

Fig. 14. The schematics of the INTT silicon ladder and full readout cable chain up to the ROC.

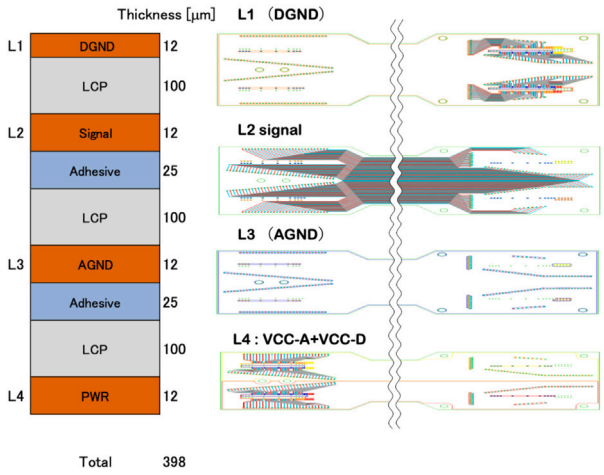

Fig. 15. Four layer structure of the BEX (left), and schematics of each conductive layer (right) from L1 to L4.

Fig. 16. A photograph of the 1.11 meter long BEX cable.

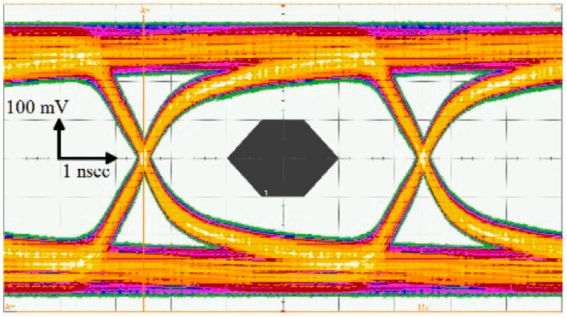

Fig. 17. The measured eye-diagram of the BEX as a result of transmitting 200 Mbit/s signals for 1 million times [13].

plugs is 26 mm which is incompatible with the 10 mm spacing of the input connector pair of the ROC. This extra spacing between the connector pairs of the BEX is caused by the difficulty to wire 122 signal lines of 130 μm line &space into the short connector spacing. Due to the incompatibility of the connector layout between the BEX and the ROC, a conversion cable was introduced from the BEX to the ROC spacing.

The bus extender successfully moderated the signal attenuation. However, the signal level is still questionable due to the extraordinarily long cable length as a multilayered FPC. The performance of signal transmission was evaluated with measurements using each of the following methods: (1) S-parameters, (2) eye-diagram, and (3) time-domain reflectometry (TDR). The resulting insertion loss measurement is presented in Section 4.3 and compared with these of other readout cables. The measured eye diagram is shown in Fig. 17. The waveform is confirmed to exhibit a sufficient margin to a defined mask[4] by observing 1 million waveforms of the 200 Mbit/s signal (see the solid hexagon in the middle of Fig. 17). The measured characteristic impedance was 90 Ω differential in the TDR measurement. This is 10% smaller than the default 100 Ω, it is confirmed to be permissible by the return loss measurement of the daisy chain with the conversion cable as discussed in Section 4.2.

4.2. Conversion cable

As discussed in previous sections, the FPC is the first choice of technology to satisfy the high-performance requirements of signal transmission, high signal-line density, and flexibility. However, it is difficult for the FPC to satisfy an additional and unique requirement: the flexibility in three dimensions to connect the downstream end of the BEX and the input connector ports of the ROC board without introducing any stress at the connection. If the FPC cable has directivity, then stress is induced at the connector end, which would bend the cable to the transverse direction of the cable plane.

A μ-coax technology was chosen. Although the signal line density cannot be as high as for the FPCs and the differential signal is split to two coaxial cables, the LVDS pairs of the INTT readout chain can be regarded as almost single-ended, as they are almost immune to electromagnetic effects between pairs. The coax cables thus does not introduce unique transit time and common mode effects among the readout cable series. Therefore, the three dimensional flexibility offers a good trade-off in the INTT readout design. According to an engineering study, due to its lack of flexibility the FPC solution would require as many as 14 different designs in curving and length to interconnect mismatching connector geometries between the BEX and input connectors of the ROC. Furthermore, spare cables of all designs would be needed for risk management, which leads to high cost inefficiency. The μ-coax solution reduces the number of designs to be only two in different lengths.

The CABLINE-UX II model manufactured by I-PEX Inc. [28] was employed as the last stage of the signal transmission cable chain for the INTT ladder. The AWG#44 harness is made of silver-plated copper alloy with a center conductor insulated by 30 μm thick perfluoroalkoxy alkane (PFA) dielectric material from tin-plated copper alloy with wire wrapping in the outer spiral shield. The shield is covered by

[4] Private communication with the FPHX chip developers.

Table 16
Specifications of the conversion cable. The characteristic impedance is given in differential of the LVDS pair.

Item	Specification
μ-coax make	I-PEX Inc.
μ-coax model	CABLINE-UX II [28]
Harness AWG	44
Characteristic impedance	90 Ω
Number of harness per bundle	50
Number of bundle	3
Power/ground cable AWG	24
Number of power cable	2
Number of ground cable	2
Length	15 & 25 cm

the outermost jacket made of the PFA, as well forming a four-layered coaxial cable with total thickness of 0.24 ± 0.01 mm. The characteristic impedance of the harness is 45 Ω (90 differential for a LVDS pair). A slim plug and small connectors are assembled for both ends of the harnesses to bundle 50 harnesses in the wire spacing with 0.25 mm pitch. Finally, the harness bundle is wrapped by an acetate cloth adhesive tape (see Fig. 18).

The conversion cable interconnecting between the BEX and ROC comprises three μ-coax bundles, two power and two ground cables, and the PC boards in both ends. The AWG#24 power and ground cables in both ends are assembled with HJ-3 male pins manufactured by MAC EIGHT Co. Ltd.. The male pin and the receptacle connection are secured by the HH-3-R lock. The wire gauge is optimized to be AWG#24 to drop the voltage properly and to provide the FPHX chip power from the slightly higher regulator voltage output at the ROC. Details of the voltage drop is discussed in Section 4.4.

Three UX II receptacles and four HH-3-G sockets (manufactured by MAC EIGHT Co. Ltd.) are implemented on the top side of the PC board and two DF18C-100DS-0.4V(81) receptacle connectors are implemented on the bottom side of the board. The PC board is fabricated by Hayashi-REPIC Co. Ltd. and eight layered with dedicated layers for the digital and the analog-power and ground. The dimensions are 48 mm wide × 52 mm long for the BEX end to match the size of the connector end, while the ROC side is rather compact with dimensions 25 mm wide × 25 mm long. There are two types of conversion cables namely "type-AC" and "type-BD". The channel map of the type-BD is arranged to be the mirror image of the type-AC in the ROC side to be compatible with the input ports of the columns A&C and B&D of the ROC, specially designed for the FVTX detector [11]. There are two different lengths of harnesses for the power and ground cables, which are 15 and 25 cm, respectively. Specifications of the conversion cable are summarized in Table 16.

4.3. Signal transmission performance

As discussed in Section 2, the absolute limit of the total signal transmission loss is −12 dB at the LVDS driving current of 2 mA. This limit is the LVDS driving current dependent. It is ideal to operate the FPHX with the lowest 1 mA LVDS driving current to minimize heat generation. However, it requires transmission loss of better than −3.6 dB (30%) which is not feasible to achieve due to the limited space to run the cables.

The measured insertion loss for the 40 cm HDI,[5] the 1.11 m BEX, and a 20 cm CC[6] are compared in Fig. 19. Although the BEX is longest among these three cables, the HDI showed the largest insertion loss. The conversion cable showed the modest insertion loss. This ordering is qualitatively understood by the combination of the length of the cable and the resistive loss.

[5] The result of the HDI is actually the measurement of the prototype of the FPC version of the conversion cable, which has exactly the same line & space, 7-layer structure, materials, and length with the HDI.

[6] The model of μ-coax harness for this measurement was XSL series of KEL co.. Although it is different model and make, but it is the same AWG#44 and the signal transmission performance is similar to the CABLINE-UX II model of I-PEX.

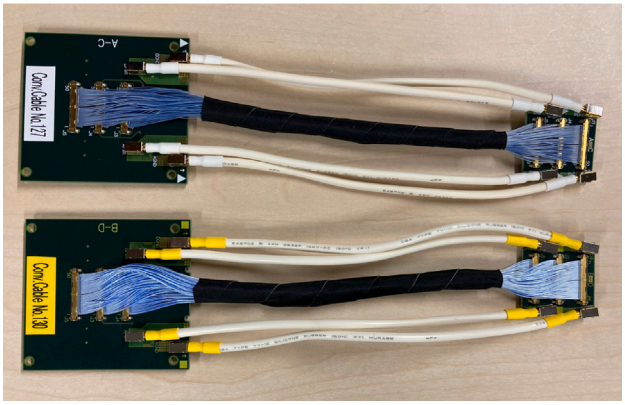

Fig. 18. Conversion cable type-AC (top) type-BD (bottom). The bundles in the middle of the cable are 15 cm length μ-coax harnesses with four white jacket cables for the power and ground cables. The larger PC board is the connector for the BEX side and the smaller board is for the ROC side.

Table 17
Numerical insertion losses of the HDI, the BEX, the CC, and the total at frequencies of 100, and 500 MHz.

Frequency [MHz]	HDI [dB]	BEX [dB]	CC [dB]	total [dB]
100	−2.07	−2.53	−0.07	−6.02
500	−5.26	−4.31	−1.67	−11.24

The total insertion loss of these three cables in series was calculated by adding up each individual insertion loss. The insertion losses of each cables are numerically tabulated in Table 17 for frequencies at 100 and 500 MHz. As shown in the black curve, the total insertion loss is achieved to be moderate than the allowance limit of −12 dB at 500 MHz, which was estimated in Section 2. The 500 MHz is the knee frequency and thus this corresponds to the safety factor of five or larger counting from the Nyquist frequency of 100 MHz. As described in Section 3.2, the LVDS driving current can be operated up to 8 mA which leaves enough room to extend the safety factor larger than 10 as the trade off of more power consumption. Considering the observed total insertion loss performance, long-term stable operation of the INTT ladder can be ensured with the LVDS current of $4 \sim 6$ mA, which provides factor of 3 to 4 larger amplitude than that of 1 mA.

More details of the s-Parameter measurements of the BEX cable are discussed in else where [13].

4.4. ROC

The readout card (ROC) is a multilayered circuit board implemented outside of the TPC volume. The ROCs were refurbished after the FVTX operation in the PHENIX experiment and reused for the INTT. ROC details are described elsewhere [11]. Any aspects of ROC usage that are different from the FVTX or customized for sPHENIX are discussed below.

Twelve pairs of DF18C-100DP-0.4V(51) plug connectors and four pairs of DF18C-60DP-0.4V(51) are implemented in the ROC as input ports for a half ladder. The DF18C-60DP-0.4V(51) plug connector has 60 pins and is not used for the INTT.

The ROC boards are originally implemented with 2.5 V regulators to provide analog and digital power for the FPHX chips with an operating voltage of 2.5 V for both analog and digital [8–10]. The voltage drop in the power-transfer line was smaller in the FVTX owing to the short

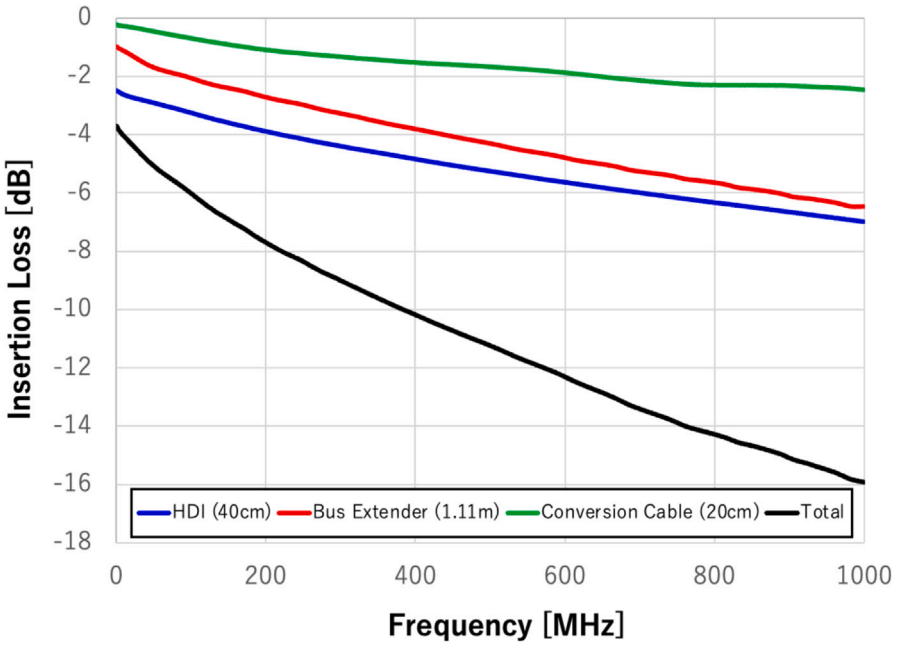

Fig. 19. Insertion loss performance for readout cables as a function of the frequency up to 1 GHz. Curves are the performance of the HDI(blue), the BEX(red), the CC(green), and total(black), respectively.

readout-cable length and low power consumption of the FPHX chip. On the contrary, as discussed in Section 4.3, the INTT operates in the higher-power consumption mode by 30 ∼ 40% to keep the signal amplitude above the driver threshold by operating higher LVDS current of 4 ∼ 6 mA.

The maximum drawing current per half ladder (26 FPHX chips) for the analog and digital power of the FPHX chips is measured to be 0.21 and 0.42 A, respectively. Although the ROCs are designed to allocate reasonably large physical cross sections or american wire gauge (AWG) for the power transmission lines, the resistances of these cables is a few hundred mΩ. The resulting voltage drop of the daisy chain of the readout cables amounts to as much as 0.2 to 0.4 V which is sizable enough for the FPHX chips to possibly malfunction due to insufficient voltage supply.

To compensate for the voltage drop, the surface mounted regulators for the FPHX power are upgraded to supply larger output voltages. The pin layouts of the upgraded regulators match the pad pattern of the ROC. Newly implemented regulators are MCP1700-2802E/TT and MCP1726-3002E/MF (Microchip Technology Inc.) with outputs of 2.8 and 3.0 V for analog and digital power, respectively. With drawing currents increased for higher voltage outputs, the supplied voltages at the FPHX location are calculated to be ≈ 2.5 to 2.6 V for both analog and digital. At a slightly higher than design operation voltage, the chip will not be damaged within the range of ± 10% of 2.5 V.[7]

5. Radiation hardness

In the INTT readout system (see Section 4), there are a few materials for which radiation hardness is either not known or known to be not durable. In this section, the radiation hardness is evaluated for these items. Also discussed is the study of the potential radiation damage of the ROC boards during the preceding PHENIX operation.

5.1. Bus extender

The FPC with standard polymide is widely used in radiation environments and its radiation hardness is well established. However, because LCP is a relatively new material being used for the dielectric layer of the FPC, the radiation hardness of the FPC with LCP has not been established as well as that of the polymide. The radiation hardness of the LCP material itself is proven to be as durable as polymide [29] although, the radiation hardness of the bonding sheet employed for the BEX was not known. The overall mechanical characteristics of the BEX after assembly was measured before and after a radiation exposure rather than investigating the radiation hardness of the bonding sheet itself. The primary concerns are the degradation in the flexibility of the BEX and the peel strength of the bonding sheet due to radiation damage.

A few samples of the BEX cable were exposed to ^{60}Co source for 7.2 kGy, 685 kGy, 1.45 MGy at National Institutes for Quantum Science and Technology, Japan. The expected radiation dose at the location where the BEX is installed in sPHENIX is approximately 5 kGy for five years operation.[8] The mechanical performances were evaluated by the following two tests: (1) stress test to evaluate the flexibility, and (2) peel strength test between the copper and the LCP layers [13]. As the test item (1), the Young's modulus was measured for the samples before and after the radiation exposure. Fig. 20 shows the Young's modulus of these samples based on natural frequency measurements. No degradation of flexibility was observed within the accuracy of the measurements (7%) in any samples. The error was estimated by the standard deviation of multiple samples within the same radiation dose group.

For test item (2), approximately 50% and 70% degradations were observed in the peel strength for 685 kGy and 1.45 MGy samples, respectively as shown in Fig. 21. However, the measured peel strength of 18 N/cm for the 7.2 kGy sample proved to be sufficiently strong

[7] private communication with FPHX developers

[8] Including an extra two years of operation beyond the officially approved three years.

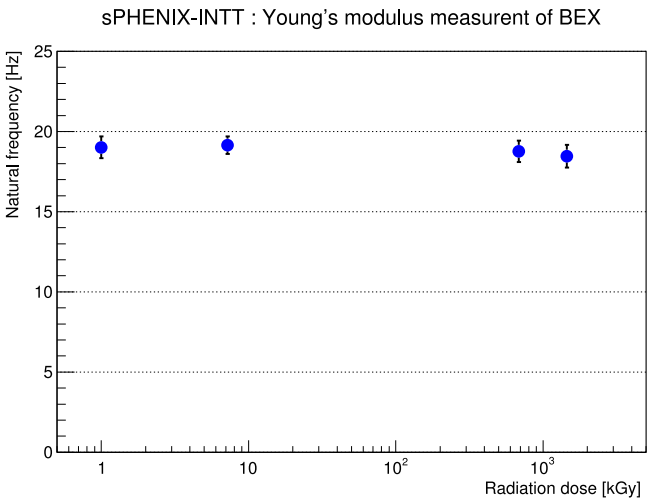

Fig. 20. The Young's modulus measurement results of samples exposed to various radiation dose. The vertical axis is the natural frequency in the unit of Hz, while the horizontal axis is the radiation dose in the unit of kGy. The measurement of the sample with no radiation exposure is plotted purposely at 1 kGy.

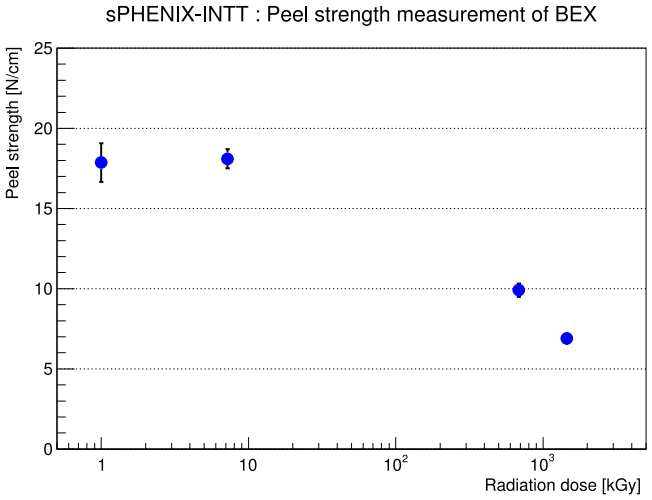

Fig. 21. The peel strength measurement results of samples exposed to various radiation doses. The vertical axis is the peel strength in units of N/cm, while the horizontal axis is radiation dose in units of kGy. The measurement of the sample with no radiation exposure is plotted at 1 kGy on purpose.

and is similar to the typical level of polymide-based FPC. Although the safety margin to keep this peel strength for possible unexpected extra radiation dose may be marginal, it is unlikely that FCCL layers would fall apart by gravity even if the peel strength were weakened by 50%. It was thus concluded that the radiation hardness of the BEX is expected to be durable for the duration of sPHENIX operation.

5.2. Conversion cable

The material "fluorinated resin", which is used as a dielectric insulator for the μ-coax cable [28], is reported to be weak against radiation [29] compared to popular dielectric insulator materials like polyimide or LCP. The estimated equivalent neutrons at the location of conversion cables to be installed is $0.15{\times}10^{12}$ for three years of sPHENIX operation.

In order to address the radiation hardness of the μ-coax harness for three years of sPHENIX operation, the effect of radiation was studied at the RIKEN Accelerator-driven compact neutron systems facility (RANS), Japan. Three samples of harness bundle were exposed to the RANS neutron beam at energies up to 5 MeV. Each sample was exposed to 1.3, 2.6, and 4.0×10^{12} equivalent neutrons. These are factors of 9, 17, and 27, respectively, more than the estimated radiation dose for the INTT operation in sPHENIX. The signal transmission performances were compared before and after the irradiation to evaluate the radiation effect. The comparisons were made for the S-parameters, the eye diagrams, and the TDR. No degradation was observed for all samples in any of these measurements, regardless of the exposed radiation dose. Thus, it is reasonable to conclude that the radiation hardness of the conversion cable is durable for the INTT operation as well.

5.3. ROC

The radiation dose of the ROC boards throughout five years of operation of the FVTX detector in PHENIX is estimated to have been approximately 300 Gy, while the corresponding radiation dose for three years of the INTT operation in sPHENIX is estimated to be approximately 50 Gy. The dose for the INTT is moderate owing to the relatively farther distance of the ROC position from the collision point compared to that of the FVTX in PHENIX. Here the radiation hardness of the ROC board is evaluated with respect to the total dose of 350 Gy.

The ROC board is designed to be radiation hard and in fact it utilizes the FLASH-based ACTEL ProASIC3E FPGAs [11] which is known to be radiation hard. The optical data transmission system of the ROC board comprises the model TLK2711 (Texas Instruments) as the serializer/deserializer of data. There is a study of the radiation tolerance of the TLK2711 [30]. In this study, the increase of leakage current and the bit-error rate was monitored as a function of radiation dose. The first bit error appeared ≈280–420 Gy and the TLK2711 encountered functional failure as low as 700 Gy depending on the beam condition of the radiation exposure, e.g., high (low) intensity and short (long) duration. While the leakage current stays the same up to 400 Gy, a rather rapid increase of current was observed beyond that point.

According to the above study, the condition of the TLK2711 are already in the range that some bit error symptoms may start after FVTX usage. Although it was preferable to replace them all before the reuse for the INTT, the model was discontinued. Unfortunately, insufficient quantities were available in the market place to replace them all. Hence, the replacement candidates are prioritized and limited to only those which already have bit-error symptoms. The only ROCs installed are those which passed the various function tests including no bit-error symptoms.

6. Summary

A new silicon-strip detector was developed for the sPHENIX experiment at RHIC. The silicon ladder consisted of silicon-strip sensors, FPHX chips, HDIs, and a high thermally conductive carbon-fiber stave. The ladder was designed to be as thin as $X/X_0 = 1.14\%$. The bus extender and the conversion cables were developed to transmit signals from the ladder to the ROC board. The 1.11 m long bus extender cable employs the novel low water absorption LCP as the dielectric material of the FPC. The conversion cable employs μ-coaxial harnesses to secure flexibility in three dimensions in order to connect the bus extender end to the input/output ports of the ROC board without introducing any stress at the connection.

The result of the study indicated that both the bus extender and the conversion cables are sufficiently radiation hard against estimated radiation dose for three years of the INTT operation in the sPHENIX experiment. In contrast, the exposed dose for TLK2711 chips of the ROC board throughout five years of the FVTX operation in the PHENIX experiment caused some bit errors to start to appear. Any chips showing these symptoms were replaced with new chips. The ROCs are installed relatively far away from the collision point for INTT operation in

sPHENIX as opposed to FVTX in PHENIX. Thus, the radiation dose for the ROC boards in three years of INTT operation in sPHENIX is estimated to be relatively moderate, i.e. 1/6 of that of the FVTX in PHENIX.

CRediT authorship contribution statement

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Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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