Development of a Solid State Transformer for HEMP/GMD Common Mode Current Mitigation

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***Abstract*—A high-altitude electromagnetic pulse (HEMP) or other geomagnetic disturbance (GMD) has the potential to severely impact the operation of electric power grids by introducing low-frequency common-mode (CM) currents. These currents, which flow through grounded power transformers, can lead to magnetic saturation in the transformer core and significantly deteriorate their performance. In this work, a solid-state transformer (SST) that can replace susceptible equipment and improve grid resilience to these threats is developed. An overview of the power electronics and controls architecture required to enable this protection is provided, and the details of a prototype SST hardware design are described. Finally, the performance of the SST is evaluated in both steady-state and in response to a CM insult. The SST is shown to be able to successfully respond to this insult, and future research will focus on how the SST can be deployed in the grid to maximize overall resilience.**

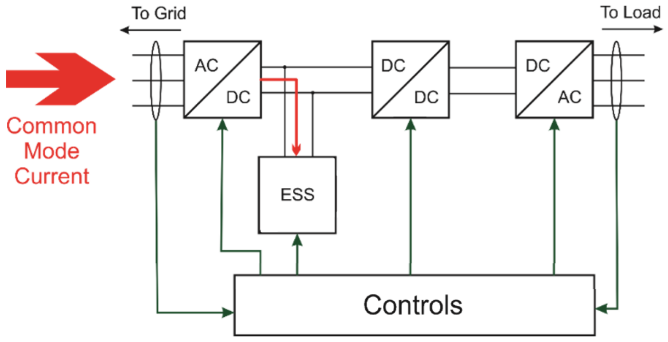
***Index Terms*—solid-state transformer (SST), high-altitude electromagnetic pulse (HEMP), geomagnetic disturbance (GMD)**

I. Introduction

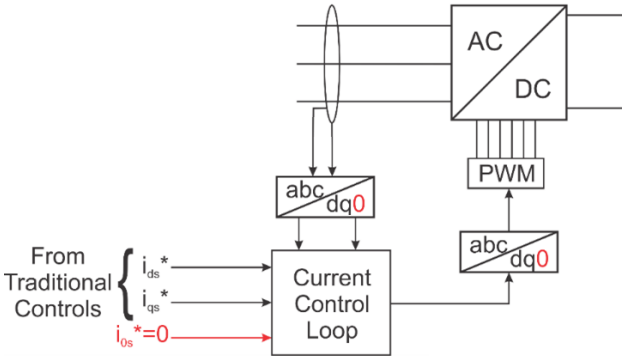
Today's electric power grid is susceptible to the effects of both man-made and naturally occurring geomagnetic disturbances (GMDs), such as from a high altitude electromagnetic pulse (HEMP), or from space weather [1], [2]. One way these events can impact grids is by inducing low-frequency common-mode (CM) currents which couple to the grid through long transmission lines and return to earth through grounded power transformers. The geomagnetically induced currents (GICs) which result from these events can cause the magnetic cores of transformers to become saturated, leading to increased losses and the potential for transformer damage, cascading blackouts, and other system instabilities [2].

Several approaches for minimizing the impact of GICs on power system operation have been investigated, including: passive blocking devices [3], corrective line switching [4], and more recently active devices to disrupt GICs in the transformer neutral [5], [6]. At the same time, solid-state transformers (SSTs) have emerged as a technology to supplant conventional magnetic transformers with designs based on modern solid-state switching devices [7]. This research describes a unique SST which is designed to perform the conventional capabilities of a transformer while also mitigating the low-frequency CM insults that can result from a HEMP/GMD event [8], [9].

A schematic of the proposed SST is shown in Fig. 1a. It consists of a primary-side ac-dc converter, an energy storage system (ESS), an intermediate dc-dc converter, and a secondary-side dc-ac inverter. The SST is designed to control the power from the primary to the secondary, as well as control the flow of unintended low-frequency CM currents, as shown in Fig. 1b. In this design, the energy from the CM insult is directed to the on-board ESS, so that the nominal input/output behavior of the transformer remains unaffected during a HEMP/GMD event.



(a) SST architecture



(b) Controls used to regulate CM current

Fig. 1: SST designed to replace conventional magnetic transformers and enhance grid resiliency by neutralizing common-mode insults.

The remainder of this paper is organized as follows: in Section II, the power electronics and controls architecture of the proposed CM-resilient SST is described. In Section III, hardware testing of the SST in both steady-state and in

response to a CM insult is evaluated. Finally, in Section IV, conclusions and directions for future research on the application of this SST are outlined.

II. Solid State Transformer Design

A. Four-Leg Inverter

Traditionally, a three-phase, three-leg inverter is used in grid applications. This circuit enables control over the fundamental AC components of grid waveforms – D and Q in the DQ0 frame of reference [10]. However, it does not allow for full control over the zero-sequence component [11], which for current is defined as the average of the phases:

$$i_{cm} = i_0 = \frac{i_a + i_b + i_c}{3} \tag{1}$$

Since the proposed SST requires control of this component, a three-phase, four-leg architecture, whose fourth leg introduces an extra degree of freedom to control D, Q, and zero-sequence components was selected for this design [8], [9]. A schematic of the four-leg inverter is shown in Fig. 2. This includes the dc filter, four half-bridges, an ac filter, and a four-wire output connection with the fourth-wire tied to ground.

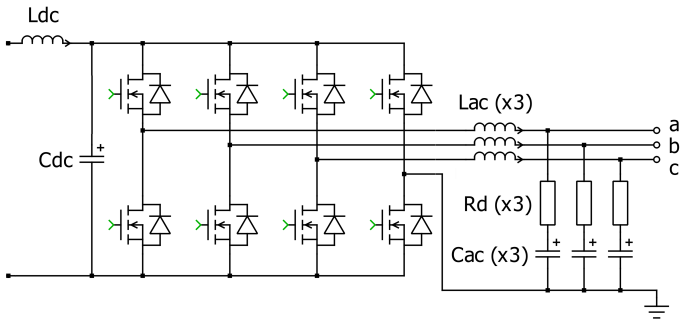
The design of the inverter was accomplished using standard power electronic design techniques. The ac filter was designed to have a cut-off frequency equal to the geometric-mean of the fundamental inverter frequency (60Hz) and the PWM switching frequency (40kHz). The dc capacitor was sized to limit ripple voltage to below 1%. The passive parameters for the inverter system are shown in Table I.

For the active components, four 1.2kV silicon carbide (SiC) half-bridge power modules [12] (CAB450M12XM3) were selected, along with compatible gate-drivers (CGD12HBXMP). The SiC MOSFETs enable higher voltage operation and faster-switching capabilities than conventional silicon MOSFETs and insulated-gate bipolar transistors (IGBT). A picture of the inverter hardware is shown in Fig. 2b.

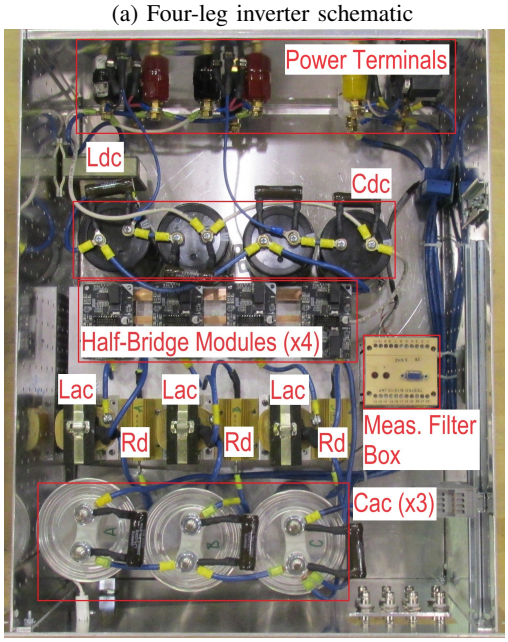
B. Dual Active Bridge & Energy Storage System

Besides the four-leg inverter, the SST also includes a dc-dc converter and an energy storage system (ESS). The dc-dc converter was selected to be a dual-active bridge (DAB), which provides galvanic isolation between the two-halves of the SST and enables the SST to have large step-up/down voltage ratios. The ESS in this prototype design is achieved by including additional capacitance on the dc ports of the DAB. However, in future development, the ESS may be replaced by alternative energy storage devices such as batteries, super capacitors, flywheels, etc.

On the hardware-design, a DAB consists of two full-bridge converters on either side of a high frequency transformer. A schematic of this is shown in Fig. 3a. The DAB operates by adjusting the relative-phase of the two full-bridges to control power flow through the transformer. DC capacitors on the input and output ensure the voltage at these terminals remains steady, which in this case were oversized to function as an effective ESS.



(a) Four-leg inverter schematic



(b) Picture of four-leg inverter hardware

Fig. 2: Four-leg inverter design

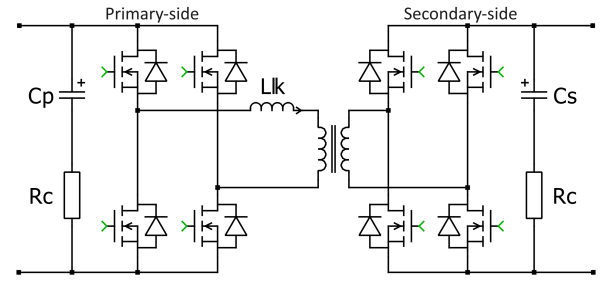
TABLE I: SST Parameters

Four-leg Inverter Parameters					DAB/ESS Parameters		
L_{dc} [mH]	C_{dc} [mF]	R_d [Ω]	L_{ac} [μH]	C_{ac} [μF]	C_p, C_s [mF]	R_c [Ω]	L_{lk} [μH]
1	1.8	2.5	380	53	5	0.01	20

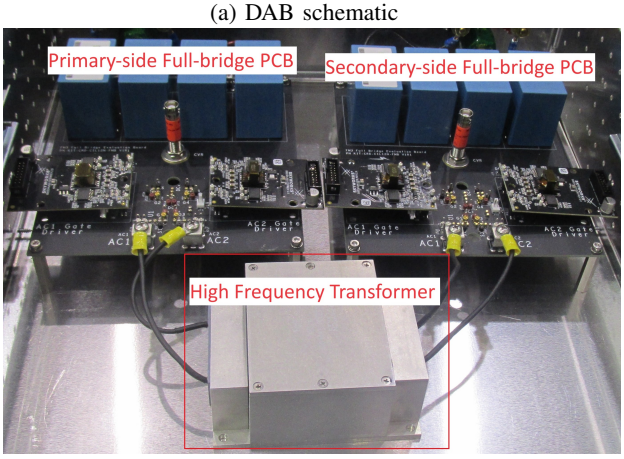
To be physically compact, the DAB must operate at a high frequency [13]. This design uses two 1.2kV SiC full-bridge power modules [12] (CBB032M12FM3) for the switching devices, and a planar transformer for the isolation stage [14]. The SiC MOSFETs were again selected for their high-voltage and high-frequency capabilities, and the transformer magnetic design uses ferrite 3C97 core material [15] also for high frequency operation. The transformer is rated for 100kHz and 10kW power. The parameters for the DAB, and ESS which whose capacitance is lumped with C_p and C_s, are provided in Table I. A picture of the DAB is shown in Fig. 3b.

C. Controls

The controls of the SST can be considered in two parts: 1) the ac/ac (i.e., dq) control behavior, and 2) the zero-



(a) DAB schematic



(b) Picture of DAB hardware

Fig. 3: Dual-active bridge (DAB) isolated dc/dc converter

sequence control behavior. Moving from the secondary-side to the primary-side of the SST, the ac/ac controls are configured such that the secondary-side dc-ac converter can act as either a grid forming (GFM) or grid-following (GFL) source. The DAB regulates a constant secondary voltage to feed this converter, and the primary-side ac-dc converter draws enough power into the SST via a d-axis current command to feed the DAB. This is accomplished using a PID regulator to ensure that in steady-state, the power entering/leaving the ESS is zero. This overall scheme illustrated in Fig. 4. For the zero-sequence control of the SST, the primary objective is to ensure that during a CM insult, the CM current is returned to zero as quickly as possible. Like the d- and q-axis current controls, the zero-sequence current is controlled via a PID regulator. The 3D-space vector modulation (3D-SVM) scheme described in [8], [16] is used to generate the switching signals for the inverters, and a phase-shift modulation scheme is used to control the DAB [17]. All control signals are generated on a real-time Speedgoat control computer [18], as shown in Fig. 9.

III. Experimental Testing

A prototype of the proposed SST has been developed to test the CM-resilient architecture in hardware. The hardware testing was performed on the Secure Scalable Microgrid Testbed (SSMTB) at Sandia National Laboratories, which includes three DC microgrid systems designed to operate at 400Vdc, and two AC microgrid systems designed to operate at 480Vac. The SSMTB also includes a central bus cabinet for connecting various components and microgrids, control computers, a data acquisition system, a graphical user interface for coordinated experiments, and a variety of AC and DC loads [19].

Multiple hardware experiments have been conducted to test the performance of the SST. First, component testing of the individual SST converters was conducted to validate their design. Secondly, a back-to-back test of the two four-leg converters was conducted to demonstrate how the SST responds to a simulated CM insult. Finally, a complete test of the assembled SST was conducted to ensure the nominal input/output behavior of the device. The results of these experimental tests are included in the following subsections.

A. Converter Testing

1) Four-leg inverter: The four-leg was the first component that was assembled and tested. The schematic of the inverter and picture of the assembled hardware is shown in Fig. 2. This converter was tested up to a dc voltage of 400Vdc. During these tests, the performance of the SiC power modules, ac filters, and the ability to control the D, Q, and zero-sequence components of the ac waveform were tested.

A oscilloscope plot of the inverter operating is shown in Fig. 5. This image shows the a-phase line-to-neutral voltage at the output of the inverter (V_{an}), as well as the a- and b-phase-leg midpoint voltages ($V_{a,mid}$ and $V_{b,mid}$ respectively). The fast rising- and falling-edges of the of the SiC MOSFETs leads to noise at the output of the converter, but overall the performance of the switching devices and ac filter behave as expected.

2) Dual-active bridge: Apart from the four-leg inverters, the dual-active bridge was also assembled and tested separately before integration with the full SST. A oscilloscope plot the DAB switching waveforms is shown in Fig. 6. This test was conducted with a dc voltage of 400Vdc applied on the primary-side, and a 12Ω resistor on the secondary side. The transformer primary-side voltage (V_{pri}) is shown in yellow, the secondary-side voltage (V_{sec}) is shown in blue, and the pink trace shows the current on the secondary-side of transformer (I_{sec}). In a DAB, the relative-delay between the primary- and secondary-side full-bridge converters determines the power flow across the high-frequency transformer [17]. In this case the time-delay test was set to a value of $t_d = 0.2\mu$sec, or 2% of the switching period. Overall, it was found that the DAB converter behaves as expected based on previous simulation results [8].

B. Back-to-Back Testing

In order to evaluate how the SST responds to a CM insult, a test was conducted which uses two inverters in a back-to-back configuration. A schematic of the test is shown in Fig. 7. In this test, the inverter on the left is operated open-loop as in Section III-A, and is used to model the grid with the step-change in CM voltage representing a simulated HEMP/GMD event. The inverter on the right belongs to the SST and the

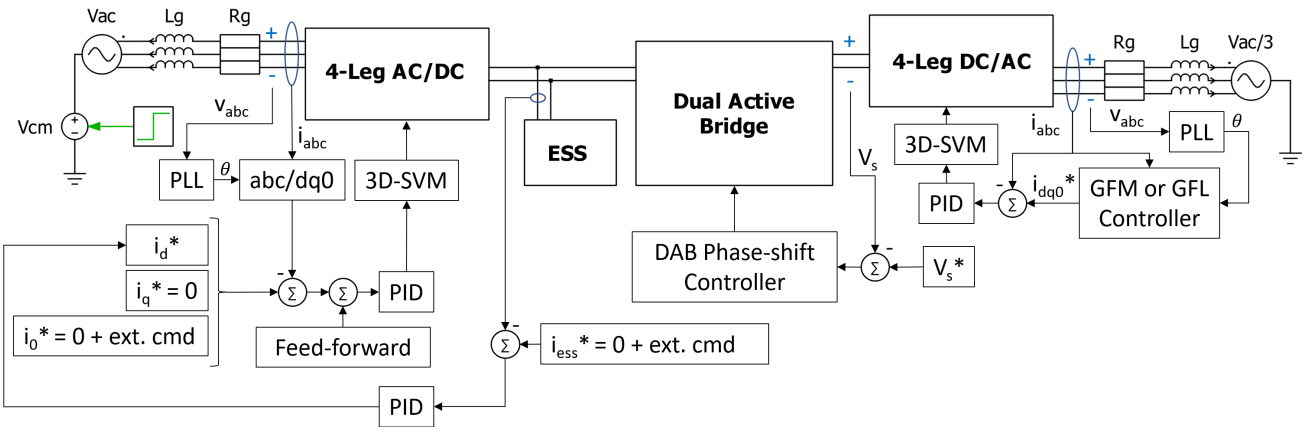


Fig. 4: SST control block diagram

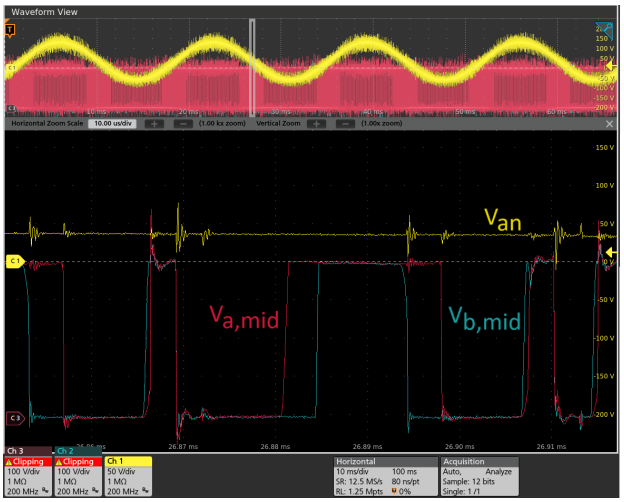


Fig. 5: Switching waveforms of the four-leg inverter

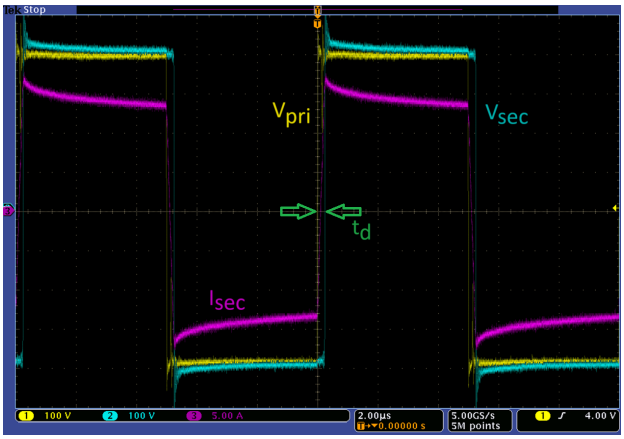


Fig. 6: Switching waveforms of the DAB

CM current entering the converter is controlled to zero using feedback controls as shown in Fig. 4.

The two converters are connected with an intermediate inductance to model a transmission line, with $L_{line} = 2.5mH$. Fig. 8 shows the simulation and hardware results for this test and in both cases the CM current is returned to zero after a brief transient. The slight discrepancy between the simulation and hardware results is likely attributable to parasitic losses/damping in the hardware setup that are not accounted for in the simulation.

C. Full SST Testing

For the final test of the proposed SST, the individual components assembled and a full system test was conducted. A picture of the SST in a 19-inch rack is shown in Fig. 9. For this test the primary-side of the SST was connected to a Pacific Power Source (MS series [20]) grid simulator and the the secondary side was connected to a resistor load bank. The results for the primary-side ac voltage and currents are shown in Fig. 10a, along with the primary-side DAB voltage (labeled v_{dc}). Similarly, the results for the secondary-side are shown in Fig. 10b. The ac waveforms are as expected and overall the SST is able to function as a isolated ac/ac transformer and deliver power from the primary to the secondary.

IV. Conclusion

This work presents the design and experimental testing of a SST that can respond to common-mode (CM) insults, such as those generated by a high altitude electromagnetic pulse (HEMP) or solar-geomagnetic disturbance (GMD). The power electronics and controls architecture of the proposed SST are described, and hardware results of a prototype SST are provided. The SST is shown to function as an effective ac/ac converter during normal operations, and respond successfully to mitigate CM current during a simulated CM insult. Future work on this topic will explore how the SST compares to a conventional magnetic transformer during a simulated HEMP/GMD event, and how the SST can be practically deployed in the grid to maximize overall system resilience to such threats.

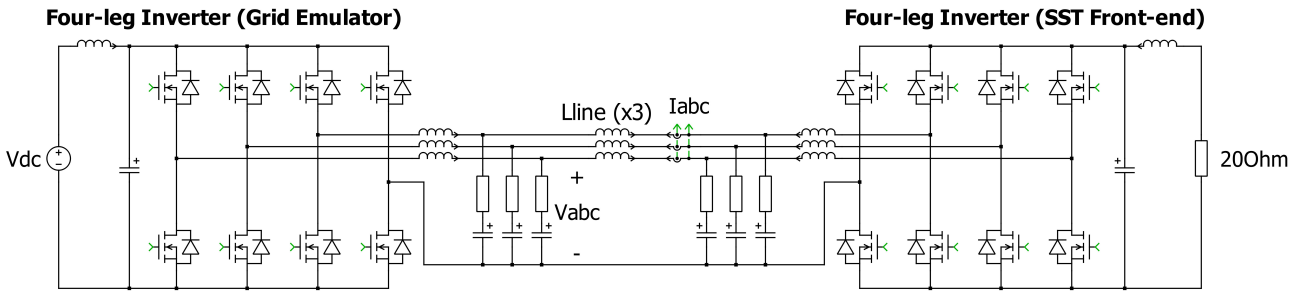
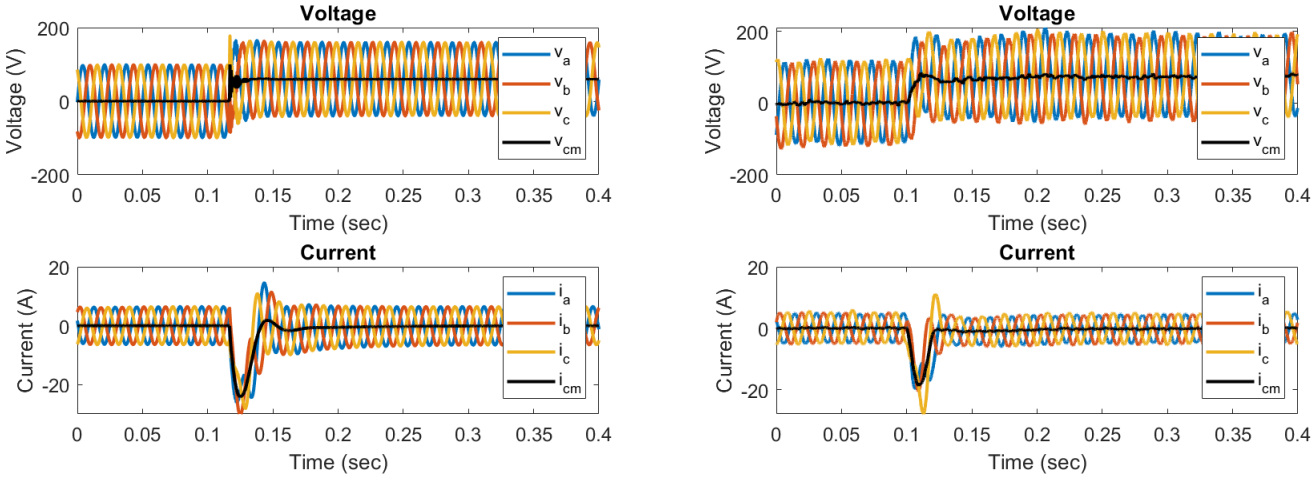


Fig. 7: Back-to-back converter test schematic



(a) Simulation

(b) Hardware

Fig. 8: Back-to-back testing of four-leg inverters, comparison of simulation and hardware results.

V. Acknowledgement

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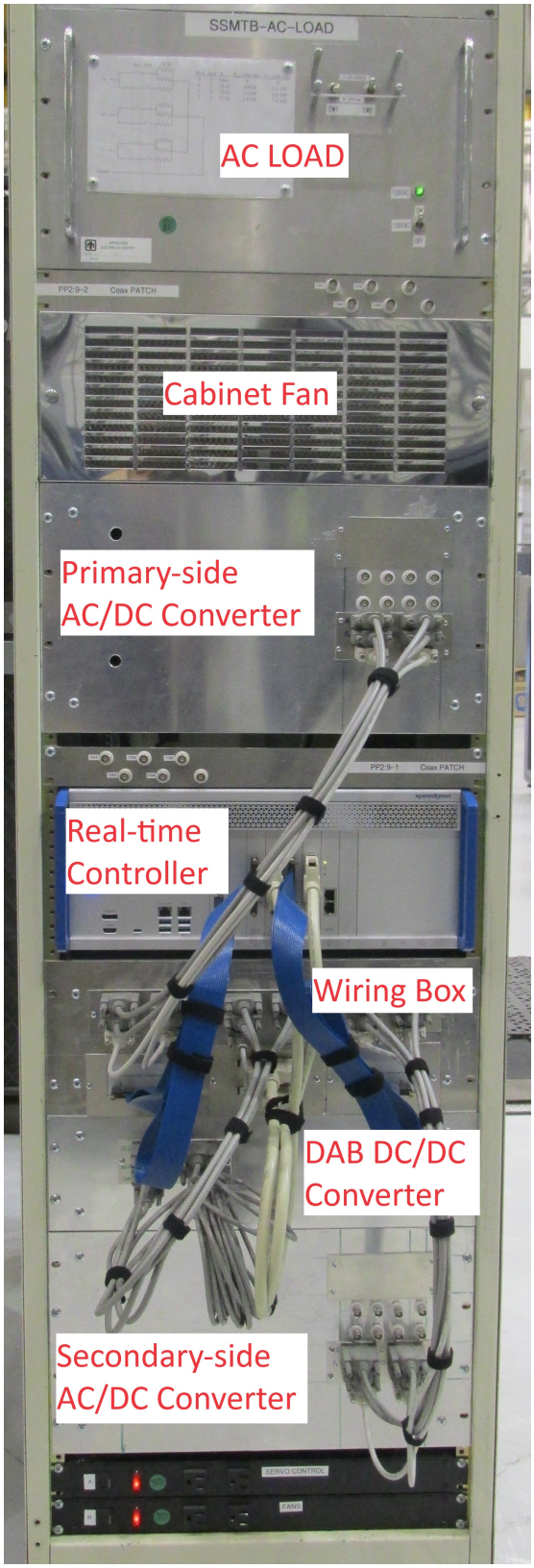
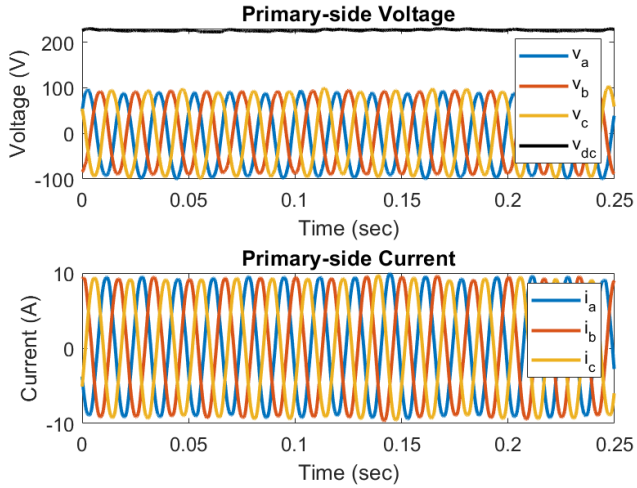
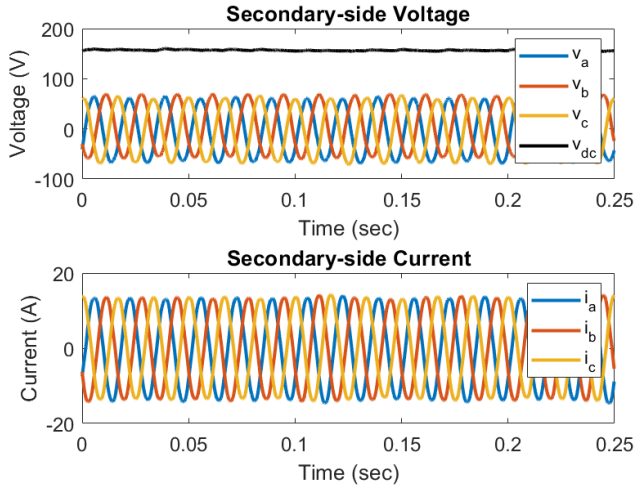


Fig. 9: Picture of SST hardware



(a) Primary-side waveforms



(b) Secondary-side waveforms

Fig. 10: SST nominal input/output waveforms

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