



Development of a Solid State Transformer for HEMP/GMD Common Mode Current Mitigation

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Outline



- Background
- Demonstration of HEMP/GMD on a conventional transformer
- Proposed SST for HEMP/GMD mitigation
- SST Design
 - Four-leg inverter
 - Dual active bridge
 - Controls scheme
- SST Testing
- Conclusion and future work

Background



The electric power grid plays a vital and growing role in society, and ensuring its reliable operation is essential from a national security standpoint

Unfortunately, high-altitude EMPs (HEMPs) and geomagnetic disturbances (GMDs) both present a potential high-impact risk to the grid

Induced currents → transformer half-cycle saturation

- increased losses, voltage degradation
- thermal damage, cascading failures, blackouts

No panacea currently available

- grid dispatch for small-medium scale events
- passive blocking devices for medium-large scale events
- no clear solution for extreme events (Carrington-level solar storm, high yield nuclear EMP)

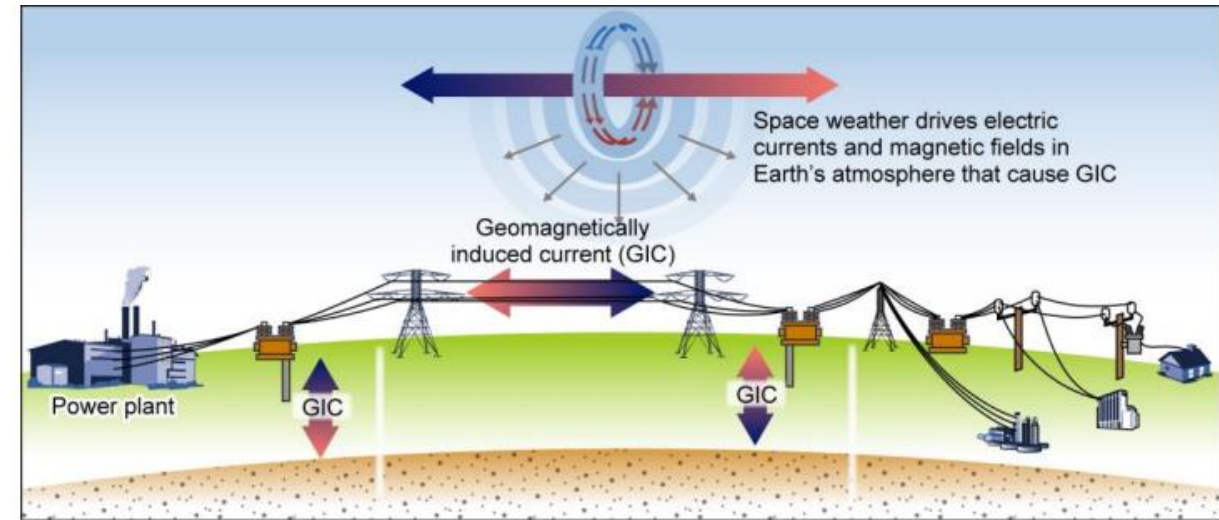
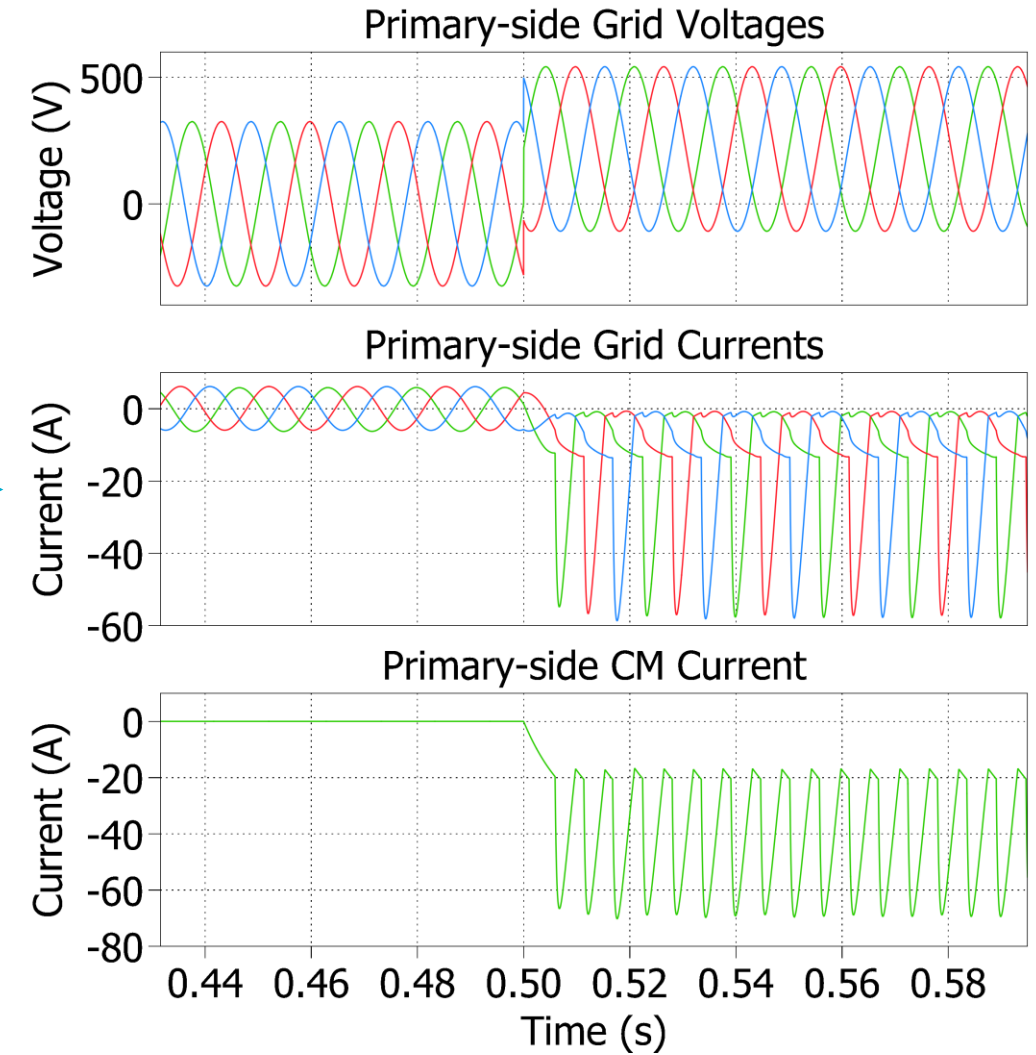
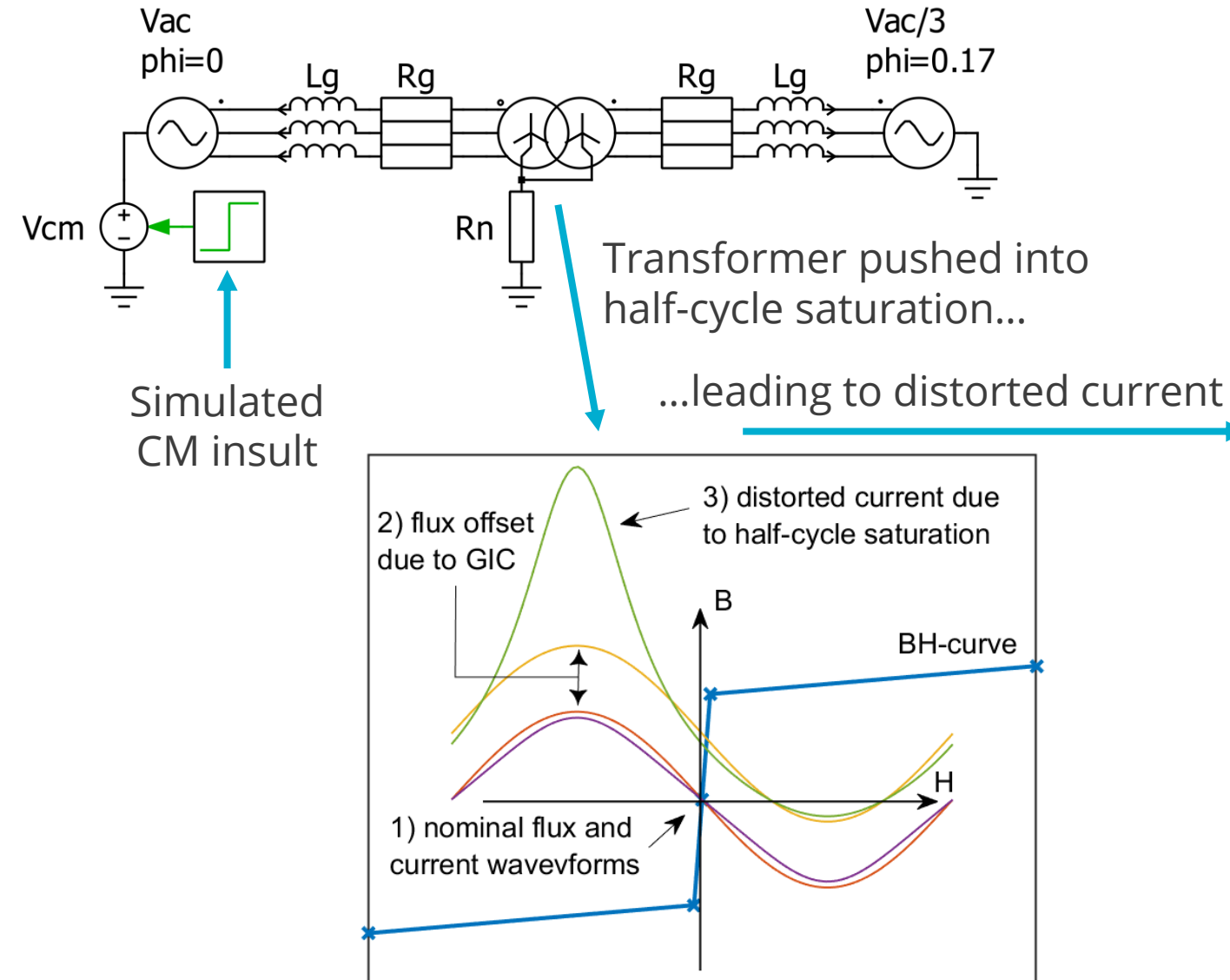


image credit: GAO-19-98

New approach/technologies needed to secure *critical infrastructure*

Conventional Transformer During HEMP/GMD

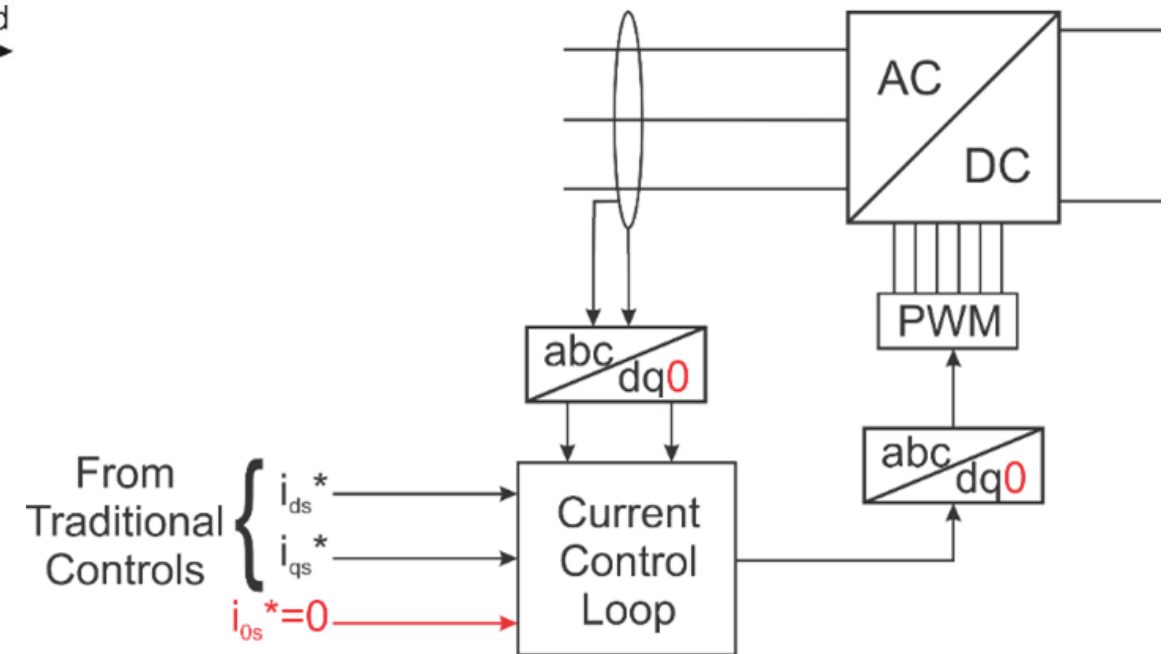
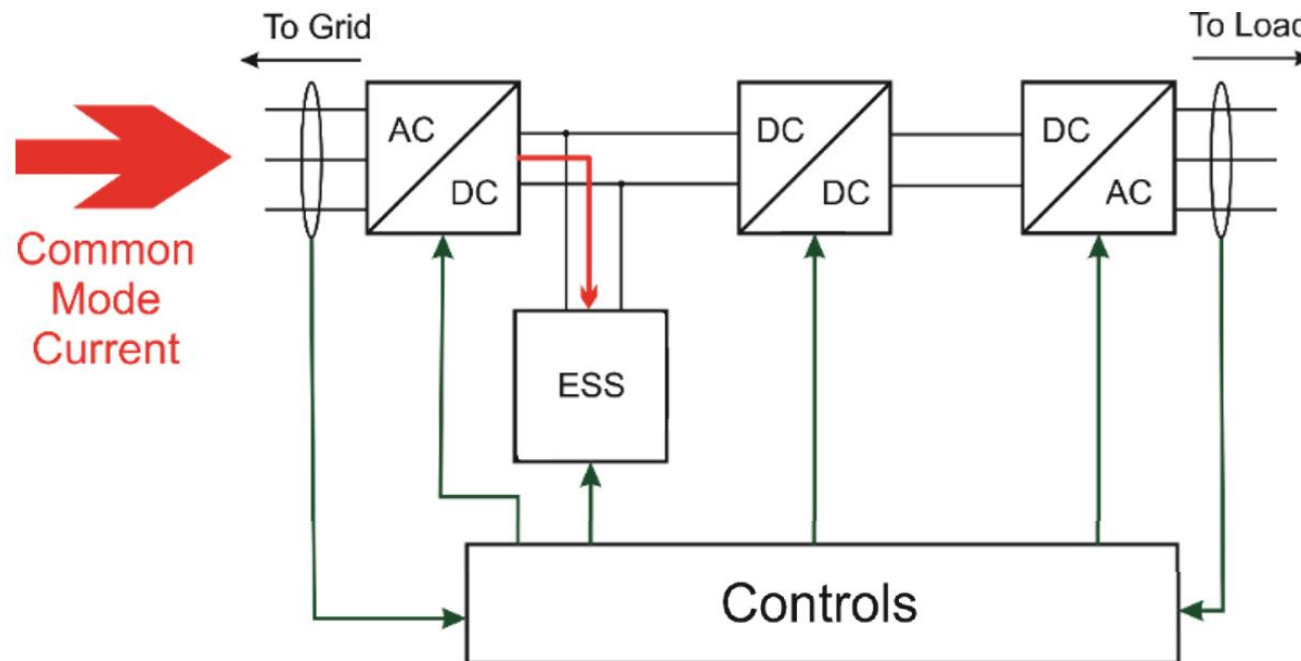


Solid-State Transformer for HEMP/GMD Mitigation



Approach is to design a solid state transformer (SST) which can replace/protect susceptible magnetic transformers

SST can absorb CM currents caused by a HEMP/GMD, without effecting power delivery



CM Solid State Transformer Design



Type-IV architecture selected to support dc energy storage and increased control flexibility [1]

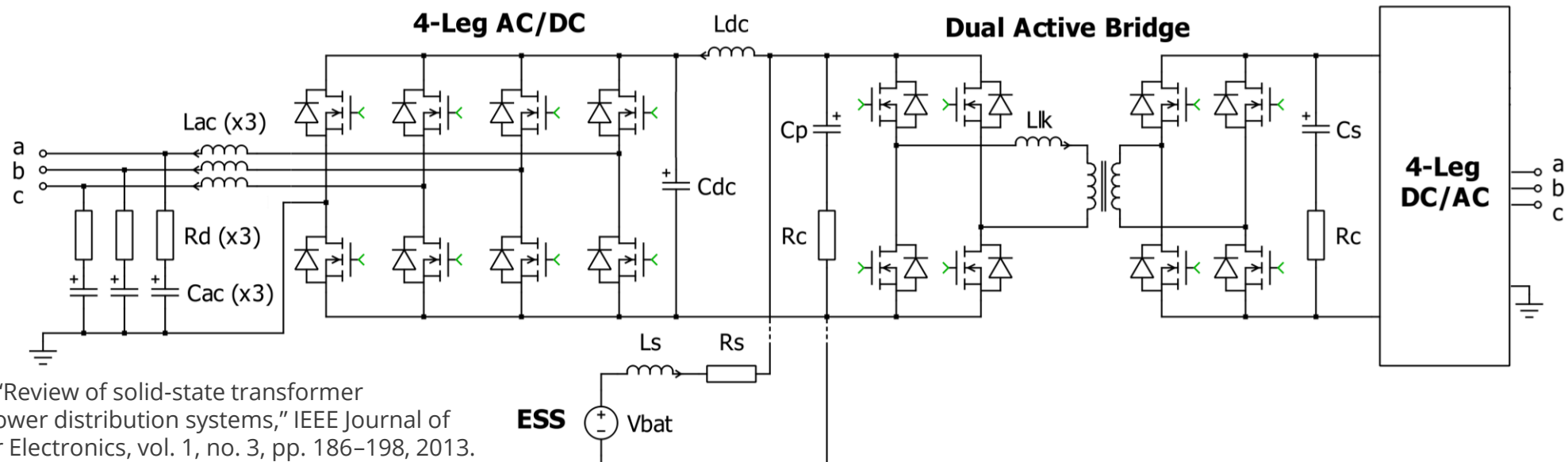
absorb CM insult from HEMP/GMD and prevent disturbance on secondary

4-leg inverter topology selected for input/output converters

enables control of d, q, **and** zero-sequence components

Dual-active bridge (DAB) selected for dc/dc converter

provides galvanic isolation and large step-up/down ratios



Four Leg Inverter



Specifications: 480Vac/120Vac, 10kW, respond to 0.5pu CM insult

3-D space-vector modulation (SVM) scheme required to control DQ0 [2,3]

Hardware designed for 800Vdc, 40kHz switching

DC parameters:

$$V_{dc} > 480 \sqrt{2}$$

$$V_{dc} = 800V$$

$$L_{dc} = 0.5mH$$

$$C_{dc} = 1.8mF$$

AC parameters:

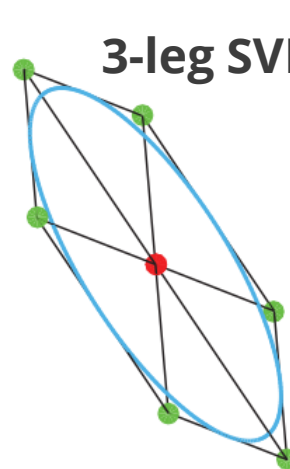
$$F_{sw} \sim 40kHz$$

$$f_c \approx \sqrt{60Hz * F_{sw}}$$

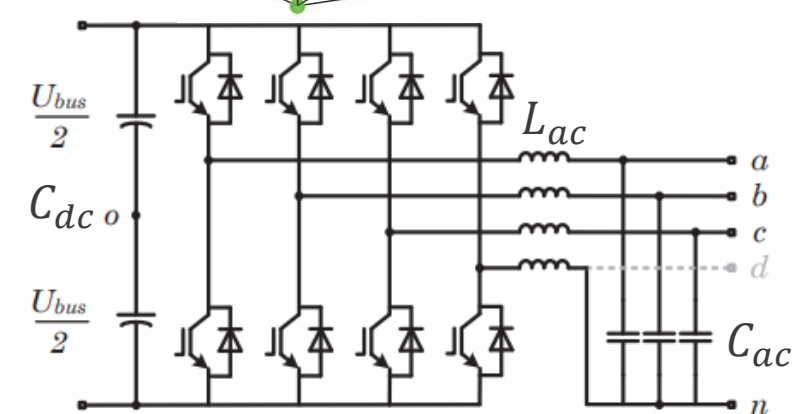
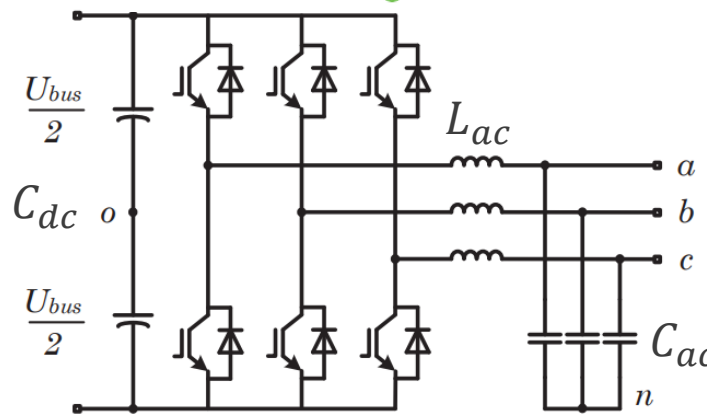
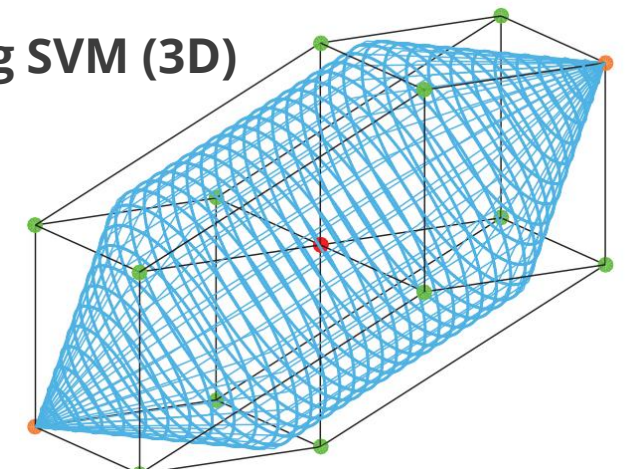
$$L_{ac} = 388\mu H$$

$$C_{ac} = 53\mu F$$

3-leg SVM (2D)



4-leg SVM (3D)



- [2] M. Perales, M. Prats, R. Portillo, J. Mora, J. Leon, and L. Franquelo, "Three-dimensional space vector modulation in abc coordinates for fourleg voltage source converters," IEEE Power Electronics Letters, vol. 1, no. 4, pp. 104–109, 2003.
- [3] Llonch, M., Heredero-Peris, D., Montesinos-Miracle, D., Rull, J. Understanding the three and four-leg inverter Space Vector. A: European Conference on Power Electronics and Applications. "EPE 2016: ECCE Europe, 18th European Conference on Power Electronics and Applications; Karlsruhe, Germany, 5-9 September, 2016". Karlsruhe: Institute of Electrical and Electronics Engineers (IEEE), 2016, p. 1-10

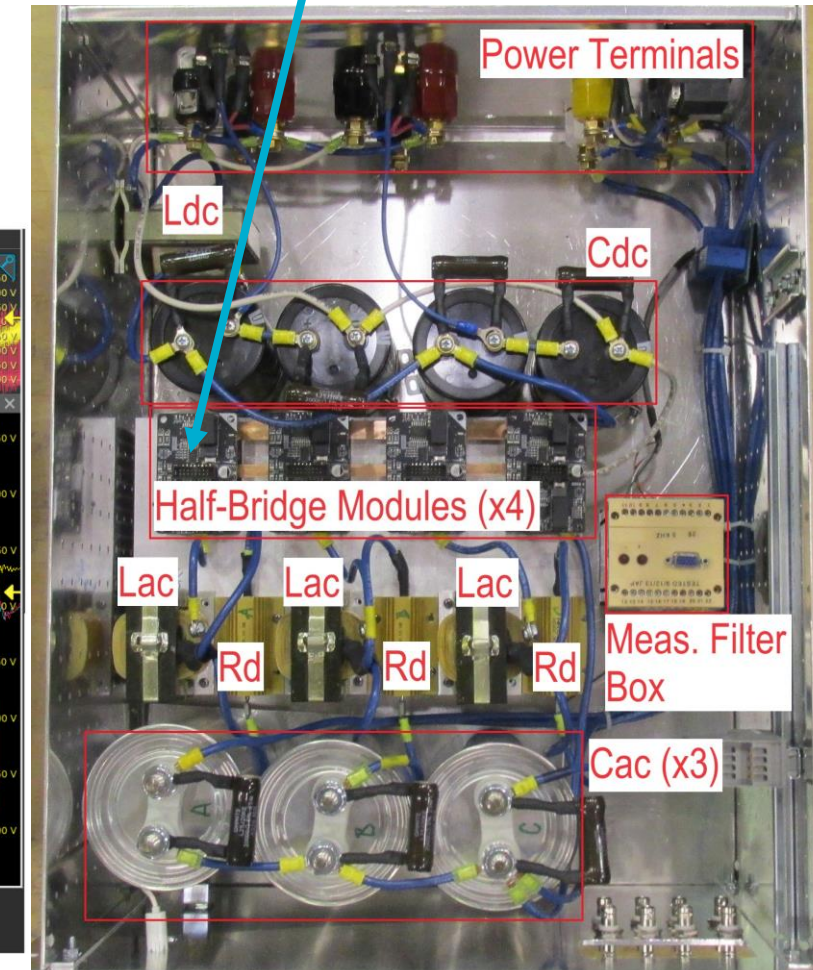
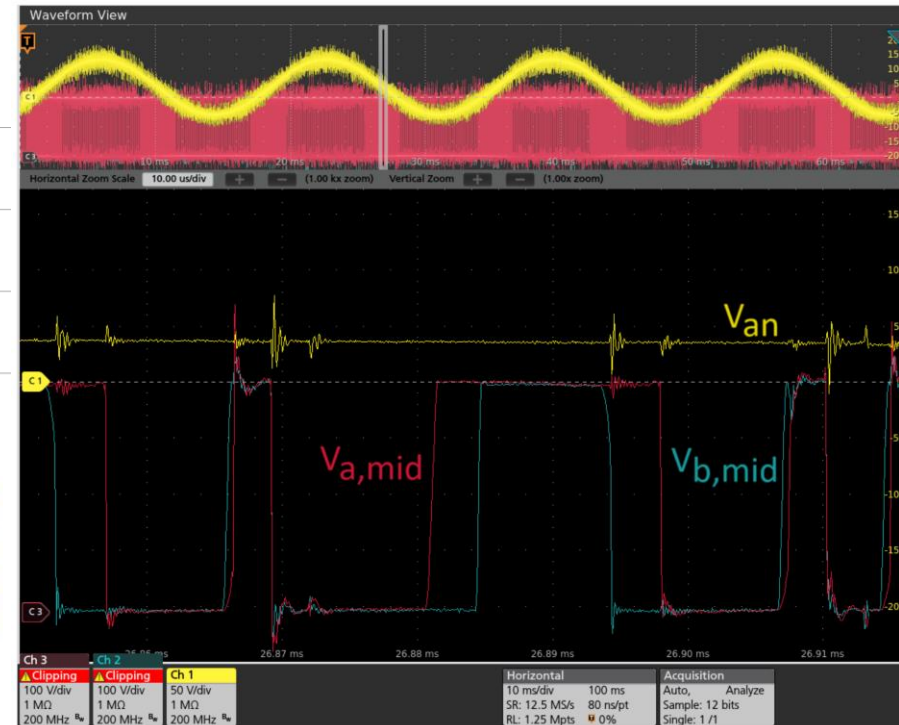
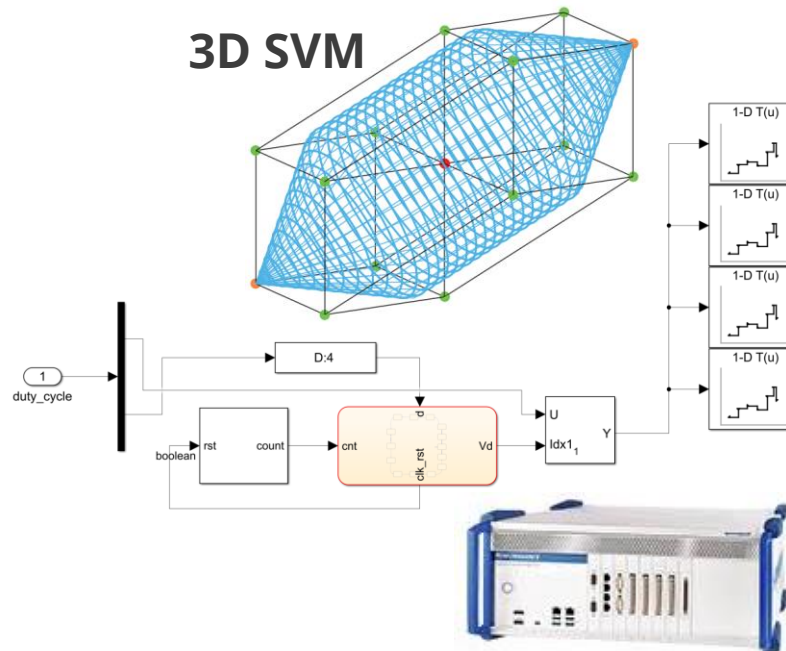
Four Leg Inverter (Continued)

Inverter design based around 1.2kV Silicon carbide (SiC) half-bridge power modules [4]

3D SVM implemented on Speedgoat FPGA module [5]

Standalone testing to ensure design meets specifications

Wolfspeed XM3
power module

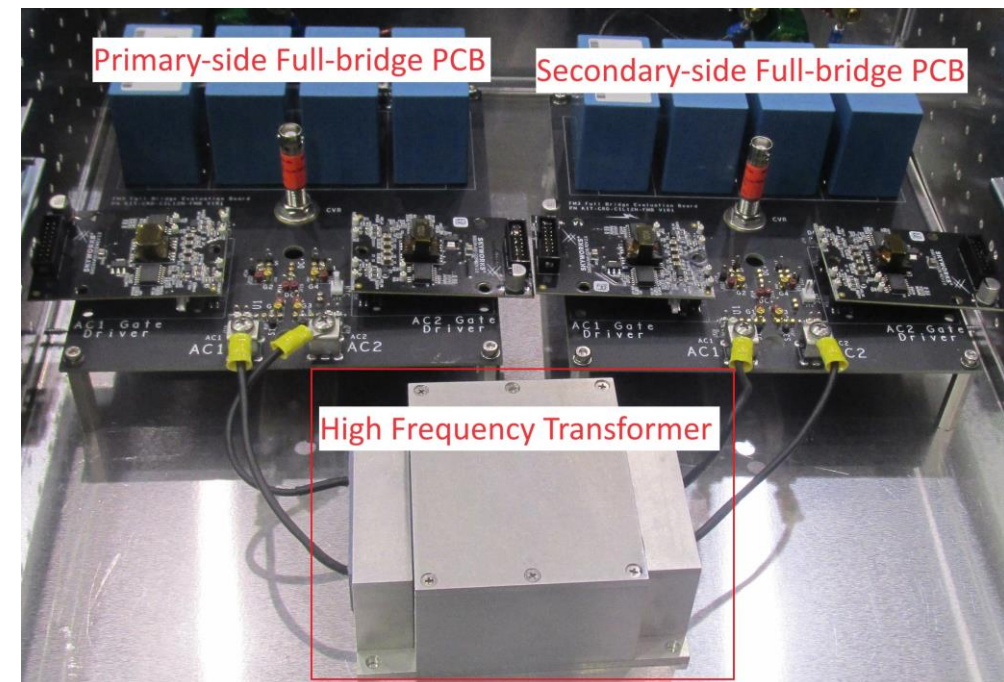
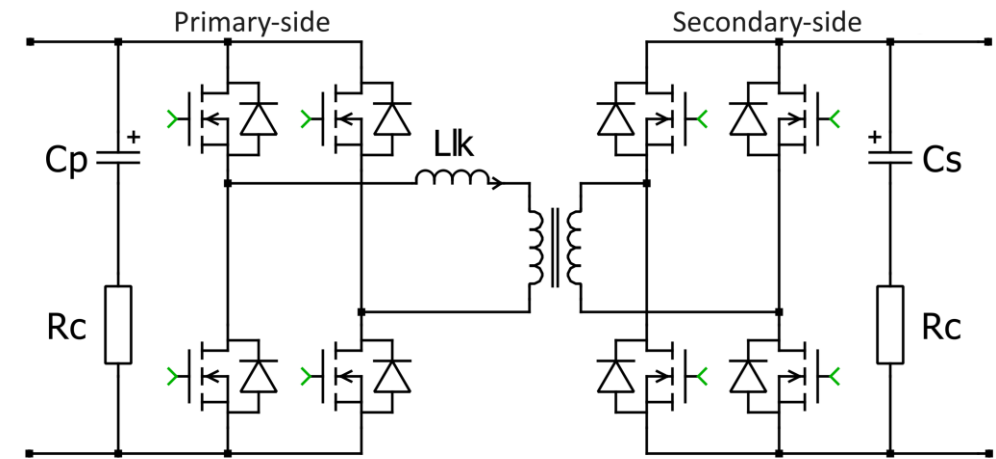
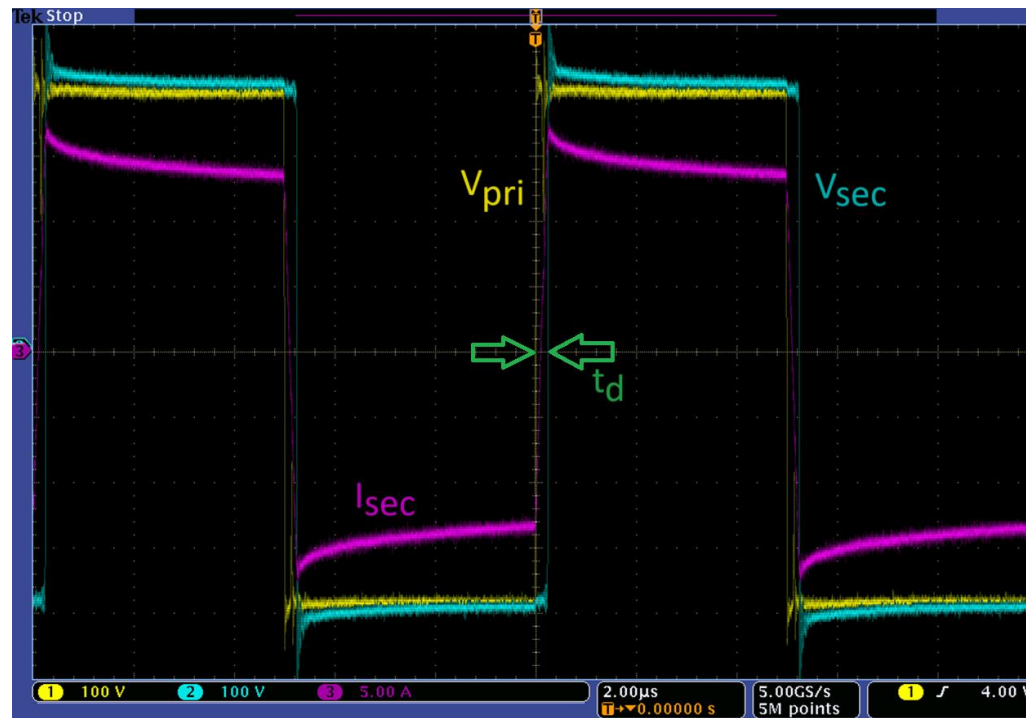


Dual Active Bridge

Dual active bridge (DAB) based around high frequency planar transformer [6]

Designed to operate at 800Vdc (input), 100kHz

Phase-shift controller [7] regulates output voltage



[6] "Payton planar," www.paytongroup.com

[7] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of Dual-Active-Bridge Isolated Bidirectional DC-DC Converter for High-Frequency-Link Power-Conversion System," IEEE Transactions on Power Electronics, vol. 29, no. 8, pp. 4091–4106, 2014

SST Controls

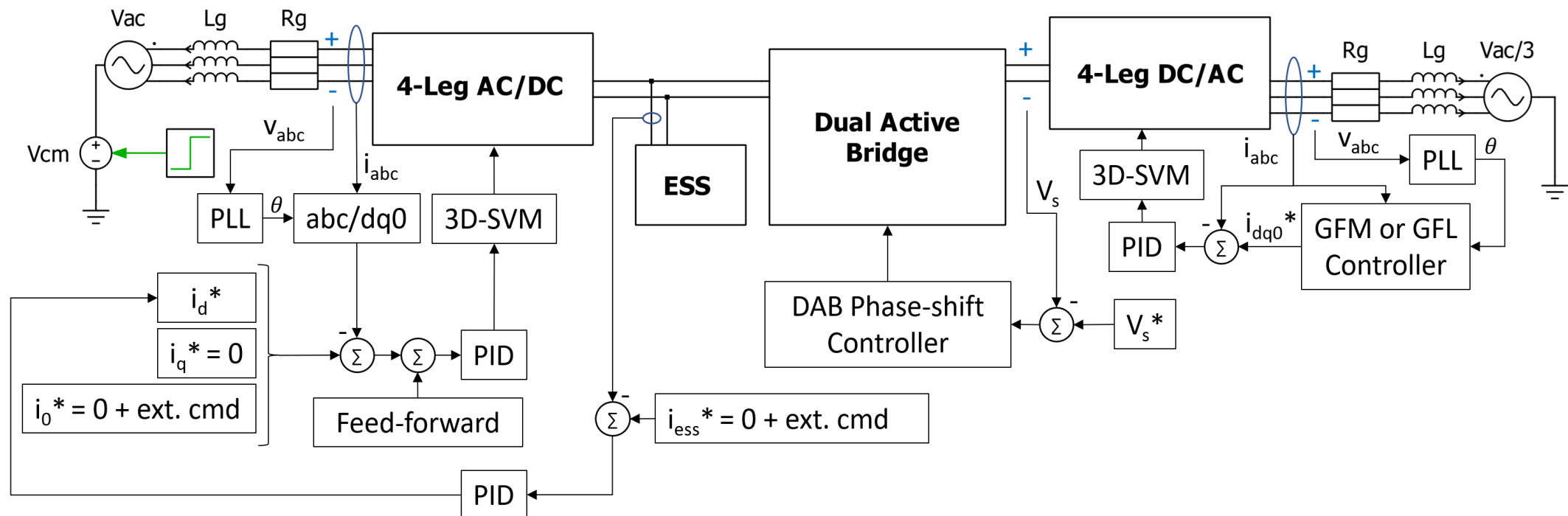


Controls are designed to transfer ac power from primary to secondary while absorbing CM insults

Primary-side AC/DC responsible for controlling CM current and drawing enough power to supply downstream load

DAB responsible for maintaining constant DC voltage for secondary inverter

Secondary inverter can be configured to be grid forming (GFM) or grid following (GFL)



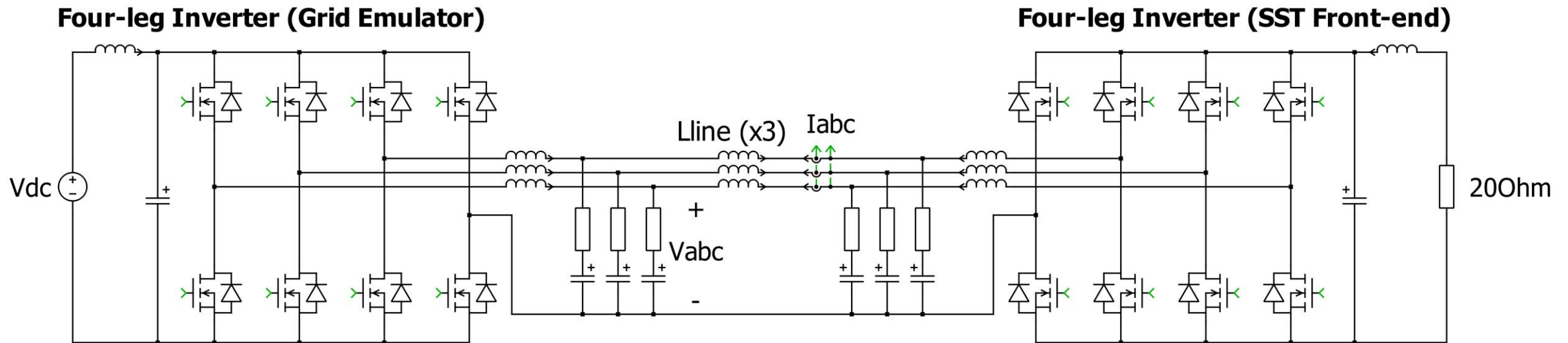
CM Mitigation Test Setup



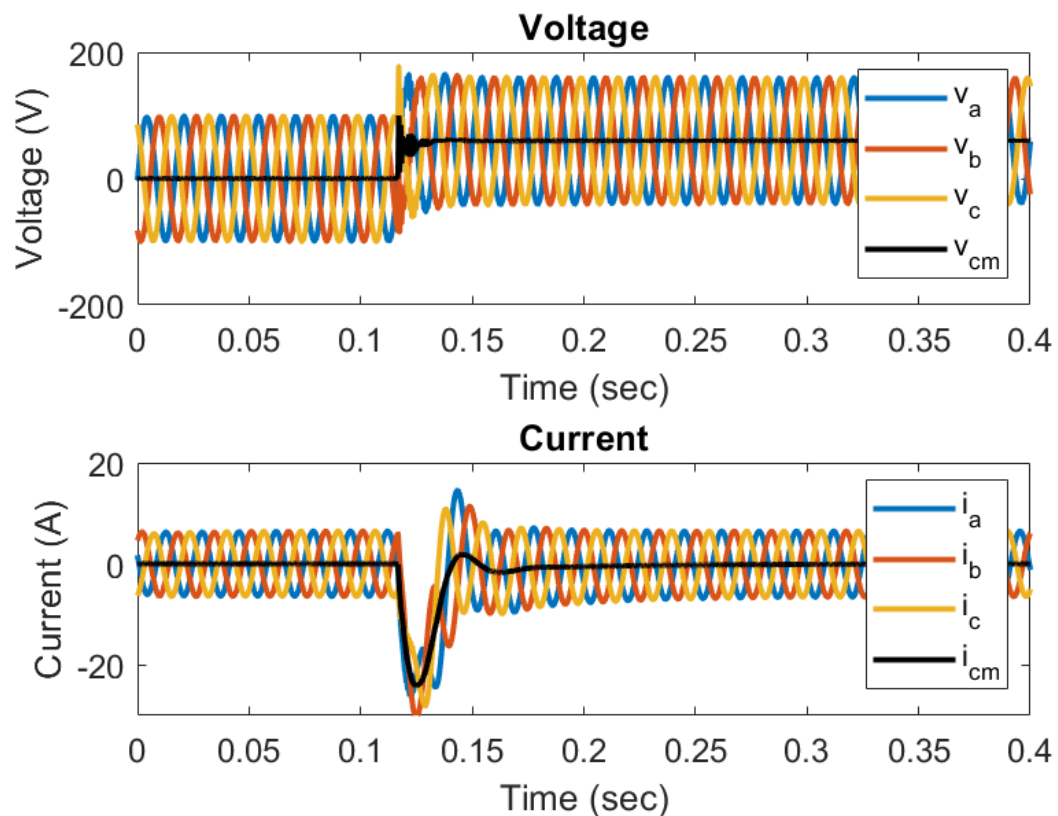
Back-to-back testing conducted to verify four-leg inverter can respond to CM insult

Left inverter acts as source (grid) and outputs AC waveforms and simulated CM insult

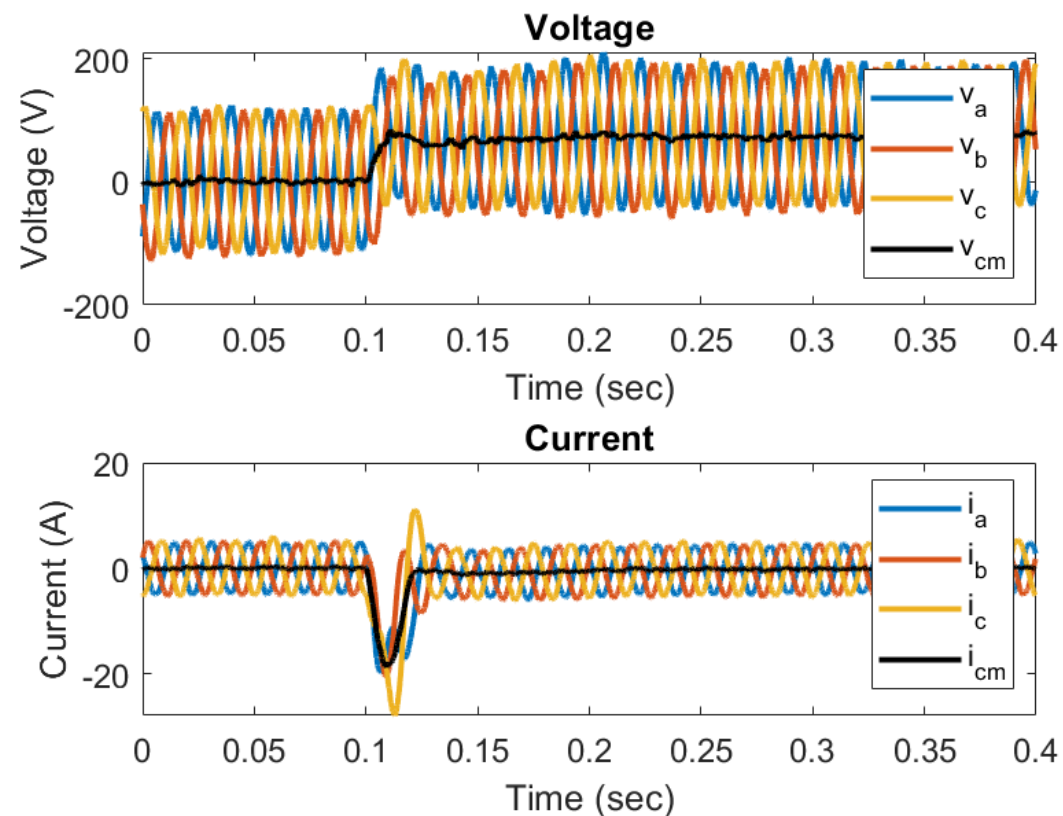
Right inverter acts as SST front-end and responds to CM insult (returns CM current to zero)



CM Mitigation Results



Simulation



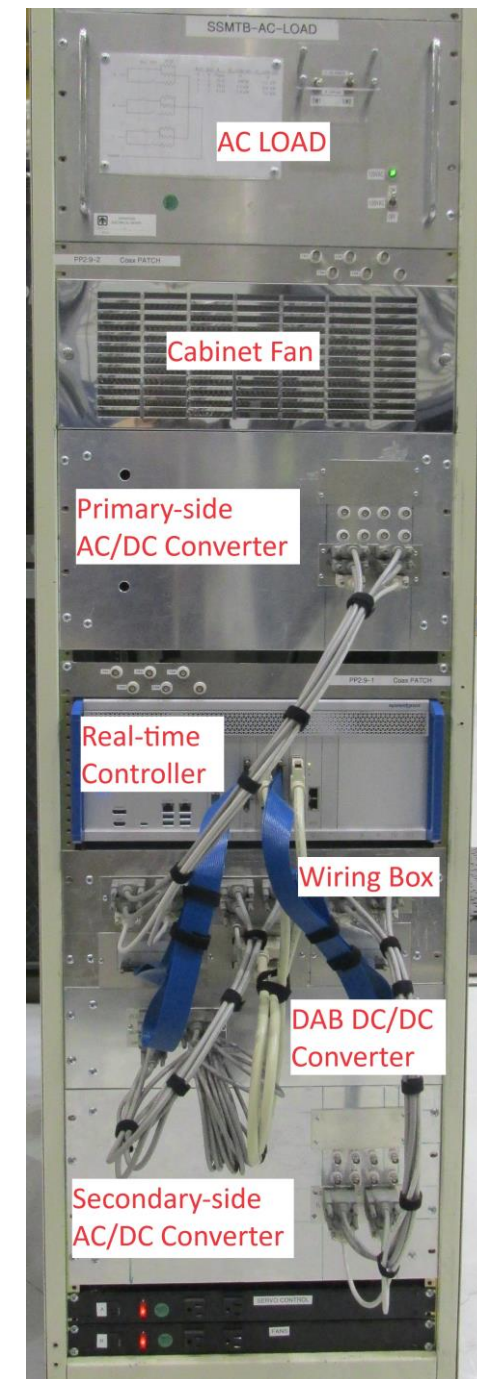
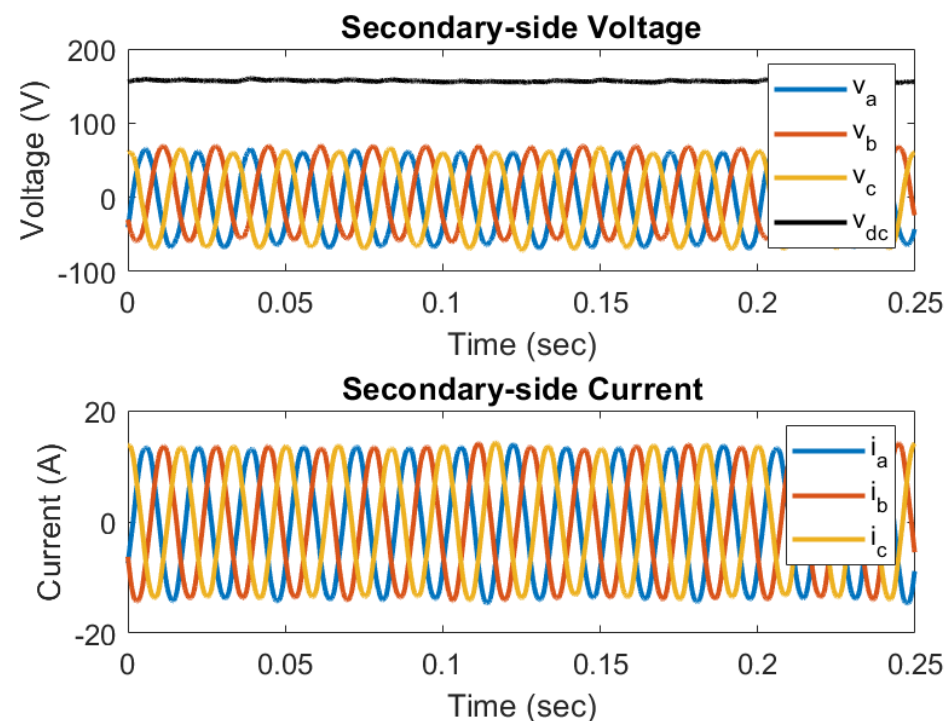
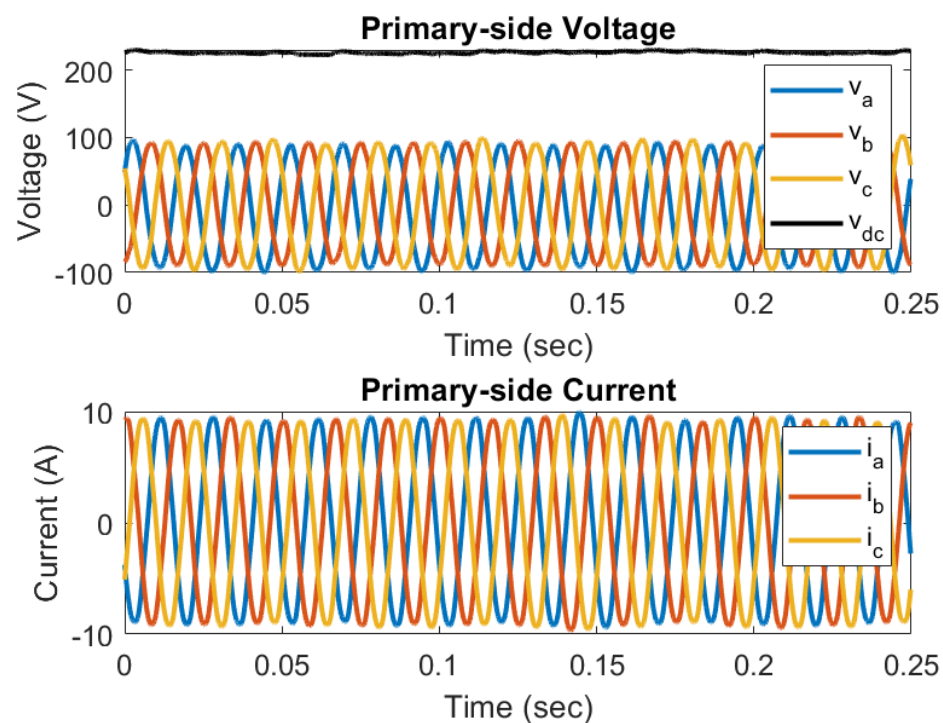
Hardware

Full SST Assembly and Testing

Full SST assembled in rack with cooling, measurement ports, wiring, etc.

Nominal ac/ac capabilities of SST tested against grid simulator

Further testing expected to evaluate performance of SST (efficiency, improved controls response, GFM/GFL output behavior, etc.)



Conclusions and Future Work



Work presented on the design and testing of an SST for HEMP/GMD CM mitigation

SST is shown to function as an effective ac/ac converter during normal operations, and respond successfully to mitigate CM current during a simulated CM insult

Future work will explore:

- Dynamic response of full SST to simulated CM insult (including energy storage requirements)
- How the SST compares to a conventional magnetic transformer during HEMP/GMD
- How the SST can be deployed in the grid to maximize overall system resilience



Secure Scalable Microgrid Testbed at Sandia [10]



Microgrid testbed facility at Sandia National Laboratories

AC, DC, and hybrid microgrid configurations

Networked control and measurement capabilities for repeatable experiments

Equipment:

- Real-time control computers
- Data acquisition system
- Custom built power converters
- Energy storage emulators
- Programmable loads
- High power supplies
- Grid simulators



Multiple Microgrid Testbed



Mechanical Source Emulators



Energy Storage Emulators



High Power Digital Resistor

