SCR-based Medium Voltage DC Solid-State Circuit Breaker

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***Abstract*— This paper describes a medium voltage solid-state circuit breaker (SSCB) based on SCR technology, featuring short fault-interruption time and a minimal turn-off auxiliary circuit. The SSCB design incorporates a specialized SCR and a commutation circuit designed with an objective to reduce the required SCR hold-off/turn-off time, t_q , which primarily determines the fault interruption duration. To validate the design, simulation analysis is presented, and a 1.5 kV 300 A SSCB prototype has been built and tested. The results confirm the effectiveness of the proposed design philosophy demonstrating the SSCB's ability to interrupt a 200 A load current in less than 50 µs. The proposed SCR-based SSCB has been developed for DC applications but is equally applicable to AC applications.**

Keywords—Medium voltage, DC circuit breaker, SCR, Design, Turn-off time (t_q).

I. INTRODUCTION

As DC distribution and transmission power systems becomes more popular due to their superior flexibility and efficiency over AC systems, DC circuit breakers (CBs) to protect such systems have received considerable interest. Nevertheless, characteristics such as faster rise rates of fault current and the absence of zero-crossing pose extra challenges for circuit breakers in isolating faults in DC systems.

Fast fault interruption and low conduction loss are the main desirable features of DC circuit breakers. Although mechanical circuit breakers are reliable and well-stablished, their response times are notably slower compared to alternative technologies, such as solid-state (SSCB) or hybrid solutions [1], [2]. Hybrid CBs are typically slower than power semiconductor-based devices and are used in high voltage (> 10 kV) applications where SSCBs are not feasible. Among the SSCBs category the interruption time is primarily defined by the turn-off speed of the power semiconductor devices, typically ranging from tens of nanoseconds to hundreds of microseconds, depending on the chosen semiconductor technology. SSCBs based on transistor family devices, such as IGBT/MOSFET, have very short turn-off times. However, IGBT/MOSFETs are limited in reverse voltage blocking capability and are connected in anti-series to achieve bi-directionality, resulting in higher conduction loss [3]. Thyristor family devices such as IGCTs are capable of reverse blocking and are connected in anti-parallel resulting in lower conduction loss [4]. A 1 kV RB-IGCT SSCB is presented in [5] for shipboard applications, however, IGCTs are costly and not readily available. Silicon-controlled rectifier devices (SCRs) are technically matured and present advantages over other semiconductors, such as reverse blocking capability, superior pulse current capabilities, lower cost, lower on-state losses [6], and are available up to 10 kV [3]. On the other hand, the technical challenge with SCRs is the need for a forced commutation method to turn them off, resulting in relatively longer turn-off times. Multiple SCR-based SSCBs have been proposed in the literature, and they have demonstrated fault interruption times of 200-300 µs [3], [7].

If the turn-off time of SCRs can be further reduced, they would be ideal for MVDC (1-20 kV) applications. Additionally, it is desirable to have a minimal commutation circuit so that it does not add to the cost and size of the circuit breaker. The main parameter determining the fault interruption time of SCR based SSCBs is the hold-off/turn-off time of the device, defined as the time from the instant the anode current falls below the holding current until the instant when the forward voltage can be reapplied [8]. The parameter t_q of conventional SCRs are typically in the range of 100-200 µs. Nevertheless, the hold-off time is a function of several parameters [8], which can be explored through the design of the external circuit imposing the physical quantities during the commutation process.

In this paper, a 1.5 kV 300 A SSCB using SCR technology was designed, built, and tested. The main contribution of the paper is to address different aspects of designing the commutation circuit for DC applications of an SCR-based CB to achieve a fault interruption time of less than 50 µs, while maintaining a compact commutation circuit with an auxiliary capacitor in the tens of µF. The proposed SSCB achieves these objectives by incorporating a specialized SCR and a commutation circuit designed to reduce the required SCR hold-off/turn-off time, which primarily determines the fault interruption duration. Simulation and experimental results are presented to validate the design.

II. SSCB TOPOLOGY AND ANALYSIS

A. Toplogy

Figure 1 shows the schematic diagram of the SCR-based DC circuit breaker. The topology consists of a main SCR (S_m), which conducts the current in normal operating mode, and an auxiliary commutation circuit comprising an inductor, capacitor, MOV, and an auxiliary SCR (S_a). The main differentiation

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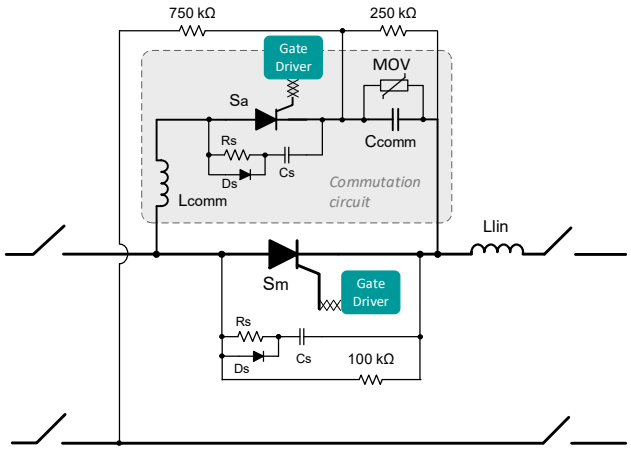


Fig. 1. SCR-based solid-state circuit breaker.

compared to traditional approaches is the design and selection of the components for a medium voltage (MV) application with the objective of limiting the fault interruption time to less than 50 µs. To interrupt the current in the occurrence of a fault, two steps are involved. Firstly, the current through the main thyristor is reduced to zero by transferring it to the commutation branch when S_a is turned on. Subsequently, S_m is reverse biased for a time duration long enough for it to regain forward voltage blocking capability, i.e., for a duration greater than its turn-off time (t_q). A passive resistor-based pre-charge circuit is used to charge the auxiliary capacitor (C_{comm}) to an initial voltage which is used to reverse bias the SCR. Snubber circuits, as shown in Fig. 1, are used to prevent unwanted dv/dt triggering the main and auxiliary SCRs.

For bidirectional operation, the circuit shown in Fig. 1 can be used with another similar branch connected in anti-parallel, as shown in Fig. 2.

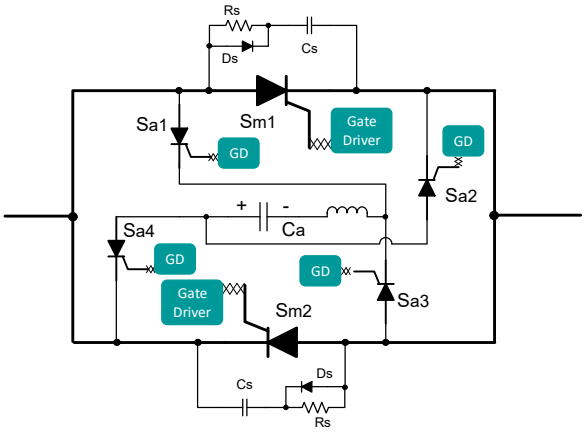


Fig. 2. Schematic of the bidirectional SSCB.

B. Operation

Figure 3 illustrates the conceptual waveform across the SCR and the main components of the commutation circuit during a breaking event. Assuming that a fault is identified at the instant $t = t_0$, the gate signal of the main SCR is removed, while the gate signal to the auxiliary SCR is enabled. The fault current then starts to flow through the auxiliary branch at a rate limited by the inductor L_{comm}, reducing the current in the main SCR at the same rate. After the current in the main SCR falls below the holding current (instant t_1), the main SCR is reverse biased (V_r) during the interval $t_1 - t_2$. To guarantee a complete turn-off process of the main SCR, the interval $t_1 - t_2$ should be greater than the turn-off time of the device (t_q), which is specified in the datasheet.

The turn-off time provided in the datasheet is based on specific operating conditions, as it depends on several parameters. The main characteristics affecting t_q include the construction of the SCR device, the anode current, di/dt of the anode current during turn-off, the negative voltage applied immediately after turn-off (V_r), dv/dt of positive voltage, and the temperature [8]. Based on this, the proposed design for the commutation circuit in this paper considers each of these parameters to reduce the required SCR hold-off time and, consequently, the fault interruption time.

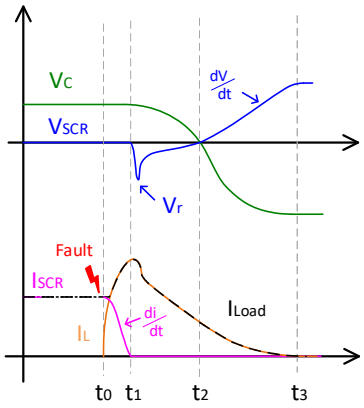


Fig. 3. SSCB conceptual waveforms during fault interruption.

III. Design and Selection of Components

Starting with the SCR fabrication itself, the doping of the SCR is modified to reduce t_q, however, as a trade-off the device voltage drop will increase. In this application, a specialized SCR (R1279NC22x) has been chosen with a t_q of 50 µs and on-state voltage drop of 1.5 V at 300 A. This will result in <0.1% losses due to the SCR based SSCB. For the selected device, t_q is defined at a di/dt of 60 A/ µs, V_r equal to 50 V, and dv/dt of 20 V/ µs [9]. To further reduce the turn-off time, the objectives of designing the commutation circuit are:

- reduce the rate of decay of forward current (di/dt);
- increase the reverse voltage (V_r);
- decrease the rate of reapplication of forward blocking voltage (dV/dt);

The design target parameters (di/dt, V_r, and dV/dt) are also shown in Fig. 3. For design purposes, one must consider that the commutating capacitor is pre-charged so that it has enough energy to drive the SCR current to zero. Additionally, the voltage of the commutating capacitor ($V_{c,comm}$) affects the following: the peak bus voltage ($V_{c,comm}$ adds to the bus voltage during commutation), voltage rating of the auxiliary SCR, and the negative voltage across the main SCR (V_r) during

commutation. While it is desirable to limit the peak bus voltage and the voltage across the auxiliary SCR, a high V_r is desirable to reduce t_q. In this design the $V_{c,comm}$ is chosen to be 1.25x of bus voltage as a compromise. The pre-charge resistors can be chosen accordingly.

The size of auxiliary capacitor is chosen to have enough stored energy to drive SCR current to zero, apply negative voltage during t_q and control dv/dt of main SCR. The commutating inductor L_{comm} is selected to limit the di/dt of the main and auxiliary SCRs. Therefore, the required commutating capacitor and inductor can be calculated as:

$$V_{c,comm} \cdot C_{comm}^2 \gg L_{comm} \cdot I_{max}^2$$

$$C_{comm} > \frac{I_{max} \cdot t_q}{V_{c,comm}} \ , \ C_{comm} > \frac{I_{max}}{dV/dt_{main\_SCR\_tq}} \quad (1)$$

$$L_{comm} = \frac{V_{c,comm}}{di/dt_{max}} \quad (2)$$

$$di/dt_{max} = \min \{\frac{di}{dt_{main_{SCR}}}, \frac{di}{dt_{aux_{SCR}}}, \frac{di}{dt_{main_{SCR_{tq}}}}\}$$

where, I_{max} stands for the maximum expected fault/load current to be commutated, $dV/dt_{main\_SCR\_tq}$ and $di/dt_{main\_SCR\_tq}$ are the dv/dt and di/dt of the main SCR at the specified t_q. The auxiliary thyristor can be chosen with a large t_q, which reduces cost and customization requirements, as it does not need to have a fast turn-off capability. The peak fault current in the circuit can be limited through the line inductor (L_{lin}) shown in Fig. 1. In this design, the peak was defined as 20% of the rated current of the CB and the was inductor calculated as (3):

$$L_{lin} = \frac{V_L \cdot t_q}{I_{pk} - I_{rated}} \quad (3)$$

Following the design criteria, the obtained parameters for the auxiliary circuit are summarized in Table I. One remaining parameter is the SCR operating temperature. In this paper, a 700 A device mounted on a heatsink has been selected, which allows for natural convection cooling at the rated 300 A.

Figure 4 highlights the main parameters addressed in the design to decrease t_q. The selected parameters that effect t_q are

TABLE I. SSCB MAIN COMPONENTS

Parameter	Value
Main SCR (S_m)	R1279NC22 / $t_q = 50\ \mu s$
Auxiliary SCR (S_a)	MCD94-22IO1B / t_q = 185 μs
Auxiliary Capacitor (C_{comm})	40 µF
Auxiliary inductor (L_{comm})	10 µH
MOV	V881BA60
Snubber (RCD)	10 Ω, 0.22 µF, GP02-30
Line inductor (L_{lin})	140 µH

compared with the parameters given in the datasheet for the selected device. As can be seen, all the relevant quantities are chosen to be within the boundaries defined by the datasheet parameters (blue curve) so as to further reduce t_q . It will be shown in the experimental results, that such a design allows operating with lower t_q and achieve faster interruption time.

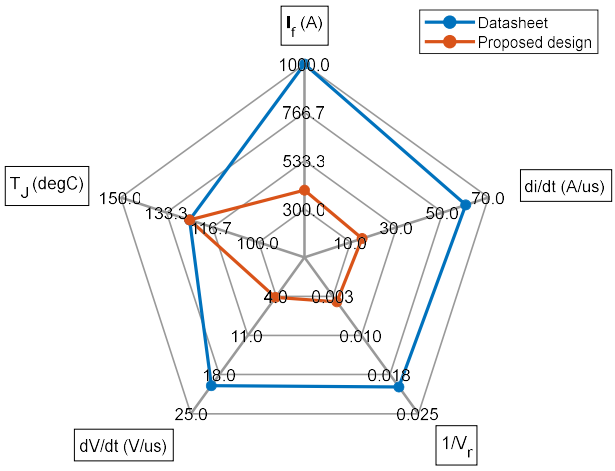


Fig. 4. Comparison between the parameters achieved with the proposed design and the parameters informed in the datasheet of the main SCR.

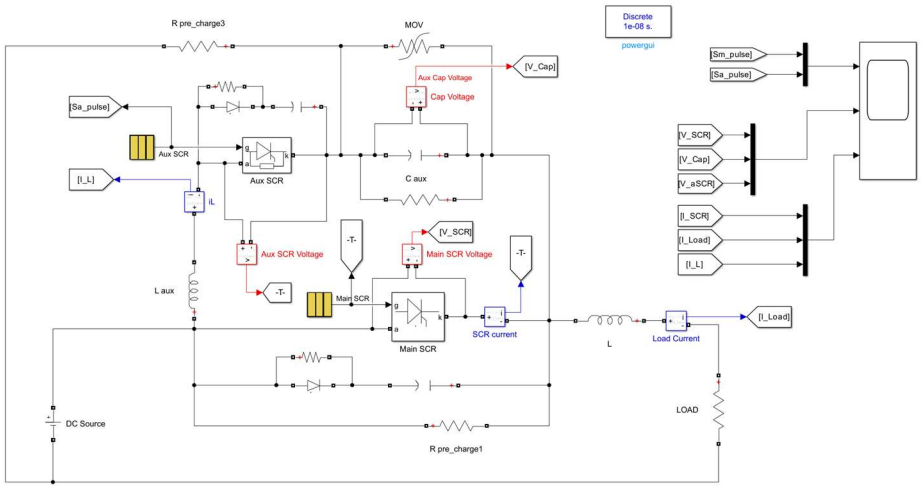
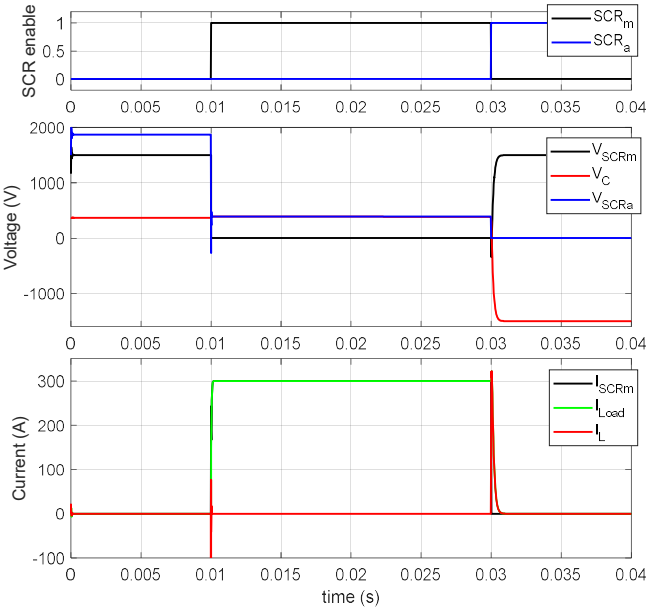


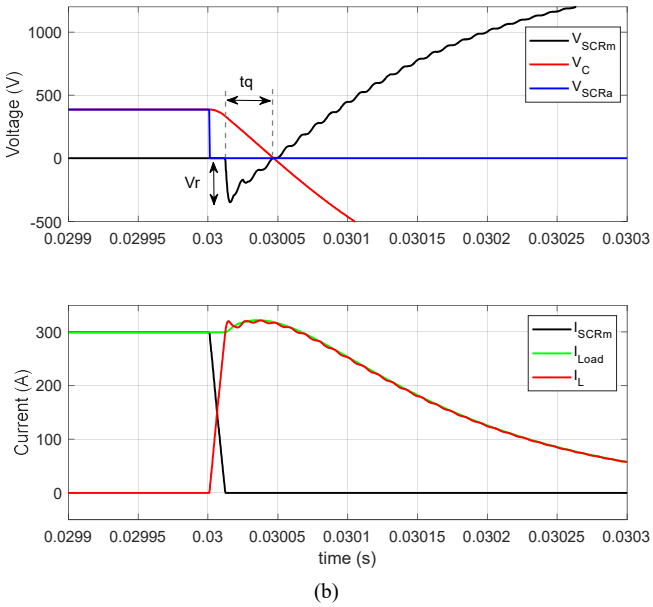
Fig. 5. Matlab/Simulink model of the proposed DC SSCB.

IV. Simulation Results

To verify the effectiveness of the design, simulation analysis were conducted using MATLAB/Simulink as shown in Fig. 5. Figure 6 presents the simulation results obtained under rated conditions, i.e., 1.5 kV and a load current of 300 A. A fault occurs at 0.03 s and from Fig. 5(b), it can be observed that the main SCR is reverse-biased for an interval of less than 50 µs, which is sufficient to ensure its complete turn-off process. The anode current of the main SCR is reduced to zero in approximately 15 µs and after that, the applied reverse voltage reaches 300 V, which is higher than the 50 V specified in the



(a)



(b)

Fig. 6. Simulation results during a fault interruption. (a) Voltage and currents on the main and auxiliar branch, along with SCRs control signals. (b) Zoomed waveforms to highlighting the details.

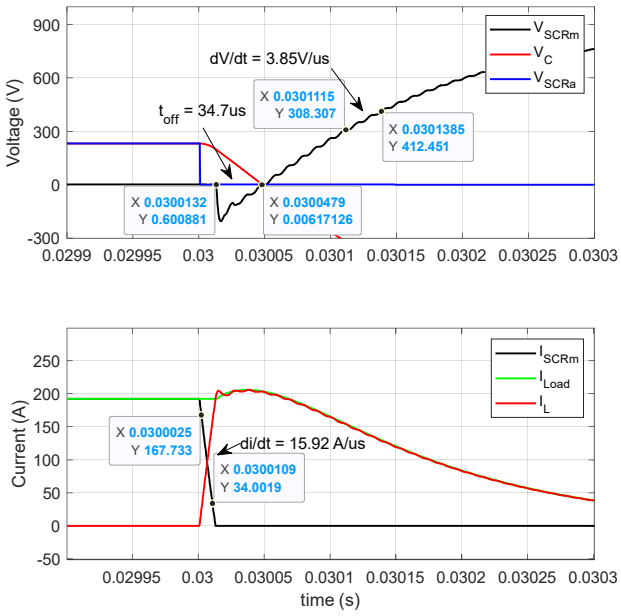


Fig. 7. Simulation results along with parameter calculations under a fault interruption at 900 V and 200 A.

datasheet. The fault current continues to flow through the auxiliary branch for approximately 400 µs until the auxiliary capacitor is fully charged. Figure 7 shows the results at 900 V, 200 A. This condition was simulated in order to later compare with experimental results shown in the next section. Once again, simulation has confirmed the SCR interruption time less than 50 µs. Moreover, the parameters affecting the turn-off time are calculated from the simulation results, as shown in Fig. 7, and it can be observed that they meet the design objectives.

V. Experimental Setup and Test Results

A 1.5 kV, 300 A SCR-based SSCB prototype was built to validate the design experimentally. Firstly, the gate drivers to trigger the main and auxiliar SCRs were designed and implemented. Afterwards, the designed commutation circuit was implemented and the breaking operations were assessed up to 200 A.

A. Gate driver

Figure 8 shows the schematic of the gate driver circuit which has been designed to meet the trigger characteristics given in the datasheet of each SCR. The main requirement for the trigger circuit is to ensure proper current flow between the gate and cathode terminals of the SCR. In addition to supplying the triggering energy, the gate driver must also provide the necessary insulation between the power line circuit and the control circuit. Therefore, galvanic isolation has been chosen and a pulse transformer was designed to provide a 10 kHz pulse train. One important parameter on the pulse transformer is the coupling capacitance. Thus, particular attention was given to separating the primary and secondary windings to achieve low coupling capacitance and avoid common noise issues. At the same time, the leakage inductance was kept below a certain value to prevent interference with the pulse current rise.

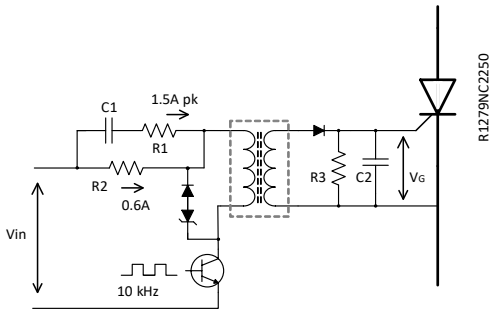


Fig. 8. Gate driver schematic.

For the main SCR (R1279NC22), the gate trigger voltage V_G is 3V and the gate trigger current I_{GT} is 0.3 A, however, a practical recommendation is to apply a peak current of five to ten times I_{GT} for a certain time (approximately 20 µs) to supply the necessary charge to trigger. Then, the so-called back-porch current is typically in the order of 1.5 times I_{GT} [10]. To meet these requirements, the pulse current with an initial peak of 1.5 A was obtained by selecting C1 and R1 in Fig. 8. The time constant of these two elements also determines the peak duration. The steady-state current value for the remaining portion of the current pulse (back-porch) was set to 0.6 A and adjusted by selecting R2. To avoid the thyristors to turn on unintentionally due to EMI, the gate circuit incorporated R3 and C2 for protection. A low shunt capacitor (C2) can reduce the sensitivity of the SCR to dv/dt while the external gate-cathode resistor R3 prevents false triggering due to leakage current. R3 also contributes to lower the t_q time by assisting in recovering the storage charge [10]. The gate drivers are supplied through a medium voltage power supply, which can generate isolated low voltage directly from the DC link [11].

B. Commutation circuit and test setup

Figure 9 shows the implemented commutation circuit in a compact form factor, based on the designed components given in Table I. This circuit is connected in parallel with the main thyristor as shown in Fig. 10. The experimental tests were conducted with a resistive load. Due to limitations in the setup, the performance of the developed SSCB was evaluated based on load current interruption rather than an actual short circuit interruption.

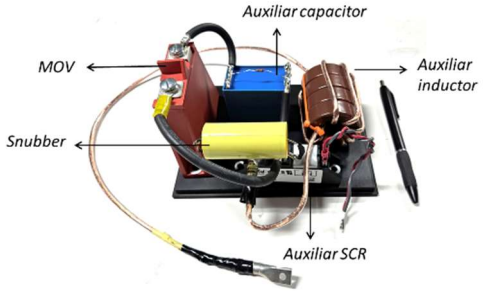
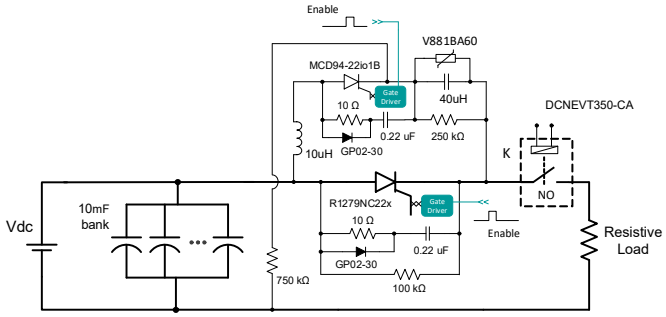


Fig. 9. Designed auxiliary circuit for SCR turn-off, with overall dimensions of 130x170x100mm, referenced to a pen.



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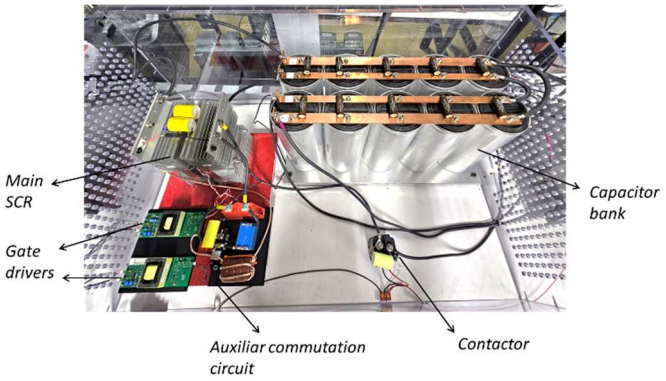

(b)

Fig. 10. SSCB test setup. (a) Schematic. (b) Workbench.

The test setup was designed based on a DC capacitor bank as presented in Fig. 10. The capacitor bank is pre-charged using a high voltage, low current power supply. Subsequently, a contactor is closed, and the energy stored is applied to a resistive load through the SSCB. The capacitor bank is sized to provide a sufficiently high current to test the CB. After approximately 30 ms, a fault is emulated, and the breaking process is initiated, as shown in the flowchart in Fig. 11.

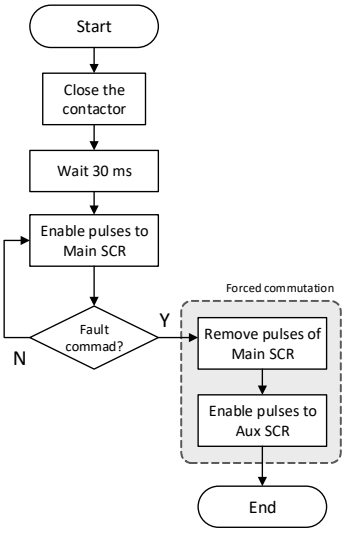

Fig. 11. Flowchart of the test sequence.

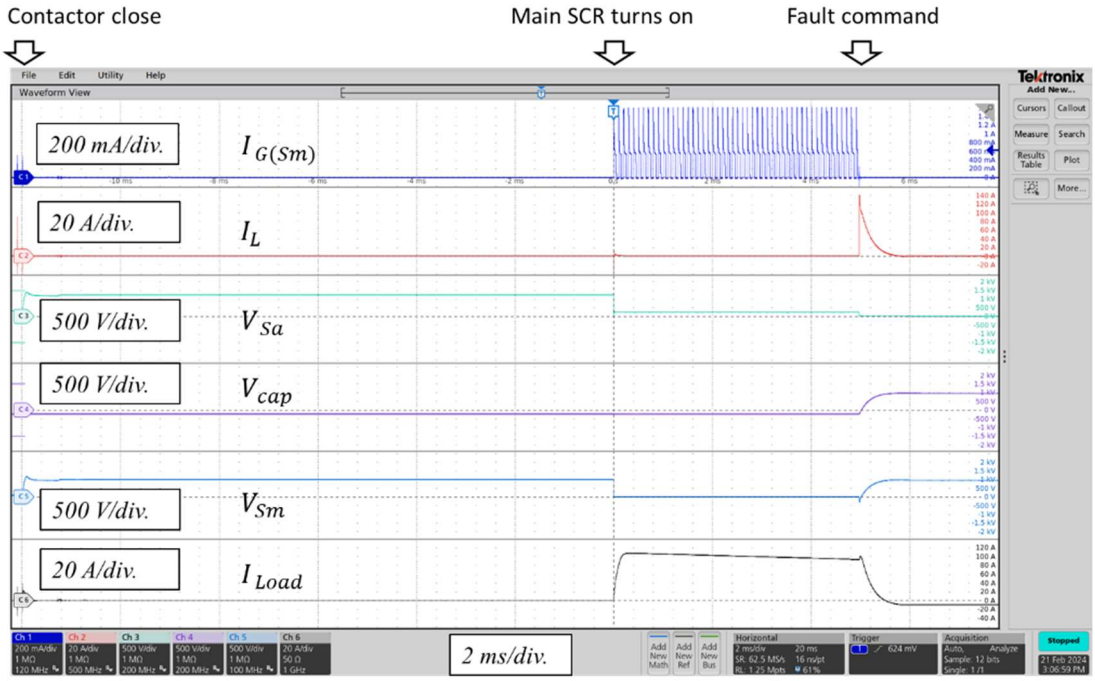

Fig. 12. Experimental results of the SSCB at 1.2 kV and 100 A.

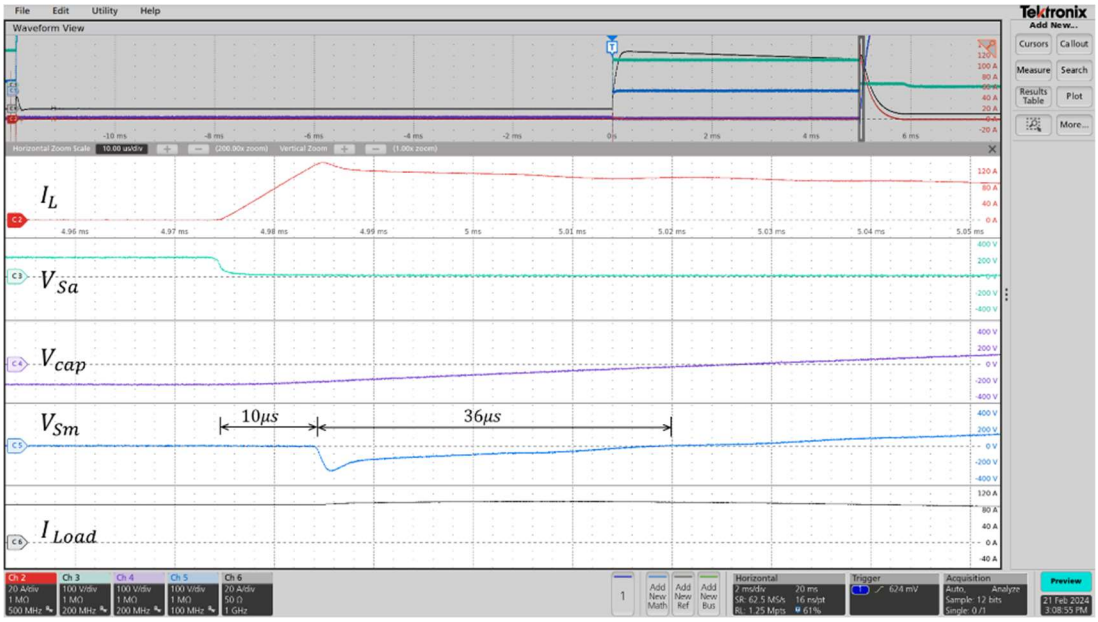

Fig. 13. Zoomed waveforms during commutation at 1.2 kV and 100 A.

C. Verification under load current interruption

Figure 12 shows the experimental results at 1.2 kV. The main SCR is turned on and the load current started to flow reaching approximately 100 A. The capacitor was pre-charged with 300 V through the resistors. When a fault is identified, the load current is transferred to the commutation branch by turning on the auxiliary SCR. Figure 13 shows the zoomed waveforms during the forced commutation. The inductor current I_L rises at a di/dt determined by V_{cap} and inductance L_{comm}. When I_L reaches the load current (100 A), the S_m turns off, which is indicated by the appearance of negative voltage across the SCR. This time takes approximately 10 μs. The main SCR voltage follows the commutating capacitor voltage V_{cap} which reverse biases S_m for approximately 36 μs. After this time the current

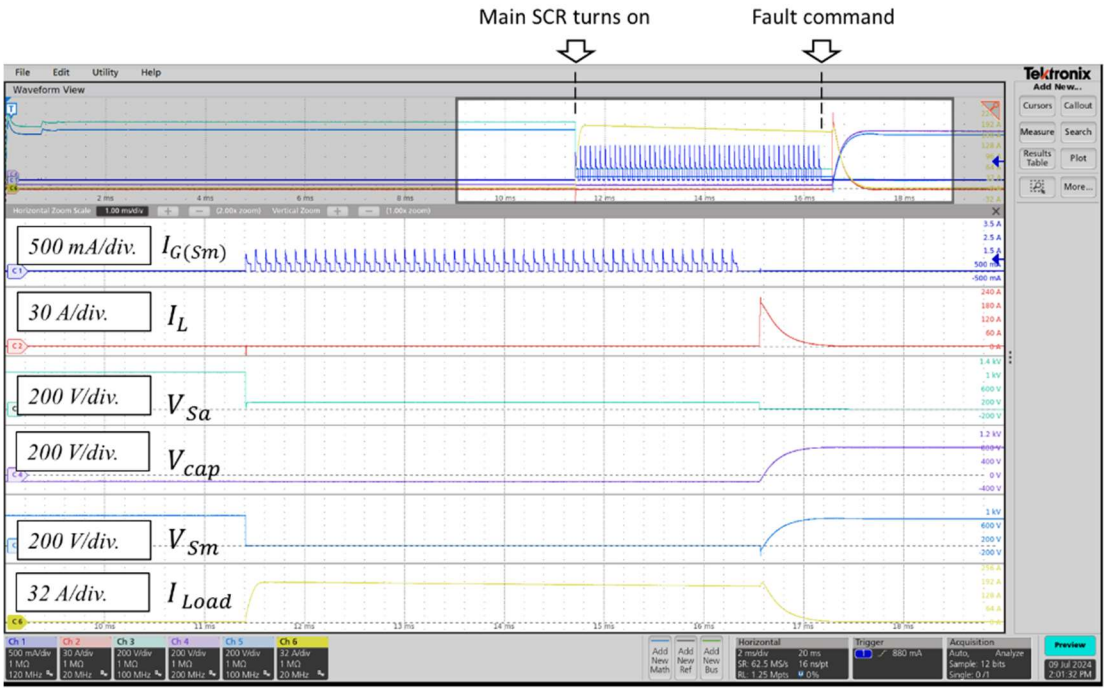

Fig. 14. Experimental results under 200 A load current interruption.

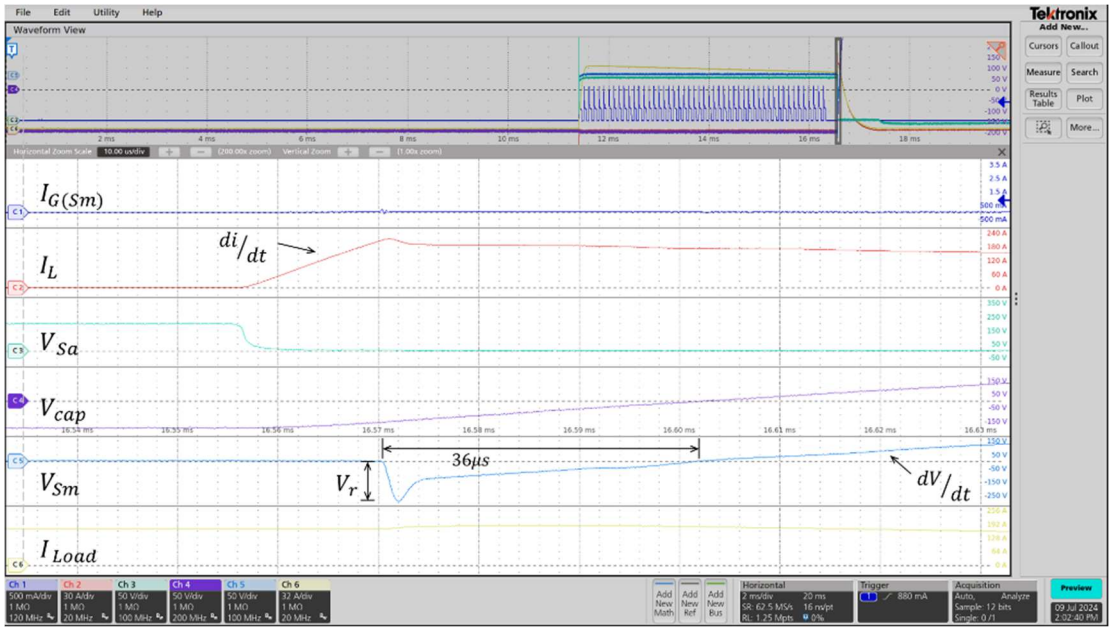

Fig. 15. Zoomed results for 200 A load current interruption ($V_r = 225V, {}^{di}/_{dt} = 15A/\mu s, {}^{dV}/_{dt} = 4V/\mu s$).

decreases for approximately 0.4 ms until the capacitor is charged with the bus voltage. The total fault interruption time is 46 µs, including 10 µs for the SCR current to reduce to zero and 36 µs hold-off/turn-off time for the SCR. The fault interruption time is defined here as the time after which the fault current does not increase measured from the point of fault inception.

Figures 14 and 15 shows the breaking operation under 200 A load current. As one can notice, the same behavior is observed as the previous test. The proposed commutation circuit successfully assist the main SCR to turn-off in less than 50 µs. Furthermore, the parameters di/dt, V_r, and dV/dt observed experimentally are in good agreement to what has been designed and verified through the simulations in section IV.

VI. Conclusion

In this paper, a SCR based SSCB with fast (< 50 µs) fault interruption time is presented for medium voltage (1.5 kV) applications. SCR is chosen as this technology is matured, is

available up to 10 kV and significantly capable of reverse voltage blocking, resulting in lower conduction loss (single device forward voltage drop) even in bi-directional applications. The major challenge with SCR is the hold-off time t_q, which drives the fault interruption time to be in the range of 200-300 µs range. Parameter t_q depends on device construction and other parameters such as dV/dt, di/dt, V_r, among others. In this paper, it is proposed that by carefully selecting each of those parameters, t_q can be further reduced. Starting with selection of SCR construction (doping levels), relevant parameters are selected to achieve a t_q of less than 40 µs. The design has been validated through experimental results at 1.2 kV, 100 A and 900 V, 200 A. In both the cases it was shown that the fault interruption time is < 50 µs. The SCR based SSCB is equally applicable for both AC and emerging MVDC applications.

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