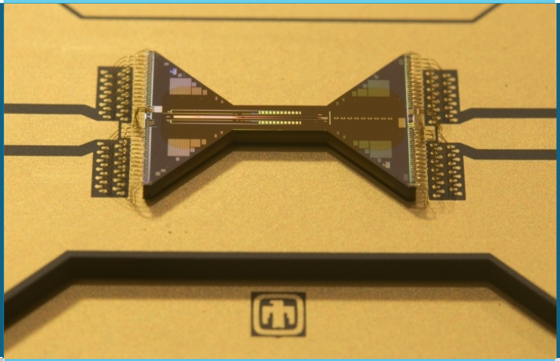
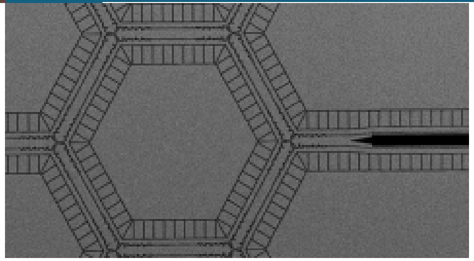
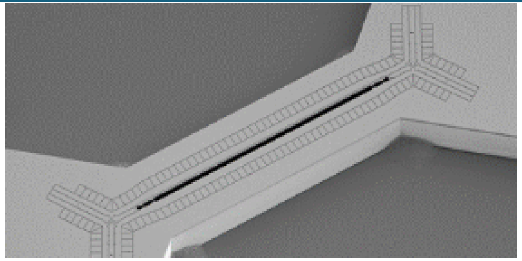
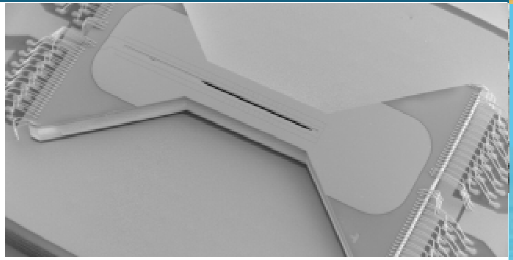
SAND2024-14661C

Ion Based Quantum Computing in Microfabricated Surface Traps









Presented by:

Melissa Revelle

October 11th, 2024

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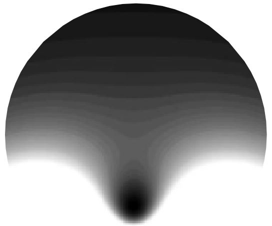
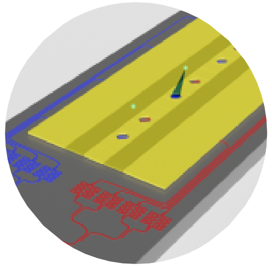
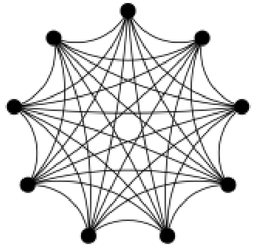
Outline



Ion Trapping Overview



Next Generation Ion Traps



QSCOUT

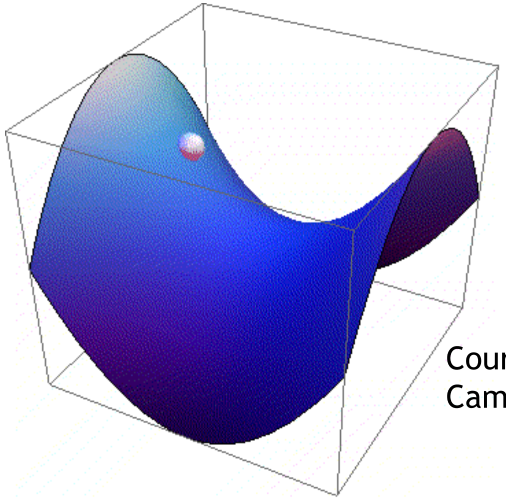
Earnshaw’s Theorem and Ion Trapping

Trapping requirement: A restoring force when displaced from trap center (in any direction)

Cannot use t

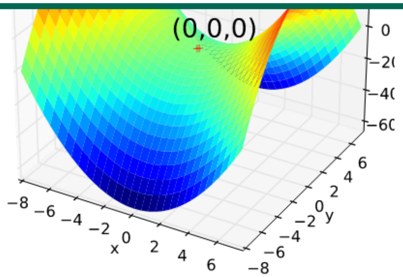
Field lines start/en

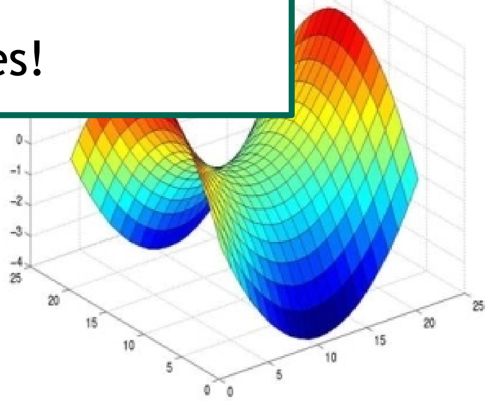
ut” and rections



Courtesy of Wes Campbell

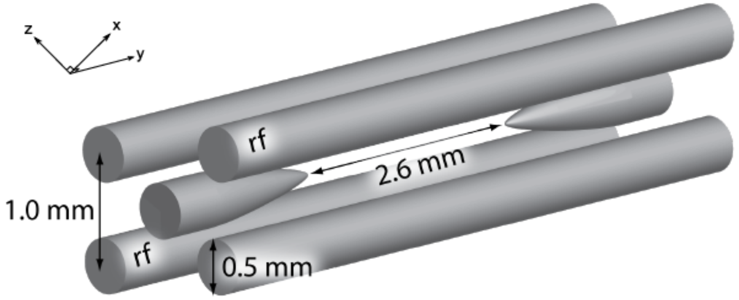
Before ion escapes, field reverses!

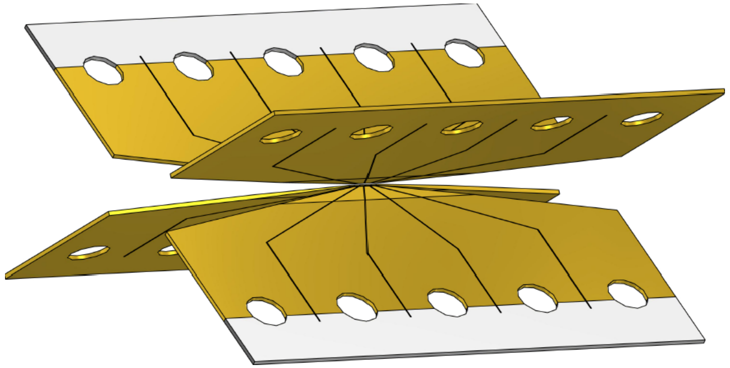


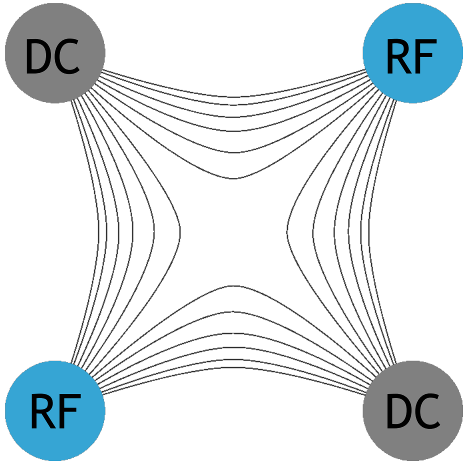


Various Trap Geometries

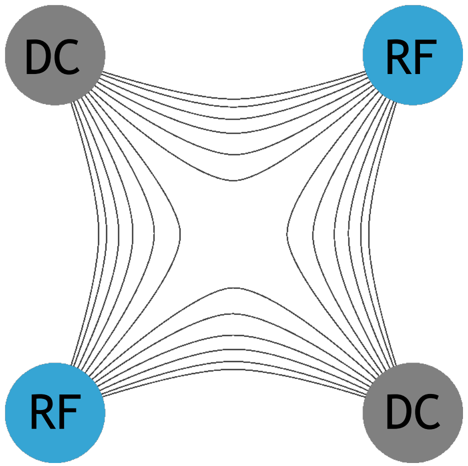
Use a combination of static and rf fields to trap ions
Various geometries possible



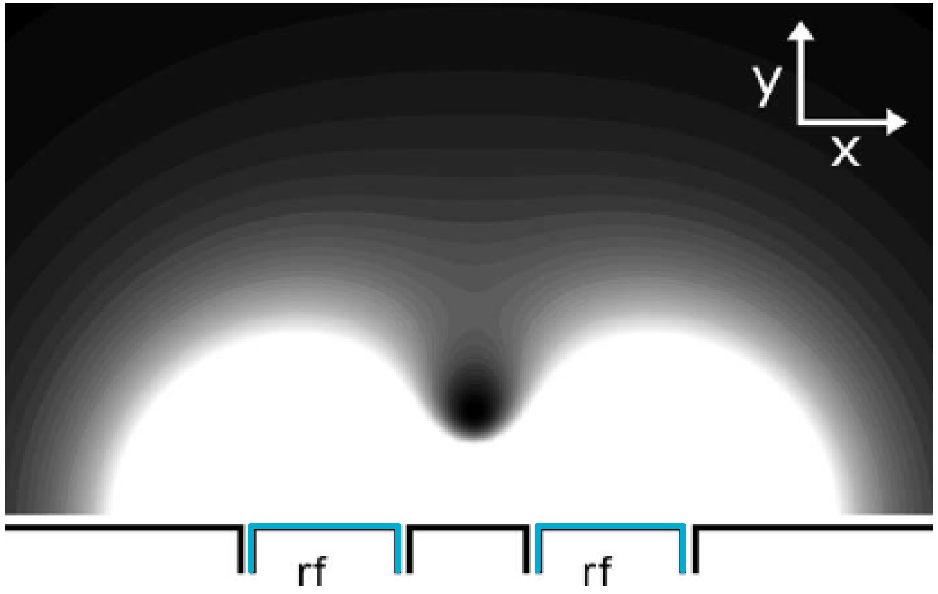


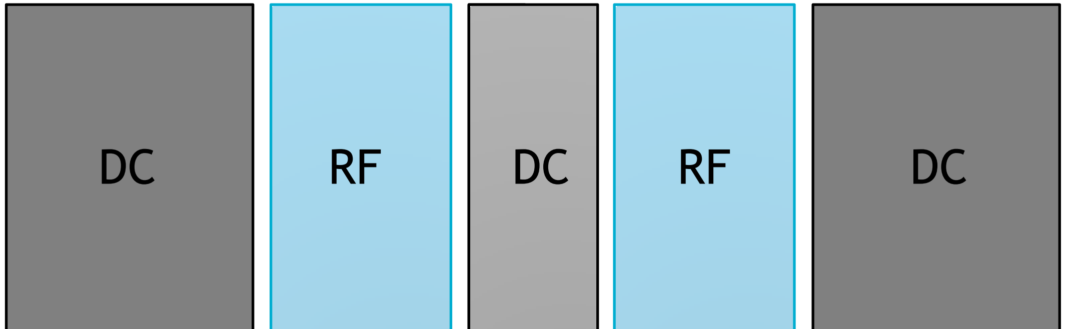


Various Trap Geometries



Pseudopotential well (dark area) formed along the axis of a surface trap

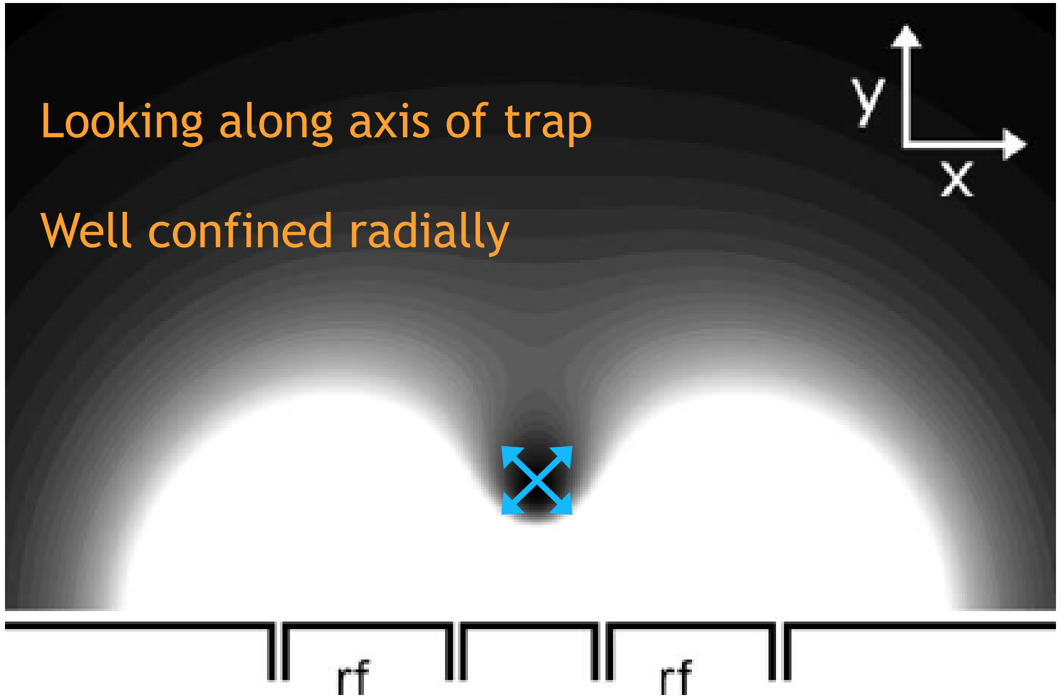




Electrodes from above

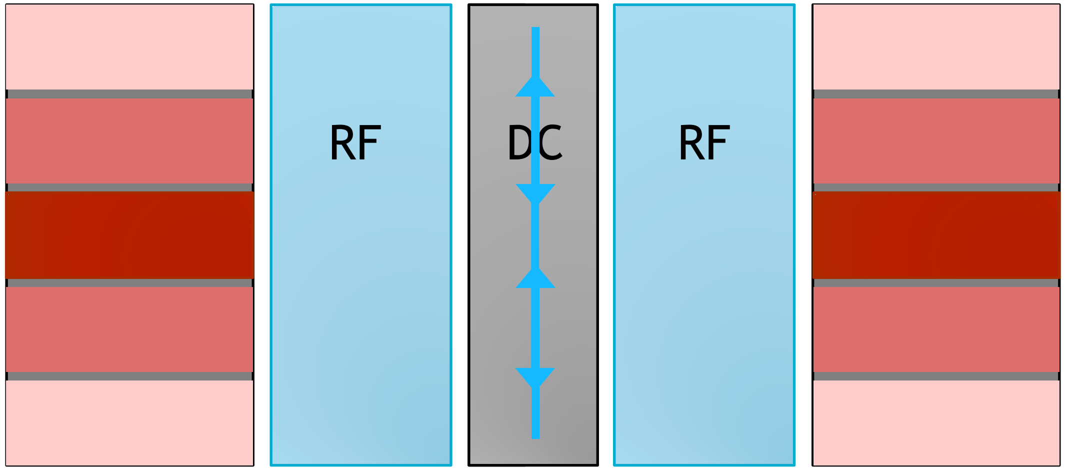
House, PRA **78** 033402 (2008)

Need for DC Fields



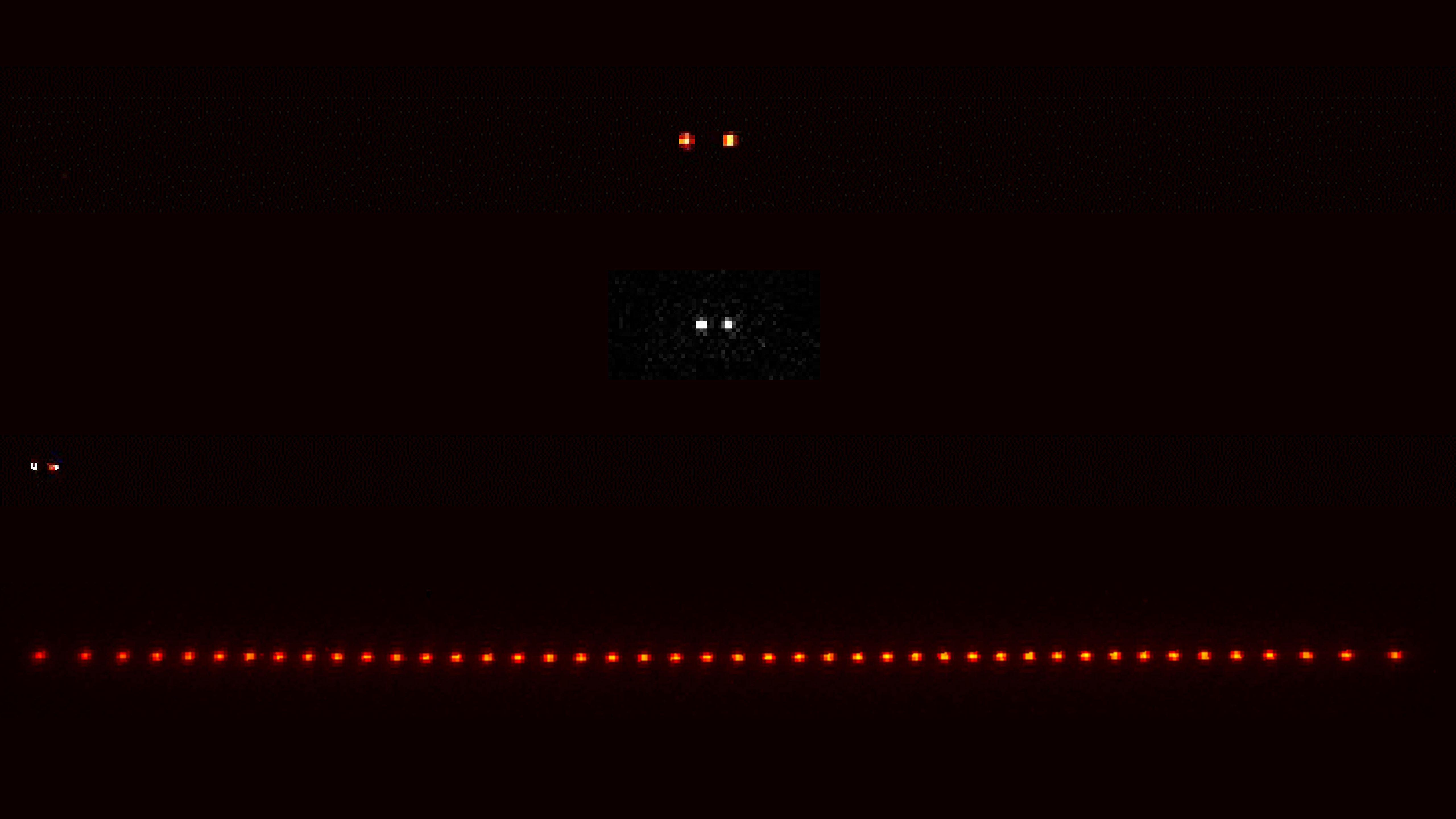
Looking at trap from above

Still free to move along axis

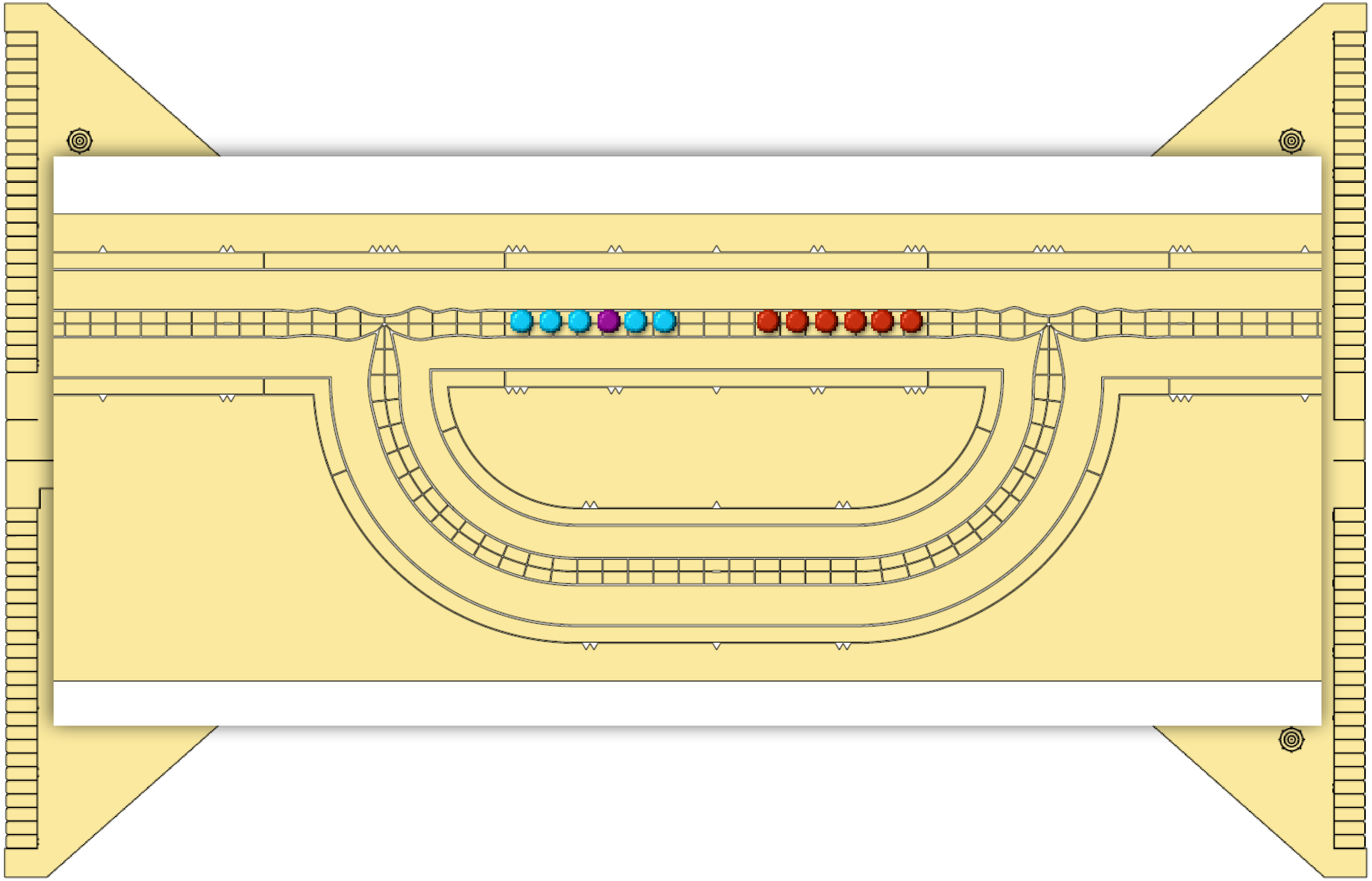


Use DC fields on the electrodes to confine

Creates a trapping potential along axis

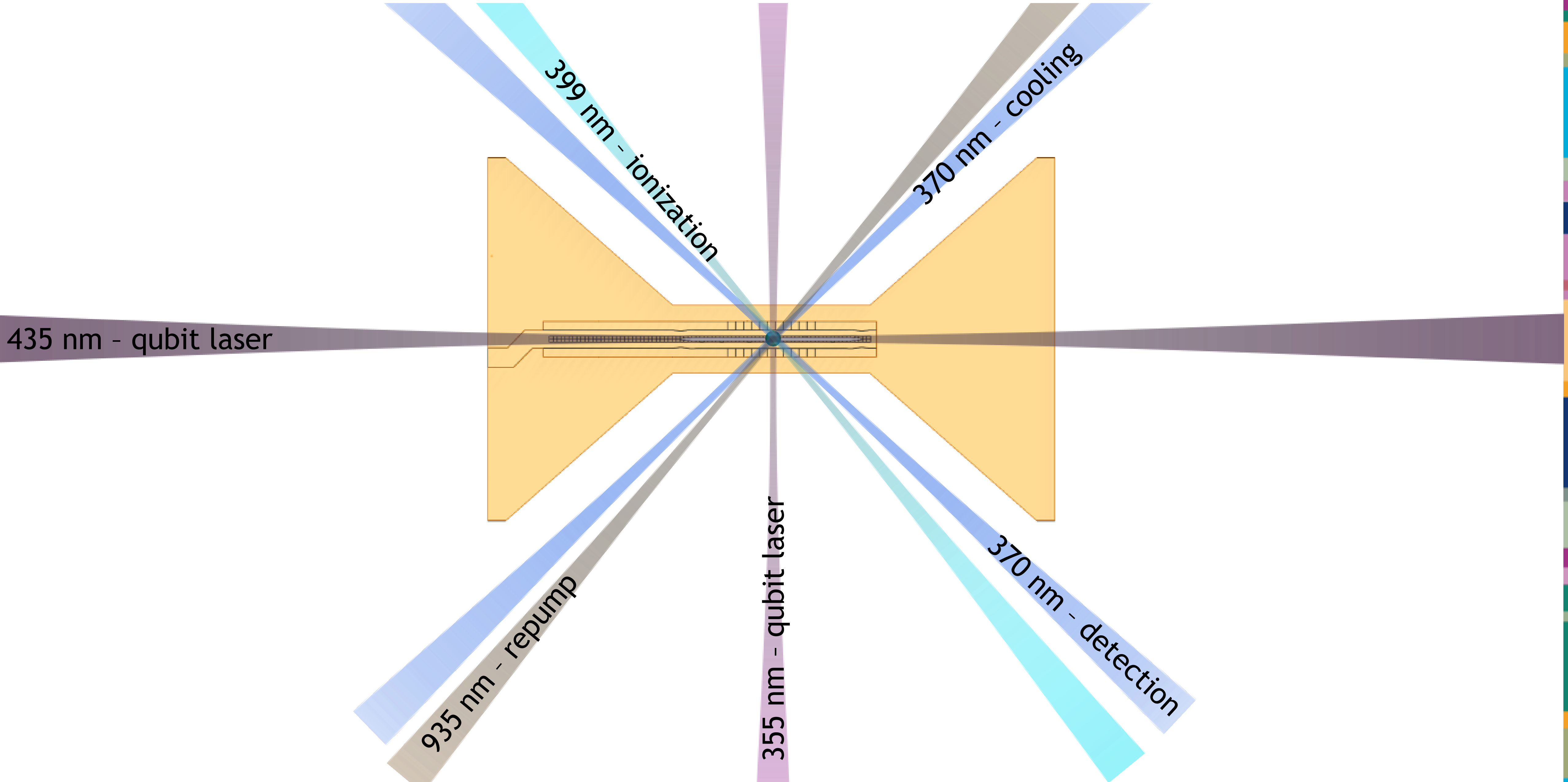


Create custom trap designs with advanced ion control



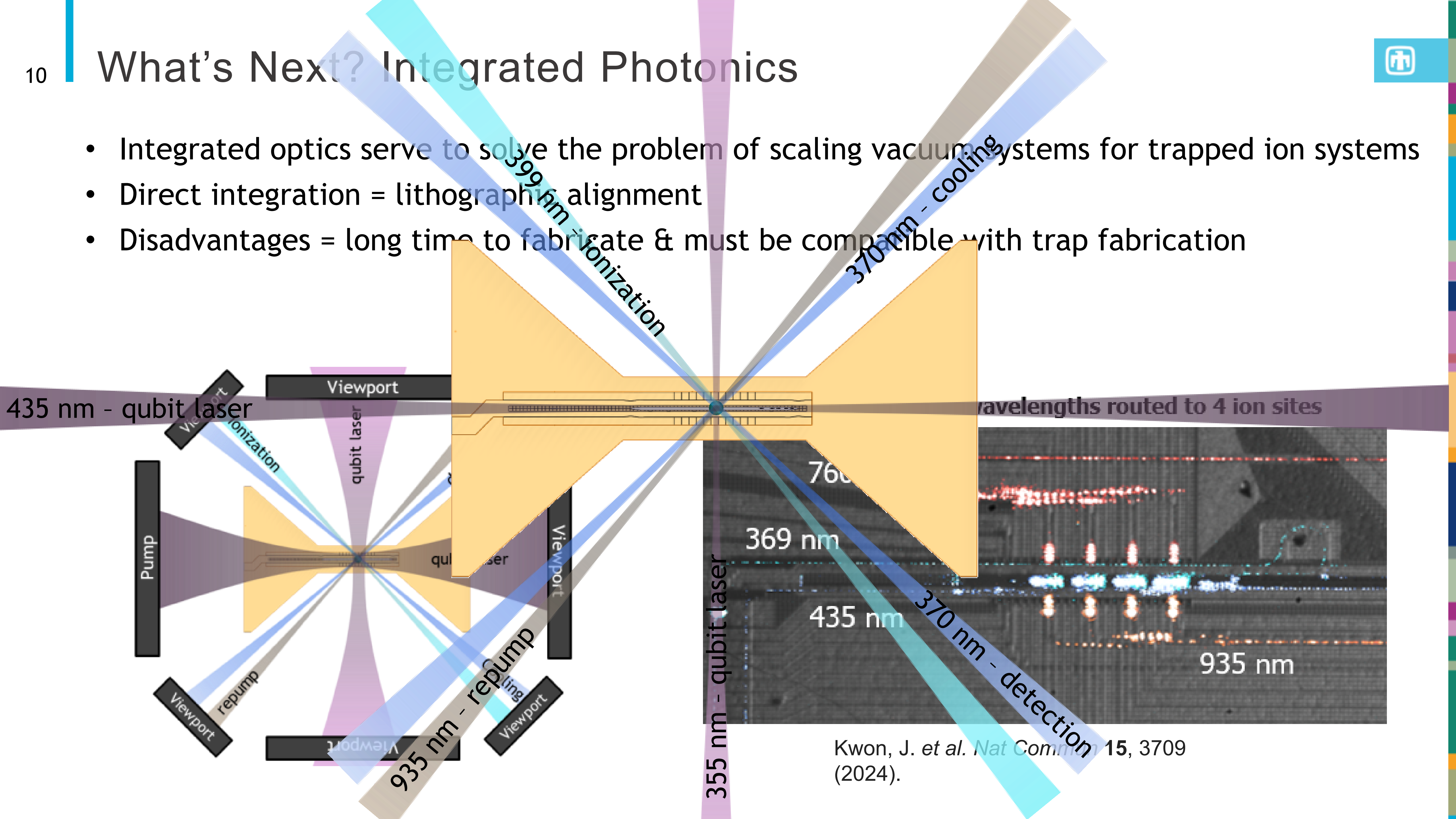
QSCOUT – Jackrabbit trap

Next Generation Traps – Increasing Optical Access



What's Next? Integrated Photonics

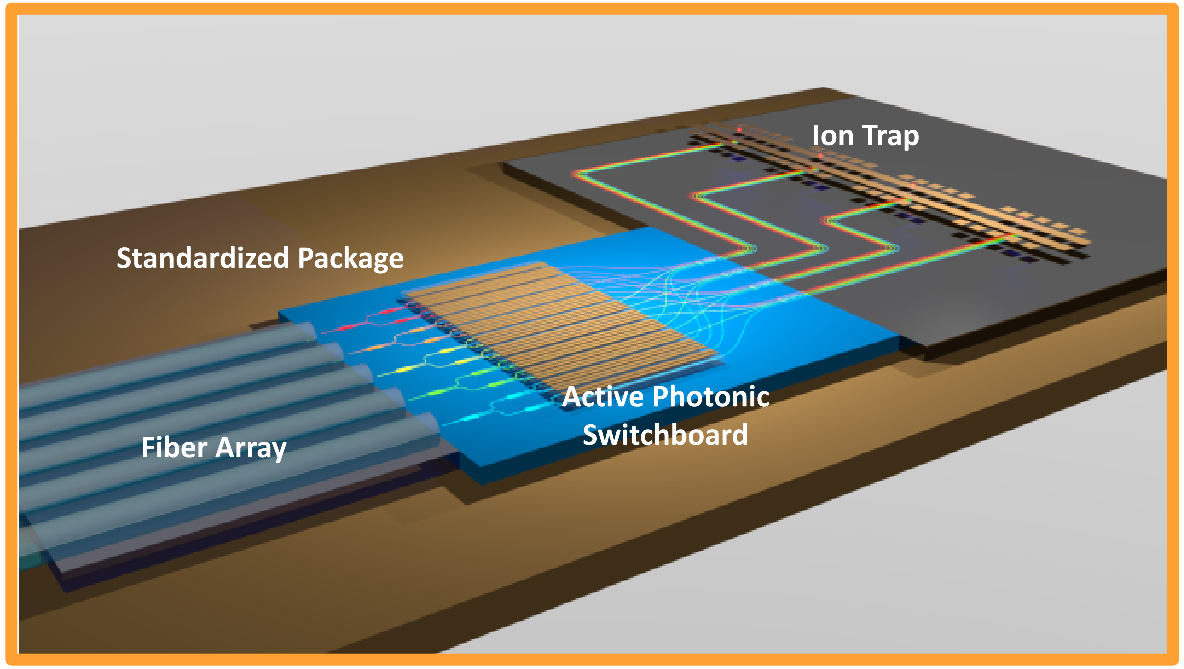
- Integrated optics serve to solve the problem of scaling vacuum systems for trapped ion systems
- Direct integration = lithographic alignment
- Disadvantages = long time to fabricate & must be compatible with trap fabrication

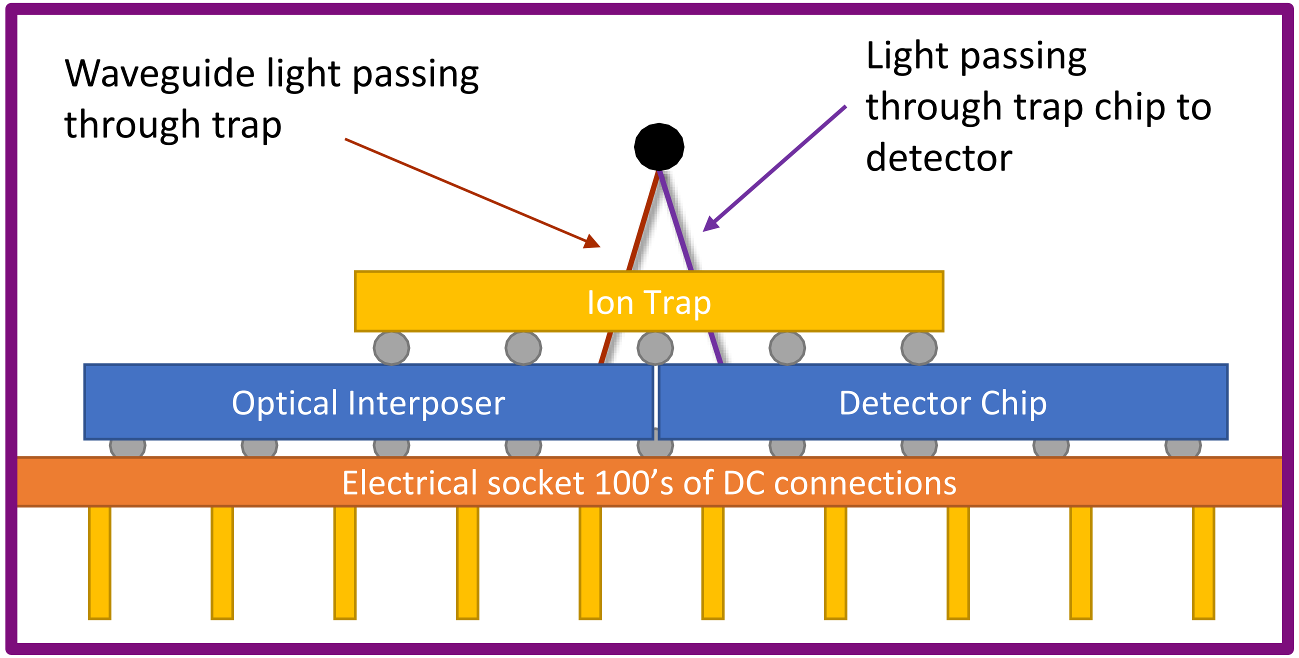


Kwon, J. *et al.* *Nat Commun* **15**, 3709 (2024).

Why Heterogenous Integration?

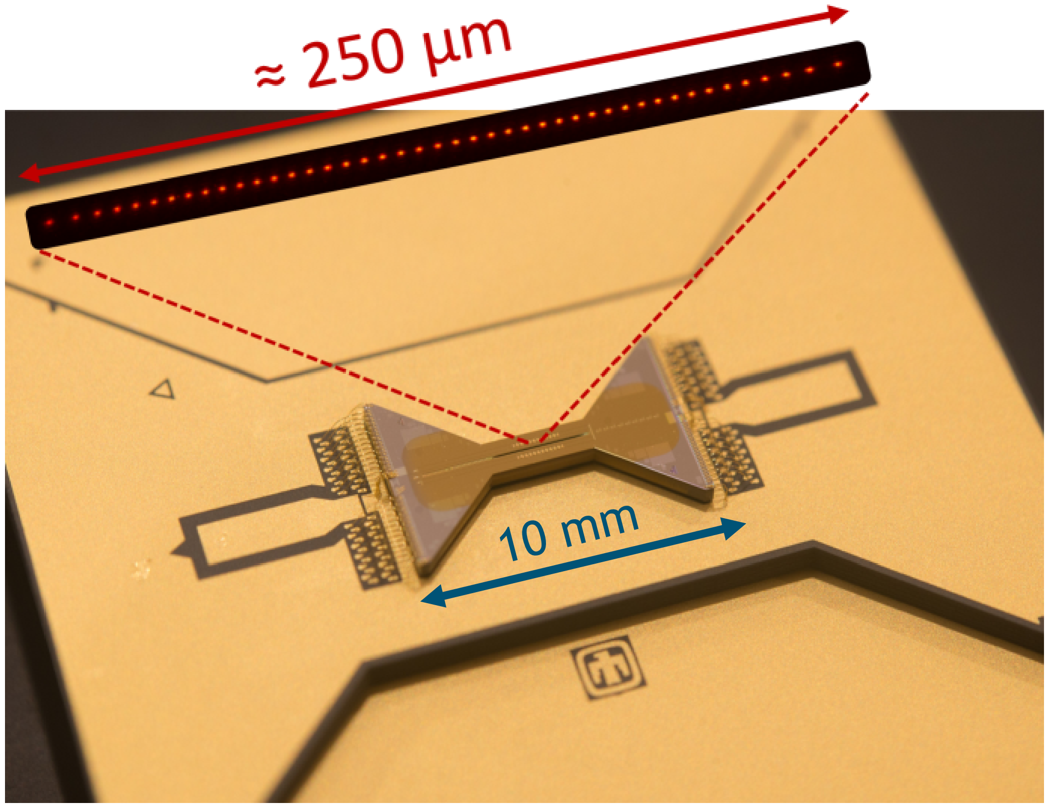
- By separating the pieces onto separate chips, we can enable faster development and more flexible designs
- Disadvantage: aligning separate pieces in a way that can survive a vacuum bake is hard
- Two different approaches:
  - A hybrid solution where exotic technology is off-chip = easier to integrate
  - The ion trap is completely separate from photonic (and other) technology

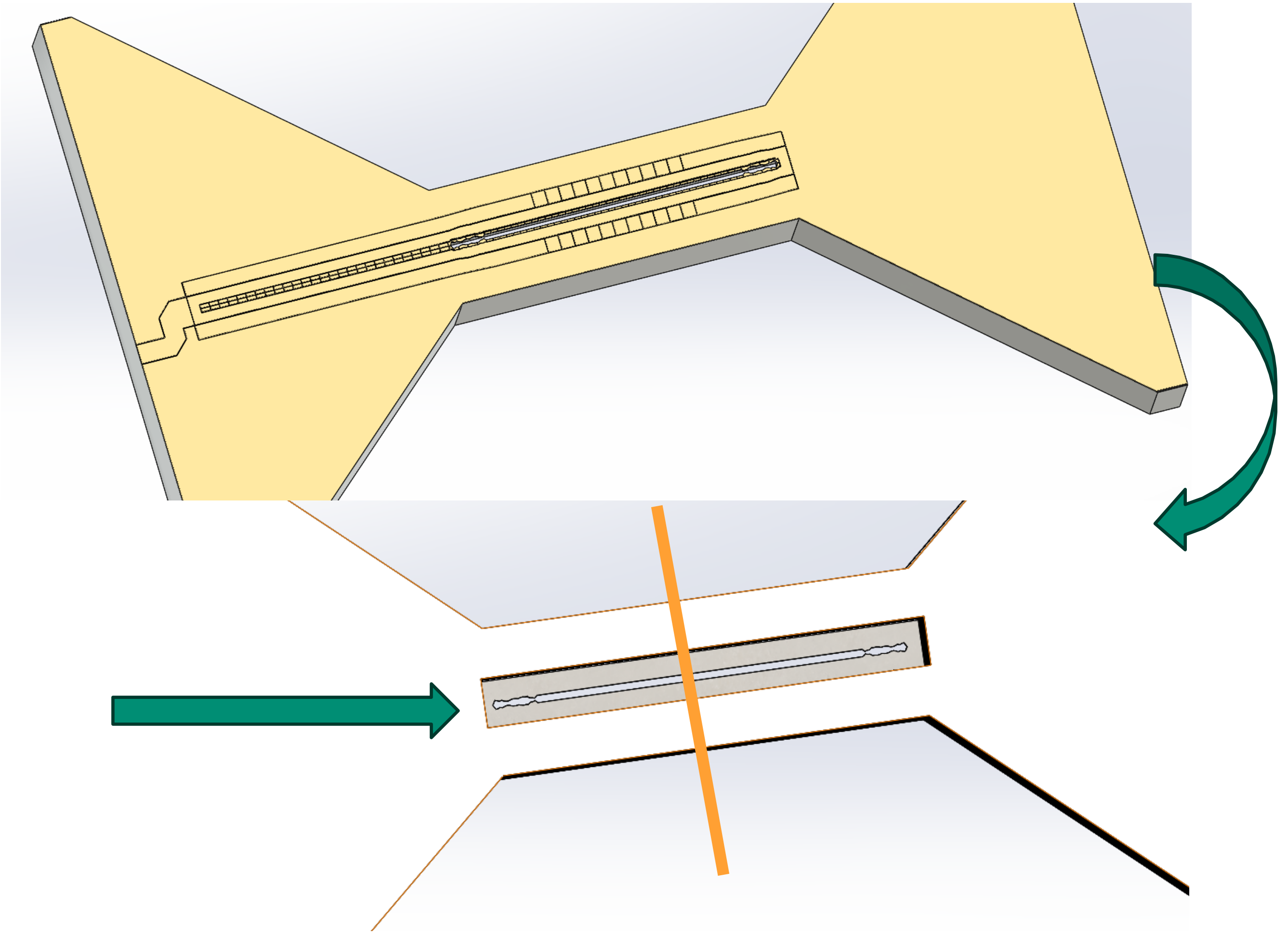




Heterogeneous Integration: Waveguides + Phoenix Trap

- Designed a 355nm waveguide chip to fit into a modified Phoenix trap
- “Micro-machining” a hole in the backside silicon to pass light through
  - Remaining handle silicon is 10um thick





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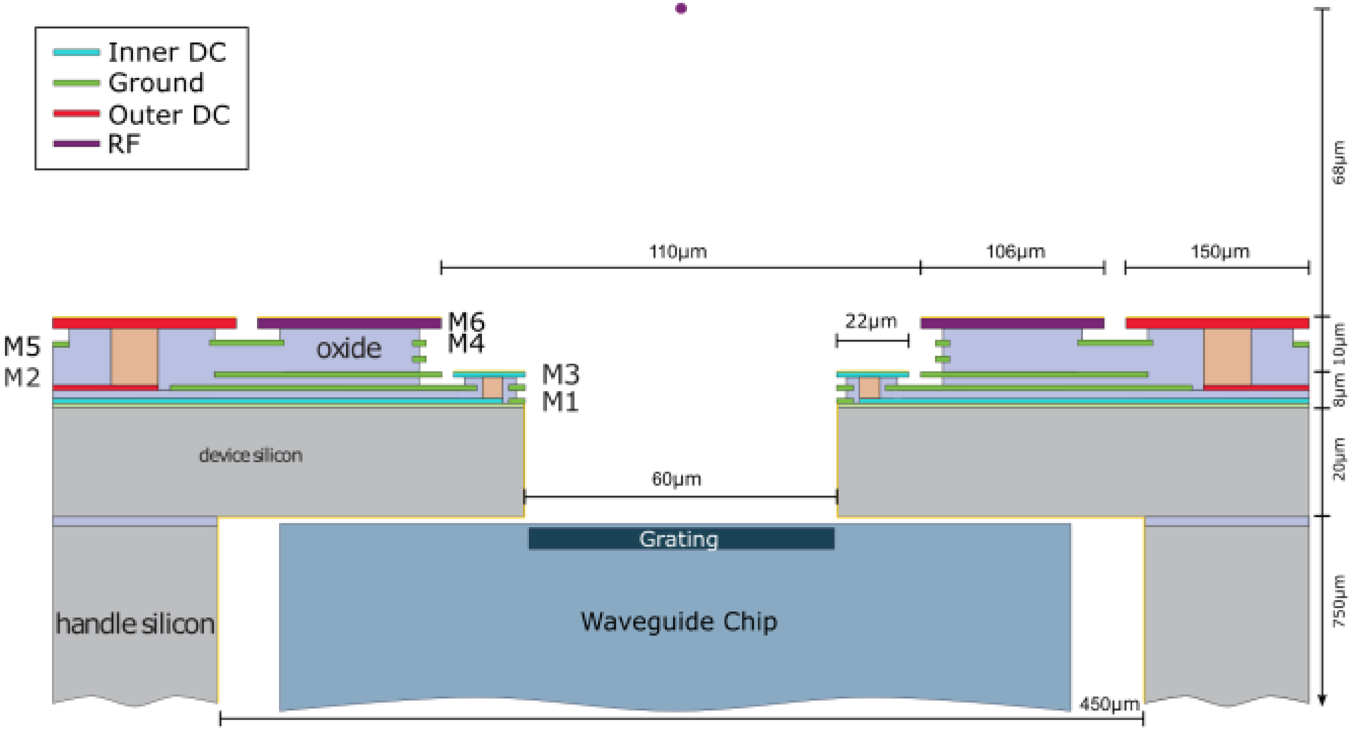
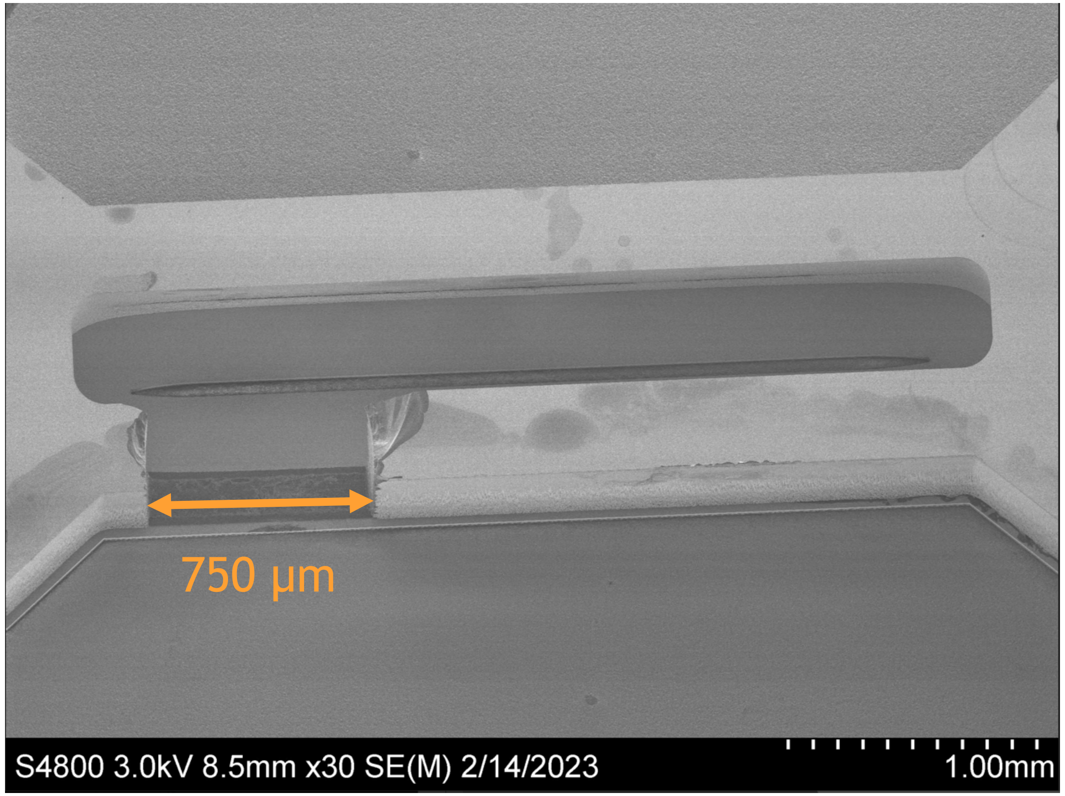
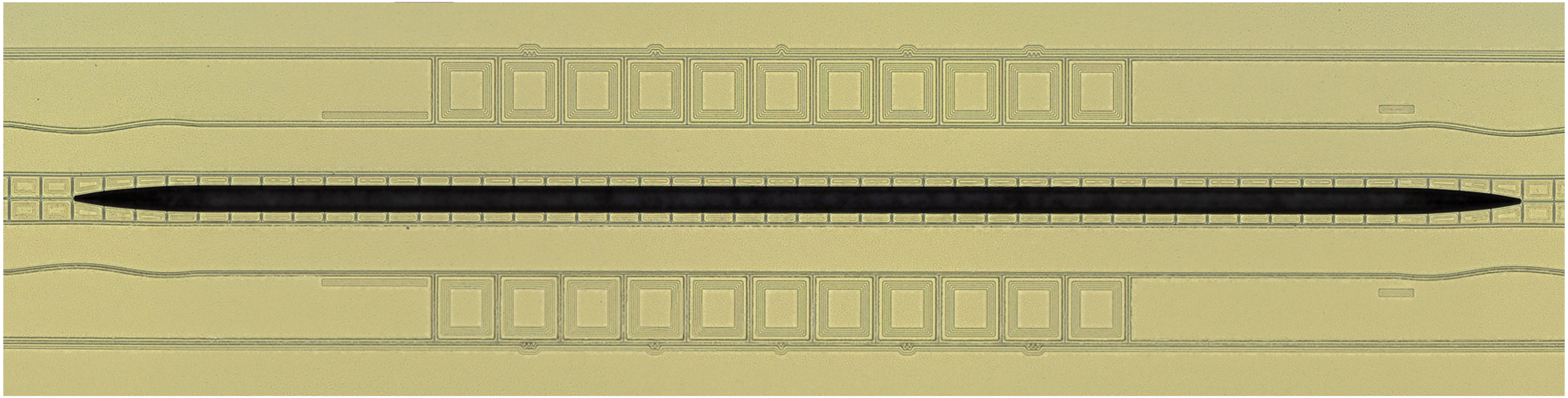




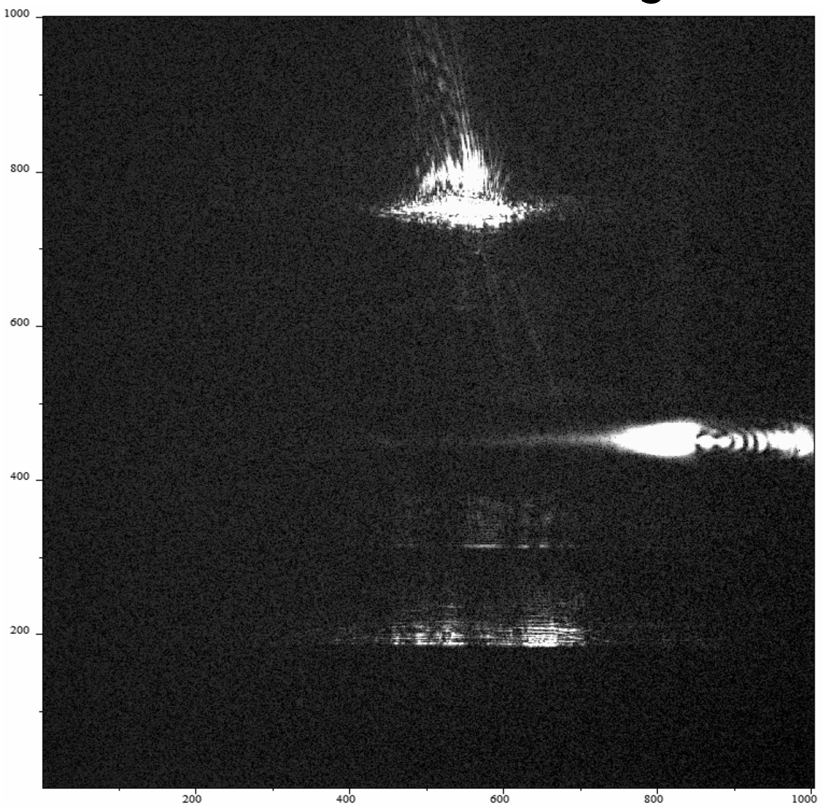
Characterize alignment using 355nm light and experiment

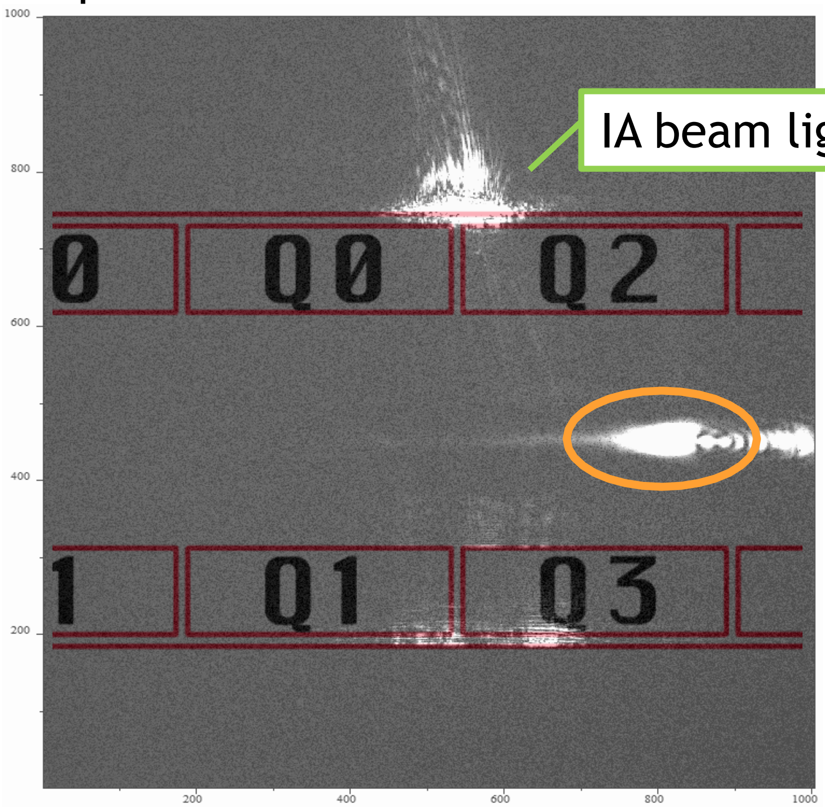


- Our trapped ion system has a high-zoom imaging system which allows for sub-micron precision in our measurements.
- We can track the light out of the waveguide with respect to the surface to determine how the waveguide shifts during a vacuum bake
  - Use the same wavelength across the surface to find the electrode edges
  - Track the light out of the waveguide as we change the focus of the imaging system getting snapshots as a function of height from the waveguide chip

Characterize alignment using 355nm light and experiment

355 light in focus at trap surface





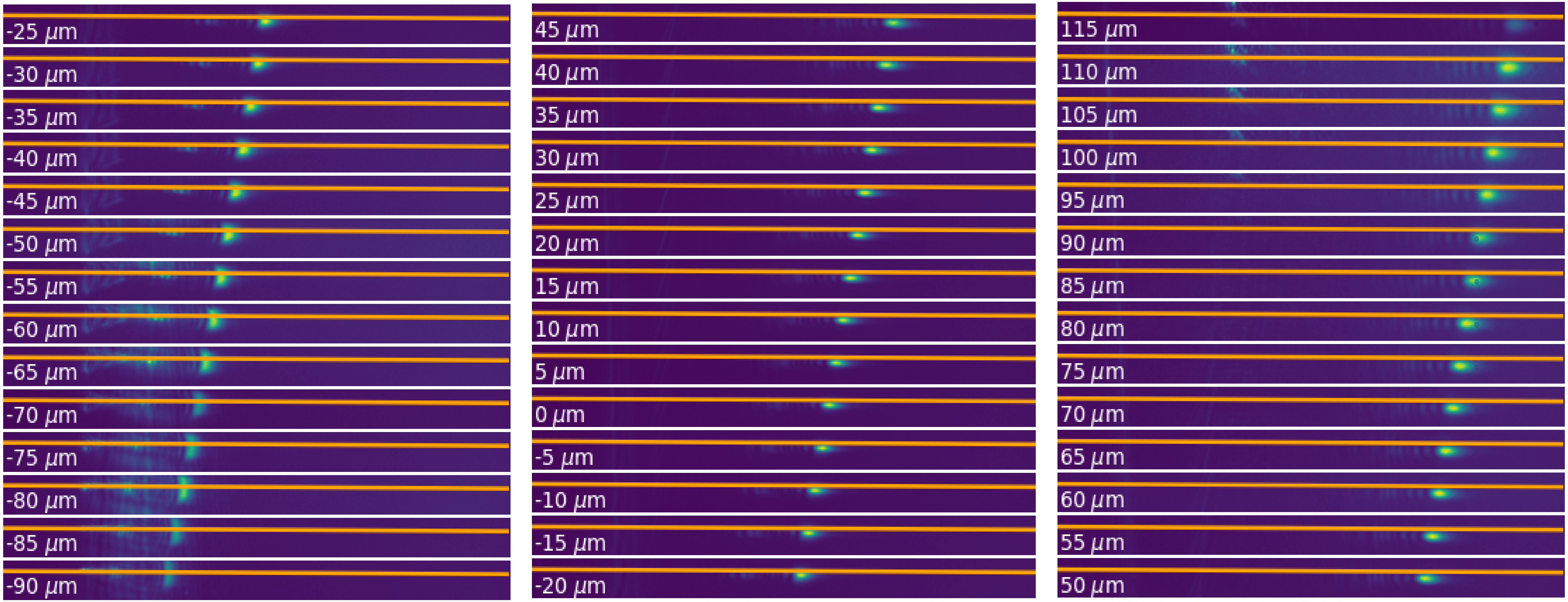
IA beam light on surface

Waveguide light

- By calibrating the imaging, we can track the output of the waveguide with respect to the ion trap chip
- Our magnification give us ~0.28um/pixel on the camera with ~1pixel uncertainty as long as the lens motors move in a single direction

Before baking track the output vs height from ion trap chip

- Using the location of the edges of the trap, we compare the output of the waveguide to the center of the trap

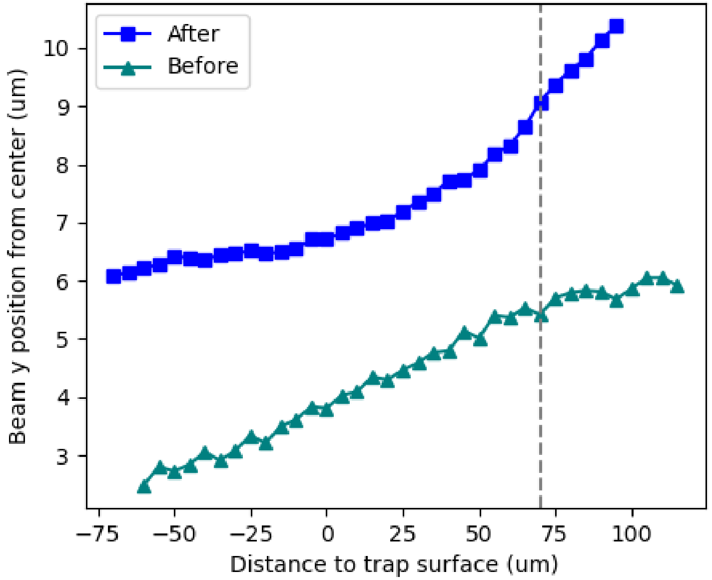


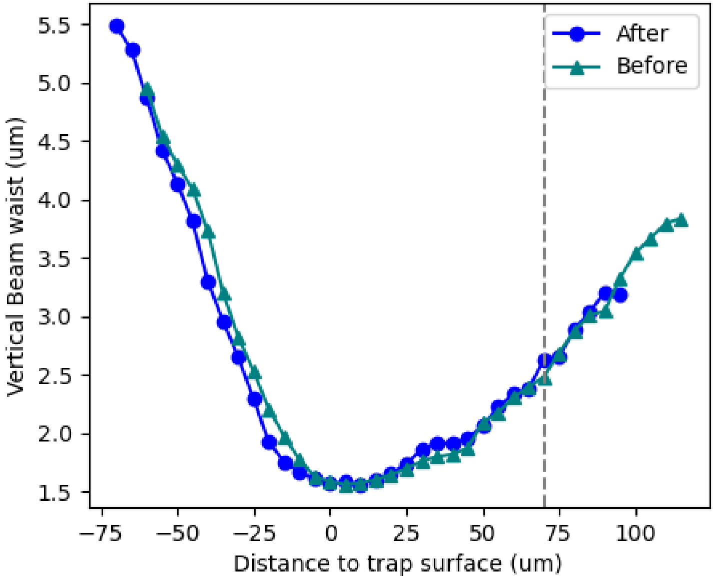
Compare output before and after bake

- Though AuSn solder should be resistant to shifting during a 150C bake, we see that the chip does shift after 5 days of baking
- We measure about 3 um of shift from a 5 day bake
- Need to develop a technique that reduces stress in the solder attach to minimize the motion

Before bake

After bake





Solder Will Move to Relax Stress

- A study has shown a relationship between temperature and stress a solder creep rate [1].

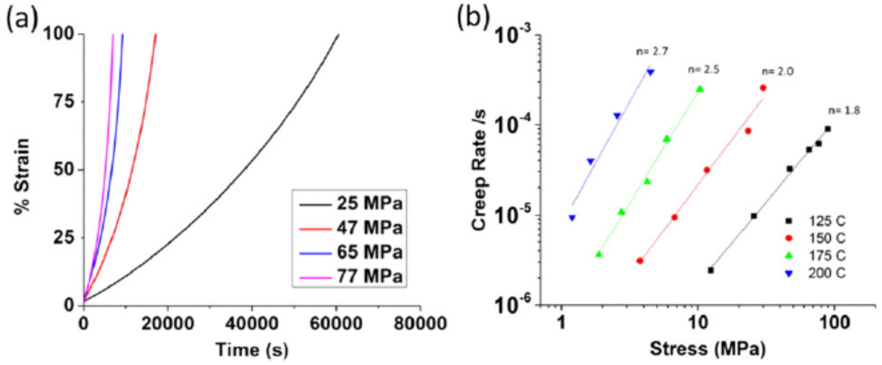
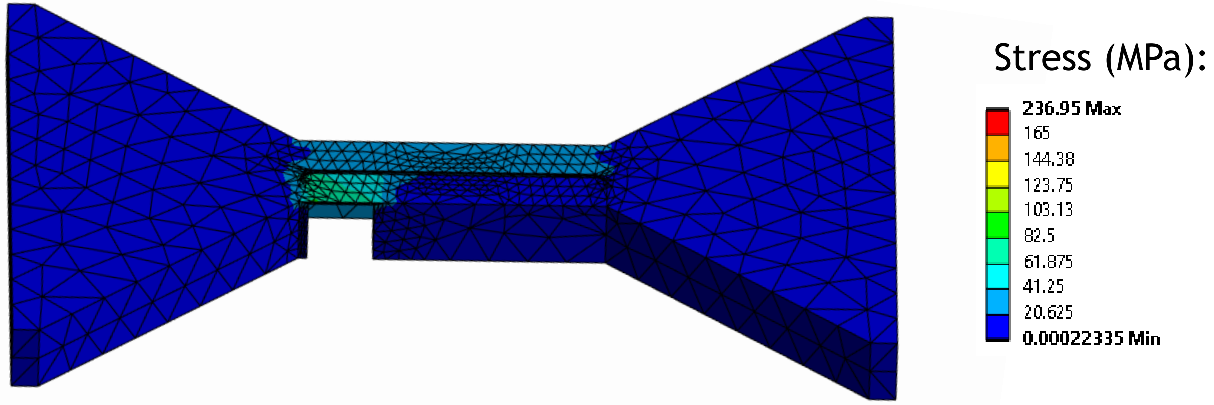


Fig. 3. a) Creep curves of AuSn at 125 °C, truncated at 100% strain, and b) creep rates of AuSn between 125 and 200 °C. The power law stress exponent, n, is indicated for each temperature.

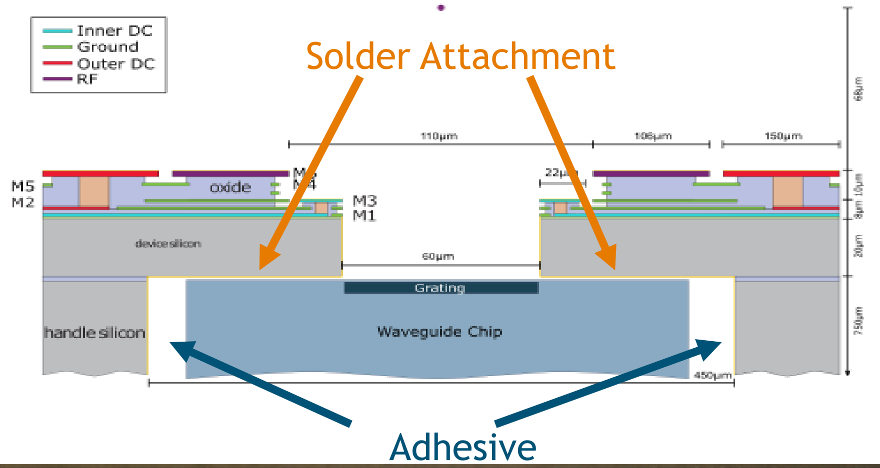
- For AuSn that melts at 280 °C, the temperature range of 125 to 200 °C represents a homologous temperature, T / TM, range of 0.72 to 0.86
- We know that 150 C falls exactly here which is demonstrated in this paper to incur creep.
- The region where the waveguide is mounted is suspected to have the highest stress, suggesting this cause

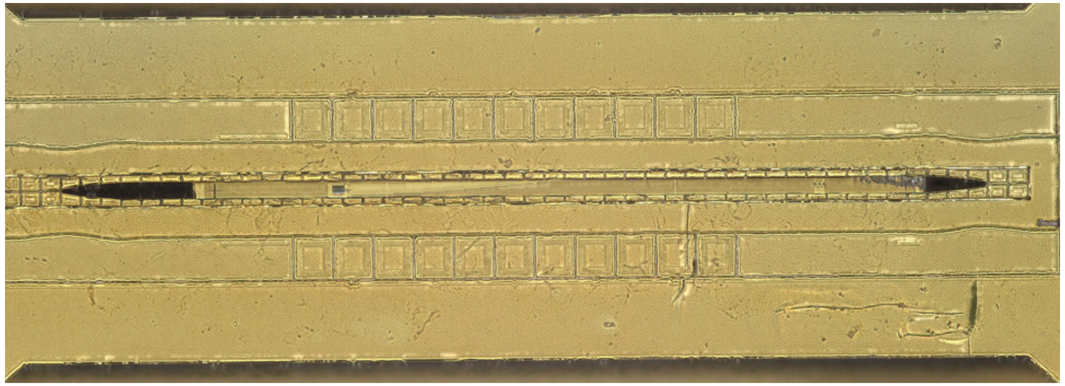


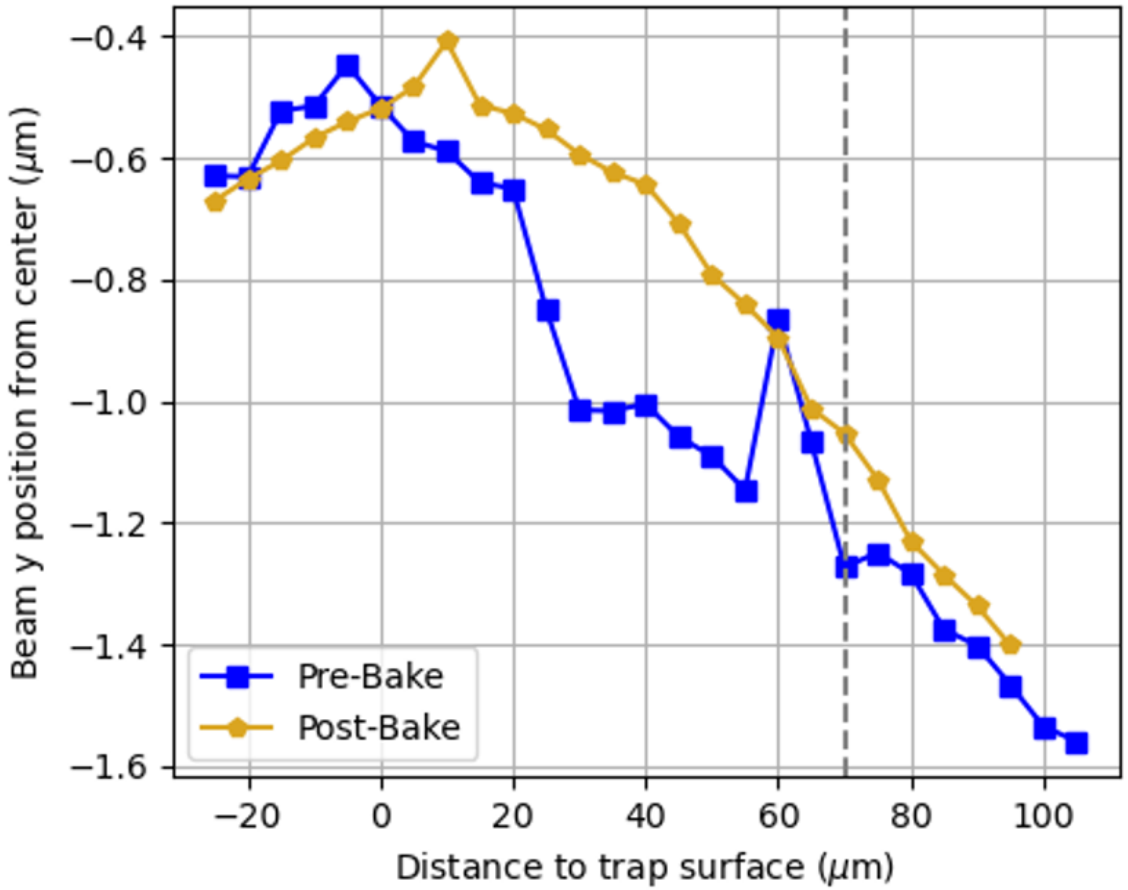
[1] J.W. Elmer, R.P. Mulay,, Scripta Materialia, vol. 120, pp. 14-18, 2016.

Reinforcing the Solder with Adhesive

- We can use an established HI practice and underfill the soldered piece with an adhesive
- Trap surface is too damaged for trapping
- Reduced the amount of shift to < 0.5 µm







Quantum Scientific Computing Open User Testbed (QSCOUT)

U.S. DEPARTMENT OF ENERGY
Office of Science

Sandia National Laboratories

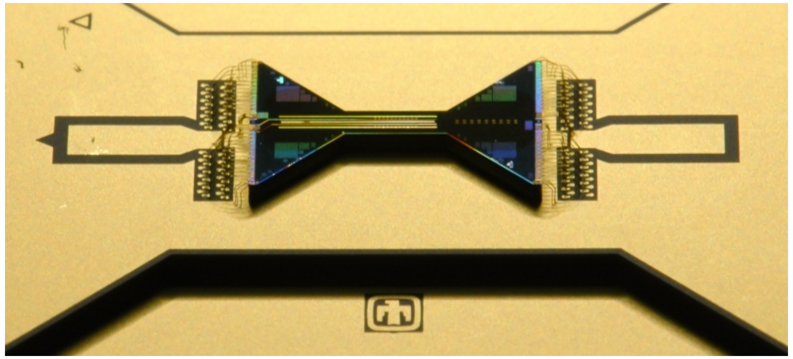
QSCOUT

qscout.sandia.gov
qscout@sandia.gov

JAQAL

A quantum computing testbed based on trapped ions for the greater quantum scientific community

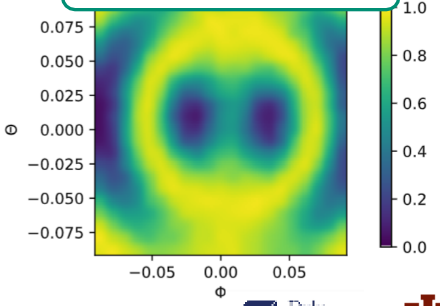
QSCOUT grants low-level access to quantum machines for free to researchers around the world to study their proposed research.



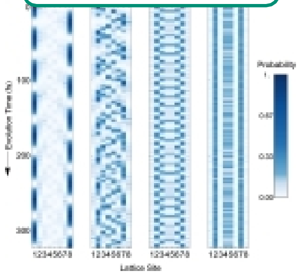
QSCOUT goals:

- Greater understanding of how quantum machine work (and fail)
- Study new techniques for encoding and compiling quantum circuits
- Construct a roadmap for building larger, more sophisticated machines

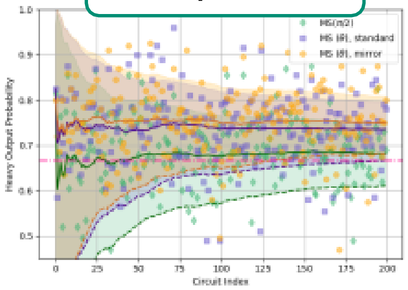
Error mitigation



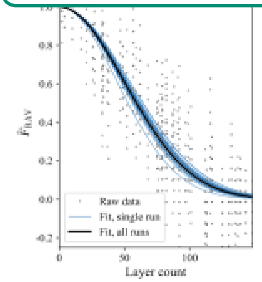
Simulation



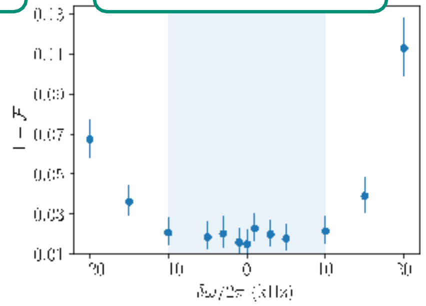
Compilation



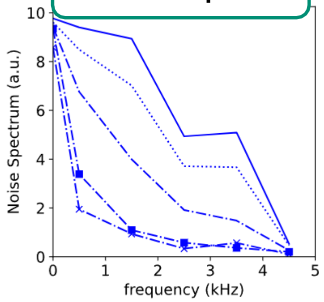
Benchmarking



Robust gates



Noise spec.



1. *Quantum* **7**, 1006 (2023)
2. *J. Phys. Chem. Lett.* **14**, 7256 (2023)
3. *in preparation (2024)*
4. *Quantum* **7**, 997 (2023)
5. *Phys. Rev. Appl.* 22, *014007 (2024)*
6. *in preparation (2024)*

Oak Ridge National Laboratory — Duke Quantum Center — Indiana University — Infleqtion — Berkeley University of California — Johns Hopkins Applied Physics Laboratory

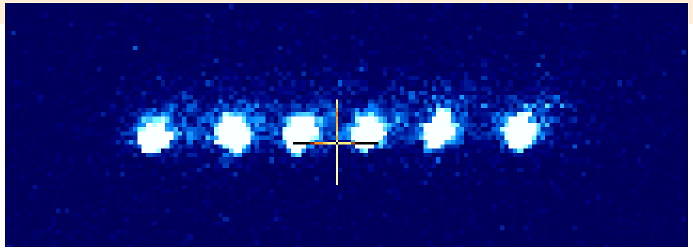
Current Specifications of the Machine

Current Specs:

- 6 ions, fully connected, individually addressable
- >0.96 fidelity two-qubit gate (any pair)
- >0.997 fidelity single-qubit gate
- >0.998 fidelity state preparation and measurement
- Can provide custom calibrations
- Can specify phase and amount of entanglement for 2-qubit Mølmer-Sørensen[1] ($\sigma_i \times \sigma_i$) gate (use as little entanglement as needed)

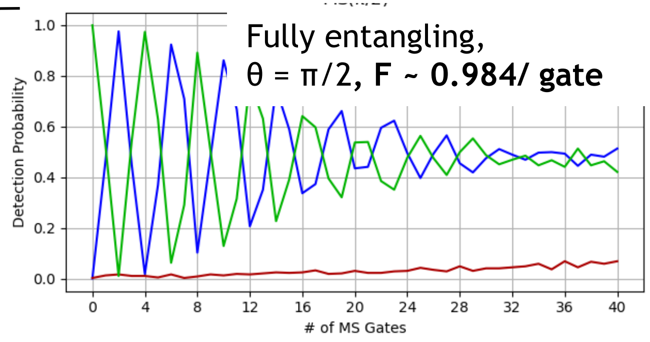
[1]Mølmer and Sørensen, *PRL* **82,** 1835 (1999)

Clark *et al.* *IEEE TQE* 2, 3102832 (2021)

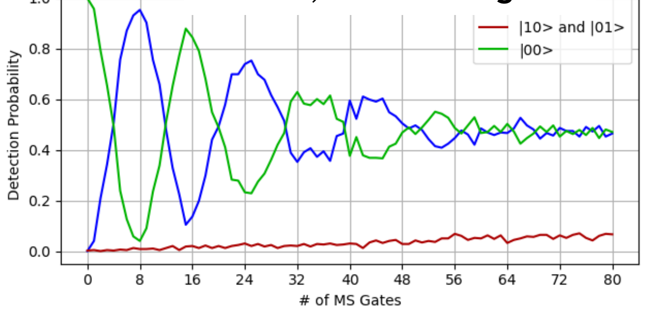


Repeated MS gates of different entangling angles

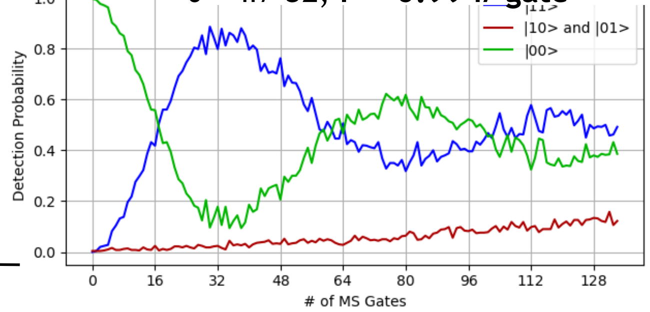
Fully entangling, θ = π/2, **F ~ 0.984/ gate**



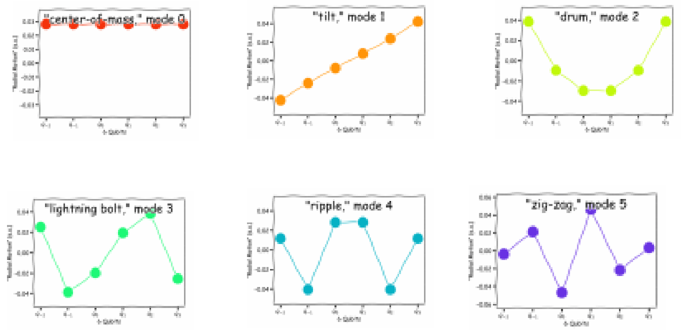
θ = π/8, **F ~ 0.992/ gate**



θ = π/ 32, **F ~ 0.994/ gate**



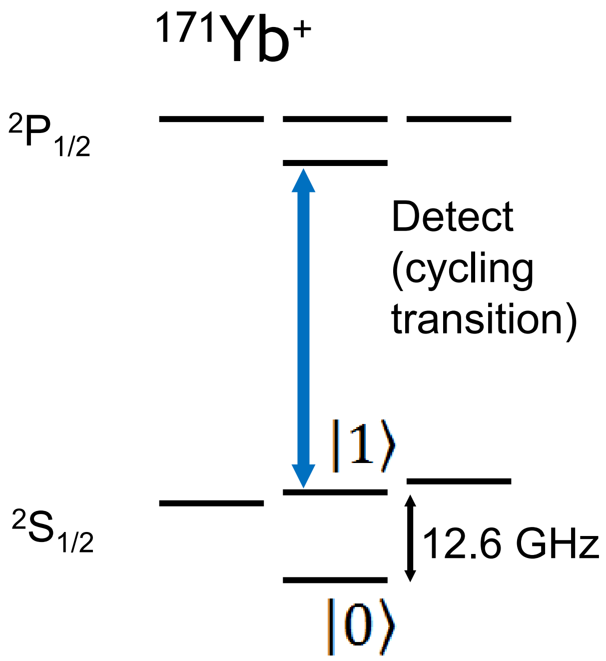
Motional modes of 6-ion chain

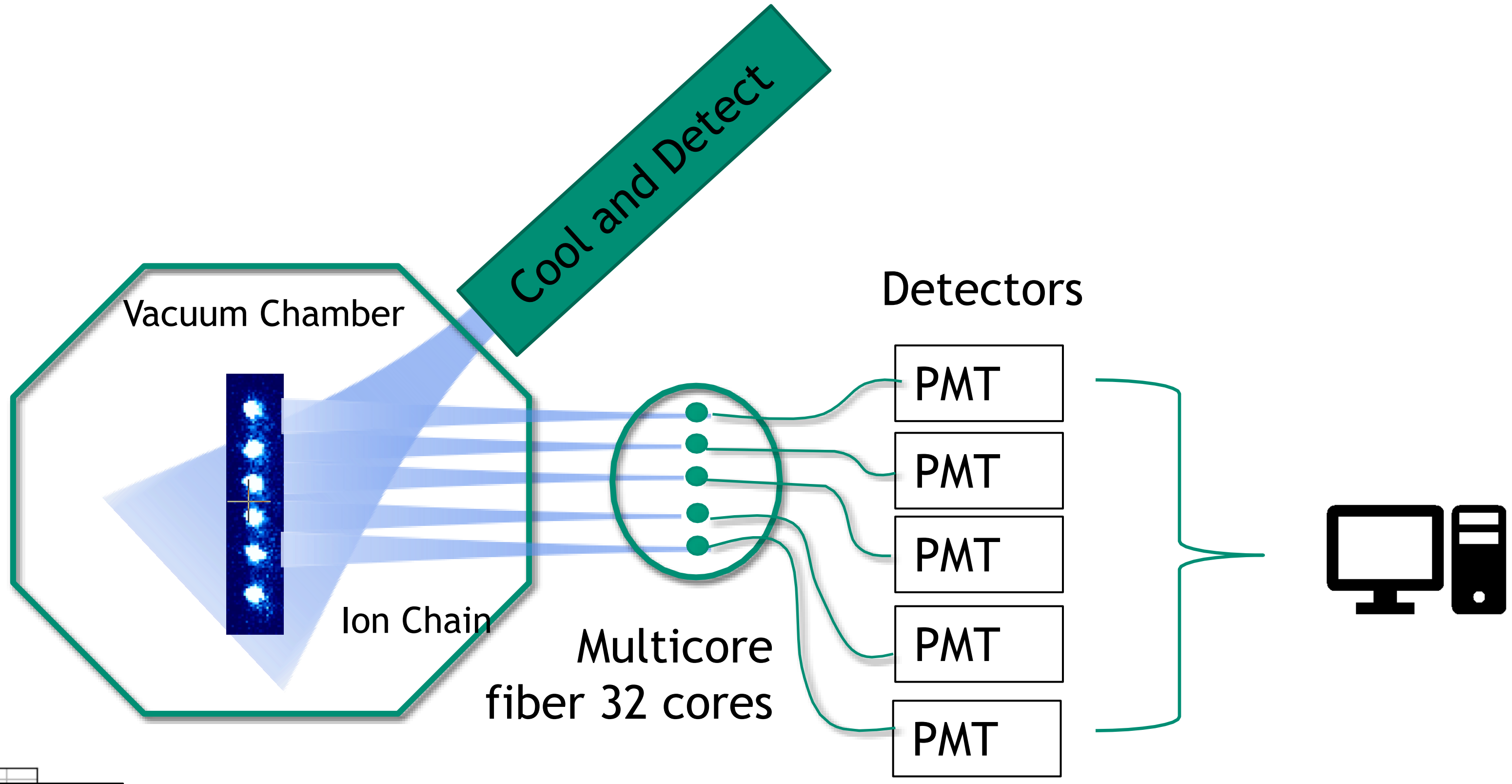


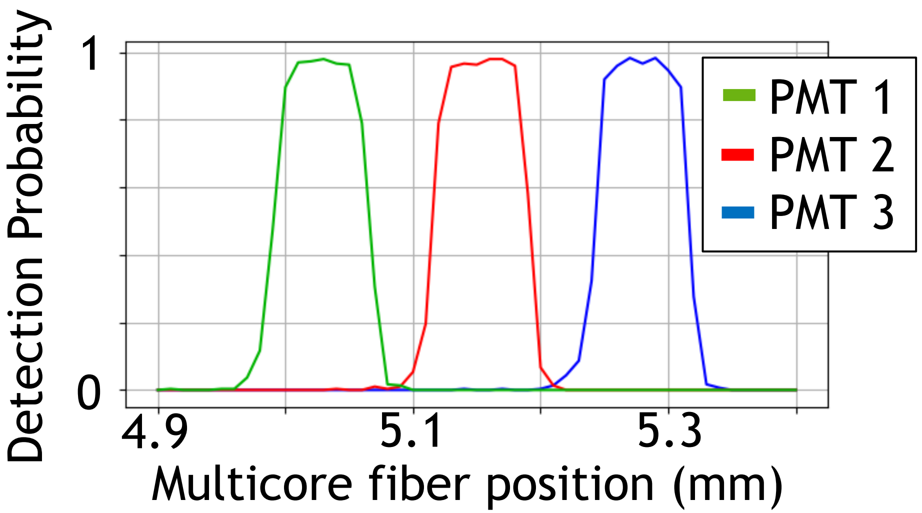
6-ion chain MS gate pairs fully entangled estimated state fidelities

Pair index	q[a]	q[b]	Mode index	Detuning (kHz)	Fidelity (%) [+1%, -2%]
0	0	1	5	43	97.1
1	2	0	4	30	95.6
2	2	1	5	35	96.8
3	0	3	5	36	95.4
4	1	3	4	35	97.8
5	2	3	4	30	93.5
6	0	4	2	22	95.9
7	1	4	3	20	95.7
8	2	4	3	26	95.9
9	3	4	3	26	95.4
10	0	5	3	23	94.0
11	1	5	2	22	94.7
12	2	5	3	25	94.7
13	3	5	2	20	93.6
14	4	5	2	20	95.2

Light from each ion is directed to its own detector





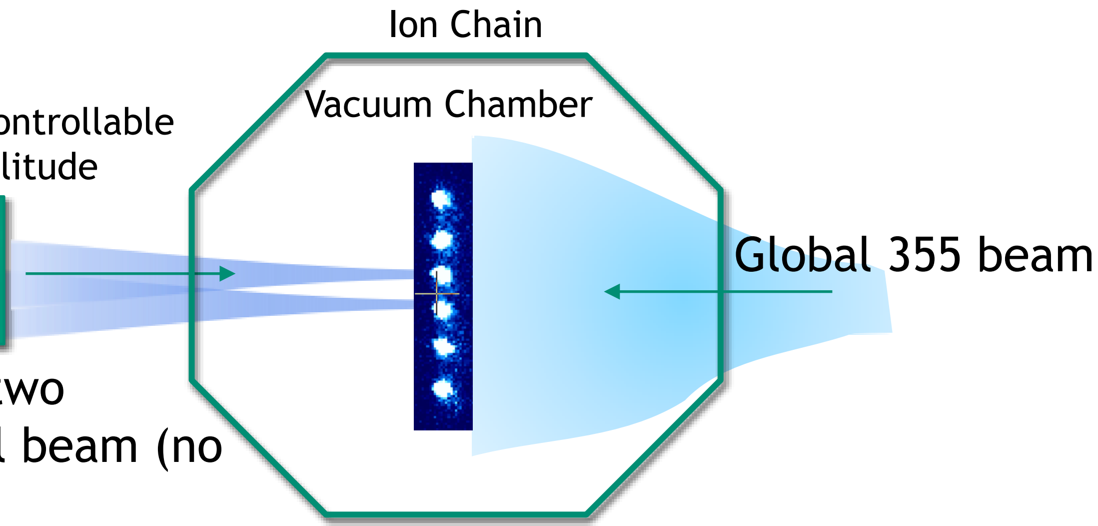


- During detection, light from each ion is collected separately
- Depending on # of photons collected, ion is determined to be bright (1) or dark (0)

Copropagating or counterpropagating configurations as needed

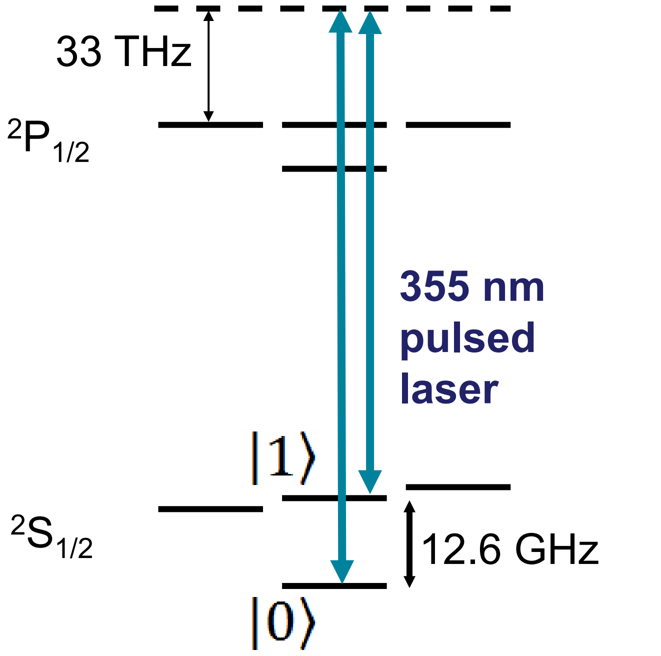
32 channel AOM, each channel controllable in frequency phase and amplitude

Individual 355 nm beams



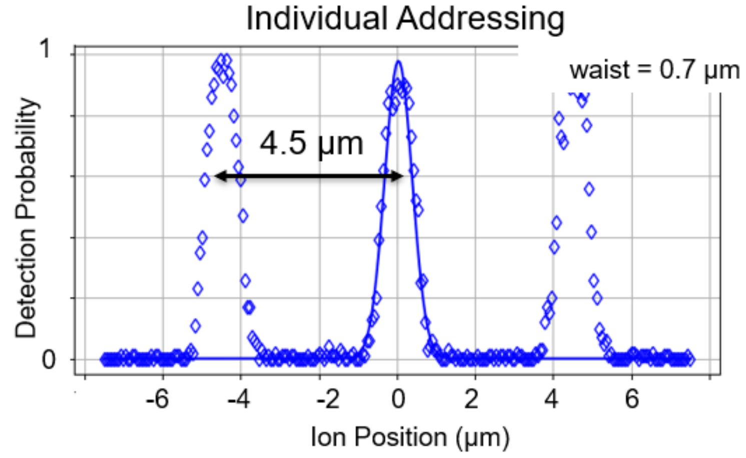
Single qubit gates, use two tones on each individual beam (no global beam)

Each spin flip needs two tones



Two Qubit Gates with Trapped Ions:

- Mølmer-Sørensen[1] σ_i x σ_j entangling interaction (choose your basis)
- Three frequencies required, counterpropagating configuration required (2 freq on individual channel, 1 freq on global channel)
- Any pair of ions can be illuminated, excite and de-excite motion of whole chain, only illuminated ions experience spin flip needed for entanglement

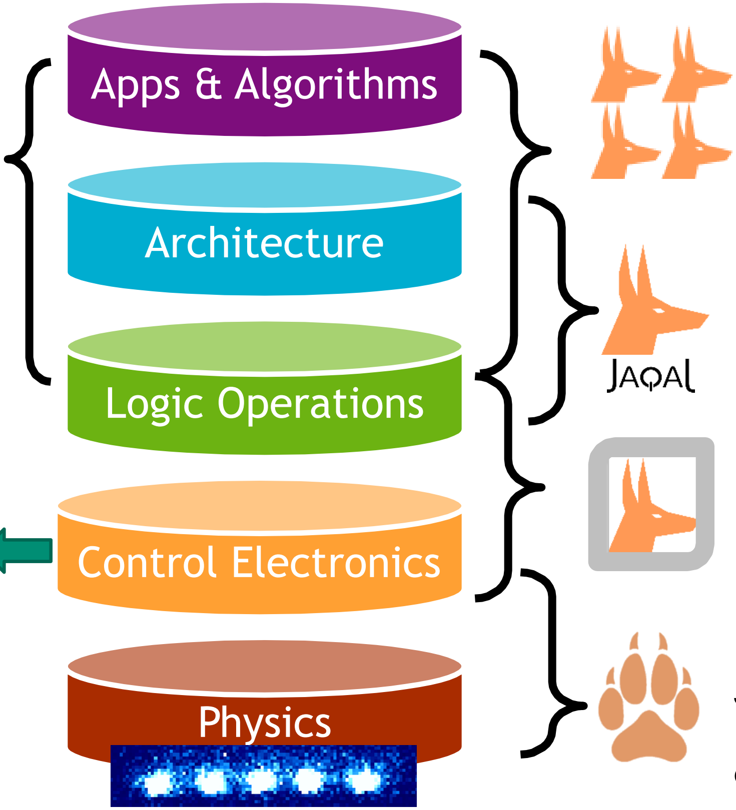


[1]Mølmer and Sørensen, *PRL* **82,** 1835 (1999)

QSCOUT uses Jaqal programming language

Just Another Quantum Assembly Language

Superstaq
Physics-aware compilation
C. Campbell, *et al.*, *2023 IEEE QCE*, 1020 (2023)



JaqalPaq
meta programming with python

Jaqal
Specify operations

Jaqal Application Framework
Hardware interface

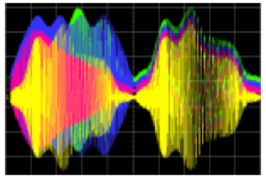
JaqalPaw
Pulse-level control

B. C. A. Morrison, *et al.* *2020 IEEE QCE*, 402 (2020)

Custom-designed RFSoC

- RF to single- and multi-channel AOM
- 8 channels, synchronized
- 2 tones per channel
- Cubic splines for

OCTET

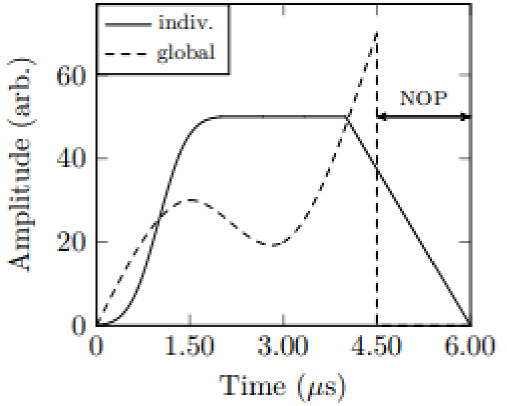


- Amplitude
- Frequency
- Phase

D. S. Lobser, *et al.*, *2022 IEEE QCE*, 320 (2022)

Pulse level control via **PulseData** class

```
def gate_G(self, qubit):
    return [PulseData(qubit, 2e-6,
                      amp0=(0,9,41,50)),
            PulseData(qubit, 2e-6,
                      amp0=50),
            PulseData(qubit, 2e-6,
                      amp0=(50,0)),
            PulseData(GLOBAL_BEAM, 4.5e-6,
                      amp0=(0,30,20,70))]
```



D. Lobser, *et al.*, *arXiv:2305.02311* (2023)

Scientific progress through low-level access: Infleqtion

Low-level native-gate aware compilation techniques to improve circuit performance

Superstaq Infleqtion

Benjamin Hall, Victory Omole, Rich Rines, Pranav Gokhale (PI)

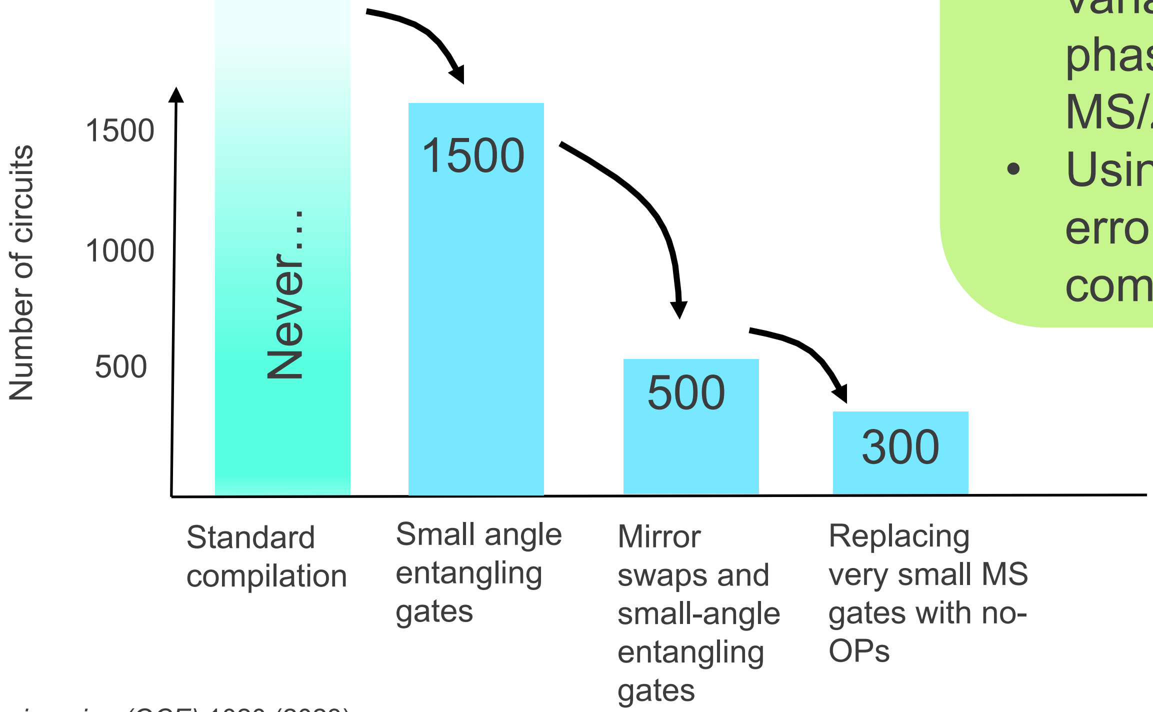
Why QSCOUT?

- Fully parametrized 2-qubit gates
- Pulse-level access to define new gate variants (ZZ and phase agnostic MS/ZZ gates)
- Using physical gate errors to inform compilation choices

Other user teams have incorporated Superstaq optimizations

User team	Optimization type	Benefit provided
LCN London Centre for Nanotechnology	ZZ(θ) instead of MS(π/2, ∅)	Higher fidelity circuits, Shorter circuits
Oak Ridge National Laboratory, UC Davis	Fewer single qubit gates	Shorter circuits Simpler circuits
ETH zürich	ZZ(θ) and mirror swaps	Higher fidelity circuits Shorter circuits

Given our error rates, compared how many circuits are required to show a convincing Quantum Volume = 2^4 measurement for different methods of compilation



Campbell *et al.*,*2023 IEEE International Conference on Quantum Computing and Engineering (QCE)*,1020 (2023).
C. G. Yale, R. Rines, V. Omole, B. Thotakura, *et al.*, *in preparation* (2024)

Scientific progress through low-level access: Oak Ridge

Characterizing and Mitigating Coherent Errors in a Trapped Ion Quantum Processor Using Hidden Inverses

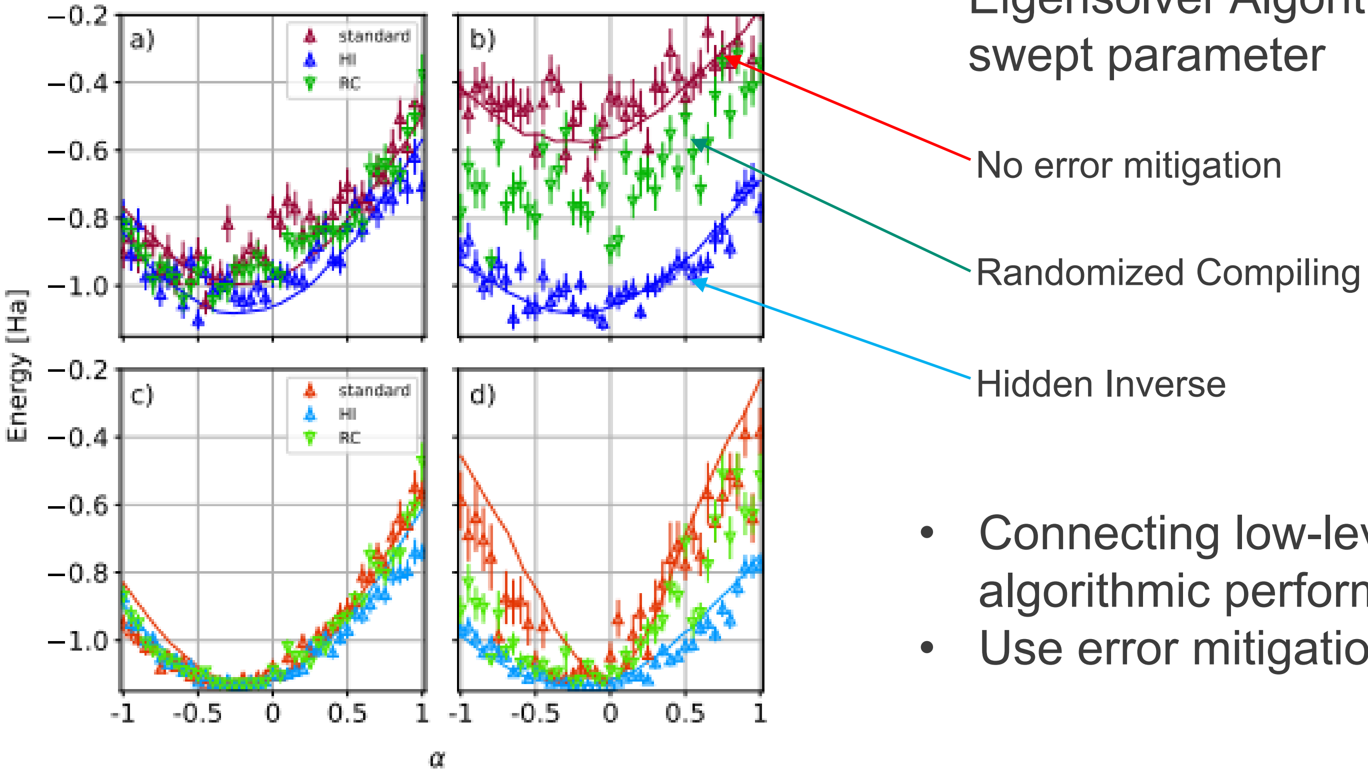
Oak Ridge National Laboratory

Quantum **7**, 1006 (2023)

S. Majumder, T. D. Morris, Raphael Pooser (PI)

No injected error

Under rotation of 2-qubit gate 0.5 rad



Variational Quantum Eigensolver Algorithm with swept parameter

Why QSCOUT?

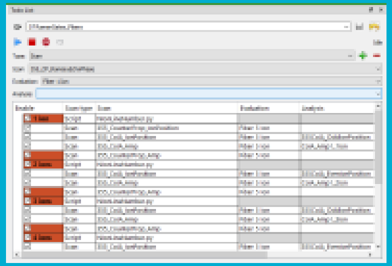
- Purposefully injected noise (different types)
- Able to run sequences back to back

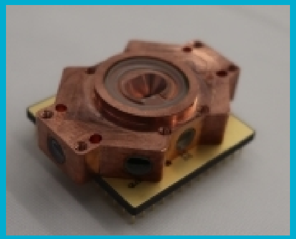
- Connecting low-level characterization techniques to higher level algorithmic performance
- Use error mitigation to determine types of errors in the system

Moving forward, 3 main goals for QSCOUT:

1. Improving uptime of the machine and increasing user base
2. Improving performance of the machine
3. New features and access

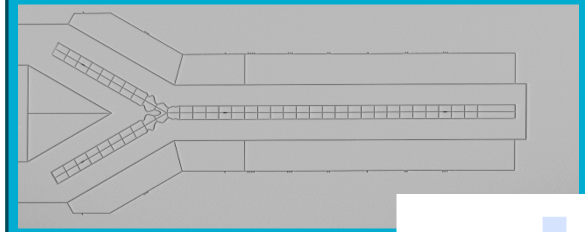
- Automated calibration
- Increased number of systems
- More representative noise models

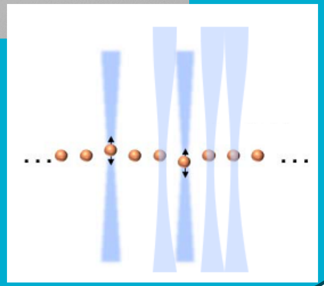




- More ions
- Higher fidelity operations
- Lower heating rates/improved cooling
- Fast feedback for drift control

- Mid-circuit measurements
- Multi-ion entangling gates
- Fast feedback
- User request





THANKS TO THE CURRENT TEAM

Experiments

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U.S. DEPARTMENT OF ENERGY
Office of Science

DARPA

LPS
The Laboratory for Physical Sciences

https://www.sandia.gov/quantum/