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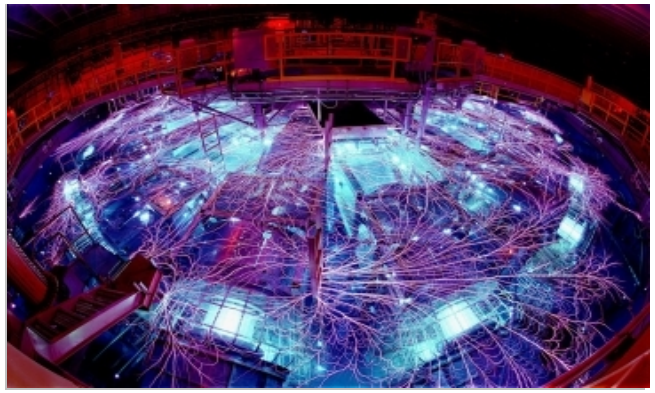

The Effects of Threshold Voltage and Number of Fins per Transistor on the TID Response of GlobalFoundries 12LP Technology

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MICROELECTRONICS RELIABILITY AND QUALIFICATION WORKSHOP (MRQW) 2023

U.S. Department of Defense

U.S. DEPARTMENT OF ENERGY

National Nuclear Security Administration

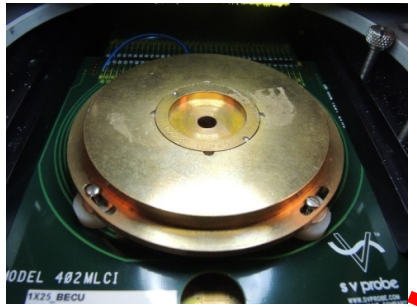
Outline

- Motivation
- Experimental Details
  - Set-up & Total Ionizing Dose (TID) Test Method
- Results
  - TID Response vs
    - Device Threshold Voltage
    - Number of Fins per Transistor
- Conclusions

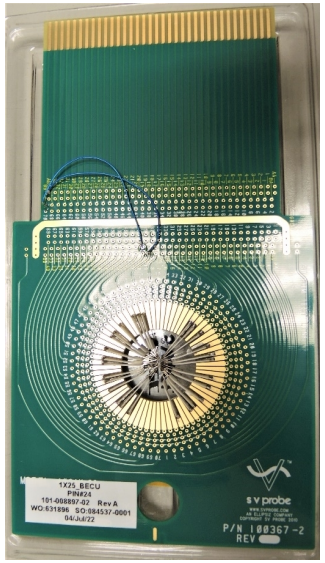
Motivation

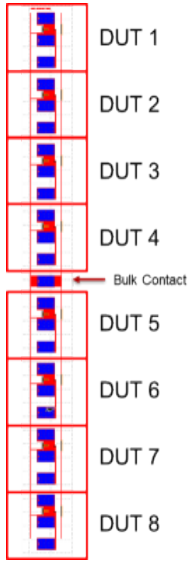
- GlobalFoundries (GF) 12LP 12nm bulk FinFET technology being studied for many rad-hard programs
- Only a few TID studies have been reported
- TID effects on Regular Threshold Voltage (RVT) digital transistors: Neuendank, 2022 and Wallace 2021
- The effect of the number of fins per transistor in charge-trap transistors: Brewer, 2021
- Performance began to degrade around 500 krad in a complex system-on-a-chip: Taggert, 2022
- We report the first TID results on a wide range of threshold voltage variants and number of fins per transistor

TID Experimental Set-Up



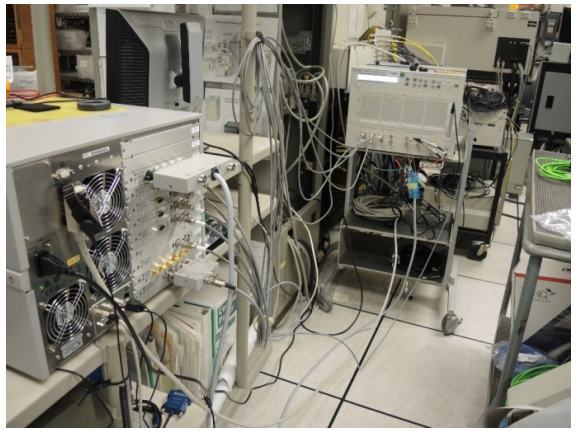
Collimator on Probe Card





1 x 25 Pin Probe Card

ARACOR 10KeV X-ray Irradiator



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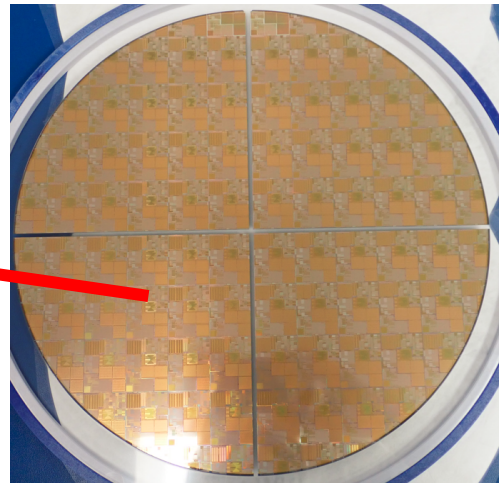
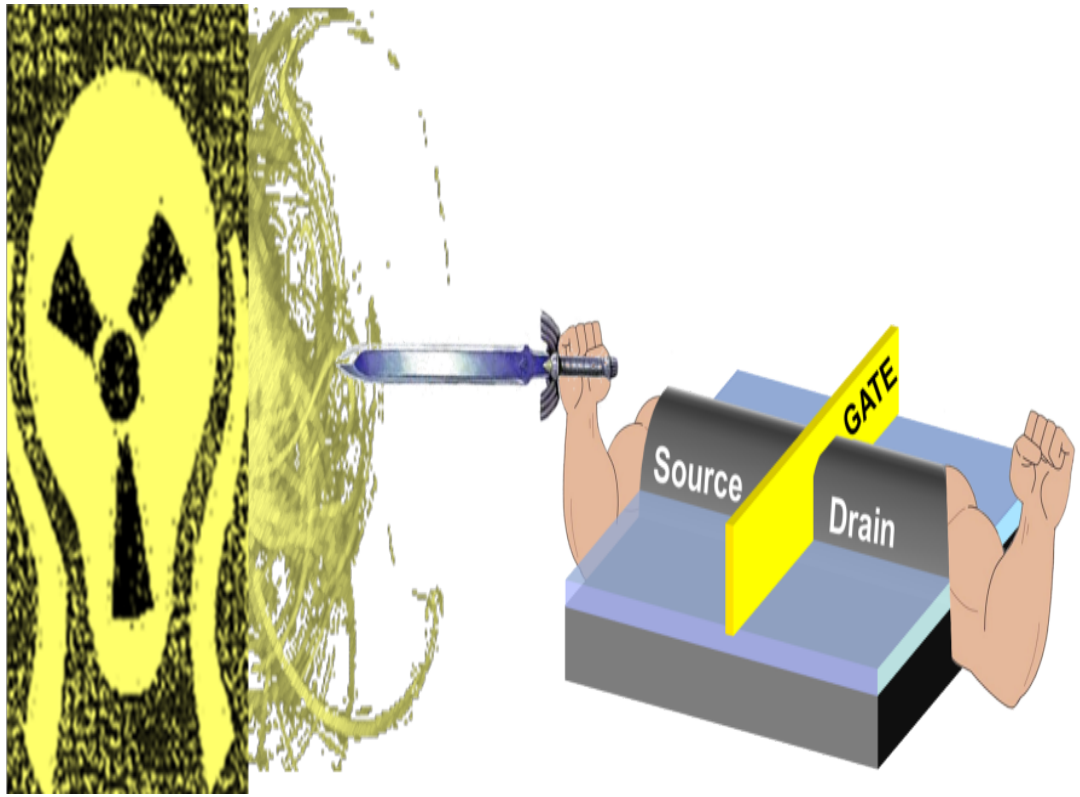


Quartered 12-inch Wafer

Structures Tested

n-type FinFETs with min L_G

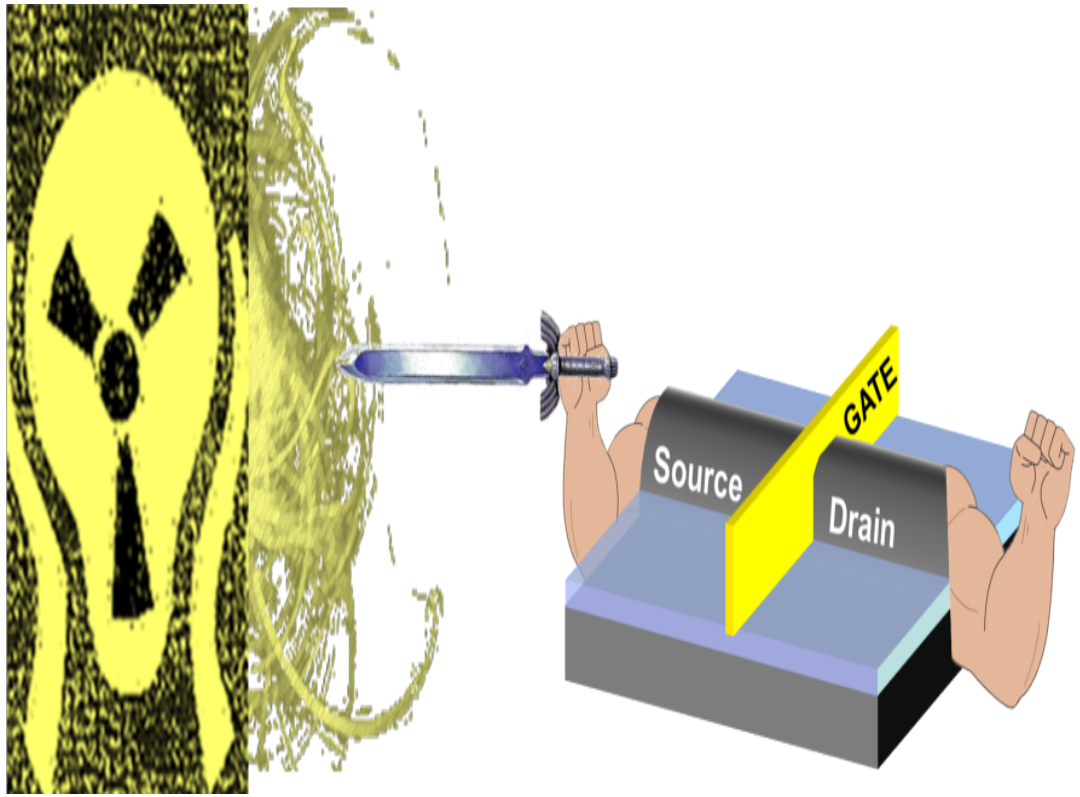


1. Threshold Voltage (VT)

VT	n_{Fins_Total}	n^{Fins}	$n_{FinFETs}$
Super-Low (SLVT)	40	4	10
Low (LVT)	40	4	10
Regular (RVT)	40	4	10
High (HVT)	40	4	10

Structures Tested

n-type FinFETs with min L_G



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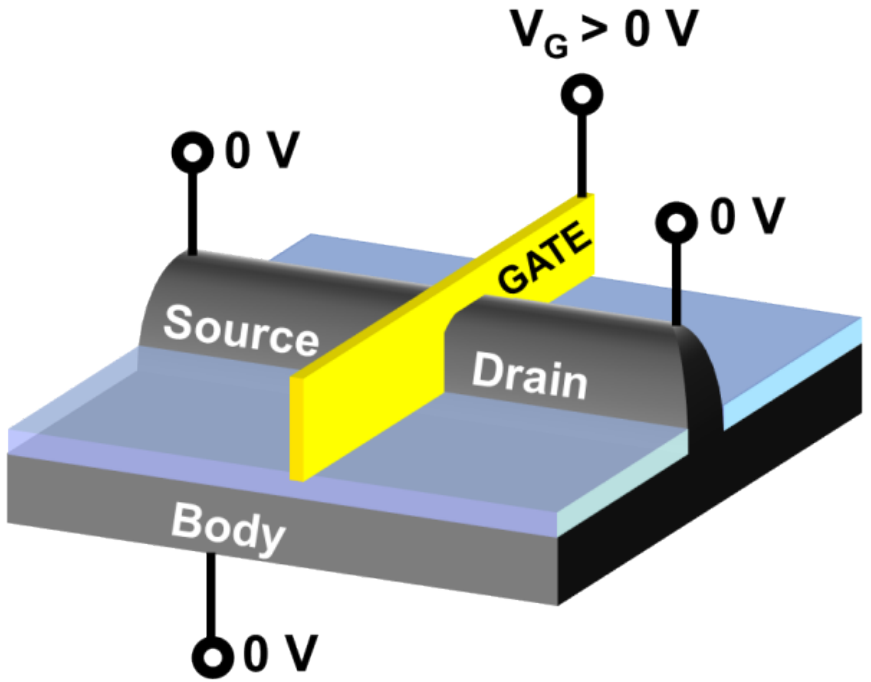
2. Number of Fins per Transistor

VT	n_{Fins_Total}	n^{Fins}	$n_{FinFETs}$
Regular (RVT)	40	1	40
Regular (RVT)	40	4	10
Regular (RVT)	40	40	1

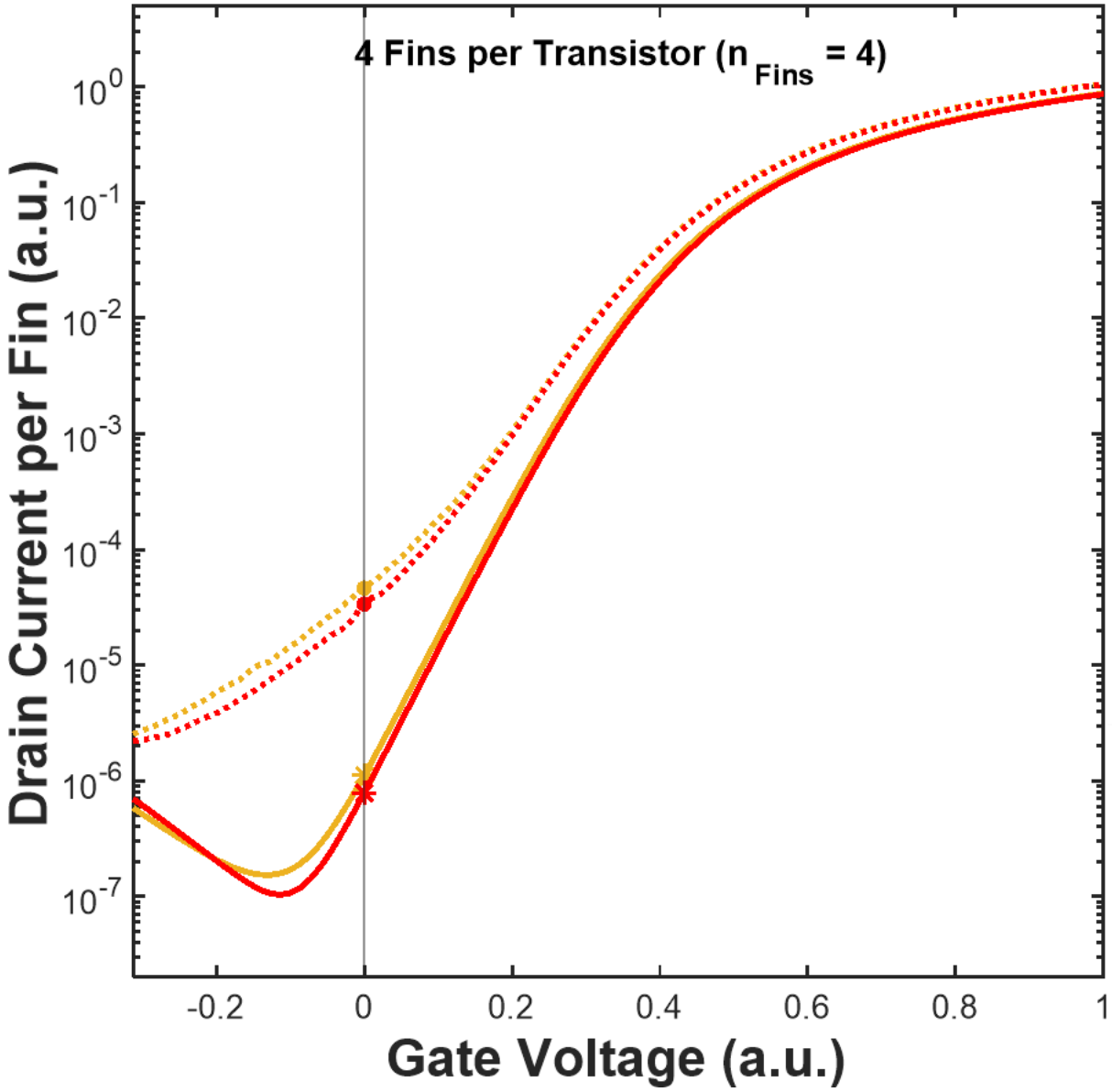
TID Measurement Process Overview

- Electrical measurements taken at different intermediate dose levels – all in-situ
- Irradiation Condition: Gate-On



Pre-Rad	100 krad(SiO_2)	200 krad(SiO_2)	500 krad(SiO_2)	1000 krad(SiO_2)	2000 krad(SiO_2)

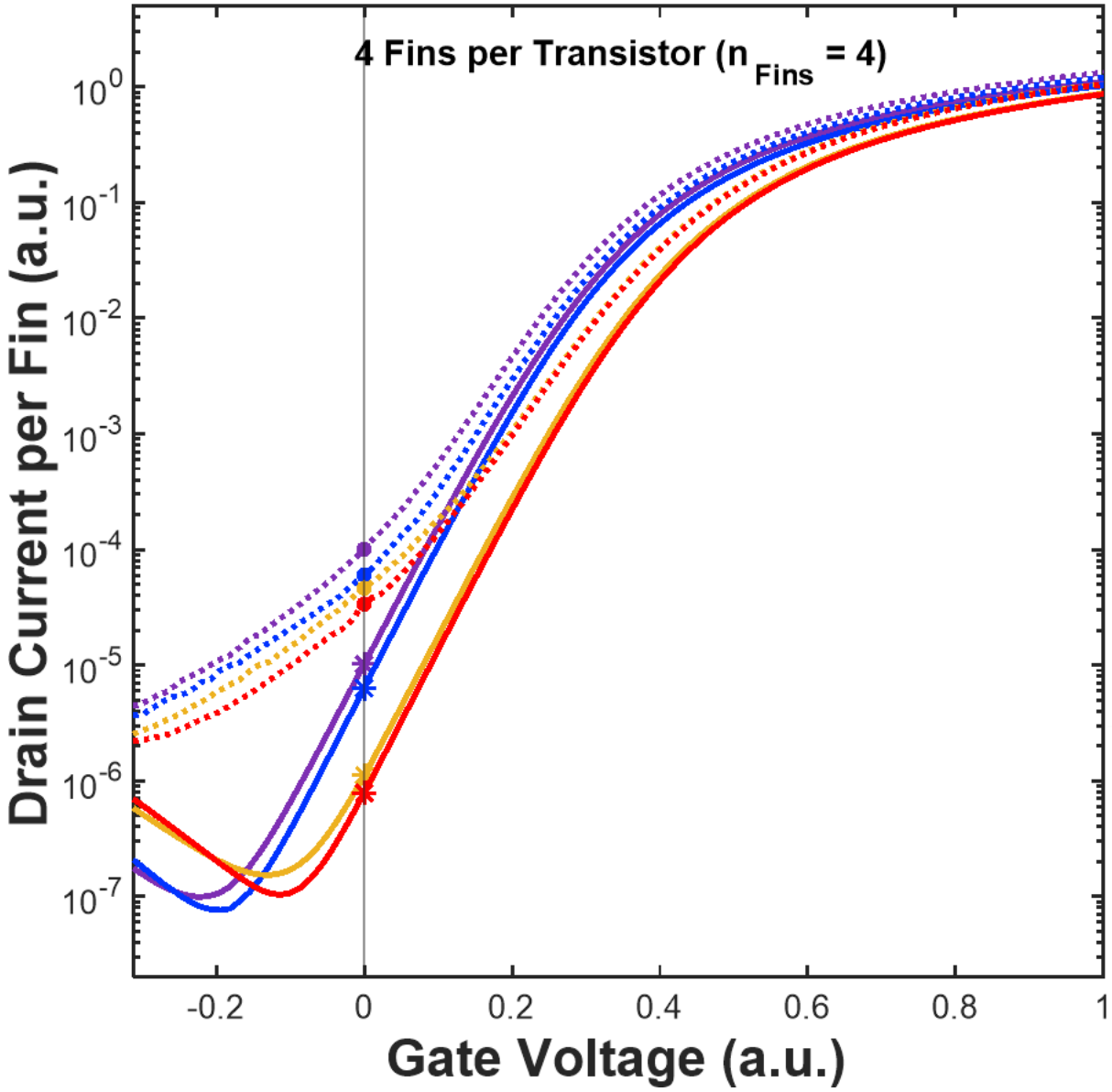
Transistor's TID Response vs Threshold Voltage



- I_{DS} vs V_G curves at saturation operation
- Pre-rad (solid lines) & 1000 krad(SiO_2) (dotted lines)
- Markers indicate leakage currents, i.e., $I_{DS,}$ when V_{GS} = 0V ($I_{DS,OFF}$)

HVT: 1000 krad(SiO_2)
RVT: 1000 krad(SiO_2)
HVT: Pre-Rad
RVT: Pre-Rad

Transistor's TID Response vs Threshold Voltage

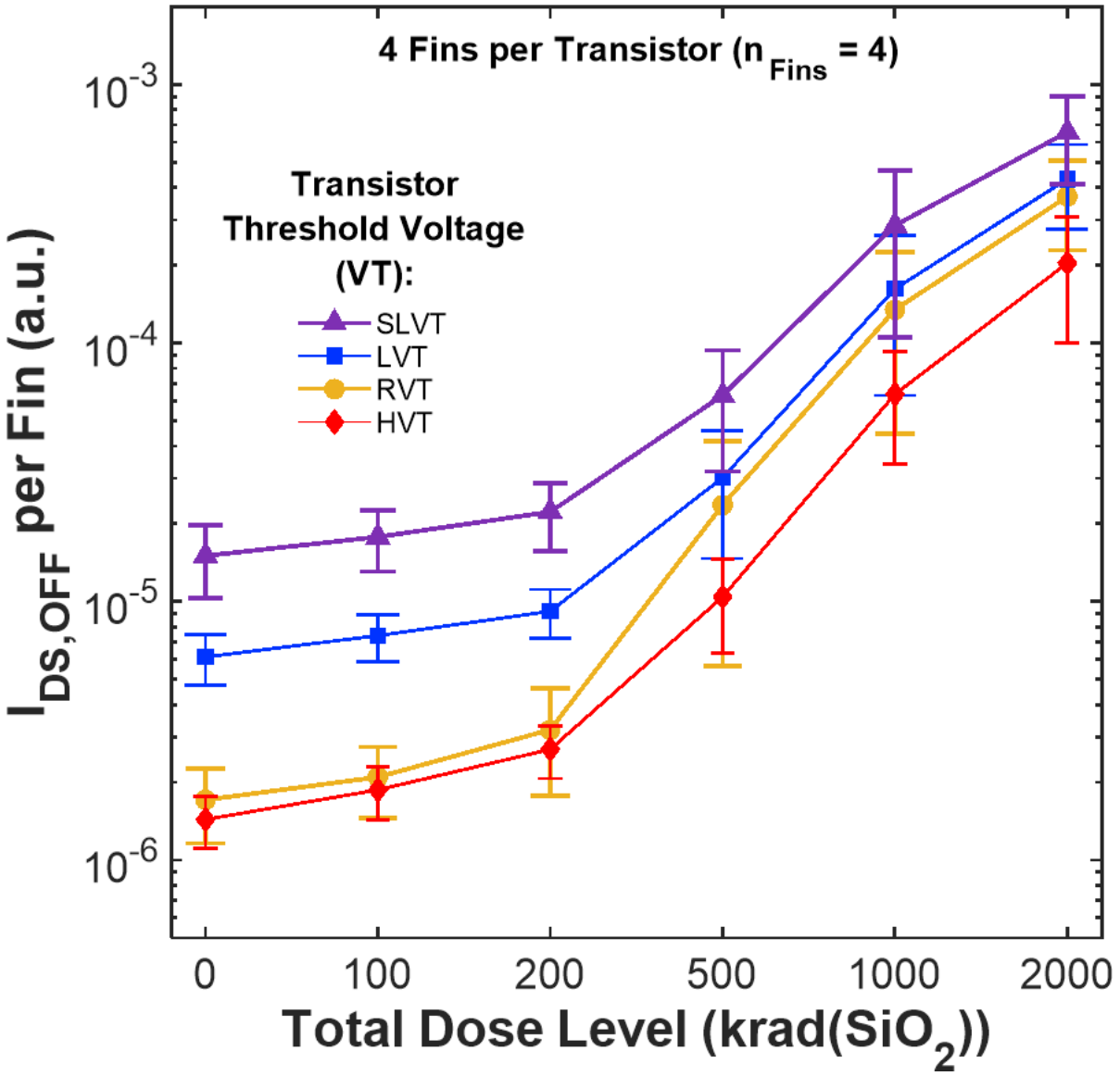


- I_{DS} vs V_G curves at saturation operation
- Pre-rad (solid lines) & 1000 krad(SiO_2) (dotted lines)
- Markers indicate leakage currents, i.e., $I_{DS,}$ when V_{GS} = 0V ($I_{DS,OFF}$)

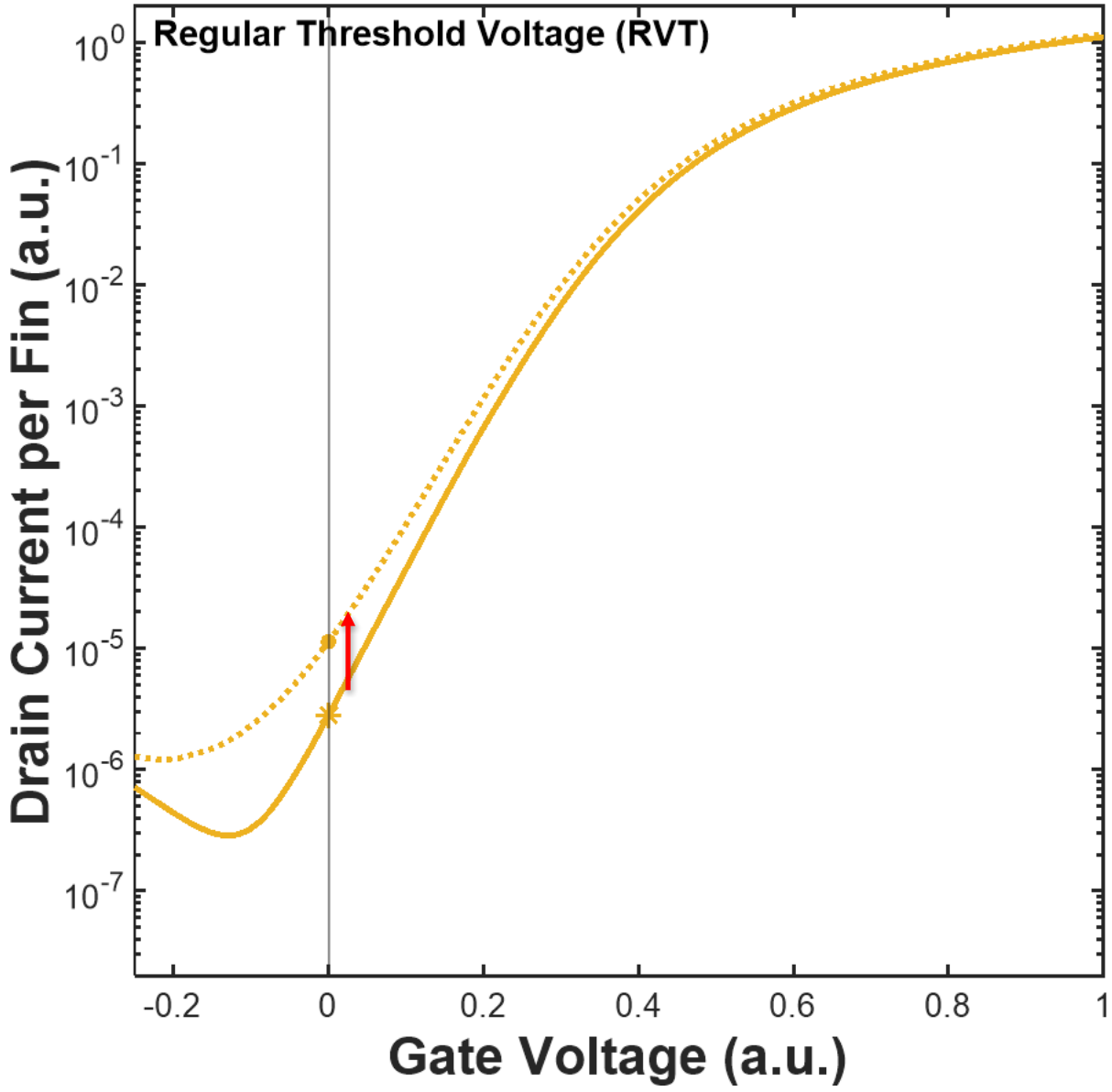
SLVT: 1000 krad(SiO_2)
SLVT: Pre-Rad
LVT: 1000 krad(SiO_2)
LVT: Pre-Rad
HVT: 1000 krad(SiO_2)
HVT: Pre-Rad
RVT: 1000 krad(SiO_2)
RVT: Pre-Rad

Transistor's TID Response vs Threshold Voltage

- Higher VT transistors (RVT and HVT) showed lower leakage currents ($I_{DS,OFF}$) pre- and post-radiation than lower VTs (LVT & SLVT)
- SLVT and LVT transistors had smaller relative increases in TID induced leakage currents ($I_{DS,OFF}$ post rad / $I_{DS,OFF}$ pre-rad)
- Above 200 krad(SiO_2), the leakage currents increase more rapidly with TID
- Low power applications using HVT transistors will experience a larger increase in off-state leakage current, while high-speed applications using SLVT transistors may be more tolerant to the TID induced leakage current increases



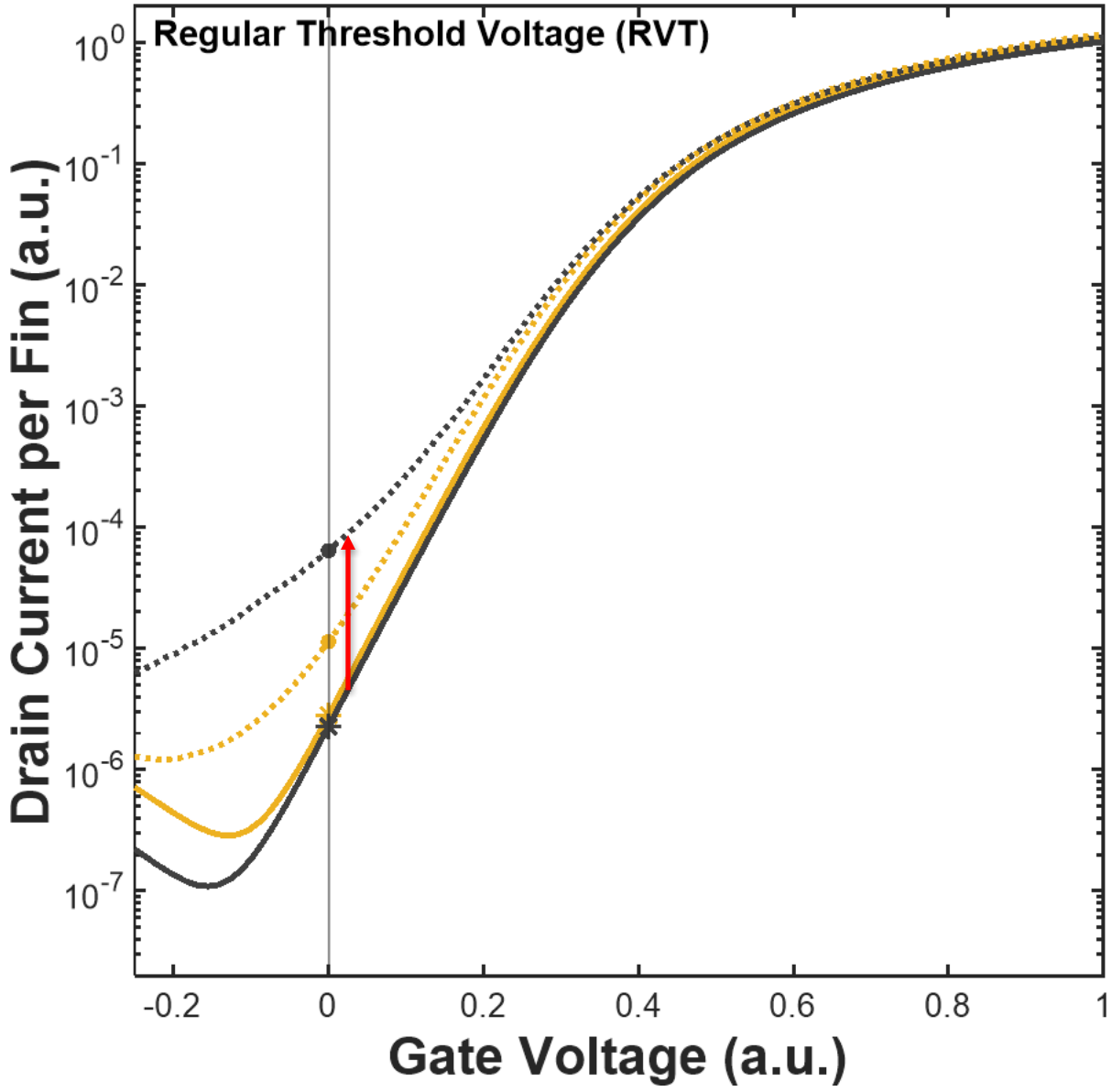
Transistor's TID Response vs Number of Fins per Transistor



- I_{DS} vs V_G curves at saturation operation
- Pre-rad (solid lines) & 1000 krad(SiO_2) (dotted lines)
- Markers indicate leakage currents, i.e., $I_{DS,}$ when V_{GS} = 0V ($I_{DS,OFF}$)

n_{Fins} = 1: 1000 krad(SiO_2) n_{Fins} = 1: Pre-Rad

Transistor's TID Response vs Number of Fins per Transistor

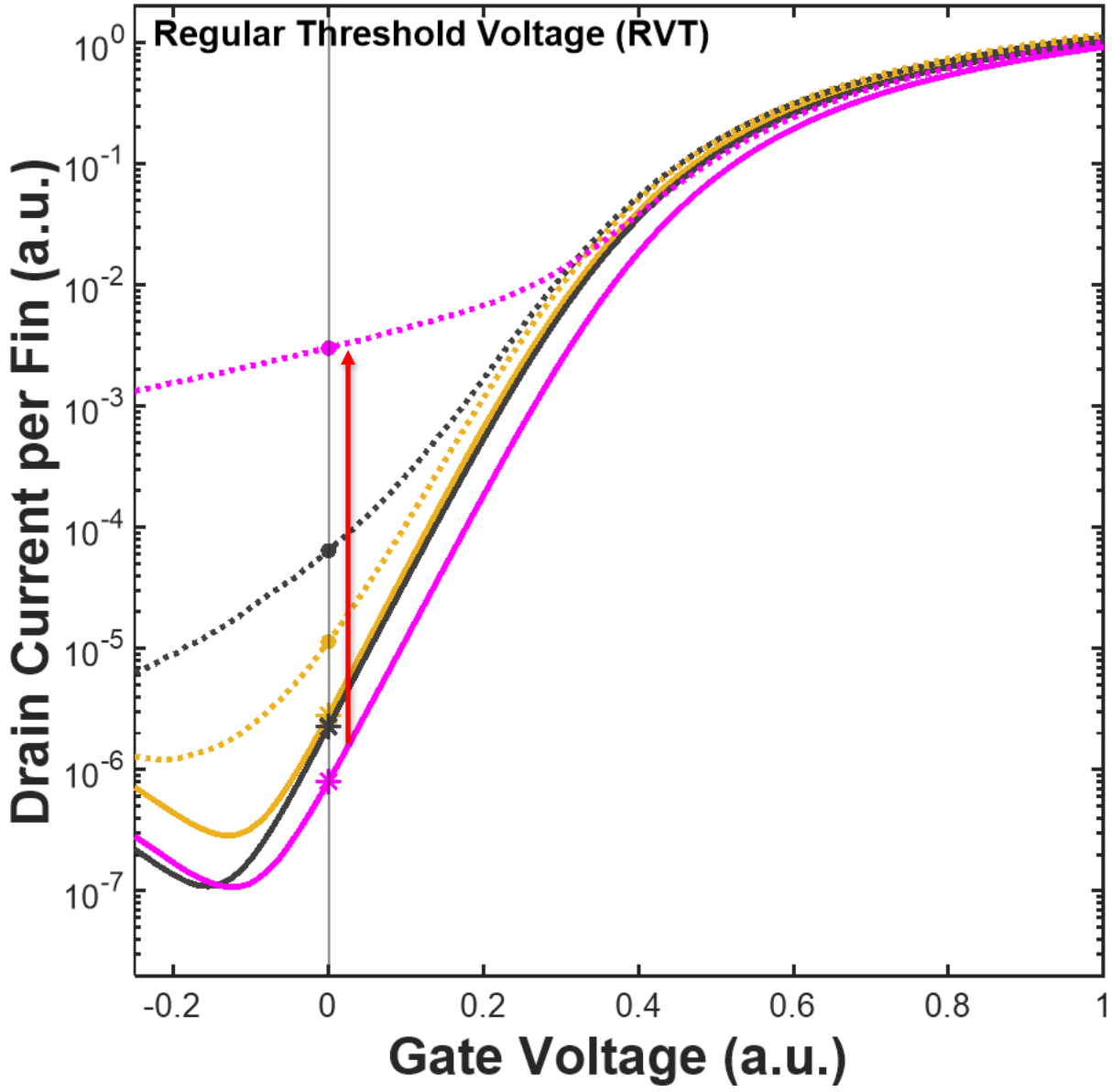


- I_{DS} vs V_G curves at saturation operation
- Pre-rad (solid lines) & 1000 krad(SiO_2) (dotted lines)
- Markers indicate leakage currents, i.e., $I_{DS,}$ when V_{GS} = 0V ($I_{DS,OFF}$)

n_{Fins} = 4: 1000 krad(SiO_2) n_{Fins} = 4: Pre-Rad

n_{Fins} = 1: 1000 krad(SiO_2) n_{Fins} = 1: Pre-Rad

Transistor's TID Response vs Number of Fins per Transistor

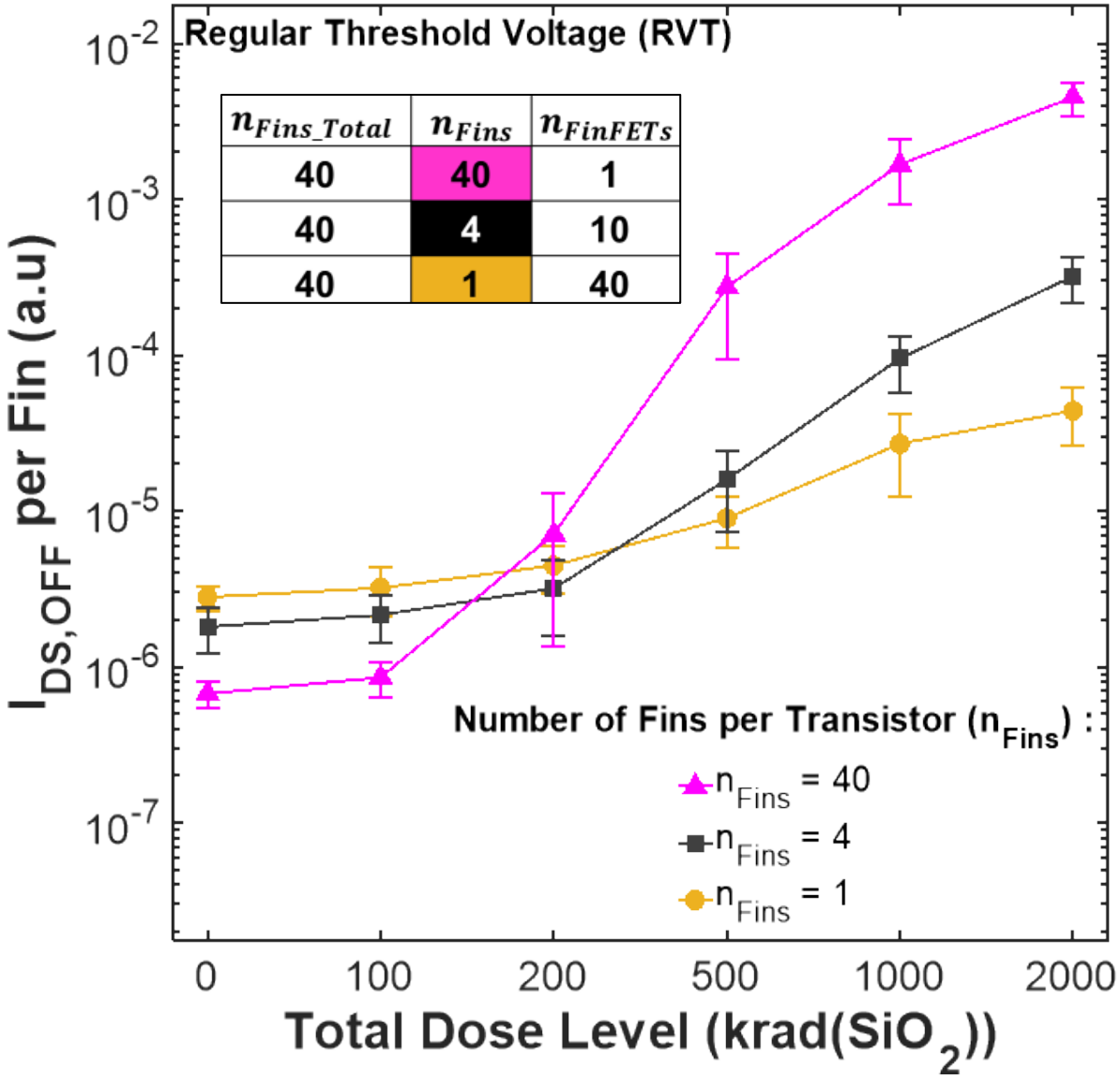


- I_{DS} vs V_G curves at saturation operation
- Pre-rad (solid lines) & 1000 krad(SiO_2) (dotted lines)
- Markers indicate leakage currents, i.e., $I_{DS,}$ when V_{GS} = 0V ($I_{DS,OFF}$)

n_{Fins} = 40: 1000 krad(SiO_2)
n_{Fins} = 40: Pre-Rad
n_{Fins} = 4: 1000 krad(SiO_2)
n_{Fins} = 4: Pre-Rad
n_{Fins} = 1: 1000 krad(SiO_2)
n_{Fins} = 1: Pre-Rad

Transistor's TID Response vs Number of Fins per Transistor

- Number of fins per transistor (n_{Fins}) has an impact on TID response
- Locations of shallow trench isolation (STI) oxides appear to influence TID response
  - Inter-fin STI (between fins) and outer-fin STI (between transistors)
  - Inter-fin STI appears to have stronger effect on TID
- Best way to minimize TID induced leakage is to use fewer fins per transistor
  - Example : Need more drive current? Use more transistors connected in parallel with fewer fins per transistor



Conclusions

- The lower the threshold voltage of the transistor, the better the TID response
- TID response is best when using fewer fins per transistor
- These findings can guide designers to further improve the TID hardness of ICs developed in 12LP
- Future work: Explore TID response using other transistor parameters, bias conditions, and the impact of annealing

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[1] J. Neuendank et al., "Single Event Upset and Total Ionizing Dose Response of 12LP FinFET Digital Circuits," 2022 IEEE Radiation Effects Data Workshop (REDW) (in conjunction with 2022 NSREC), Provo, UT, USA, 2022, pp. 1-9, doi: 10.1109/REDW56037.2022.9921478.
[2] T. Wallace *et al*., "Layout Dependence of Total Ionizing Dose Effects on 12-nm Bulk FinFET Core Digital Structures," in *IEEE Transactions on Nuclear Science*, doi: 10.1109/TNS.2022.3221060.
[3] R. M. Brewer *et al*., "Total Ionizing Dose Responses of 22-nm FDSOI and 14-nm Bulk FinFET Charge-Trap Transistors," in *IEEE Transactions on Nuclear Science*, vol. 68, no. 5, pp. 677-686, May 2021, doi: 10.1109/TNS.2021.3059594.
[4] J. Taggert, Current Total Ionizing Dose Testing of AMD Ryzen 3200G, 2022.