The Effects of Threshold Voltage and Number of Fins per Transistor on the TID Response of GF 12LP Technology

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ABSTRACT

We present experimental total ionizing dose data on GlobalFoundries 12LP 12nm FinFET technology. The TID response depends on both the transistor threshold voltage and on the number of fins per transistor.

MOTIVATION & OBJECTIVE

- GlobalFoundries (GF) 12LP 12nm bulk FinFET technology is being studied for many rad-hard programs
- As a state-of-the-art technology, 12LP offers significant performance and density advantages over older technologies.
- We report the first TID results on 12LP covering all four of the core threshold voltage variants, as well as a wide range of number of fins per transistor, both gate oxide thicknesses, and nFETs and pFETs.
- These results show designers how to maximize TID hardness in their 12LP designs.

EXPERIMENTAL DETAILS

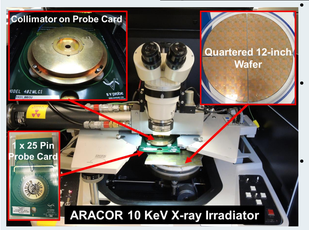
Transistor Test Structures

Type	Gate Length	Threshold Voltage (VT)	n_{Fins}	$n_{FinFETs}$	n_{Fins_Total}	
nFET	L_{Gmin}	Super-Low (SLVT)	1, 2, 3, 4, 12, 20, 40	1	1, 2, 3, 4, 12, 20, 40	1
nFET	L_{Gmin}	Low (LVT)	1, 2, 3, 4, 12, 20, 40	1	1, 2, 3, 4, 12, 20, 40	
nFET	L_{Gmin}	Regular (RVT)	1, 2, 3, 4, 12, 20, 40	1	1, 2, 3, 4, 12, 20, 40	
nFET	L_{Gmin}	High (HVT)	1, 2, 3, 4, 12, 20, 40	1	1, 2, 3, 4, 12, 20, 40	
nFET & pFET	L_{Gmin}	Super-Low (SLVT)	4	10	40	2
nFET & pFET	L_{Gmin} x 1, 6, 11, 14	Low (LVT)	4	10	40	
nFET & pFET	L_{Gmin} x 1, 6, 11, 14	Regular (RVT)	4	10	40	
nFET & pFET	L_{Gmin}	High (HVT)	4	10	40	
nFET & pFET	L_{gmin}	Regular (RVT)	1, 4, 40	40, 10, 1	40	

Type	Gate Length	Gate Oxide Thickness	n_{Fins}	$n_{FinFETs}$	n_{Fins_Total}	3
nFET	L_{Gmin}	Medium Thick	4,10,40	10,4,1	40	

1) nFET Single Transistor Structures with different number of fins per transistor (n_{Fins})
2) nFET and pFET Parallel Array Structures with 1, 10, and 40 $n_{FinFETs}$ with different number of fins per transistor (n_{Fins}) connected in parallel for total of 40 fins each
3) Medium Thick Oxide nFET Parallel Array Structures with 1, 4, and 10 $n_{FinFETs}$ with different number of fins per transistor (n_{Fins}) connected in parallel for total of 40 fins each

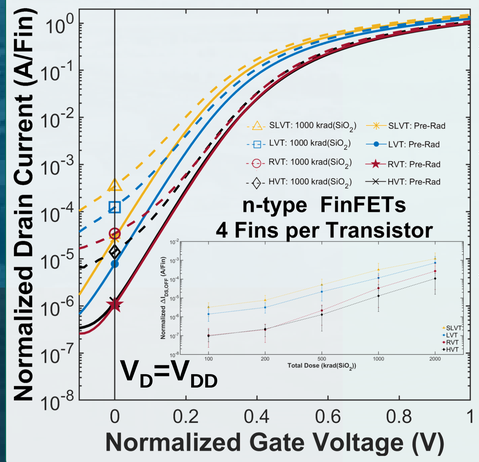
Experimental Set-Up



- Transistors were irradiated at the wafer-level across many sites with an ARACOR 10 keV X-ray source.
- Irradiation bias conditions: 1) Pass-Gate ($V_D = V_S = V_{DD}$ & $V_G = 0$ V) and 2) Gate- On ($V_G = V_{DD}$ & $V_D = V_S = 0$ V)
- Measurements and irradiation bias were done with a B1500A semiconductor analyzer and B2200A switch matrix.

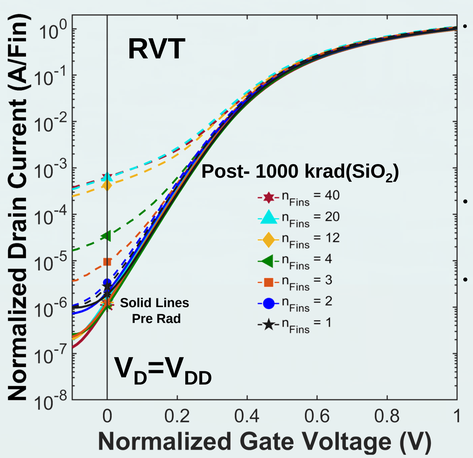
MAIN RESULTS AND OBSERVATIONS

TID induced leakage currents dependence on process threshold voltage (VT)



- The TID response strongly correlates with threshold voltage type, underscoring the influence of VT on post-irradiation sub-fin leakage.
- Lower VTs might suggest lesser doping in the sub-fin, potentially causing these devices to be more susceptible to oxide trap buildup.
- As seen in the figures in the panel below, increasing VT amplifies the impact of fin count on TID sensitivity, possibly due to more varied doping distribution across fin structures.

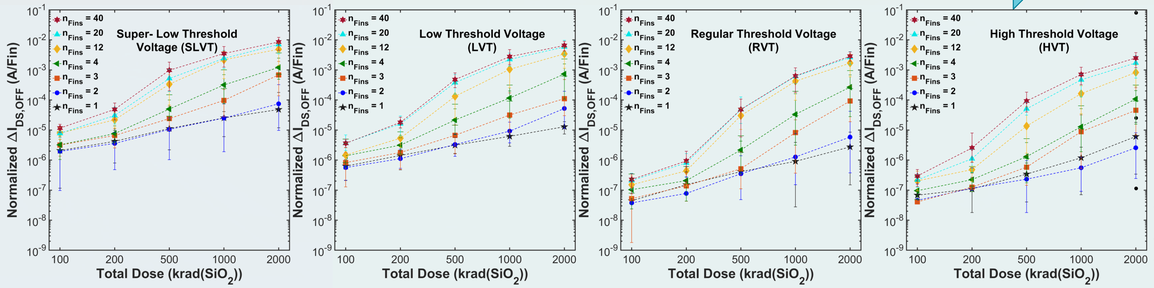
TID induced leakage currents dependence on number of fins per transistor



- TID measurements on n-type Single-Transistor Structures, exposed under "Gate-On" bias, illustrated off-state leakage current ($I_{DS,OFF}$) increasing with dose and fin count.
- High fin count transistors showed a higher TID leakage per fin.
- Data spans SLVT, LVT, RVT, HVT types, and up to 40 fins per transistor, covering typical standard libraries' density and high fin usage in analog designs.

Major Findings: The TID-induced increase in off-state leakage current is strongly affected by both the process threshold voltage (VT) and by the number of fins per transistor (n_{Fins})

12LP core transistor threshold voltage (VT) increases



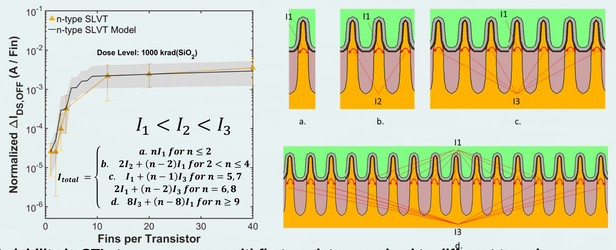
Higher VT transistors (RVT and HVT) showed lower leakage currents ($I_{DS,OFF}$) pre- and post-radiation than lower VTs (LVT & SLVT).

Above 200 krad(SiO_2), the leakage currents increase more rapidly with TID.

Results clearly indicate that the off-state leakage current ($I_{DS,OFF}$) increases with higher total dose and as the number of fins per transistor (n_{Fins}) increases.

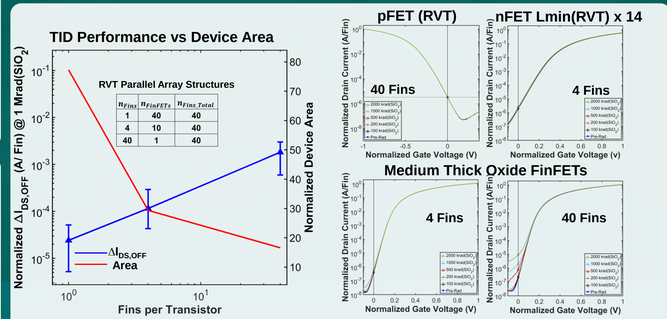
Average off-state drain-source leakage (IDS, OFF) current at 0, 100, 200, 500, 1000, and 2000 krad(SiO_2) of individual n-type transistors with 1, 2, 3, 4, 12, 20, and 40 fins per transistor for SLVT, LVT, RVT, and HVT threshold voltages. Error bars represent the min and max values.

MODEL RESULTS



- Variability in STI stress across a multi-fin transistor may lead to different trapping precursor densities or local electrical field which may cause variations in trapped charge build-up.
- A mathematical model was created to account for the potential strain-induced variability.

ADDITIONAL TEST RESULTS



- P-type device across all VTs and RVT nfins1, 40 showed no negligible TID degradation.
- The longer gate lengths tested were more tolerant to TID.
- Medium thick oxide FETs had negligible response to TID, except when using many fins in one transistor.
- Best way to minimize TID induced leakage is to use fewer fins per transistor, which comes with some area trade-off.

CONCLUSIONS

- TID response in n-channel transistors varies with threshold voltage (VT) and number of fins per transistor.
- High VT (RVT and HVT) transistors showed greater robustness to TID degradation.
- Fewer fins per transistor enhance TID resistance, making these configurations more radiation-tolerant.
- p-Channel structures across all VT variants displayed significant resistance to TID damage up to 2000 krad(SiO_2).

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