SAND2025-12838J

APL Electronic Devices

RESEARCH ARTICLE | JULY 18 2025

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APL Electronic Devices 1, 036112 (2025)
https://doi.org/10.1063/5.0279372

AIP Publishing

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Cite as: APL Electron. Devices 1, 036112 (2025); doi: 10.1063/5.0279372
Submitted: 7 May 2025 • Accepted: 2 July 2025 •
Published Online: 18 July 2025

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ABSTRACT

The poor thermal properties of Aluminum–Gallium Nitride (AlGaN) channel High Electron Mobility Transistors (HEMTs) on sapphire limit the device's maximum switching frequency due to high channel temperatures. Extracting the correct thermal time constants can provide guidelines for the device's safe frequency operation. This study experimentally quantifies the impact of pulse width and duty cycle on the transient thermal dynamics of multi-finger AlGaN channel HEMTs. In most transient thermal metrology, lock-in averaging approaches are leveraged to increase signal-to-noise ratio and measure the device's relative temperature rise. Assuming no heat accumulation, the temperature rise is used to quantify the device's thermal resistance under continued pulsed biasing. For devices grown on sapphire substrates, however, heat accumulation leads to elevated reference temperatures and causes the differential measurement to underestimate the peak temperature. This study demonstrates the capability of transient Gate Resistance Thermometry (tGRT) to measure the absolute temperature, which is required to precisely evaluate the device's thermal resistance. When an absolute temperature measurement is not feasible (such as thermoreflectance imaging), a solution is proposed to derive the peak temperature under pulsed biasing based on the differential temperature under pulsing and the steady-state thermal resistance (which is typically easier to obtain). Finally, additional tGRT (without averaging) is performed to demonstrate the temperature-dependent thermal time constants required to minimize heat accumulation effects.

Aluminum–Gallium Nitride (AlGaN) channel high electron mobility transistors (HEMTs) offer significant advantages for power electronics due to their large bandgap, which results in high breakdown voltages and low on-resistance compared to competitive material systems such as Gallium Nitride (GaN).[1–3] As a result of the large bandgap, AlGaN offers excellent resilience at high temperatures, and the material is known to demonstrate radiation hardness—the properties do not change significantly in the presence of radiation[4]—which broadens the potential for this material system in niche applications. The aluminum content of AlGaN has a strong and non-linear influence on the material properties of the system, particularly the bandgap, bulk critical electric field, and thermal conductivity.[4] When the aluminum content is low, AlGaN typically shows electrical properties similar to GaN ($E_{G,\mathrm{GaN}} = 3.4$[3] V, $E_{C,\mathrm{GaN}} = 3$[3] MV cm^{-1}, $\kappa_{\mathrm{GaN}} = 230$[1] Wm^{-1} K^{-1}) but with lower thermal conductivity ($\kappa_{\mathrm{AlGaN}} = 8.5 - 11$[2] Wm^{-1} K^{-1}) because aluminum behaves as a lattice defect and increases the rate of phonon scattering.[5] AlGaN with a high aluminum content resembles aluminum nitride (AlN) ($E_{G,\mathrm{AlN}} = 6$[6] V, $E_{C,\mathrm{AlN}} = 12.3$[7] MV cm^{-1}, $\kappa_{\mathrm{AlN}} = 319$[8] Wm^{-1} K^{-1}) but also with reduced thermal conductivity because gallium acts as a phonon scattering site.

The thermal characterization of AlGaN devices is essential for their implementation due to the poor thermal conductivity of the material. Device design must consider the thermal behavior of the semiconductor material system, or the electrical benefits of the system will not be fully realized due to poor thermal transport behavior.[9] AlGaN devices can use higher thermal conductivity substrates and thermal spreading structures[10,11] to mitigate heat accumulation, and it is important to verify that these design strategies achieve the desired results. It is not always practical to use high thermal conductivity substrates due to the small wafer sizes of AlN (typically <6 in. or 150 mm), and the additional processing complexity of the GaN–Diamond or GaN–Silicon Carbide systems results in high costs. Sapphire is a low thermal conductivity substrate that offers advantageous wafer size (commercially available at >200 mm diameter) and is already well commercialized for LED applications, leading to advantages in cost. Given sufficient time, it is likely that high thermal conductivity substrates will become commercially viable, but in the intermediate timeframe, it is prudent to consider the effects of sapphire substrates on the AlGaN channel HEMT.

Wide-field optical methods for the thermal evaluation of these devices, such as transient thermoreflectance imaging (TTI),[12] can be implemented in some cases, but as the bandgap becomes large, it becomes necessary to use deep-ultraviolet (DUV) optical systems[13] and these systems are still in their early developmental stages.[14] In addition, many AlGaN devices do not provide unobstructed optical access to the channel due to thermal spreading structures, field plates, and air bridges.[15] Gate resistance thermometry (GRT) is an alternative thermometry method particularly well suited for complex device structures.[16]

Previous work has explored the limits of thermal characterization on single-fingered HEMTs, especially as it pertains to the choice of experimental conditions optimal for TTI and Raman thermometry.[17] Lundh *et al.* reported the minimum pulse width required to reach steady state for both GaN HEMTs on Silicon and AlGaN Channel HEMTs on Sapphire. This work differentiates itself by exploring the importance of the cooling time rather than the rise time, and directly quantifies the impact of pulsed operating conditions on device thermal performance. Being a differential temperature measurement, TTI requires sufficient time for cooling to ensure no heat accumulation. The impact of heat accumulation is thus quantified, and the effects of pulse width on transient thermal crosstalk in multi-fingered devices are explored.

GRT is a thermally sensitive electrical parameter (TSEP) method in which the electrical resistance of a metallic structure, the gate, is used to evaluate the spatially averaged temperature of the gate.[16,18] For HEMTs, the maximum temperature is known to be located in the channel immediately below the gate edge on the drain side.[19–22] Based on the peak temperature's proximity to the gate, GRT has proven to be an effective temperature measurement technique for lateral HEMTs. The use of Kelvin (four-wire) probing allows for high-accuracy measurements of the TSEP, and it is known that electrical resistance varies linearly with temperature over a very wide range in metals (100–500 K is expected).[23]

As shown in Fig. 1(a), a six-fingered AlGaN channel HEMT was investigated using transient GRT (tGRT). The epitaxial structure consists of a 30-nm-thick $Al_{0.85}Ga_{0.15}N$ barrier layer atop a 360 nm UID $Al_{0.51}Ga_{0.49}N$ channel. There is an AlGaN gradient layer that transitions to an AlN smoothing layer, which itself is atop a ≈430-μm-thick Al_2O_3 (sapphire) substrate. The channel and buffer layer thicknesses are reported in Refs. 24–26. The device is a six-finger HEMT with a bridged source structure passing over each gate and drain finger five times. One central gate finger is connected to dedicated GRT probing and sensing pads, and the device does not have a field plate. The gate length is 4 μm, and each gate finger width is 100 μm. The gate-drain spacing is 8 μm, and the source-gate spacing is 4 μm. All measurements were conducted by mounting the die onto the temperature-controlled stage of a thermoreflectance imaging station (for direct thermal comparison). Silver paste was applied between the die and the stage to reduce the thermal boundary resistance, and a thermocouple was placed near the die for accurate temperature assessment during calibrations.

A Keithley 2400 SourceMeter is used to apply a probe current I_P across the dedicated probing pads, as indicated in Fig. 1(a). This current acts along the gate width of a central finger. On the opposite sides of the probing pads, a Tektronix MS044 oscilloscope is used to measure the voltage drop, V_{GRT}, corresponding to that current, resulting in a Kelvin (four-wire) resistance measurement. By controlling the device temperature and measuring the resistance, it is possible to evaluate the thermal coefficient of resistance (TCR), as shown in Eq. (1), where ΔT is the difference between the reference temperature (≈20 °C) and the calibration temperature, R_0 is the resistance measured at the reference temperature, and the ΔR term is the difference between the resistance at the calibration and reference temperatures:[16]

$$TCR = \frac{\Delta R}{R_0}\frac{1}{\Delta T}. \tag{1}$$

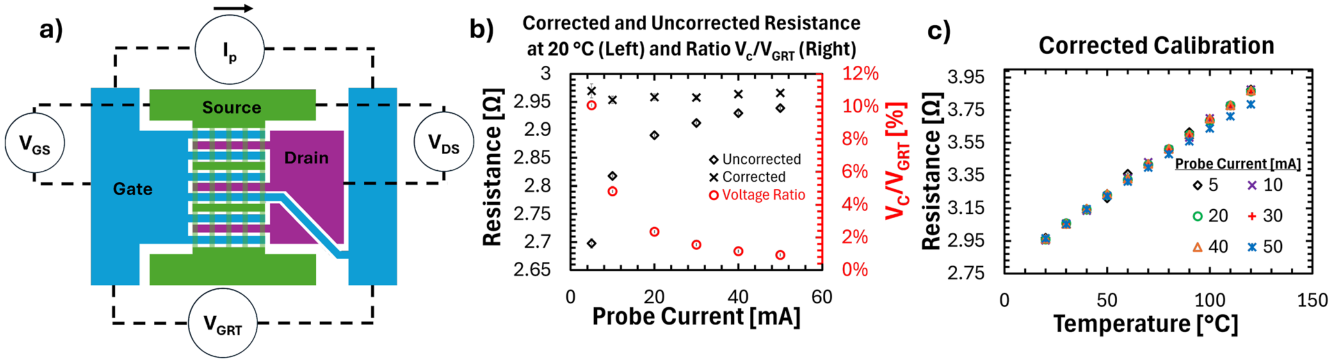

FIG. 1. (a) Simplified schematic of the six-finger AlGaN/AlN HEMT on a thick sapphire substrate that was thermally characterized. Probe locations are indicated for the Kelvin (four-wire) resistance measurement of a gate finger. (b) Gate resistances measured at the controlled 20 °C calibration point for various probe currents, as well as the fraction of the measured voltage V_{GRT} comprised by the correction voltage V_C. Error bars are present in this plot but are very small relative to the symbol size. (c) Calibration curves for the various probe currents after correction, demonstrating strong agreement except at elevated currents. Error bars are present in this plot, but they are small relative to the symbol size and are obscured. (b) Corrected and uncorrected resistance at 20 °C (left) and ratio V_C/V_{GRT} (right). (c) Corrected calibration.

Once the TCR is derived from the calibration, Eq. (1) can be rearranged to estimate the temperature rise during operation, as shown in Eq. (2), where V_{GRT} is the voltage measured during device operation and V_0 is the reference voltage used during the calibration.[16] While this is shown in terms of ΔT, it is clear that the reference temperature from the calibration may be used to evaluate an absolute temperature rather than a change in temperature. It is critical to note that the TCR is strongly dependent on the reference voltage and temperature and is generally known to be unstable over long time periods[27] or upon exposures that may result in surface chemical changes.[16] It is good practice to perform TCR calibration immediately prior to experimental characterization of the device and to avoid using the same calibration for multiple devices, even if they are located on the same wafer and share the same design:

$$\Delta T = TCR^{-1} \times \left(\frac{V_{GRT}}{V_0} - 1\right). \tag{2}$$

Based on Eq. (2), the magnitude of the measured voltage is controlled by the probe current. It was hypothesized that at low probe currents, experimental sensitivity might be poor, but at elevated probe currents, there might be probe-induced heating of the gate or an alteration of the device performance due to changes in the field induced by the additional current flow.[16] To evaluate the effects of probe current on these devices, calibrations were completed at probe current I_P values of 5, 10, 20, 30, 40, and 50 mA in the range of 20–120 °C with the gate and drain voltages held constant at zero ($V_{DS} = V_{GS} = 0$ V). These currents correspond to a potential difference of ~0.015–0.5 V across the gate width. At all probe currents, no difference was detected in the device transfer curve, but some differences were observed in the calibration. Close inspection revealed that there is a non-zero potential difference across the gate width when the probe current is off. This small voltage is likely due to current leakage from the device pulser heads used to excite the device during the experiment and from the additive series resistances of the oscilloscope probing station and is called the correction voltage V_C. As shown in Fig. 1(b), V_C is 10% of the measured V_{GRT} at the 5 mA probe current but drops to 1.6% at the 30 mA probe current. At the 20 °C calibration point, the measured resistance is shown to range from ~2.7 to 2.93 Ω. If the resistance is corrected by subtracting V_C from V_{GRT}, the resistance is shown to vary only between 2.95 and 2.97 Ω. Experimentally, V_C did not vary with temperature up to 120 °C. Figure 1(c) shows the corrected calibration curves over the entire temperature range of interest, demonstrating that if stray voltages are properly accounted for, there is no difference in the calibration curve or TCR. It is also notable in Fig. 1(c) that the 50 mA calibration is slightly different from the others, which suggests the initiation of probe current self-heating effects. For further measurements in this study, 30 mA is used as a probe current to avoid self-heating effects but maintain a high signal-to-noise ratio.

The tGRT results of the device under pulsed operation are shown in Fig. 2. Parts (a) and (b) show the complete temperature profile of the device operating at $V_{DS} = 20$ V and $V_{GS} = 0$ V for several duty cycles (α = 5, 10%, 20%, 30%, 40%, and 50%) with constant pulse width (equating to a peak power density of $\approx 1.6\ \frac{\text{W}}{\text{mm}}$). The variation in duty cycle extends the off-period between successive activations, and the data shown are averaged over 500 cycles. The figures show temperature magnitude rather than the typical ΔT presented for a GRT measurement.[16] Two key regions are shown in Fig. 2(b) for clarity, but they may be observed in parts (a) and (c) as well. These are the on-state high temperature (T_{High}) and off-state low temperature (T_{Low}). In this analysis, the key temperatures are calculated as an average over the last 5% of the on or off segment of the period, respectively. The difference $T_{High} - T_{Low}$ is the measured ΔT, which would typically be reported in GRT or other relative measurement strategies such as transient thermoreflectance imaging (TTI).[28]

Figure 2(a) shows the 0.5 ms pulse width data, and there is a clear upward trend in both the peak temperature and low temperature as the duty cycle increases. This trend is also shown in Fig. 2(b), corresponding to a 4.5 ms pulse width. Figure 2(c) shows a single-shot (unaveraged) decay from a steady-state powered

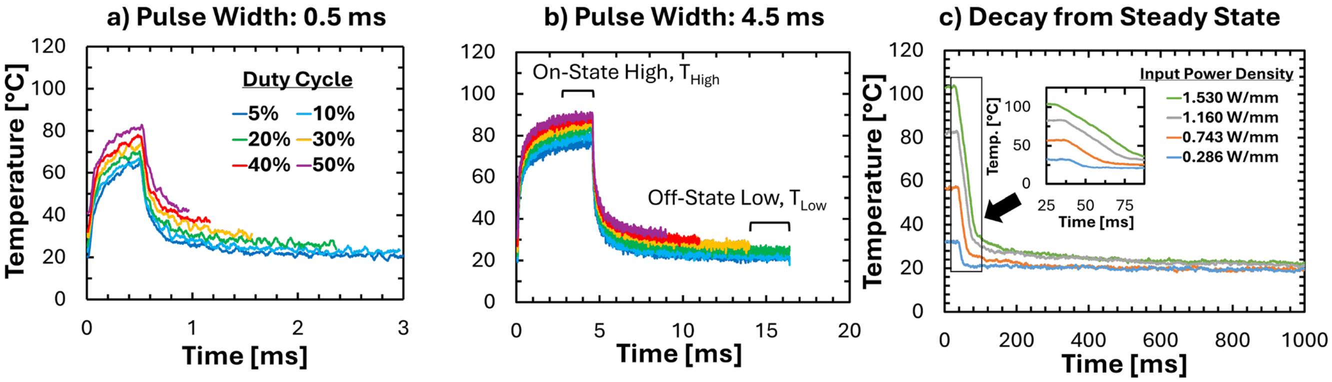

FIG. 2. (a) Temperature rise and decay profiles at duty cycles of 5%, 10%, 20%, 30%, 40%, and 50% and a constant pulse width of 0.5 ms at 20 V. Each curve is averaged over ~500 cycles, and a rise in temperature is seen with increasing duty cycle, which is attributed to heat accumulation. (b) Temperature rise and decay profiles at duty cycles of 5%, 10%, 20%, 30%, 40%, and 50% and a constant pulse width of 4.5 ms at 20 V. Each curve is also averaged over 500 cycles and demonstrates the effects of heat accumulation. Also shown are the regions of the temperature profile identified as the On-State High and Off-State Low temperatures. (c) A single-shot temperature decay from extended (steady-state) constant voltage conditions. (a) Pulse width: 0.5 ms. (b) Pulse width: 4.5 ms. (c) Decay from steady state.

TABLE I. Summary of time constants and amplitudes.

Power density $\left[\frac{\mathrm{W}}{\mathrm{mm}}\right]$	Voltage (V)	A (°C)	τ_1 (ms)	B (°C)	τ_2 (ms)
0.286	5	14.44	5.15	2.183	334.3[a]
0.743	10	57.22	10.02	7.014	188.4[a]
1.160	15	68.88	15.33	9.521	228.3[a]
1.530	20	103.3	18.33	13.09	180.6[a]

[a] Long time constants suggest that the acquisition duration may be too short. Regardless, they comprise only a small fraction of the overall decay behavior, and the rapid decay associated with the short time constant is the only part relevant to the analysis.

condition at V_{DS} = 5, 10, 15, and 20 V. The device was powered for several seconds until no change in temperature was seen prior to being deactivated. Due to the large time scale in part (c), it appears that these decays to the ambient temperature are quite rapid, but fitting the decays with a two-term exponential,[29] as shown in Eq. (3), reveals that the primary time constants follow the trends shown in Table I, where even for a 5 V operating condition, corresponding to a peak temperature rise of ~17 °C, at least a 5 ms decay should be expected before the device returns to ambient temperature:

$$\Delta T = Ae^{\frac{-t}{\tau_1}} + Ce^{\frac{-t}{\tau_2}}. \tag{3}$$

The origin of the variation of the thermal time constant with respect to the input power requires a detailed analysis that is not yet fully developed. Briefly, in this case, it is attributed to both the thermal crosstalk between fingers of the HEMT[29,30] and to the thermal penetration depth of the heating.[31] As the device is heated under higher power conditions, the rate at which heat may be extracted from the more central fingers is limited in the lateral directions by the presence of heat caused by the other fingers.[29,30] In addition, it is demonstrated in many introductory texts on heat transfer that for a slab-type heat conduction problem subjected to a constant heat flux at one surface, the thermal time constants may be well approximated by $\tau = \frac{x^2}{D}$, where x is the power-dependent thermal penetration depth and D is the thermal diffusivity. Both the crosstalk and penetration depth effects are expected to be relevant to the observed phenomenon. Similar results have been observed but not significantly discussed in GaN HEMTs.[32]

In light of the duration of the delay required for a device to return to ambient temperature from even a low-power condition, as shown in Table I, as τ_1, it is clear that under the pulsed operating conditions explored in this study, the device does not have sufficient time to reject all of the heat between cycles. Figures 3(a)–3(c) show the distribution of key temperatures over an operation cycle for various pulse-width conditions, alongside the steady-state temperatures observed at the given power conditions. The average power shown is the power density $\left[\frac{\mathrm{W}}{\mathrm{mm}}\right]$ multiplied by the duty cycle α, thus showing the average power dissipation over the complete cycle. Since each experiment within a given pulse width was performed at 1.6 $\frac{\mathrm{W}}{\mathrm{mm}}$, the increase in average power corresponds to an increase in the duty cycle. For the steady-state condition, the average power is equivalent to the DC power. The temperatures T_{High} and T_{Low} show a strong upward trend, though this trend does not exactly parallel the steady-state temperatures across the range of average powers investigated. The difference between T_{High} and T_{Low}, denoted as ΔT, is nearly constant over the range of average powers, implying that these are dynamic equilibria where heat accumulates and raises the base temperature T_{Low}. If thermal resistance were calculated based on ΔT and an assumed constant base temperature T_{Low}, the accumulation effects would not be captured, and the thermal resistance would be underestimated:

$$T_{Avg} = \alpha \times \Delta T + T_{Low}. \tag{4}$$

Figure 3 also shows the average temperature of the device, calculated using Eq. (4). By inspection, T_{Avg} corresponds very well to the steady-state temperature. Additional experimentation is required to confirm this conjecture, but it may be possible to use this relationship to predict T_{High} and T_{Low} for a wide range

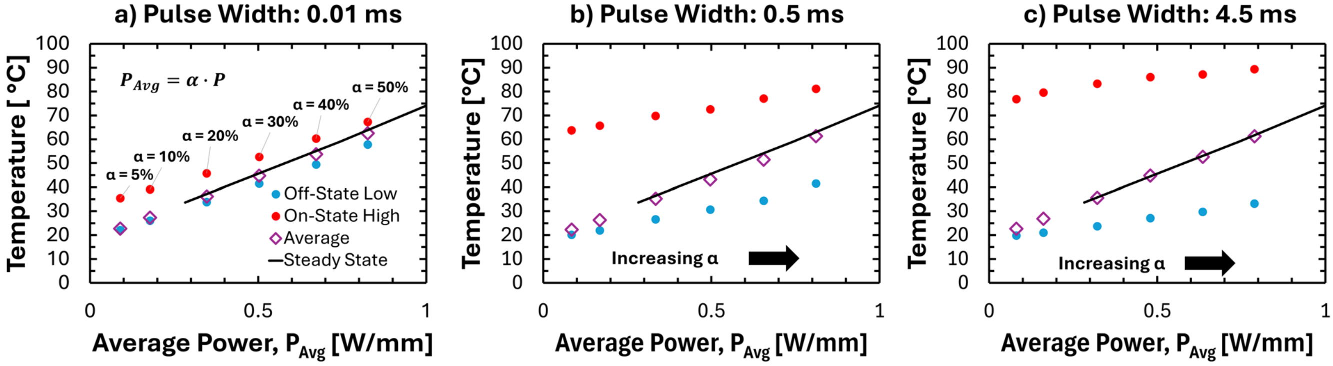

FIG. 3. (a) Key temperatures (T_{Low}, T_{High}, $T_{Average}$) observed in 0.01 ms pulse-width power cycles at 20 V for various duty cycles, alongside the calculated average temperature and the steady-state temperature. (b) Key temperatures (T_{Low}, T_{High}, $T_{Average}$) observed in 0.5 ms pulse-width power cycles at 20 V for various duty cycles, alongside the calculated average temperature and the steady-state temperature. (c) Key temperatures (T_{Low}, T_{High}, $T_{Average}$) observed in 4.5 ms pulse-width power cycles at 20 V for various duty cycles, alongside the calculated average temperature and the steady-state temperature. In all three parts of this figure, the increase in average power is attributed to an increase in the duty cycle, α, as the electrical drive parameters of the device (V_{GS}, V_{DS}) are held constant. Pulse width: (a) 0.01 ms, (b) 0.5 ms, and (c) 4.5 ms.

of operating conditions from a significantly reduced dataset. By obtaining a dataset that captures the steady-state heating behavior and thermal resistance, one can estimate T_{High} and T_{Low} from the measured ΔT and known duty cycle α, under the assumption that $T_{Steady\ State} = T_{Avg}$.

As previously established, heat accumulation can reasonably be expected when the device does not have sufficient cooling time (Off-State) to reject all the heat produced during the On-State. We can estimate the required off-period by investigating the time constants of the thermal decay from steady state. The first time constant from Eq. (3), τ_1, is responsible for ≈86.9 – 89% of the decay, which makes it a reliable estimator for the minimum cooling time between cycles to prevent the accumulation of heat. It is reasonable to expect that the time constants are dependent on many features of this device, including multi-finger thermal crosstalk and heat transfer through the multi-layered structure into the substrate and thermal chuck.[33] The presence of a device package would also influence this, if it were present. Within the limiting case of an unpackaged device, Fig. 4(a) shows τ_1 plotted against both the steady-state power density and the peak temperature. A good linear fit is displayed against both parameters. A linear relationship between power and temperature rise is expected when the thermal conductivity does not change significantly over the given temperature range, so the linear relationship between the input power and the time constants may only be valid for the temperature range for which the thermal diffusivity is approximately constant.

The accumulation effects are also visible in Figs. 4(b) and 4(c), where the temperatures T_{Low} and T_{High} are shown as functions of pulse width. In Fig. 4(b), at a low duty cycle ($\alpha = 5\%$), the off-state temperature (T_{Low}) varies by 11% across the range of explored pulse widths. In contrast, at higher duty cycles ($\alpha = 50\%$), reducing the pulse width is shown to increase T_{Low} by 74% due to heat accumulation. During low-frequency operation (longer pulse widths), the off-state temperature will tend to be less sensitive to the duty cycle because there is more time for cooling to occur in all duty cycle cases, and T_{Low} will trend toward its steady-state behavior. For example, at a 0.01 ms pulse width, reducing the duty cycle from 50% to 5% reduces T_{Low} by 62%, but the same duty cycle change at a 4.5 ms pulse width reduces T_{Low} by 40%. A similar trend is observed in Fig. 4(c). At low duty cycles ($\alpha = 5\%$), the on-state temperature (T_{High}) can be reduced by 54% by reducing the pulse width from 4.5 to 0.01 ms. The effect is less prominent at higher duty cycles ($\alpha = 50\%$), where the reduction is only 25% over the same interval. For a 0.01 ms pulse width, reducing the duty cycle from 50% to 5% reduces T_{High} by 47%, but the same duty cycle change at a 4.5 ms pulse width reduces T_{High} by only 14%. During low-frequency operation (longer pulse widths), the on-state temperature (T_{High}) trends toward a pseudo-steady state based on the power input, but during higher-frequency operation (shorter pulse widths), the device does not reach a fully heated condition because of the limited time for heating to occur. At high frequencies, the duty cycle is an effective tool for controlling T_{Low} and T_{High}, but at lower frequencies, the pulse width effect is much more dominant. This correlates well with experiments showing higher switching efficiency during high-frequency operation.[34]

For the design of systems and application of devices, it is often beneficial to estimate reasonable operational limits. If the time constant for a device at a particular power is known, it is possible to calculate the upper limit of the allowable pulse width from the desired duty cycle, as shown in Eq. (5), where PW_{Max} is the upper limit of the allowable pulse widths. If the pulse width is the preferred control feature, it can also suggest a limit on the allowable duty cycle:

$$\frac{\tau}{\alpha} = PW_{\mathrm{Max}}. \tag{5}$$

In the final analysis, this AlGaN channeled, multi-fingered HEMT demonstrates heating behavior dominated by the accumulation of heat in the device between individual pulses. The magnitudes of the temperatures shown in Figs. 2(a) and 2(b) demonstrate behavior suggestive of a dynamic equilibrium state and illustrate the effect of substrate heat accumulation. Figure 2(c) shows the relatively long thermal time constants inherent to this device, summarized in Table I, which supports the claim that there is insufficient time to reject heat during the device-off duration. The analysis of the key operating temperatures shown in Fig. 3 indicates a conjectured

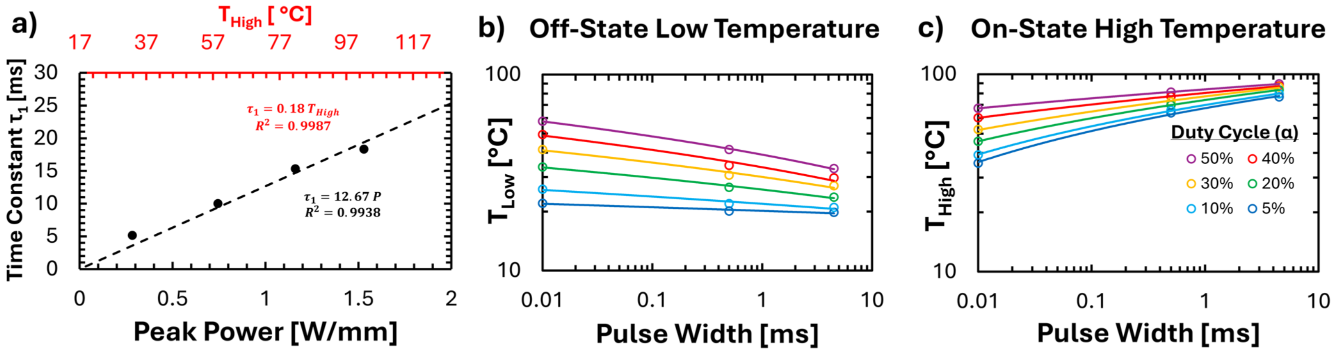

FIG. 4. (a) First (dominant) time constant in the two-term exponential fit [Eq. (3)] to the steady-state temperature decay, related to both the steady-state device power density and temperature, showing a linear relationship between the time constant and both operating parameters. (b) Off-State low temperature for each duty cycle across the range of pulse widths explored in this study. (c) On-State high temperature for each duty cycle across the range of pulse widths explored in this study. (a) T_{High} (°C). (b) Off-state low temperature. (c) On-state low temperature.

relationship between the steady-state operating temperature and the averaged operating temperature of the device, which may also be related to the heat accumulation effect. The primary time constant in this device is relatively long, as shown in Fig. 4(a), and within a region of linearity, we can estimate it. This allows for predicting the domain of operating conditions where heat accumulation poses a risk. It is also possible to draw some reasonable inferences about the operation of devices of this type from Figs. 4(b) and 4(c), suggesting operating conditions that may reduce the risk of heat accumulation.

Sandia National Laboratories is a multi-mission laboratory managed and operated by the National Technology & Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy's National Nuclear Security Administration under Contract No. DE-NA0003525. AlGaN HEMTs were provided by Sandia National Laboratories as part of the sponsorship of Muhammad S. Jamil during the academic year 2023–2024. Dominic Myren was supported by the Department of Defense (DoD) through the National Defense Science and Engineering Graduate (NDSEG) Fellowship Program.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

D. Myren: Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Writing – original draft (lead); Writing – review & editing (lead). **M. S. Jamil**: Data curation (equal). **B. A. Klein**: Conceptualization (equal); Resources (equal). **A. A. Allerman**: Conceptualization (equal); Resources (equal). **A. M. Armstrong**: Conceptualization (equal); Resources (equal). **L. Yates**: Conceptualization (equal); Formal analysis (supporting); Funding acquisition (equal); Project administration (lead); Resources (equal); Supervision (equal); Writing – original draft (supporting). **G. Pavlidis**: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Project administration (equal); Supervision (equal); Writing – original draft (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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