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LABORATORY DIRECTED RESEARCH & DEVELOPMENT
WHERE INNOVATION BEGINS

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LDRD PROJECT NUMBER: 25-0667
LDRD PROJECT TITLE: Ion Traps and Packaging for Heterogenous Integration - Chimera
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ABSTRACT:

Microfabricated surface ion traps and silicon-based photonics are critical technologies for scaling quantum systems. Current ion trap architectures face scalability and integration challenges due to limitations in optical access, fabrication techniques, and material compatibility. State-of-the-art quantum computers and atomic clocks are investigating monolithic integration, which necessitates custom traps for each ion species and has not overcome the integration hurdles presented by merging these technologies. The Chimera (Ion Traps and Packaging for Heterogeneous Integration) project proposes a novel approach utilizing heterogeneous integration (HI) of ion traps and photonic circuits. This separation of components allows for flexibility in ion trap design and reduces fabrication compromises.

The Chimera project specifically designed an ion trap to interface vertically with a separately fabricated waveguide chip and demonstrates the first steps to integrating them at the packaging level. The ion trap features a large area of removed silicon, allowing the photonics chip outputs closer to the ion trap, improving alignment and packaging processes. The alignment must be accurate to < 1 μm to ensure that the light from the waveguide can overlap with the trapping region. This fine alignment must also be maintained through an ultra-high vacuum bake, a critical step in preparing an ion trap experiment.

By combining separate chips, we demonstrate a new path for scaling trapped ion technology that is less reliant on monolithic integration. We successfully fabricated a trap with a large area of oxide removed, resulting in a region thinned to about 40 μm, a key milestone toward successful integration.

INTRODUCTION AND EXECUTIVE SUMMARY OF RESULTS:

Trapped ion technology continues to stand out as a leading platform for quantum computing and atomic clocks [1-3]. To increase the ion numbers in an individual system or miniaturize the technology, we need to increase the optical access for laser addressing and detection. Traditional systems, and most of the state-of-the-art systems are still forced to use lasers external to the

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vacuum system and a single, large, detection system. These requirements are partially due to the integration challenges of bringing the technologies on chip.

While there several successful demonstrations of monolithic integration of individual technologies, such as detectors or waveguides [4-7], these have yet to be integrated at a commercial level due to fabrication limitations. These approaches have shown critical steps towards scaling, such as the powers needed to drive gates, and the control that can be achieved. Additionally, the light and ion now have a common control surface, removing the influences of vibrations and leading to a more stable trapping environment and lower decoherence. However, large scale commercial systems require extremely reliable ion performance to achieve high fidelities. The fabrication challenges that arise with monolithic integration can lead to poor beam shape and difficulties introducing detectors. To truly scale these systems, the integrated technology needs to go beyond grating couplers, and this is a more difficult barrier.

To combine these integrated technologies has been a challenge due to the incompatibility of some fabrication steps and the sensitivity of the ions. Often, some components or fabrication processes need to be skipped to accommodate the final product. As a result, the performance of the ion trap or the photonic components is reduced. To create a scalable quantum computer, extremely high-fidelity quantum operations are required, these compromises in fabrication can directly detract from this goal.

In contrast to monolithic integration, this work studied the potential advantage of combining technology at the packaging level (similar to classical computing components) or a heterogenous integration (HI) approach. Unlike monolithic integration, HI cannot rely purely on lithography for aligning the photonic components to the ions. However, the mechanical alignment introduces the ability to make separate pieces that are more interchangeable, most notably allowing for a single ion trap to be designed for all ion species and only specializing the photonic integrated circuit (PIC). This interchangeability of parts can reduce turn-around time on advancement by reducing the time to fabricate new PICs as the overhead for the ion trap is separate. To succeed, the PIC outputs need to be aligned to within 1 μm of the trapping region (a limit determined by the trapping volume and beam size overlap). Previous work has demonstrated that a 1D alignment transverse to the trapping axis is possible within this tolerance [8]. Here we will show the vertical placement can also be achieved within 3 μm of the target and with less than 1 μm of variation. Such that the intended target can be modified to account for initial discrepancies.

Vertical integration of a PIC and ion trap is complicated by the thickness of the silicon chip. To minimize the horizontal spread of the optics on the PIC, the output couplers should be as close to the ion as possible. Additionally, getting gratings to focus much further than 200 μm from the PIC surface is challenging. To overcome these obstacles, we thin the ion trap in the region of PIC integration to allow for the PIC surface to be less than 200 μm from the ion. This development and resulting demonstration of PIC integration is the key milestone towards HI. In combination with the previous work highlighting the horizontal placement, we show that the vertical placement is possible using processing compatible with wafer scale fabrication.

The Chimera trap was designed to integrate to a larger footprint PIC, comparable to what a full-scale ion trap may require. The PICs used in this work are the same chiplets from [8] but diced in a larger size to better reduce tilt errors in the vertical integration. The trap has a slot in the center for allowing light from the waveguide chiplets to pass through to the ion. The surface electrode geometry is relatively simple facilitating manufacturing such that a trap could be produced within the timescales of this project. To thin the ion trap such that the surface of the waveguide chip is < 200 µm from the ion over the entirety of the chip could cause the chip to become extremely fragile and challenging to handle. Alternatively, we chose to expand on the process for creating slots to remove a large area on the backside and leave a full thickness edge around 3 of 4 sides of the trap. To enable soldering of the PIC directly to the ion trap, thus creating the base for a stable interface, we coat the backside of the trap with gold after removing the handle silicon and the buried oxide trench etch. We use these as the mechanical interface to the ion trap and demonstrate the ability to repeatably align to the trap within 1 µm of the desired height.

DETAILED DESCRIPTION OF RESEARCH AND DEVELOPMENT AND METHODOLOGY:

The chimera trap design (shown in Figure 1) is based on the unit ion trap first utilized in [9] and later adapted for monolithic photonic integration. We selected this trap design because it is relatively simple, straight-forward to modify, and successfully trapped ions. Following published RF electrode geometry guidelines [10], we modified the RF electrode to include a 20 µm through-substrate trench in the trapping region with a targeted ion height of 50 µm above the electrode surface. The trench was chosen as it enables backside loading of ions and optical access to the trapped ions. Also, the trench enables freedom in alignment along the trap axis.

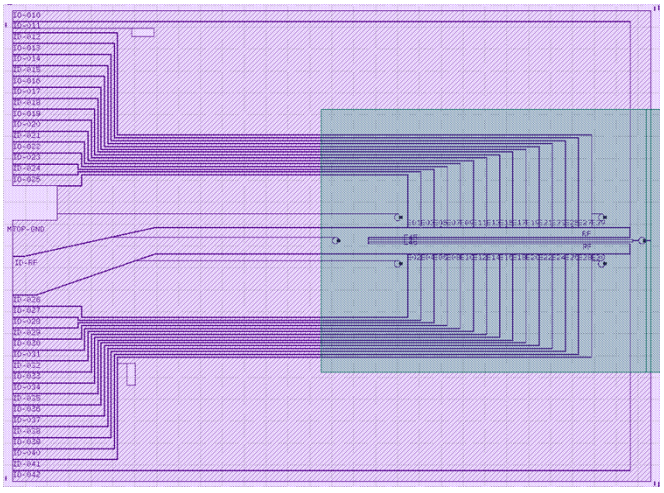

Figure 1: GDS layout of the Chimera trap. The trap is a 2-layer trap, where the bottom layer is continuous ground and only the top layer is patterned for simplicity. The green square is the region where the handle silicon is removed to allow the optical interposer to sit close to the trap surface.

We ran RF simulations on the trap design to confirm the ion height and trapping potential. The results indicate a true ion height of 55 µm as opposed to 50 µm. The simulated ion height and trap depth were within expected margins of errors to the designed values, so the design progressed to the tool fixture and packaging compatibility stage. Figure 2 shows the simulation results.

Additional design considerations for the chimera trap include using on hand tool fixtures, packages, and existing waveguide chips. We selected the 10x6 mm tool tip because it required minimal

trap electrode routing. A standard bow-tie ceramic package because electrode pitch between trap and package match. The physical placement of the trap onto the tool tip and package were verified in Klayout using the image import feature.

Fabrication Plan 1

The fabrication process plan for the Chimera trap was designed to be simple and fast. There are two metal layers with the first one serving as a ground plane. A large M1 pad is etched to eliminate the need for fabricating vias. The metal layers are primarily gold, which is favored for ion trapping top metal (no native oxidation formation) and compatible with anhydrous HF. The dimensions of the 20 µm wide through wafer trench in the trapping region can facilitate a 12 µm oxide etch + 20 µm silicon etch using the same photomask minimizing overhead for additional masks.

The preliminary Chimera trap fabrication process was:

1. Inspection of starting material (8" SOI material with 20 µm device Si / 1 µm buried oxide / 700 µm Si / 1 µm backside oxide)
2. Pre-metal dielectric deposition (1 µm PETEOS)
3. M1 lithography
4. M1 evaporation (0.02 µm Ti/ 1.0 µm Au)
5. M1 Liftoff
6. Intermetal dielectric deposition (10 µm PETEOS)
7. M2 lithography
8. M2 evaporation (0.02 µm Ti/ 1.0 µm Au)
9. M2 liftoff
10. Top metal oxide (1 µm PETEOS)
11. M1 pad lithography
12. M1 pad etch & strip
13. Trench lithography
14. Trench oxide etch + silicon etch
15. Backside lithography
16. Backside Si etch
17. Dicing singulation
18. Anhydrous HF

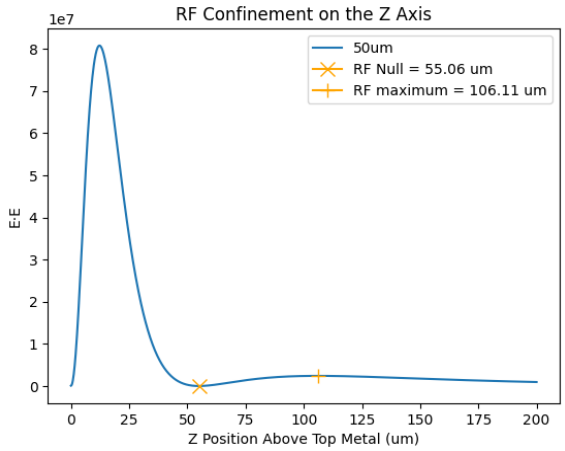

Figure 2: Chimera trap simulation results. The plot shows the simulated RF pseudopotential as a function of distance from the trap surface. The large asymmetry is typical in surface traps. The minimum at 55 µm, marked with an X, is the location of the RF null, where the ion sits. This determines where we aim to align the waveguide output coupler.

Fabrication 1 Results

The first fab run was stopped at step 9 (M2 liftoff) in the process flow due to wafer-wide PETEOS oxidation delamination in the trap

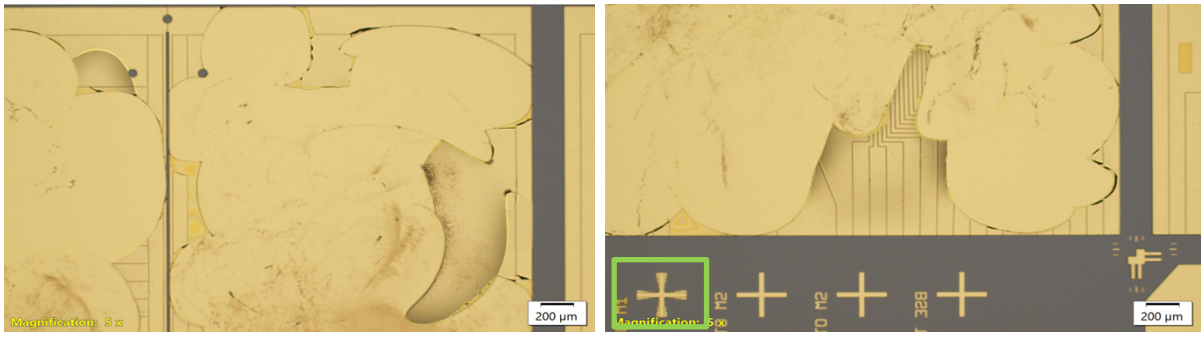

Figure 3: Images of chimera trap fabrication run 1, wafer 1. Top metal trap region encountered delaminating oxide in Chimera trap chip. Top metal pattern isn't present in the delaminated regions. Of note is the M1 and M2 alignment marks, in green box, did now show evidence of oxide delamination. Blistering did not occur in regions without M1, suggesting a problem with the M1/oxide interface.

region. Figure 3 shows microscope images of the wafers after the lot went through an O_2 ash process to cleanup post-liftoff residues.

We conducted a causal analysis and reached out to in-house fab subject matter experts to determine the root cause and generate corrective actions. Based on the evidence, we attributed the cause of the failure to a poor adhesion between the gold and silicon oxide. Therefore, step 4 of the process flow was modified to include a 20 nm adhesion layer on the top of the Au metal stack. This is the same adhesion film used to help bond the bottom of the metal to the pre-metal dielectric film.

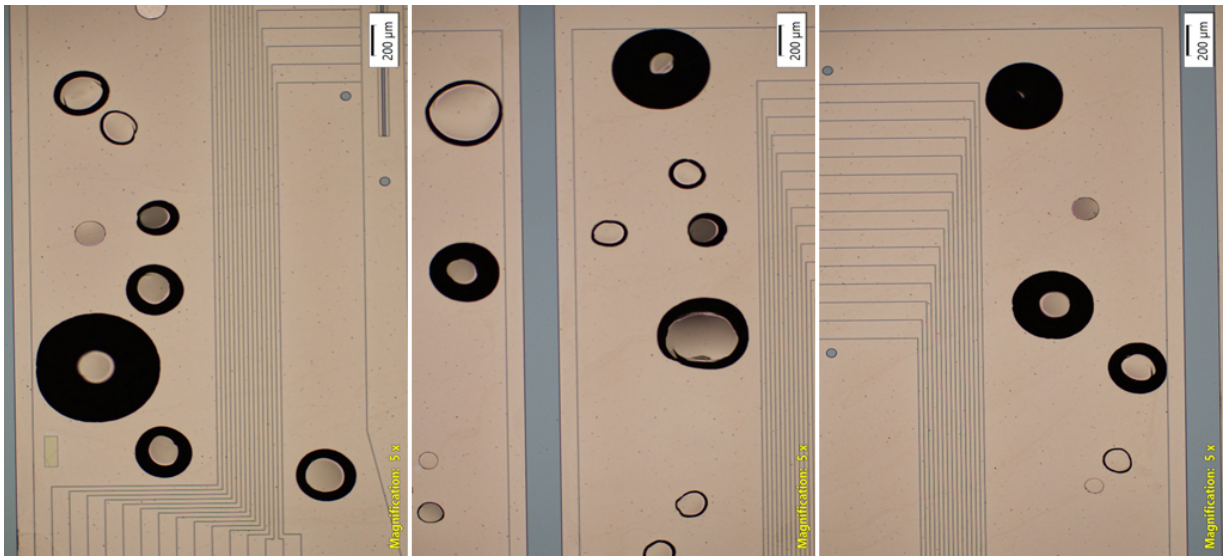

Figure 4: Images of chimera trap run 2 after top metal oxide deposition [step 9]. Blistering occurs primarily over regions of blanket M1 & M2 patterning. Aside from one instance, the M2 patterned regions do not show this defect.

Fabrication Plan 2

After modifying the plan, we repeated the attempt to fabricate the Chimera trap. This run successfully processed through step 9, which was the point of failure in run 1. Unfortunately, run

2 encountered PETEOS film delamination problems during the subsequent step: 1 µm PETEOS deposition over M2. We collected microscope and SEM images to help narrow in on the root cause. The delamination on run 2 was not as severe as run 1, and the occurrence pattern also differed. As shown in Figure 4, the delamination occurred on regions with large coverage of M2. Aside from one delamination defect observed inside the M2 pattern region, all other delamination defects occur in the M2 ground plane. This defect occurrence pattern differs from run 1 where the entirety of the M2 region was affected.

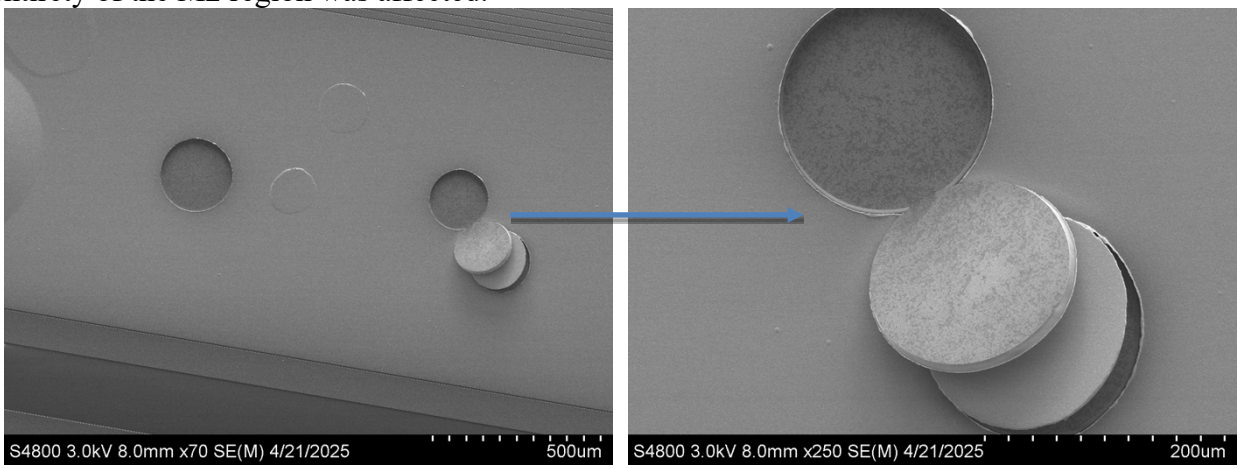

Figure 5: SEM analysis of run 2 blister defects. SEM indicates these defects result from the oxide + M2 stack delaminating from M1.

We further characterized the defects under SEM defect review. The analysis shows the delamination occurs at the M1/oxide interface as shown in Figure 5, which is the same point of failure observed in run #1. The addition of the Ti adhesion layer appeared to help but was not sufficient to completely prevent delamination defects.

Due to time constraints on this project, the goal of the fab 2 causal analysis was to ensure the success of fab run 3, as opposed to isolating a specific root cause. Therefore, we casted a broad net of potential root causes and ways to mitigate/prevent their formation which were:

- Weak M1-oxide interface.
- PETEOS oxide film off gassing.
- Post-liftoff residues on M1.

To mitigate these identified risks, the following changes were proposed for fab run 3. First, switch M1 to TiN / AlCu / TiN film stack. This is a proven film stack used on other ion trap designs, which should mitigate risks of M1/oxide interface defects. To facilitate this change, the first oxide film and this metal stack are deposited in the MESA CMOS fab prior to transferring over to the MESA compound semiconductor fab. Next, switch from 10 µm PETEOS to 5 µm CVD silicon oxide process. This is a denser oxide with a lower likelihood to off gas versus PETEOS. Oxide

thickness was reduced to 5 µm to prevent excessive wafer bow. Originally, 10 µm was desired to attempt to develop another thick oxide process that is compatible with ion traps as another method to reduce potential RF breakdown [11]. Finally, switch M2 film stack from 0.02 µm Ti / 1 µm Au to 0.02 µm Ti / 1 µm Al / 0.02 µm Ti / 0.01 µm Pt / 0.250 µm Au. This is representative of the standard Sandia top metal stack. Addition of Pt diffusion barrier between the titanium and gold to mitigate risk of Ti/Au alloy formation which may have compromised the M1/oxide interface in run 2.

Fabrication Plan 3

The third process flow incorporates all the process changes recommended in run 2's causal analysis and yielded usable parts. The modified process flow was:

1. Inspection of starting material (8" SOI material with 20 µm device Si / 1 µm buried oxide / 700 µm Si / 1 µm backside oxide)
2. Pre-metal dielectric deposition (1 µm PETEOS in MDL)
3. M1 deposition (0.05 µm TiN/ 1.2 µm Al / 0.15 µm TiN)
4. Move from SiFab to uFab
5. M1 lithography
6. M1 etch & PR strip
7. Intermetal dielectric deposition (5 µm CVD oxide)
8. M2 lithography
9. M2 evaporation (0.02 µm Ti/ 1.0 µm Al / 0.02 µm Ti / 0.10 µm Pt / 0.25 µm Au)
10. M2 liftoff
11. Top metal oxide (1 µm PETEOS)
12. M1 pad lithography
13. M1 pad etch & strip
14. Trench lithography
15. Trench oxide etch + silicon etch
16. Backside lithography
17. Backside Si etch
18. Backside oxide etch
19. Backside metal deposition (0.02 µm Ti / 0.10 µm Pt / 0.25 µm Au)
20. Dicing wafer into quarters.
21. Dicing to singulate die in quarter of wafer.
22. Mount die to carrier wafer.
23. Silicon oxide etch.
24. Unmount die from carrier wafer.

The M1 pad etch landed properly. The frontside and backside trench etch steps, which were anticipated to the be challenging parts of the process flow, worked surprisingly well. Figure 6 shows a Chimera trap part post-trench etch with and without backside illumination.

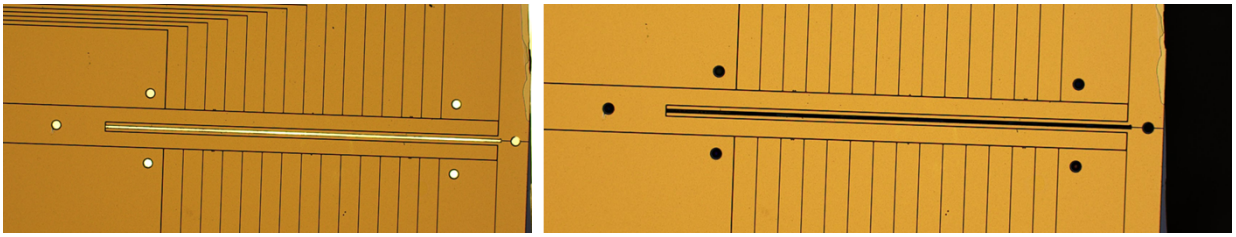

Figure 6: Chimera trap with (left) and without (right) backside illumination. The trench and Femto II fiducials (circles) allow light to pass through, indicating the through-wafer etch is successful.

RESULTS AND DISCUSSION:

After fabricating the traps, they need to be singulated by dicing. We anticipated challenges at this step because we are cutting into the backside trench region. This results in the dicing saw cutting through the suspended 20 µm device silicon and oxide films. We believed that wider trenches posed more of a risk of the saw catching the thin device region and tearing it out. To mitigate this risk, we included several backside trench widths ranging from 600 µm to 2.4 mm. The MESA packaging team recommended these dicing conditions: place trenches towards the tape (i.e. frontside up), use UV tape and after expose to break bond, and place assembly on porous ceramic vacuum dice chuck to keep wafer flat while removing UV tape. In addition to those specifications, we chose to forego a photoresist (PR) protect layer. Other groups at Sandia have anecdotal evidence suggesting PR protect causes silicon oxide chipping; therefore, we relied solely on the frontside 1 µm oxide film to protect top metal.

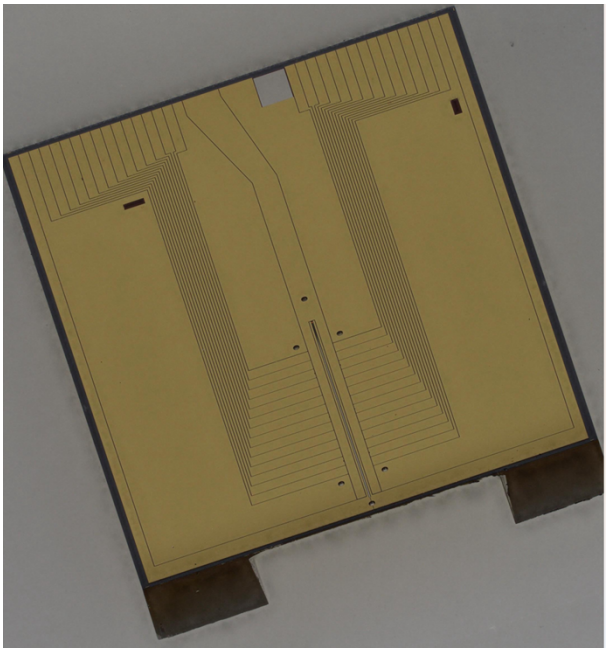

Figure 7: Microscope image of diced Chimera trap taken in 45-degree fixture and tilted slightly. Image obtained by using a focus scan to keep the entire trap in focus. The backside trench region is visible on the bottom. The full handle silicon (700 µm) is present on each end of the trap and along the sides where the trench has been removed, the remaining silicon appears dark brown in this image.

The dicing was done on a per quarter wafer basis in the event that an entire dicing run failed. Fortunately, the first dice process yielded about 25% good die. Most of the yield loss was particle defects. Only a couple parts showed potential evidence of dicing saw chipping in the trap region. An isometric view of a diced Chimera trap is shown Figure 7, which shows the top trapping region along with the backside trench.

The next step in the trap fabrication process is removing the protective 1 µm oxide film off the top metal using anhydrous HF. The

anhydrous HF process resulted in a lot of residues on the frontside metal. Our efforts to clean up the residues using solvent and ash steps were not successful, and the exact root cause is unknown. Fortunately, MESA's ability to mount chips to carrier wafers improved over the course of this project and allowed us to switch from an anhydrous HF process to a plasma dry etch process, which yielded good results. Figure 8 shows a Chimera trap that underwent either anhydrous HF (left) or plasma dry etch process (right) to remove the oxide over top metal.

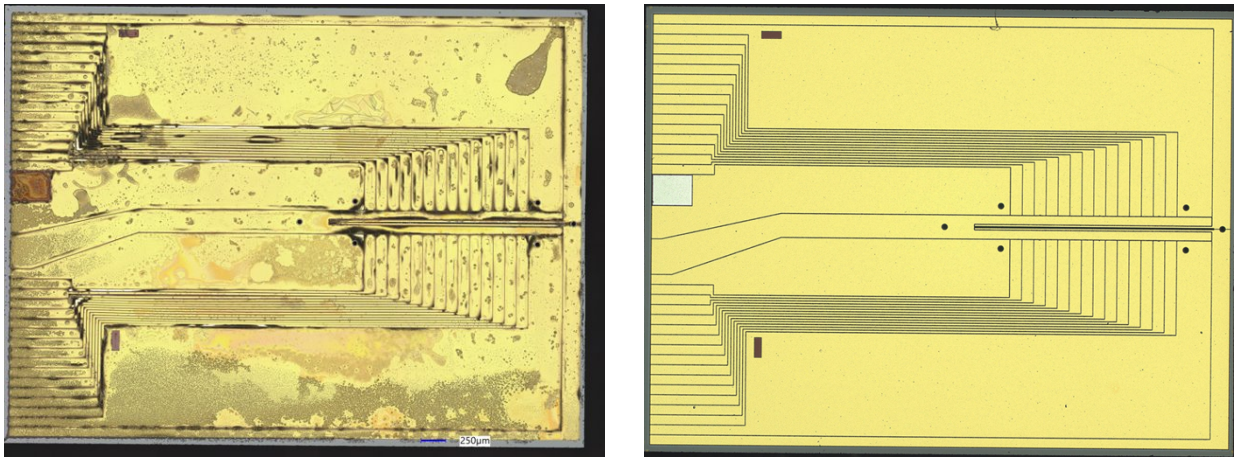

Figure 8: Image of Chimera trap after anhydrous HF process (left) and image of another Chimera trap after silicon oxide dry etch process (right).

After the plasma dry etch, the parts were binned as good for packaging or setup and delivered to the packaging lab for assembly.

The resulting traps had successfully had large regions of oxide removed and singulated with a 25% yield. Ion traps can afford lower than perfect yields as not many traps are needed for an experiment, in fact typically a single good device is sufficient. While the yield may seem low, it is well within the acceptable yield ranges. From the singulated die, we package the devices where our second achievement comes to light.

The Chimera trap was fabricated with dedicated through-substrate alignment fiducials which were necessary to accurately attach the waveguide chip to the underside of the device while aligning to the metal features on the topside of the device. In conjunction with the purpose-built Chimera trap, several changes were made to the processing of the waveguide chiplets. Due to the larger backside cavity on the trap, the waveguide chiplets could have a larger footprint; previous iterations of

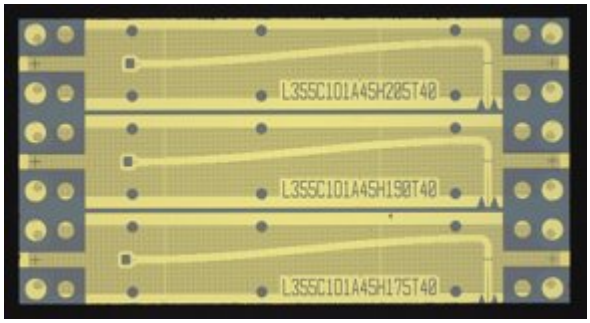

Figure 9: Optical image of the waveguide chiplet used for the Chimera trap. Only the bottom waveguide is intended to interact with the ion, the others are left attach to increase handling area.

the waveguide chiplet were taller than they were wide, which made them difficult to handle and align. The waveguide chiplets for this project used the same reticle set used previously; however, the waveguide chiplets were diced into blocks of 3 die (shown in Figure 9), instead of diced individually. To be compatible with the trap-package assembly, the waveguide chiplets were thinned to a total thickness of 550 µm so that they did not protrude beyond the bottom of the trap surface when assembled; previously, the waveguide chiplet would protrude beyond the bottom surface of the trap, creating an additional handling consideration.

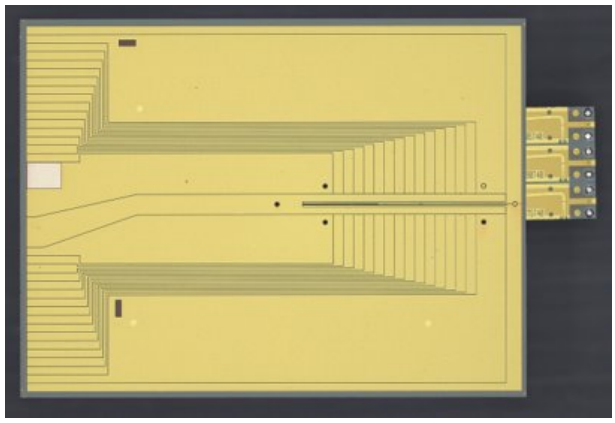

Figure 10:Image of the Chimera trap with the waveguide chiplet attached to the back. The output grating coupler is seen in the center of the trap slot as a small green dot.

While we were unable to complete the full assembly procedure for the Chimera device, we were able to test several key aspects of the packaging process and learn more about the limits of the precision die bonding tool. One of the die used in the assembly tests in shown in Figure 10. During assembly tests, we were able to tune the z offset of the waveguide chiplets to within 3 µm of the target height by compressing or stretching the solder balls when melted during the bonding process. This result was consistent between assemblies using the same bonding parameters, albeit with a small sample size.

We also found that the larger footprint waveguide, which accommodates a larger number of solder balls is less sensitive to variations in solder ball volume when performing roll and pitch alignment on the die bonding tool. Previous solder ball heights had to be individually measured to ensure that the waveguide chiplet could be aligned to the device using just four points of contact. The larger chiplets were jetted with 12 solder balls and did not need to be individually measured.

During the bonding tests, we discovered several limitations of the die bonding tool related to the machine vision system and alignment accuracy. The machine vision system could not accurately locate fiducials of the same shape that were within 250 µm of each other, regardless of the image processing and alignment settings. For example, the circles used as alignment marks shown in Figure 8 and Figure 10. This will be a serious design consideration moving forward. Furthermore, the assemblies exhibited systematic errors in the y-axis and theta that were difficult to fully correct during assembly. To position the waveguide outlet at the center of the trap slot, an offset of 6 µm had to be applied to all alignment marks. An additional y offset for one of the alignment marks was used to attempt to correct for the systematic theta error, which was consistently around 1 degree out of alignment. These systematic errors highlight the need to develop a more rigorous error correction method than the factory default, which uses a specially dedicated glass chip on an

unheated portion of the stage. Additional error correction may also be necessary to account for thermal expansion of the stage components during heated solder attach procedures.

ANTICIPATED OUTCOMES AND IMPACTS:

Advancements in trapped ion hardware are critical to the scaling of quantum systems. This project represents a critical step forward in addressing the challenges of scaling hardware by focusing on the development of heterogenous integration of PICs with trapped ions. This innovative approach allows for greater flexibility in ion trap configurations, as new systems can be designed with photonic circuitry in mind, but without committing to exact layouts or species. The technology can be more easily upgraded over time allowing for easier continuous development. The large cut-away demonstrated in the Chimera trap is a first demonstration of how traps can be fabricated specifically for this interfacing without compromising the fundamental performance of the trap itself. Though this trap was simple by ion trapping standards, the cut-away was compatible with all the standard trap ion processing and release steps. Thus, this cut-away validates a critical step forward towards HI and the future advancement of quantum technologies which aligns with national interests by allowing for the potential integration of a broader range of technologies beyond just ion traps.

For this method to be truly successful, we must demonstrate an alignment accuracy of less than 1 μm between the ion trap and the photonics chip. This tight tolerance is due to two major factors. (1) The tight beam waists required to keep the power at the ion small, ideally on the order of 2-3 μm for a qubit beam. (2) Small trapping volume of the ion trap, moving the ion from the center of the RF trap leads to increased motion and thus decoherence. Once the beam is more than a beam waist off of the RF node, the ion will be sampling a large gradient in power which can lead to decoherence. Together, these determine that the overlap is critical to the assembly process. In this work, we showed that we were able to achieve heights repeatably within a 1 μm of each other. This repeatability can be used to dial in the intended height to the same precision, a key step in HI. Together with the previous work [8], we believe this shows we have the tools to align 2 of 3 dimensions within the necessary tolerance. With creative trap design and better alignment marks, the third dimension should be achievable as well.

Leveraging heterogeneous integration (HI) in ion traps holds significant promise for enhancing throughput not only in the manufacturing of traps but also across all technologies related to trapped ions. This initial demonstration of HI serves as a foundation for integrating additional technologies into various quantum devices, thereby broadening the scope of applications within the quantum computing landscape. The alignment tolerances required for trapped ions are among the most stringent in the field, as ions have very limited radial movement within an ion trap. However, the benefits of photonic devices extend to any quantum technology that relies on light. For instance, recent efforts in neutral atom quantum computing have begun to incorporate photonic modulators to facilitate scaling [12], demonstrating the versatility of this approach. Lasers, which are integral to numerous areas of quantum research, can also benefit from robust methods of coupling

technologies across chip boundaries. This capability is particularly important for integrating these systems into cryogenic and ultra-high vacuum (UHV) environments, where precision and reliability are paramount.

Addressing the challenges associated with positional alignment and stability amid temperature fluctuations is critical for the successful heterogeneous integration of ion traps. This research shows that these obstacles can be effectively managed through strategic approaches, such as co-designing traps and chips to facilitate easier alignment and adhesive application. To scale these quantum systems, we need methods to improve turn-around time for developments which underscores the urgent need for innovative packaging methods, enhanced alignment accuracy, and advanced techniques for chip-to-chip registration and attachment. Scaling the support technology for quantum systems is vital for the overall advancement of quantum technology itself. The heterogeneous integration of ion traps will enable the incorporation of more sophisticated photonics and additional technologies, thus aligning with national interests by fostering a wider array of quantum technologies. This approach has the potential to significantly increase throughput in trap manufacturing and other related fabrication technologies, ultimately contributing to the growth and sustainability of the quantum computing field.

CONCLUSION:

The Chimera project made significant steps towards advancing the integration of ion traps with photonic circuits, where we addressed critical challenges in the scalability and performance of quantum systems. This research demonstrated the potential to enhance the design and function of ion traps through etching interfaces for proximity mounting without compromising the fabrication processing steps.

Successful heterogenous integration of photonic chips with ion traps highlights the needs for tight alignment precision. This work has shown that co-designing the trap with the photonics chip can lead to easier integration by facilitating the alignment. These advancements are critical for enabling precision alignment in all spatial dimension as well as maintaining that alignment though achieving an ultra-high vacuum environment.

Expanding optical access is critical for scaling trapped ion technology, which is fundamentally necessary for advancing quantum computers and atomic clocks. Traditional ion trap setups face constraints imposed by vacuum chambers and large light collection optics. As quantum computers scale from tens to millions of ions, the current approaches encounter barriers related to resource scaling, thermal dissipation, and fabrication.

Transitioning away from monolithic integration enables the incorporation of more advanced technologies allowing us to overcome immediate scaling. This work suggests that packaging chips together, in a 3-dimensional stack, is possible which paves the way for more sophisticated and scalable quantum computing systems. By confidently designing separate pieces and assembling them together into an ion trap processor, we can integrate all necessary supporting technology into a single packaged device, marking a significant step towards the future of quantum computing.

REFERENCES:

[1] M. C. Marshall, D. A. Rodriguez Castillo, W. J. Arthur-Dworschack, A. Aeppli, K. Kim, D. Lee, W. Warfield, J. Hinrichs, N. V. Nardelli, et al. High-Stability Single-Ion Clock with 5.5×10^{-19} Systematic Uncertainty. Physical Review Letters, 135, 033201 (2025).
[2] M. DeCross, R. Haghshenas, M. Liu, E. Rinaldi, J. Gray, Y. Alexeev, C. H. Baldwin, J. P. Bartolotta, M. Bohn, et al. Computational Power of Random Quantum Circuits in Arbitrary Geometries. Physical Review X, 15, 021052 (2025).
[3] E. Tham, M. Ye, I. Khait, J. Gamble, N. Delfosse. Distributed Fault-Tolerant Quantum Memories over a 2×L2×L Array of Qubit Modules. arXiv:2508.01879 [quant-ph] (2025).
[4] K. K. Mehta, et al. Integrated optical addressing of an ion qubit. Nature Nanotechnology, 11, 1066 (2016).
[5] J. Stuart, et al. Chip-integrated voltage sources for control of trapped ions. Physical Review Applied, 11, 024010 (2019).
[6] M. Ivory, et al. Integrated optical addressing of a trapped ytterbium ion. Physical Review X, 11, 041033 (2020).
[7] W. J. Setzer, et al. Fluorescence detection of a trapped ion with a monolithically integrated single-photon-counting avalanche diode. Applied Physics Letters, 119, 15, 154002 (2021).
[8] M. Revelle, A. D. Burch, L. Ijzerman, R. Haltli, E. Ou, T. Redhouse. SIREN: Scaling Ion-Traps by REquiring iNnovative Heterogeneous Integration. Technical Report (2024).
[9] Stick, D., Barrick, T., Blain, M., Lepkowski, S., & Nordquist, C. Understanding Voltage Noise in Ion Traps (UNIT). Sandia National Laboratories. SAND2021-12930 (2021).
[10] S. Hong, M. Lee, H. Cheon, T. Kim, & D.-il "Dan" Cho. Guidelines for Designing Surface Ion Traps Using the Boundary Element Method. Sensors, 16(5), 616 (2016).
[11] J. M. Wilson, J. N. Tilles, R. A. Haltli, E. Ou, M. G. Blain, S. M. Clark, & M. C. Revelle. In situ detection of RF breakdown on microfabricated surface ion traps. J. Appl. Phys., 131, 134401 (2022).
[12] Dong, M., Zimmermann, M., Heim, D. et al. Programmable photonic integrated meshes for modular generation of optical entanglement links. npj Quantum Information 9, 42 (2023).