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Non-Destructive Interlevel Dielectric Via In-Line Process Monitoring by Atomic Force Microscopy

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Abstract

A new application using atomic force microscopy (AFM) for in-line process control monitoring (PCM) of an interlevel dielectric via etching step is reported. The AFM with its near atomic-level resolution is capable of non-destructively measuring whether micron-sized vias have been etched to completion. Etch completion is determined by comparing the AFM measured etch depth of adjacent via holes through ~4000 Å thick Si_3N_4 over Au-based ohmic and W gate metallizations. Due to etch selectivity, of the SF_6/O_2 reactive ion etch (RIE) generated plasma, the ohmic metal acts as an etch stop whereas the W-based refractory gate continues to etch. For etch times beyond endpoint in the range of 20 to 50%, the AFM measured via etch depth differences is 250 to 400 Å when comparing via depths over ohmic metal and W gate metal. This etch depth difference is a specific marker for etch completion and it is measured non-destructively at a point in the process where rework is still a feasible option.

Introduction

During the processing sequence for digital integrated circuits such as a GaAs-based complementary heterostructure field-effect transistors (CHFETs) [1], numerous situations exist where an in-line, non-destructive, PCM step is required. Traditional characterization techniques such as SEM and optical microscopy are either destructive or not capable of resolving micron-sized features. The example to be presented in this paper is the development and utility of an interlevel dielectric via etch process characterization step for a multilevel metal interconnect. Underetched via holes lead to "opens" between the interconnect metal and underlying ohmic or gate metal pads due to Si_3N_4 left in the via. Using surface profilometry measurements on larger area etched features for process monitoring is an option but, the results can be misleading due to microloading effects (differing etch rates for small and large area features) and etchant transport effects (etchant is less efficient getting into small diameter deep features) which are common in RIE. PCM of the via etch was previously characterized using destructive cross-sectional SEM analysis. The atomic force microscope (AFM) [2] is capable of directly measuring the etch depth for micron-sized features. In this paper we will report a new AFM-based characterization technique for a interlevel dielectric via process which operates in an in-line, non-destructive fashion. This technique will be an important yield-enhancing tool for IC manufacturing.

Results and Discussion

The GaAs-based FET fabrication steps relevant to this work are as follows: (1) Refractory gate definition with a 3000 Å thick W film and RIE; (2) Ohmic metal definition with ~3000 Å of GeAuNiAu; (3) Interlevel dielectric deposition using ~4000 Å of Si_3N_4; and (4) Fabrication of 1.25 μm via holes defined by optical lithography and etched in a RIE SF_6/O_2 generated plasma. Endpoint is determined during the plasma etch using in-situ optical interferometry on large open areas. If the via hole resist mask is even slightly underexposed or underdeveloped, resist may remain in the via resulting in an incomplete etch and cause an "open" in the circuit. Optical inspection of individual 1.25 μm via holes cannot

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distinguish between vias with resist scum and those without. Using Dektak measurements on larger etched features is an option but, the results can be misleading due to RIE-associated microloading and transport effects, and differences in Si_3N_4 thickness of larger areas and small areas over metal. SEM analysis has also been unsuccessful unless operated in the destructive cross section mode. Via etch rates and etch depths can also be determined by destructive and time consuming SEM analysis on sacrificial devices. This technique works for characterizing a process but is unsuitable for in-line process monitoring.

Because of the destructive nature and limitations with other characterization techniques, development of an in-line, non-destructive AFM-based analysis method for the interlevel dielectric via etch process was investigated. An AFM image of five etched Si_3N_4 via holes over two ohmic Au-based metal pads and a W gate metal pad (a refractory gate FET) is shown in Figure 1. These images are generated by performing tapping mode AFM on a Digital Instruments, Dimension 3000 AFM system in a normal cleanroom environment after the via patterning step is completed. SEM images similar to this AFM image can be obtained non-destructively, but, 3-D digital height data is not available with SEM. Using the measured 3-D AFM data, the images are analyzed in cross section by taking line traces through the vias. Etch depths of 4018 Å and 3993 Å are measured for the vias in Figure 2. These values are correlated to previously recorded Si_3N_4 thickness values which were measured by ellipsometry. Using the AFM, we have determined that the deposited Si_3N_4 thickness on top of the metal ohmic and gate pads is 85 ±5% of the thickness measured optically over larger field areas. The optically measured field area thickness was also confirmed by performing AFM measurements on larger etched areas. For this sample, the average Si_3N_4 thickness in the field was 4450 Å which correlates to a Si_3N_4 thickness on metal pads of 3782 Å based on 85% thickness variation. Comparing the 3782 Å value to the AFM measured via etch depths of 4018 Å and 3993 Å, we conclude that the vias are etched to completion. Although this technique has measurement uncertainties on the order of ±5% which limit its ability to detect if the last 100 to 200 Å of Si_3N_4 are removed, it is a significant improvement in detecting non-destructively, unopened vias.

In order to identify a more highly controlled process control monitor using the AFM, vias were etched from 20 to 150% of endpoint. AFM characterization of the vias were evaluated over ohmic and gate metal for etch depth, RMS surface roughnesses, and via dimension. RMS surface roughness and via dimensions showed virtually no effect as a function of etch time. However, comparing the etch depth for vias over Au-based ohmic and W-gate metals as a function of etch time showed a difference as the vias were overetched. The etch depth for vias over the ohmic metal remained essentially unchanged whereas the etch depth over gate metal continued to increase due to the poor selectivity of Si_3N_4 over W in this plasma chemistry. Therefore an etch marker for completion was identified.

In Figure 3 the AFM measured etch depth for the vias over the gate and ohmic metals are plotted as a function of etch time. More significantly, the *difference* in measured etch depth between the gate and ohmic based vias are also plotted in Figure 3. The via depth over the Au-based ohmic metal reaches a maximum value, whereas, the via depth over the W metallization continues to increase. The F-based plasma etch chemistry used to etch the Si_3N_4 attacks the W gate once the Si_3N_4 is cleared but does not etch the Au-based ohmic. The amount of W removed during the Si_3N_4 etch was quantified by removing the Si_3N_4 overlayer with buffered oxide etchant (BOE) and then re-measuring by AFM. The selectivity of Si_3N_4 over W in BOE was quite high with virtually no loss of W. An AFM image of the 50% overetched sample is shown in Figure 4. The circular depression in the W gate and the lack of these features in the adjacent Au-based

ohmics represents the via chemistry selectively etching the W; this region of the W gate is exposed during the via overetch. This depression was measured by AFM to be 450 ± 50 Å; this equates to an etch rate of W in the SF_6/O_2 plasma of 690 Å/min (the Si_3N_4 etch rate is 3000 Å/min). The AFM measured depression depth and the previously measured gate - ohmic via depth difference are both plotted in Figure 5 as a function of percentage of endpoint. As expected, there is good agreement between these independently measured results. This difference in measured etch depth on adjacent via holes over ohmic and W metals is a non-destructive marker of via etch completion. The via process typically includes a 20% overetch to account for uncertainties in endpoint, microloading effects, Si_3N_4 thickness non-uniformities, and etch non-uniformity. With this specific process marker, we conclude that the vias are etched to completion as long as a 200 - 500 Å via etch depth difference (see Figure 5) is measured on adjacent gate- and ohmic-based vias by AFM,. Consequently, this in-line process check has been added to our GaAs IC fabrication sequence.

Conclusions

Using AFM we have developed an in-line non-destructive PCM technique for an interlevel dielectric via etch process. This technique relies on the difference in etch rate for Au-based and W-based metallization when exposed to the RIE generated SF_6/O_2 plasma used to dry etch the Si_3N_4 interlevel dielectric. During the 20% overetch the underlying Au-ohmic and W-gate metal pads are exposed to plasma when the via clears. During the overetch portion of the via process, Au is not noticeably etched whereas the W is etched at a rate of 690 Å/min to a depth of 250 to 300 Å; an etch depth difference easily detectable by AFM. Hence, if an etch depth difference less than ~100 Å is measured on adjacent gate- and ohmic-based vias, we conclude that the vias are underetched and the process limits have been exceeded. This process inspection technique is now routinely used in-line during CHFET fabrication in our laboratory.

We have found that by performing this type of AFM characterization in-line, we can conclusively identify failures at a point in the process where rework is still a feasible option.

Acknowledgments

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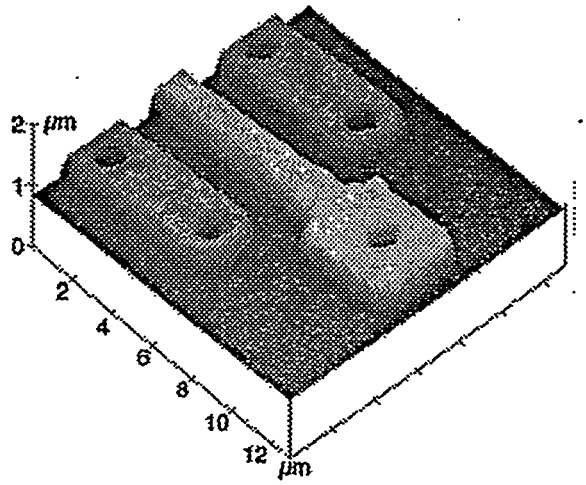

Figure 1.
AFM image of 1.25 μm via holes etched in Si_3N_4 which is covering a W gate and two ohmic pads.

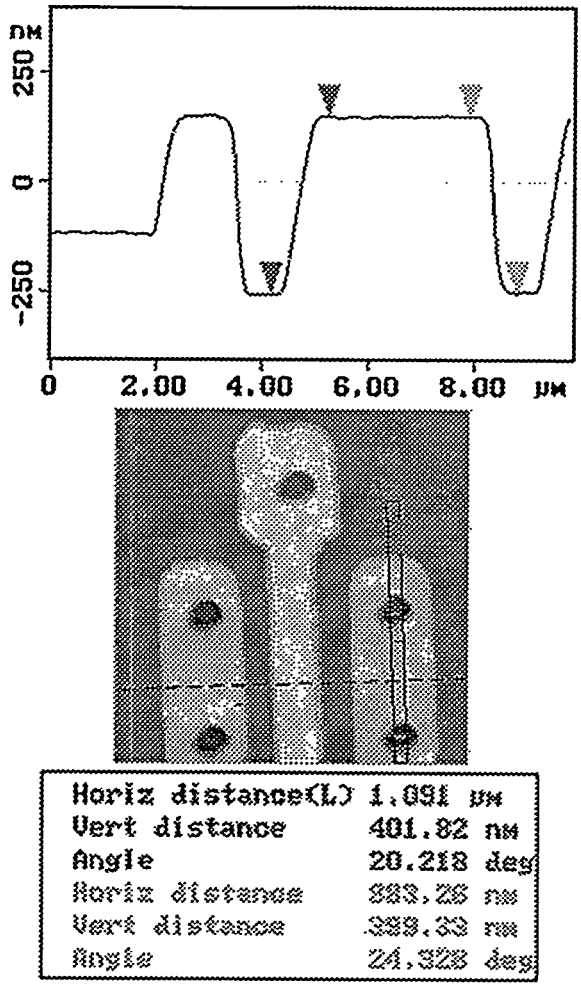

Figure 2.
Cross-sectional analysis method for determining via etch depth. The cursor placement yields via depths of 4018 Å and 3993 Å.

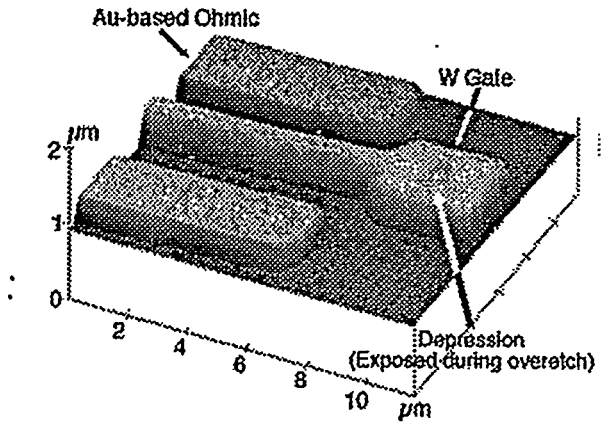

Figure 3.
AFM image of the 150% etched sample after the Si_3N_4 was chemically removed. Note the depression in the W gate and lack thereof in the ohmics.

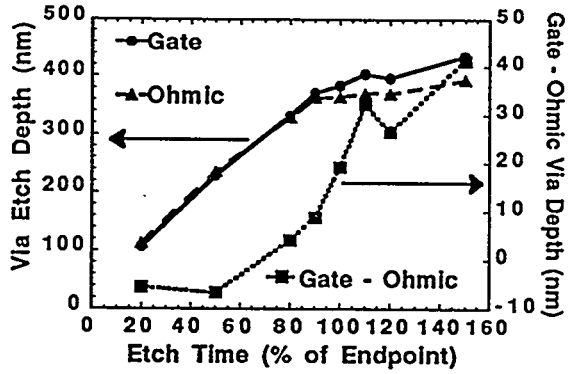

Figure 4.
Plot showing the AFM measured via etch depth over ohmic and gate metallizations as a function of etch time. The second plot is of the measured via depth over gate minus the via depth over ohmic; the difference increases due to W plasma attack during overetch.

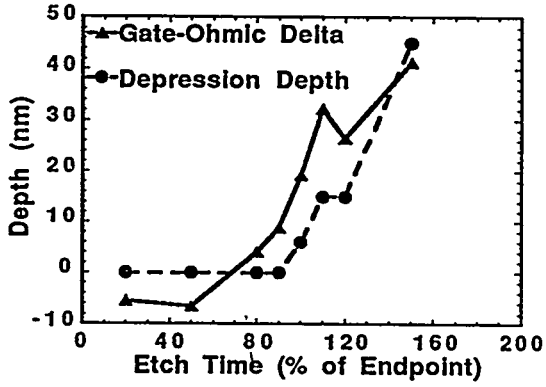

Figure 5.
A comparison between the AFM measured via depth over gate minus via depth over ohmic difference and the measured etched depth into the W gate metal (after Si_3N_4 removal) as a function of etch time.