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A. L. Wintenberg, J. P. Jones, Jr. and G. R. Young
Oak Ridge National Laboratory

C. G. Moscone
University of Tennessee

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A CMOS Integrating Amplifier for the PHENIX Ring Imaging Cherenkov Detector*

A. L. Wintenberg[1], C. G. Moscone[2], J. P. Jones[1], and G. R. Young[1],

[1]Oak Ridge National Laboratory, Oak Ridge, TN 37831-6006

[2]The University of Tennessee, Knoxville, TN 37996-2100

Abstract

A CMOS integrating amplifier has been developed for use in the PHENIX Ring Imaging Cherenkov (RICH) detector. The amplifier, consisting of a charge-integrating amplifier followed by a variable gain amplifier (VGA), is an element of a photon measurement system comprising a photomultiplier tube, a wideband, gain-of-10 amplifier, the integrating amplifier, and an analog memory followed by an ADC and double correlated sampling implemented in software. The integrating amplifier is designed for a nominal full scale input of 160 pC with a gain of 20 mV/pC and a dynamic range of 1000:1. The VGA is used for equalizing gains prior to forming analog sums for trigger purposes. The gain of the VGA is variable over a 3:1 range using a 5-bit digital control, and the risetime is held to approximately 20 ns using switched compensation in the VGA. Details of the design and results from several prototype devices fabricated in 1.2 μm Orbit CMOS are presented. A complete noise analysis of the integrating amplifier and the correlated sampling process is included as well as a comparison of calculated, simulated and measured results.

I. INTRODUCTION

The PHENIX Ring Imaging Cherenkov detector is used for particle identification using the Cherenkov photon ring generated in a gas radiator and imaged on a photon detector using a spherical mirror. The charge measurement electronics for the RICH detector are ultimately used to locate and measure rings, but the lowest level function of the electronics is to determine the number of photo-electrons generated in each photomultiplier tube (PMT) during a given interaction. One interaction will produce only a few photoelectrons at most in a single photomultiplier - assuming a maximum of 10 gives a considerable safety margin. The tubes (Hamamatsu H3171S) chosen for this detector will operate at gain of 10^7, so one photoelectron will produce an output of 1.6 pC. Because this is a relatively small charge (at least relative to other PMT-based detectors such as calorimeters), it would be advantageous to mount the electronics on or near the PMT to minimize any ill effects such as pickup, loss or distortion due to a long cable. However, since the radiator gas is flammable and the gas vessel is somewhat inaccessible, remotely-located electronics would be desirable for safety and repair access convenience. It was decided that a reasonable compromise would be to put a fast amplifier with 50-Ω input and output impedance and a gain of 10 into a 50-Ω load inside the gas vessel, and to locate the remainder of the electronics remotely.

The basic architecture of the PHENIX RICH front end electronics is shown in Figure 1. The output of the PMT preamp drives both a charge measurement and a timing measurement channel. The outputs of both are captured in an analog memory clocked at the bunch crossing rate (9.4 MHz). The charge outputs of several channels are summed together and flash converted for use in the experiment trigger logic. Information stored in the analog memory is digitized on demand by a multi-channel ADC. The RICH detector characteristics, PHENIX operating modes and this architecture place a number of constraints on the integrating amplifier. It must respond linearly for inputs ranging up to 160 pC (10 photoelectrons x 10^7 x 10), and properly terminate the coaxial line coming from the preamplifier. The noise of the electronics must be sufficiently low (160 fC rms at the input of the integrator) so the uncertainty in the number of photoelectrons measured is due to the statistics of the photomultiplier and not due to the amplifiers, the analog memory or the digitization process. The amplifier must respond and settle in considerably less than one bunch crossing time (approximately 106 ns) as it feeds an analog summing circuit whose output is digitized on every bunch crossing and is an input to the trigger logic for the experiment.

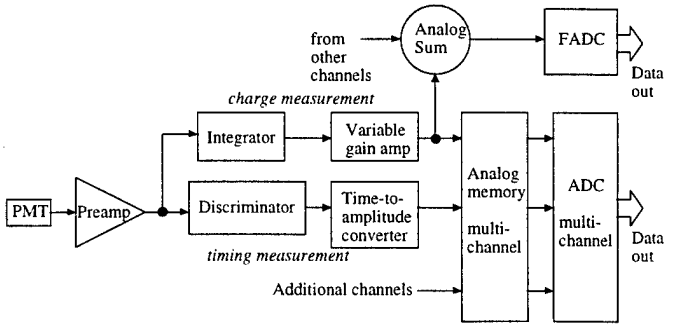

Figure 1: RICH front end electronics block diagram.

The charge integrating amplifier and indeed the overall architecture is much like that used for the WA98 lead glass calorimeter [1], but adapted for the PHENIX RICH detector. As shown in Figure 2, the coaxial cable termination is primarily determined by a fixed resistor, so a good termination is achieved. The voltage developed by the termination provides a good input for the timing channel discriminator, and even though the fraction of charge integrated is small, sufficiently low noise can be achieved even for a calorimeter requiring wide dynamic range [2] and should be more than sufficient for the RICH detector.

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As shown in Figure 2, the charge integrating amplifier is followed by an variable gain amplifier (VGA). This VGA design was based on an earlier design [3], but was revised to have a PMOS input stage to allow operation with a low dc input voltage. The gain of the VGA is programmable over a range of 4 to approximately 12 using a 5-bit digital control, and the risetime (step input) is held to approximately 20 ns using switched compensation. The VGA allows equalizing the gain of different channels due to variations in PMT or preamp characteristics. This equalization (gain and transient response) is needed to allow accurate analog summing for trigger purposes.

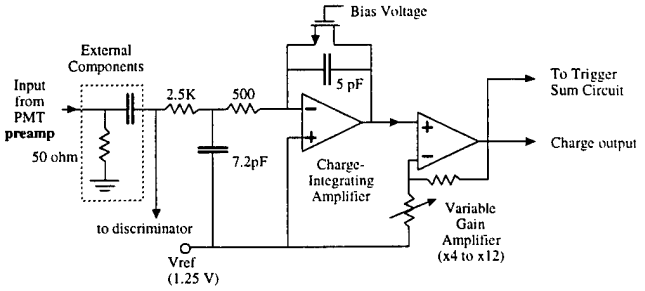

Figure 2: Charge integrating amplifier diagram.

II. Integrator Circuit

The charge integrator design is very similar to that used for the WA98 lead glass calorimeter [1] and to prototypes made for the PHENIX lead scintillator calorimeter [2]. Relative to those designs, the fraction of the charge integrated has been increased by reducing the input resistance. This improves the signal-to-noise ratio by increasing the signal term. The noise has also been lowered primarily by increasing the g_m of the input differential pair of the opamp (Figure 3.) The opamp has a nominal bias current of 140 μA which results in power dissipation of 6.75 mW (at 5 V). It occupies an area of 170 μm by 139 μm and has a positive slew rate greater than 100 V/μs.

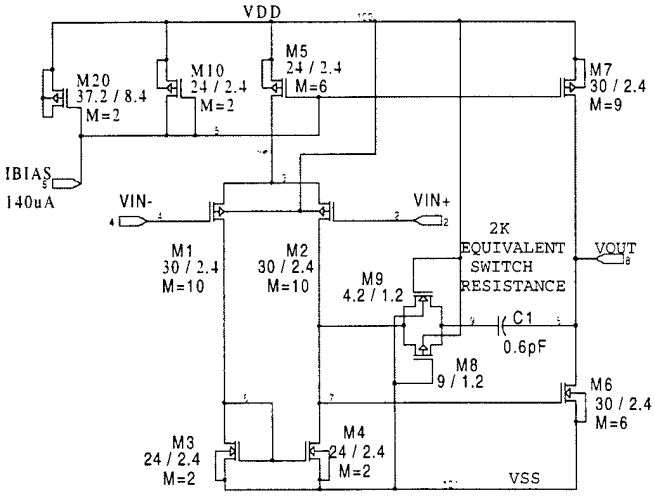

Figure 3: Operational amplifier for the integrator.

The nominal charge gain of the integrating amplifier including the 50-Ω termination (20 mV/pC) was determined from the nominal full-scale charge input (160 pC) and the maximum output dynamic range of the VGA (3.25 V). Based on the choice of a 5-pF integrator feedback capacitor and the nominal VGA gain (6.5), the nominal integrator full-scale charge was 2.5 pC, and the proportion of input charge to be integrated was 0.0156:1. In turn, this determined the input resistance (3kΩ) of the integrator. The maximum input charge allowed is determined by the minimum VGA gain (4) and is 160 pC x 6.5/4=260 pC. This requires the integrator output must be linear up to 0.81 V.

III. Variable Gain Amplifier Circuit

The variable gain amplifier used is essentially a redesign of the VGA designed for the PHENIX electromagnetic calorimeters [3]. A number of modifications to the opamp were made to allow for its use with dc input voltages near ground instead of near the positive supply.

Figure 4 shows the Amp11_rich opamp used in the VGA. Relative to the previous design, PMOS devices have replaced NMOS devices and vice-versa. PMOS input devices are used to allow biasing the input near the negative supply voltage. This is needed for the active-integrator implementation, where the input to the VGA is basically a positive step and biasing that input near the negative supply allows a large output dynamic range. The nominal bias current is 50 μA and the power dissipation is 13 mW (at 5V). The opamp is compact and occupies an area of 151 μm by 189 μm.

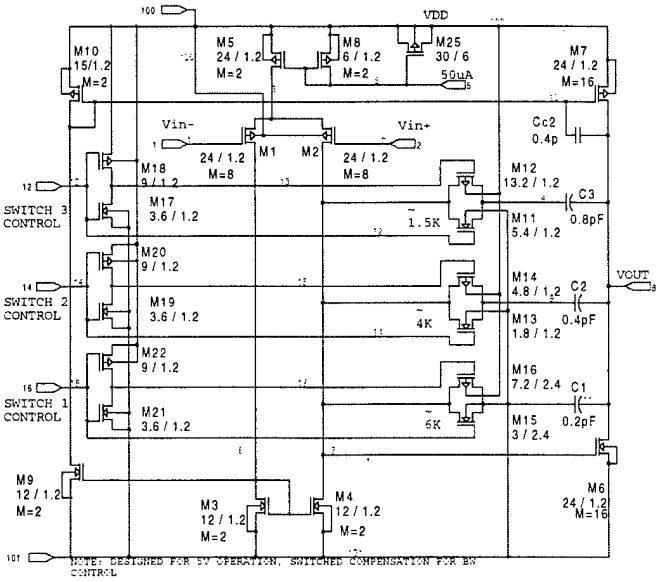

Figure 4: Amp11_rich operational amplifier schematic.

The conversion of the opamp from NMOS to PMOS inputs required changes to the compensation. As before, any combination of three compensation capacitors (0.2, 0.4 and 0.8 pF) may be switched in to compensate the opamp and adjust the gain-bandwidth. An additional compensation capacitor, C_{c2} was added to the gain path involving M3, M9,

M10 and M7. The resistances of switches (M11-M12, M13-M14 and M15-M16) and the capacitances were adjusted to optimize the phase margin of the opamp.

IV. Noise Analysis

The circuit shown in Figure 5 was used to analyze the noise performance of active integrator and VGA stage. To allow algebraic solution of the problem, a number of simplifying assumptions were made. It was assumed that the noise of the variable gain stage would be negligible compared to that of the integrator, that the VGA stage could be modeled as having a single pole role-off, and that the correlator would be noiseless. Also, it was assumed that the $S_n(\omega)$, the equivalent input noise power spectral density of the amplifier used in the integrator stage would be white, i.e., there would be no $1/f$ term. This is not a very realistic assumption, but due to the reduction of low-frequency noise by the double-correlated sampling process, it should have little effect on the results.

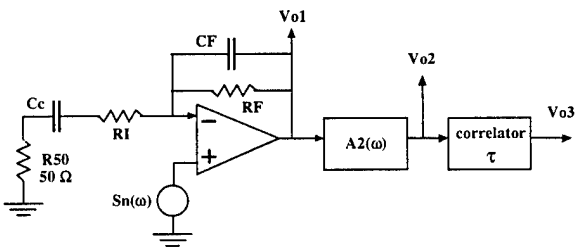

Figure 5: Passive integrator circuit for noise analysis.

Let

$$R_{IN} = R_I + R_{50}, \tag{1}$$

$$\omega_I = 1/(R_{IN}C_I), \tag{2}$$

$$\omega_F = 1/(R_F C_F), \tag{3}$$

$$\omega_0 = 1/(R_F C_c), \tag{4}$$

$$Z_F = R_F \| (1/sC_F), \tag{5}$$

$$Z_I = R_{IN} + (1/sC_I), \tag{6}$$

$$A_2(\omega) = \frac{A_2}{1 + j\omega/\omega_2}, \tag{7}$$

and

$$S_n(\omega) = \overline{e_n^2}. \tag{7}$$

Defining $S_{no2}(\omega)$ as the noise power spectral density at the output of the variable gain amplifier and calculating gives

$$S_{no2}(\omega) = \left[\begin{array}{c} 4kTR_I \left|\frac{Z_F}{Z_I}\right|^2 + \overline{e_n^2}\left|1 + \frac{Z_F}{Z_I}\right|^2 \\ + 4kTR_F \left(\frac{1}{1+\omega^2/\omega_F^2}\right) \end{array} \right] \left(\frac{A_2^2}{1+\frac{\omega^2}{\omega_2^2}} \right). \tag{8}$$

A more useful expression may be obtained if the approximation $1 + Z_F/Z_E \approx Z_F/Z_I$ is used. This is a reasonable approximation for the purpose of calculating the total noise as this gain is much greater than unity except at very low and very high frequencies. The noise gain will be attenuated at high frequencies by the VGA response and at low frequencies by the correlator. Then, assuming that the decay time of the integrator is long compared to the risetime of the VGA ($\omega_F << \omega_2$), Eq. 8 reduces to

$$S_{n02}(\omega) = \left[\frac{\left(4kTR_I + \overline{e_n^2}\right)(\omega^2/\omega_0^2)}{1+\omega^2/\omega_I^2} + 4kTR_F \right] \left(\frac{A_2^2}{1+\frac{\omega^2}{\omega_F^2}} \right), \tag{9}$$

The noise transfer function of a double correlated sampler was given by Buttler [4] as

$$|H_N(\omega)| = |2\alpha \sin(\omega\tau/2)|, \tag{10}$$

and the signal transfer function as

$$|H_S(\omega)| = |\alpha|. \tag{11}$$

For a sampler subtracting the baseline from the signal, $\alpha = 1$, and the time between samples is τ. The output noise power spectral density at the output of the correlator is then given by

$$\begin{aligned} S_{no3}(\omega) &= S_{n02}(\omega)H(\omega)H^*(\omega) \\ &= 2S_{no2}(\omega)(1-\cos(\omega\tau)) \end{aligned} \tag{12}$$

Thus

$$S_{no3}(\omega) = 2\left[\frac{k_3 \frac{\omega^2}{\omega_0^2}}{(1+\frac{\omega^2}{\omega_I^2})(1+\frac{\omega^2}{\omega_F^2})} + \frac{k_4}{1+\frac{\omega^2}{\omega_F^2}} \right](1-\cos\omega\tau), \tag{13}$$

where

$$k_3 = A_2^2\left(4kTR_I + \overline{e_n^2}\right), \tag{14}$$

$$k_4 = A_2^2(4kTR_F) \tag{15}$$

The mean-squared output noise voltage is

$$\overline{e_{no3}^2} = \int_0^\infty S_{no3}(\omega)\,d\omega. \tag{16}$$

Evaluating the integral gives

$$\overline{e_{no3}^2} = k_5\left(1 - \frac{\omega_I e^{-\omega_I\tau} - \omega_F e^{-\omega_F\tau}}{\omega_I - \omega_F}\right) + \pi k_4 \omega_F (1 - e^{-\omega_F\tau}) \tag{17}$$

where

$$k_5 = \frac{\pi k_3 \omega_I^2 \omega_F^2}{\omega_0^2(\omega_I + \omega_F)}. \tag{18}$$

For the values shown in Figure 2, and with a decay time of 3 μs, a correlation time of 300 ns, a 0.22-μF input coupling capacitor, the VGA set for a gain of 8 and an e_n for the integrator opamp of 5 nV/Hz$^{1/2}$, Equation 17 gives a value of 1.8 mVrms. The RICH specifications call for a 1000:1 dynamic range, so for a maximum output of 3.25 V, the rms noise must be less than 3.25 mV. For the nominal charge gain of 20 mV/pC, this corresponds to 160 fC.

V. RESULTS

A prototype device including several opamps, integrators and VGAs was fabricated in 1.2 mm Orbit CMOS and tested. This allowed evaluation of the individual circuit elements as well as the complete signal processing chain. Figure 6 shows the VGA gain as a function of the programming code. The gain varies smoothly from 4 to approximately 11 with no more than a 2.4 percent deviation from a linear fit.

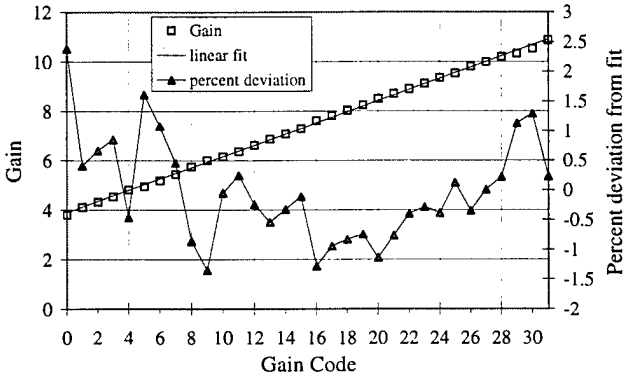

Figure 6: VGA gain as a function of gain code.

For the analog summing circuits that follow the integrating amplifier to complete processing within one bunch crossing time, the risetime must be 20 ns or less. Figure 7 is a plot of the integrating amplifier (integrator and VGA) small-signal risetime for all possible gain and capacitor codes. By the proper choice of the codes, it is possible to keep the risetime between 10 to 21 ns for any gain.

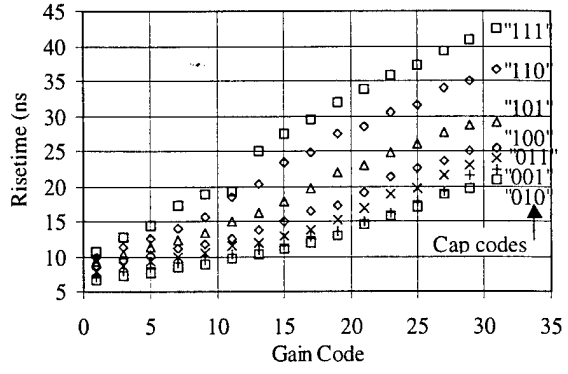

Figure 7: Integrating amplifier risetime as a function of VGA gain and capacitor code.

Figure 8 shows a typical output pulse for the integrating amplifier. As the integrator has a risetime of 9 ns, the overall risetime is dominated by the VGA. There is very little overshoot, and the pulse has settled sufficiently to allow sampling with τ=200ns.

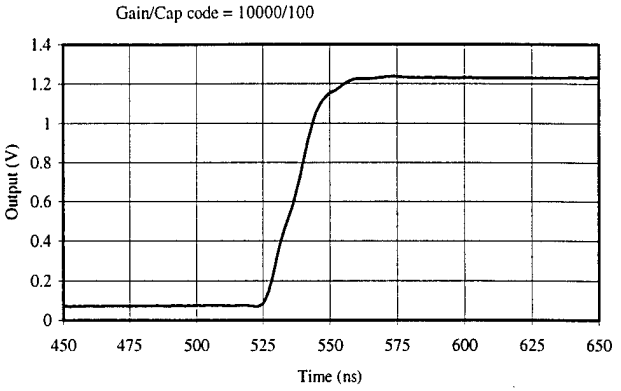

Figure 8: Typical output pulse.

Figure 9 is a plot of the integrating amplifier output as a function of the input charge. In this case the VGA was programmed for a gain of 4. The integral nonlinearity (INL) was +/-1%, which is sufficient for the RICH detector.

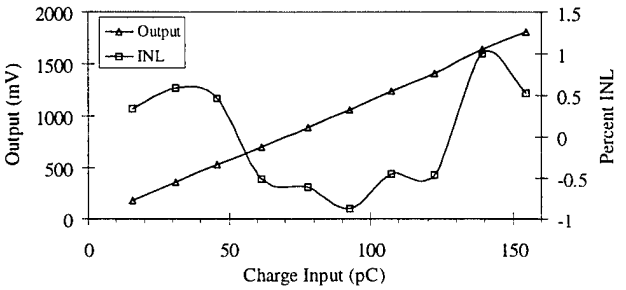

Figure 9: Integrating amplifier linearity.

The output noise of the integrating amplifier was measured using an HP 3589A spectrum analyzer, and the wideband rms noise was computed by numerically integrating the spectrum up to 50 MHz. The test fixture noise floor was approximately 0.25 mV rms, which is sufficiently low to allow measuring noise levels of a few mV rms. The amplifier was set for a typical case with a VGA gain of 8 (gain code 10000), overall risetime approximately 20 ns (capacitor code 100), and a decay time of 3 μs. In PHENIX, the output from the integrating amplifier will be sampled and double-correlated, so this effect was achieved by multiplying the spectrum by the frequency response of the correlator and numerically integrating the result to obtain the noise level that would be expected after correlation. The power spectral density of the output noise both before and after correlation is shown in Figure 10, and the rms values are given in Table 1. A correlation time of 300 ns was used in all cases.

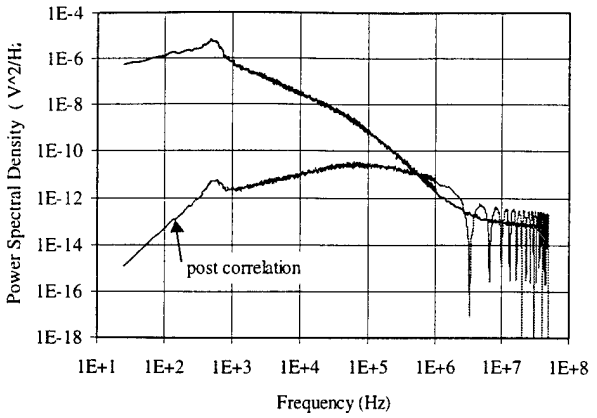

Figure 10: Power spectral density of output noise.

Table 1
Integrating amplifier output noise.

Method	Noise before correlation (mVrms)	Noise after correlation (mVrms)
Spectrum analyzer	63	5.0
Digital scope	58	4.3
SPICE	6.9	1.8
MathCAD	5.1	1.7
Equation 17	Does not apply	1.8

The output noise measurements made using the spectrum analyzer were compared to SPICE simulations of the circuit, calculations using Eq. 17, and data taken using a digital oscilloscope. These results are also given in Table 1. The digital scope was used to take pairs of samples that were used to calculate the rms noise after correlation. There was good agreement between the digital scope and the spectrum analyzer methods. MathCAD software was used to evaluate the model presented in Figure 5 without the simplifications needed for the algebraic solution (Eq. 17). Good agreement between SPICE, MathCAD and Eq. 17 was obtained.

The measured noise after correlation was approximately 2.8 times that predicted by calculations and approximately 50% more than desired. There are several possible explanations for this discrepancy. The modeling of 1/f noise is not included in the Figure 5 model and the transistor model used by SPICE may not accurately represent the 1/f noise of the circuit. This would artificially lower the calculated noise. Another possibility is additional noise due to the voltage references on the test fixture. The gain from the reference input of the integrator to the output is quite high over a wide range of frequencies. The peak in the noise spectrum just below 1kHz may be indicative of such a problem. Extremely low noise voltage references are needed for single supply operation. Additional possibilities for the discrepancy in the noise level include noise pickup on the test fixture or interference from other test circuits constructed on the same IC.

VI. Ongoing Work

Optimization of the integrating amplifier circuit is continuing. As there is a tradeoff between decay time and the noise performance, this issue will be explored in terms of detector performance and ease of data reduction. A long decay time is reduces or eliminates the need to correct for the exponential decay of the signal, but results in increased noise.

The amplifier layout is being modified slightly to allow arraying on a multi-channel IC and to allow the addition of a shift register to control the VGA gain and bandwidth. Each channel will contain an integrating amplifier, a discriminator and a time-to-amplitude converter. The IC will also contain the analog summing portion of the trigger circuit.

VII. Conclusions

The integrating amplifier prototypes designed for the PHENIX RICH detector have exhibited the range of adjustability in gain and bandwidth needed. The charge gain (20 mV/pC) is correct and the output dynamic range of the amplifier is sufficient. The measured output noise levels are slightly high, however, adjustments to the decay time and coupling capacitor value or improvements to the circuit wiring and implementation will likely reduce the noise to the needed level.

VII. References

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