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A SILICON MICROBENCH CONCEPT FOR OPTOELECTRONIC PACKAGING

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ABSTRACT

Optoelectronics (o/e) is currently too expensive for widespread application. The packaging (or fiber pigtailing) of o/e components may comprise up to 90% of the component's cost for some high performance components, and usually at least 50%. The development of an automated packaging system can greatly lower these packaging costs, enabling a host of new applications in areas of great economic and defense benefit to the US, including optical computer interconnects for advanced computing and ATM switch backplanes, advanced optical networks, and fiber optic gyros, to name just a few potentially high-impact applications.

We believe that the pigtailing process must be automated to realize a significant reduction in the cost of o/e packages. We are addressing issues of automating the fiber pigtailing process on silicon waferboards or microbenches. This paper focuses on reflowing solders for the attachment of o/e components. We have recently developed miniature polysilicon heaters which are integrated on silicon microbenches. These miniature heaters avoid the problem of raising the entire microbench to the solder melting point to attach components. Most importantly, these miniature heaters are completely compatible with automating the attachment process.

Designing silicon microbenches with on-board heaters requires some care. The thermal properties of the microbench itself along with all coatings on the surface and any heatsinking materials must be understood. The heaters must operate in a current and voltage regime compatible with the overall characteristics of the o/e package. Inadvertently reflowing solder in unanticipated locations may occur unless the thermal behavior of the microbench is thoroughly known. This paper describes the design and fabrication of our microbenches and an experimental and theoretical study we have performed on these silicon microbenches which gives us a complete picture of their thermal behavior.

KEY WORDS: silicon optoelectronic microbench packaging laser diode soldering reflow

INTRODUCTION

The fundamental reason for the high cost of optoelectronic packaging can be traced to the sub-micron positional tolerances that are usually required for the packaging (or fiber optic pigtailing) of high-performance optoelectronic components. For example figure 1 shows the measured amplitude loss as a conically tapered single mode fiber is scanned through the center of the beam profile of a typical single mode laser diode operating at 800 nm. From this figure we see that less than 1 µm of tolerance exists to get maximum coupling to the single mode fiber. More careful measurements indicate that alignment tolerances approaching 0.2 µm are needed to maximize the coupling. Manually achieving such precision is extremely labor intensive and expensive. We will briefly discuss below two approaches that we are pursuing at Lawrence Livermore National Laboratory that can help to minimize these costs. The first is an automated fiber alignment and attachment system, and the second is the silicon microbench.

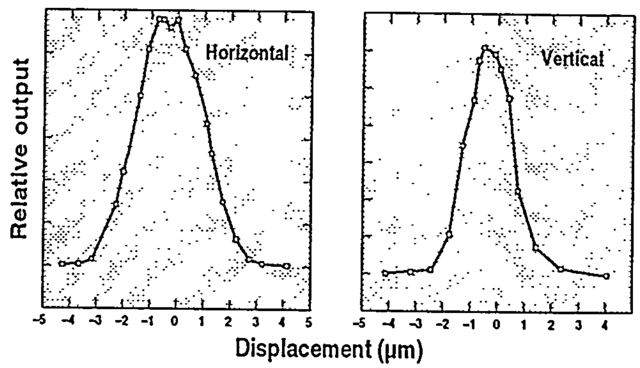

Figure 1. Relative output power vs position of a conically polished fiber scanned across the output of a single mode laser diode.

AUTOMATED OPTOELECTRONIC PACKAGING

Automation of the precision positioning may help reduce the costs of optoelectronic components. In an attempt to quantitatively analyze what might be a tolerable cost of such an automated positioning machine and what an economically sensible market volume might be, we have developed a simple model that relates the cost per pigtail to the volume of components that are packaged.

In our model, the per pigtail cost is given by

$$C = (C_{op}\,(r/R) + C_{eq})/r + C_{mat}$$

where C_{eq} is the cost per unit time of the machine (we assume that it has a 5 year lifetime), C_{mat} is the material costs for each packaged device, C_{op} is the cost per unit time of the person operating the machine, r is the market demanded production rate, and R = machine limited rate of production. These equations are plotted in figure 2 for various values of the parameters. Note that as the speed of the machine goes up (time per pigtail decreases) high volume packaging becomes very inexpensive, as one might expect.

It is further interesting to note that as the machine cost goes down, money is saved by automating at lower volumes. Thus a low-cost machine will provide the economic drive for automation at surprisingly small market volumes.

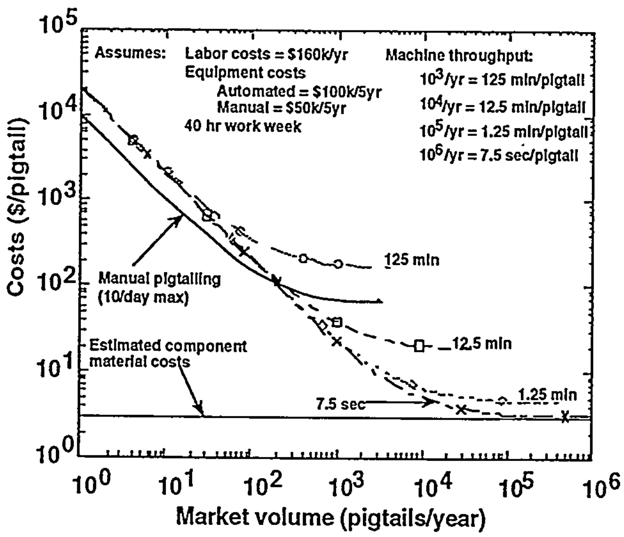

Figure 2. Results of packaging cost model.

As can be seen in figure 2, o/e packaging using this automated machine is expected to be cheaper than manual packaging at pigtail volumes just over 100 per year. This volume would appear to be well within the present market reach of most o/e manufacturers including small companies Note that as the time per pigtail decreases, the cost decreases greatly at high volumes.

Our approach to automation, an Automated Fiber Pigtailing Machine (AFPM), is described in a companion paper [1]. In the following discussion, we concentrate on a silicon microbench technology that is compatible with automated parts placement and pigtailing.

SILICON MICROBENCHES WITH MANUFACTURABLE SOLDER REFLOW

There is a large body of literature on the exploitation of the etching properties of Si to produce v-grooves mesas, and positional stops on silicon substrates to "passively" align optical components. Much work has also been done exploring the use of "solder bumps" to precisely position components in a passive sense. In the interests of space, we make no attempt to review that large body of work, rather we briefly describe what we believe to be an interesting adjunct to these two important packaging technologies.

Nearly ten years ago, miniature metallic heaters to reflow solder for the attachment of o/e components on ceramic waferboards were developed[2]. Since then many variations of this concept have been tried. We have developed silicon microbenches with integrated polysilicon heaters to improve the manufacturability of soldered silicon o/e packages[3].

Our initial work involved the development of silicon microbenches to pigtail high-powered 800 nm laser diodes to single-mode fibers. The success of the prototype has led us to develop several new designs. For example, the microbench shown in figure 3 is for packaging a 1550 nm DFB laser.

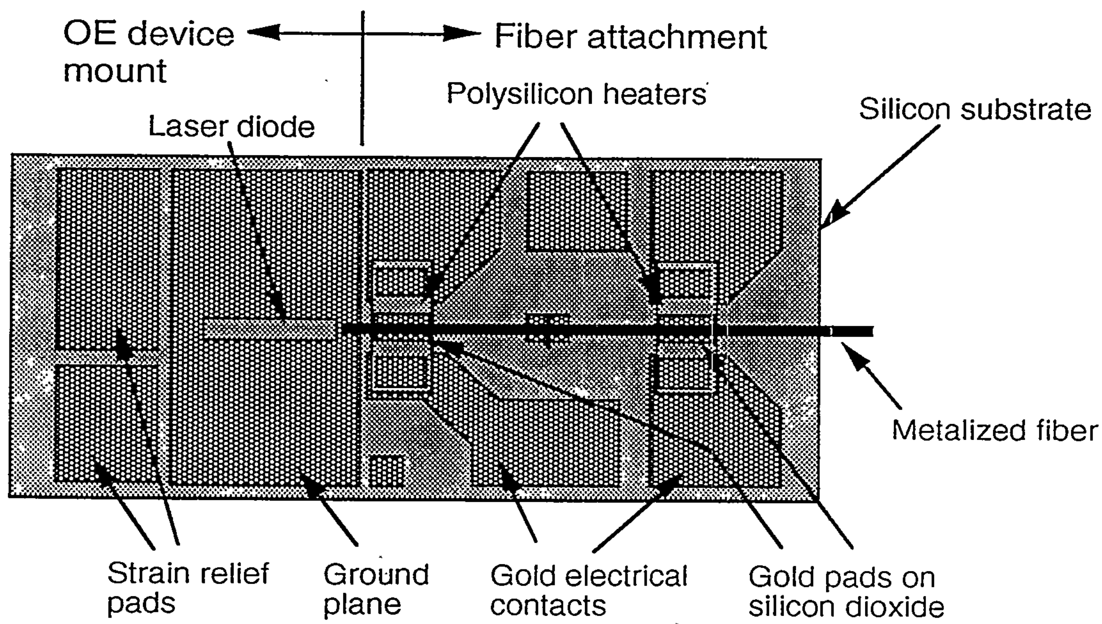

Figure 3. Silicon microbench with built-in polysilicon heaters for manufacturable solder reflow.

On the left side of the microbench, we photolithographically pattern gold pads to provide a ground plane for the laser and strain relief for the wire bonds. To attach the fiber on the other side of the microbench, we build two heating elements of polysilicon which are attached to gold bonding pads for electrical contact. In the center of each heater, we pattern a gold pad on a layer of silicon dioxide. This gold pad provides the solder attachment base while the silicon dioxide electrically isolates the gold pad from the polysilicon heater. The gold pads are 1 mm by 0.5 mm each and are sufficiently large to solder up to a 250 micron diameter fiber at the two attachment pads. Presently, we use either 100-micron diameter solder balls or solder paste to attach the metallized fiber.

Construction of our silicon microbenches begins with single-crystal silicon wafers as a substrate. We use a standard silicon wafer thickness of 400-500μm. Wells and pedestals are etched into the silicon as needed to approximately align, in the vertical direction, the optical axis of the various components to be mounted. Next a thick layer of silicon dioxide (SiO_2) is deposited and etched to provide some degree of thermal isolation of other areas from the heaters. The thermal resistance of SiO_2 is approximately two orders of magnitude greater than that of silicon so a 5μm thick layer of SiO_2 is thermally equivalent to a 500μm thick layer of silicon. With plasma-assisted Chemical Vapor Deposition, it is possible to deposit layers of SiO_2 up to 20-30μm thick. We generally use a thickness of 5-10μm depending on the needs of each application.

The heaters are made by depositing, doping, and patterning an approximately 1μm thick layer of polycrystalline silicon (polysilicon). The doping is adjusted to result in a resistance of the heaters of approximately 10-50Ω. Resistors in this range give the greatest control at the temperatures of interest with standard laboratory power supplies. A thin silicon dioxide layer on top of the polysilicon provides electrical isolation of the solder attachment pads to prevent shorting out of heaters. This step is not always necessary. Because of the excellent thermal conduction of silicon, it is often acceptable to allow current to flow through the solder attachment pads as long as there is an adjacent region of non-metallized polysilicon that can act as a heater.

A final metal layer of a standard Cr/Au or Ti/Au metallization completes the interconnect structure to provide electrical connections to the heaters and a layer of metal that is strongly adherent to both silicon and SiO_2 and to which most standard solders will adhere.

The performance of the polysilicon heaters on our prototype is very reproducible with a specially constructed power supply that allows us to accurately control the magnitude and time of the applied current. Fiber positioning is done by active alignment to sub-micrometer tolerances. We typically apply one amp of current for approximately 0.5 sec to reflow solder at the fiber attachment points. We observe no decrease in the light coupled from an 800 nm laser diode into a single-mode fiber before and after the solder reflow and cooling, and have achieved up to 65% optical coupling with conically machined fiber end-facets.

Our microbench geometry with on-board heaters also allows rapid attachment of the other components to be placed on the microbench. Applying larger currents for longer periods of time allows solder reflow at some distance from the heaters. Using solders with different melting temperatures and judiciously choosing the order of attachment allows a variety of components to be soldered to the microbench without movement of previously attached components.

Generally, components furthest from a heater are attached first using a high current through the heater. We can manually place and solder a thermoelectric cooler, a thermistor, and a laser diode onto our microbench at different distances from the heaters in less than 15 minutes. We envision that the placement and soldering of these components, which does not require sub-micron alignment, could be performed by an automated system in less than a minute. As the last step, the fiber must be aligned to sub-micron tolerances and is attached using the least current through the heaters.

These microbenches are fabricated using standard silicon microelectronics processing technology. Several hundred parts can be fabricated simultaneously on a single silicon wafer. For simple designs that do not require a well or pedestal etched in the wafer, or insulated attachment pads, we can fabricate a batch of microbenches using a single photolithographic mask. In that case the cost per part can be much less than $0.50.

We also use a standard silicon etching technique employing a potassium hydroxide (KOH) solution to etch wells (& pedestals) in the silicon substrate that can be as deep as 200 μm with a tolerance of less than ± 5 μm. This etch technique is compatible with v-groove formation used by others to precisely place fibers on microbenches, and allow precise vertical alignment of the optical axes of components mounted on the microbench.

The idea of on-board heaters lends itself to applications other than packaging laser diodes. We have designed a longer microbench with heaters at each end to pigtail both ends of a semiconductor optical amplifier. We are also investigating geometries compatible with high speed applications in which on-board transmission lines will be needed to provide sufficient bandwidth for the o/e device.

THERMAL STUDY OF MICROBENCHES

Designing silicon microbenches with on-board heaters requires some care. The thermal properties of the microbench itself along with all coatings on the surface and any heatsinking materials must be understood. The heaters must operate in a current and voltage regime compatible with the overall characteristics of the o/e package. Inadvertently reflowing solder in unanticipated locations may occur unless the thermal behavior of the microbench is thoroughly known. This section describes an experimental and theoretical study we have performed on these silicon microbenches which gives us a complete picture of their thermal behavior. We have two goals. First, we want to understand the temperature distribution on our existing microbench designs. Secondly we want to develop a computational tool to model the thermal behavior and help us to design future microbenches.

Thermal Modeling and Simulation

A mechanical finite-element modeling code called COSMOS/M[4] was used to develop a predictive model of the temperature response of the silicon microbench to various heating pulses. Full three dimensional simulation is needed to account for all the heat flow in the structure, however we found that we could simplify the model by approximating the three dimensional physical structure as a two dimensional axisymmetric problem. This was justified because the microbench is thin compared to its overall width and length dimensions. Heat penetrates quickly through the thin wafer and then spreads radially outward.

Our strategy here was to compare the model to measured results at two extremes of heatsinking. First, heat sinking only around the edge of the microbench simulates minimum cooling where just natural convection of air provides the cooling. Second, heat sinking under the entire microbench provides much larger thermal losses and simulates the attachment of the microbench to a real package. For comparison with our experiments, we modeled different types of heatsink materials including glass, brass, and a thermoelectric cooler. We did not permanently solder the microbenches to the heatsinks, so that the benches and the heatsinks could be reused. The microbenches were attached to the heat sinks by a thin layer of silicone grease (heatsink compound).

Because the edge boundaries of the microbench are relatively far from the heat source we can use a circular heat source in the model to approximate the actual rectangular heat source. This gives accurate central temperatures, relative edge temperatures at the source boundary, and accurate temperatures far from the source except near the very edges of the microbench. Local temperature prediction at the heater determines the melt or remelt of the solder, while temperatures far from the heater determine the fate of the other solder junctions on the microbench.

The thermal model developed for the microbench assumes axial symmetry and is a plane section cut radially from a cylindrical piece of silicon. A sketch of the axisymmetric model is shown in figure 4. The height of the rectangular plane is equal to the thickness of the silicon (450 μm) plus a 25 μm height that approximates the 5 μm or thicker insulation layer of silicon dioxide. The insulation layer was purposely made thicker so that fewer nodes would be required in the simulation. The material properties of the insulation were adjusted to match the thermal properties of the 5 μm silicon dioxide layer. Since it is simply being used for its thermal properties here the thickness of the insulator can be simulated just by scaling its thermal material properties.

Natural convection heat transfer removes some heat from the surface of the microbench but the majority of the heat is removed through contact resistance with heat sinks located near the bottom edges of the microbench or under the entire microbench.

The contact resistance between the microbench and a heat sink is a large thermal barrier to heat flow. This resistance is difficult to predict accurately because of uncertainties in the gap height between contacting parts. The contact conductance for the edge cooled model was estimated by knowing that the microbench was supported near each end by a block of alumina. In this case air thermal conductivity (k_a) and the gap (δ) between the microbench and the alumina determined the thermal contact conductance which is k_a/δ. We calculate a thermal conductance in this case of approximately 7×10^{-5} W/mm^2 -°C.

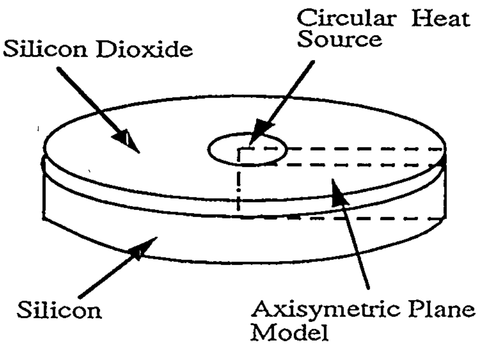

Figure 4. Thermal model of the silicon microbench showing the cylindrical approximation to the physical model and the planar section used in the simulation. Heat is removed by natural convection from the top surface and by a heat sink located under the microbench.

When the microbench is resting on a continuous heat sink making contact over its entire bottom surface, silicone grease is used to improve the thermal contact. The thermal conductance for this case is determined by the gap and heat sink thickness along with the thermal conductivity of the silicone grease and the heat sink. The thermal conductance used for a 0.25 mm thick layer of silicone grease and a 6.0 mm thick brass heat sink is approximately 1.5×10^{-3} W/mm^2 -°C. While these estimates give us a starting point, it is most expeditious to let the contact resistance be a variable to be calibrated by comparison to experimental results.

We are running COSMOS/M on a Macintosh II with a 16 MHz 68030 processor and a math co-processor. On this somewhat primitive platform we can perform steady state simulations in less than 10 minutes and transient simulations in less than 30 minutes.

Experimental Setup

The experimental data was gathered using a flexible IEEE-488 bus controlled measurement system. Measurements were taken of temperature vs. time with a variety of applied electrical power pulses and at several locations on the microbench. For transient measurements shorter than one second we found that it was necessary to attach miniature chip thermistors to the microbench. The thermal response time of even the smallest thermocouple we had available was too long (several seconds). Thermistors, however, are restricted to a temperature range below 150°C. So, for short pulses our experimental data is restricted to that range. We can extrapolate the experimental data to higher temperatures with the computer simulations. Three chip thermistors were mounted on each microbench tested: one on top of the central heater, the next approximately 2mm away on the diode mounting pad, and the third on one of the strain relief pads about 5mm from the heater.

Experimental Results

Figure 5 shows a plot of steady state temperature vs. electrical power applied to the heater for several different cooling coefficients in units of W/mm^2-°C. The experimental data allows determination of the effective cooling coefficients which contain the unknown contact resistance variable. From such plots we can calibrate the model for a particular cooling mechanism. Using this model, we can make this kind of plot for any location on the microbench.

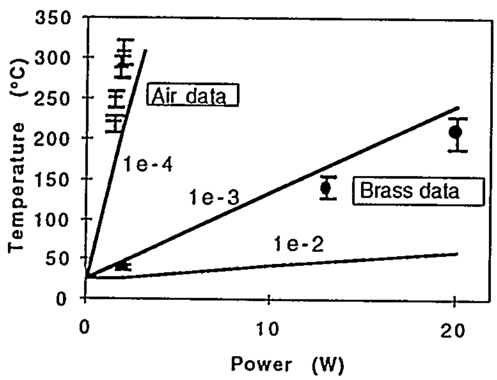

Figure 5. Simulated and experimental plot of steady state temperature with various values of cooling coefficients to represent heatsinking.

We can compare experimental results using the computer controlled measurement system described above to calculated temperature vs time at any radial distance on the microbenches. Such a comparison is illustrated in figure 6. Here the temperature vs. time profile is plotted for the three thermistors mounted on a microbench as solid lines. The calculated temperature vs. time for the equivalent radial distances are plotted as dots. We note that here the calculations are slightly higher than the experimental data. From plots like these we can calibrate the cooling coefficient for a given heatsink and thermal contact arrangement allowing us to know very accurately how the microbench temperature will behave for a given current pulse width.

By making a series of these plots for different heatsinks and different mounting configurations, we can fully characterize the thermal behavior of our microbenches. We can, for example, minimize the heatsinking and use long applied electrical pulses to obtain uniform distribution of heat to melt solder over a large area of the bench. On the other hand, if we use a good heatsink with low contact resistance and short current pulses, we obtain very localized heating just over the heater area to prevent the reflow of solders in other locations while attaching components directly over the heaters.

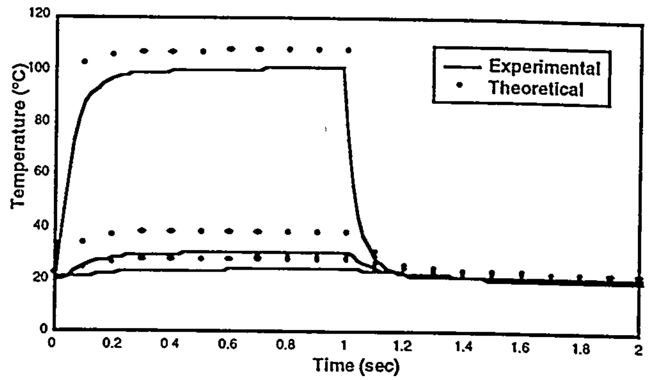

Figure 6. Typical transient measurement of temperature at three locations on the Microbench using thermistors for a 1.0 sec current pulse.

Figure 7 shows the decrease in temperature with distance away from a heater for different electrical pulse lengths. This information allows one to determine how far apart to design the attachment points of components which must be soldered sequentially in time. One wants to maintain the first component at a temperature lower than the melting point of the solder while attaching subsequent components..

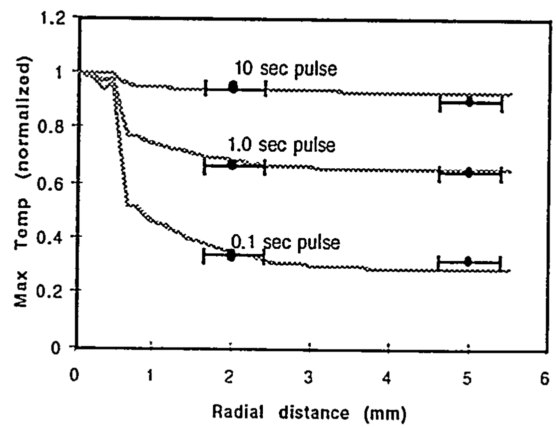

Figure 7. Typical plot of normalized temperature vs. radial position for various lengths of electrical pulses applied to the heater

As one would expect, a short pulse results in a larger decrease in temperature with distance because the heat is initially concentrated only at the heater. Note that the error bars for the experimental data on this plot are horizontal because the size of the thermistors (approximately 0.8 mm square) results in a measured value which is an average over some distance. Again, similar plots can be made for different heatsinking schemes to fully characterize the microbenches

CONCLUSION

High-precision packaging of optoelectronic o/e components is a labor-intensive and expensive process. We believe that the pigtailing process must be automated to realize a significant reduction in the cost of o/e packages. We are addressing issues of automating the fiber pigtailing process on silicon waferboards or microbenches. We have recently developed miniature polysilicon heaters which are compatible with silicon microbenches. These miniature heaters avoid the problem of raising the entire microbench to the solder melting point to attach components

At present, we have applied our silicon microbench designs with on-board heaters to only laser diode packages. We are presently designing microbenches for other devices such as semiconductor optical amplifiers. We continue to investigate simpler processing geometries, short-term stability, long-term drifts, and improved compatibility with automated alignment techniques.

An experimental and theoretical study has been conducted of the thermal behavior of silicon microbenches with on-board heaters for solder reflow. The combination of selected experimental measurements with finite element simulation of the thermal behavior of the structure allows us to gain a good understanding of temperature distributions on the microbench under various conditions of power applied to heaters and for different heatsinks. The result is an accurate predictive model of the silicon microbench.

We have described some of our on-going efforts at Lawrence Livermore National Laboratory to reduce the costs of optoelectronic packaging. Our silicon microbench designs with on-board heaters are compatible with automated alignment techniques. Our efforts in machine vision and automated alignment are reported in the next paper at this conference. We will also be exploring the compatibility of our automated packaging with passive alignment techniques.

ACKNOWLEDGMENTS

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[3] A recent patent describes a similar device - Blonder & MacDonald, “Article that comprises a laser coupled to an optical fiber,” U.S. Patent #5,307,434

[4] Available from Structural Research Analysis Corp., 1661 Lincoln Blvd., Suite 200, Santa Monica, CA 90404, Phone: (310) 452-2158