High-Frequency Voltage-Controlled-Oscillator for Use With Inverted-Mesa Quartz Resonators*

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Abstract

An oscillator circuit has been developed at Sandia National Laboratories that uses Inverted-Mesa resonators, in a high-precision VCO application, at frequencies historically dominated by SAW designs. This design incorporates a frequency tripler that provides a 600 MHz output capability using a 200 MHz 3rd overtone resonator. This design has some advantages over equivalent SAW alternatives: lower power-consumption, superior aging characteristics, linear frequency pulling and low frequency versus temperature sensitivity. The VCO presented demonstrates > +/- 60 ppm pullability (0 to 7V control), tuning linearity better than +/- 5% with phase noise at 1 kHz < -110 dBc/Hz. This oscillator-tripler exploits the nonlinear characteristics of an emitter-coupled-pair differential amplifier to obtain a high-performance oscillator design.

Introduction

By using inverted-mesa techniques to selectively thin the resonator, the practical-use frequency of AT-cut resonators has risen dramatically over the past several years. Resonator frequencies to approximately 200 MHz in either fundamental or overtone modes are available and are of very high quality. Resonators operating at frequencies greater than 400 MHz have been made by some manufacturers but they are usually not very consistent in quality and are not ideal for high-precision applications. The author believes that if bulk-wave devices at high-frequencies had a "generic" oscillator design that was adaptable to various oscillator needs then the inverted-mesa resonators would be a more attractive option for high-frequency (>100 MHz) applications. The SAW two-port "design world" has a significant advantage at high frequencies in that the basic oscillator configuration is relatively standard and is piecewise more charaterizeable due to the fact that it is based on a 50Ω characteristic impedance measuring system. This is not to say that SAW oscillator design is easy, it's just more standardized than bulk-wave (negative resistance) oscillators. Bulk-wave oscillator designs vary greatly with desired frequency and performance attributes. This paper will describe a high-frequency VCO with very good performance characteristics and more importantly offers a design topology by which high-frequency oscillators may be designed. This oscillator topology is versatile and readily designed for a wide range of frequencies and applications.

Design Goals

A 585 MHz VCO was designed for a satellite application. This application required the following basic specifications for the oscillator:

Power Supply	7 Volts
Input Current	<10 mA
Output Power	- 5 dBm
Phase Noise	< -100 dBc/Hz
Pullability	> 60 ppm
Aging	< 15 ppm in 15 years
Temperature	-40°C to 75°C

The output harmonic design goals were flexible in that the system could provide additional filtering of the output waveform. These design goals may have been met using SAW oscillator technology but due to

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some economic and technical advantages the following design was developed.

Emitter-Coupled Pair Oscillators

The building block for the oscillator is an emitter-coupled pair differential amplifier. This amplifier is superior because of the symmetrical transfer function and the ability to function at large signal amplitudes without serious phase degradation due to saturation and bias shift.

Emitter - Coupled Pair
Differential Amplifier
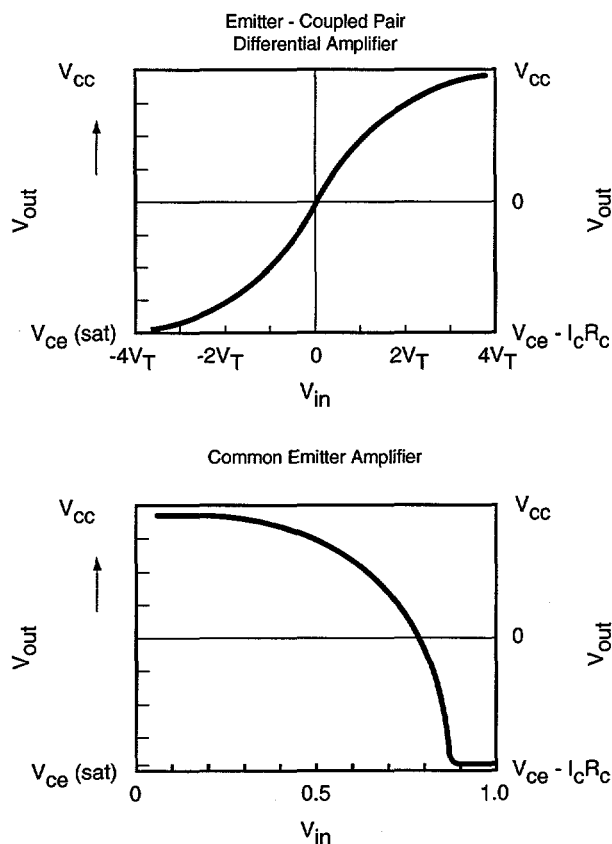
Common Emitter Amplifier

Figure 1. Transfer Function Comparison

Figure 1. demonstrates graphically the difference between an emitter coupled pair and a single transistor common emitter transfer functions. The emitter coupled pair has a broad linear region of operation and smoothly and symmetrically limits while the common emitter transfer function is grossly nonlinear and nonsymmetric. The emitter coupled pair can easily be designed to keep the transistors out of the saturation region. It can be relatively difficult to keep a single transistor design from limiting in

the saturation region. When a transistor is in saturation the effective transistor collector to emitter impedance decreases dramatically, the transistor β goes to zero and the base-collector-emitter become one ac node. These nonlinearities severely degrade phase-noise, and load and power supply pulling.

The cut-off region does much less degradation to oscillator performance due to the high transistor impedances generated which are usually swamped out by external imedances of the oscillator circuit. In most oscillators signal levels greatly exceed small-signal levels and only when automatic level control (ALC) is employed can a single transistor circuit design be kept in a relatively linear region of operation.

Emitter-coupled pair oscillators have been presented by Benjaminson[1] where he presents techniques for using a differential amplifier in combination with a balanced bridge to provide a high degree of $d\phi/df$ (phase slope) near circuit resonance for very high frequency stability and therefore low-phase-noise.

Wessendorf[2] has described techniques for using emitter-coupled pair designs to realize oscillators for use with resonators in fluid sensing applications. In these applications the resonator loss becomes large and most common oscillator designs will not operate.

Negative-Resistance Model

A simplified version of the differential oscillator used for this design is shown in Figure 2. It contains no bias circuitry or frequency selecting components other than the resonator Y_1 . In this design R_f, R_C , h and r_e set the negative resistance of the oscillator. For most practical circuit values R_e can be considered an open and is only used to set the bias. The transistor parameter h is 1/gm of the transistor and is set by the bias current. The bulk emitter resistance r_e is relatively small (3 Ω) but is required for accurate modeling, especially at high currents.

R_f , R_C, h and r_e establish the magnitude of the negative resistance seen at the resonator port, the base of Q_2, Figure 3.
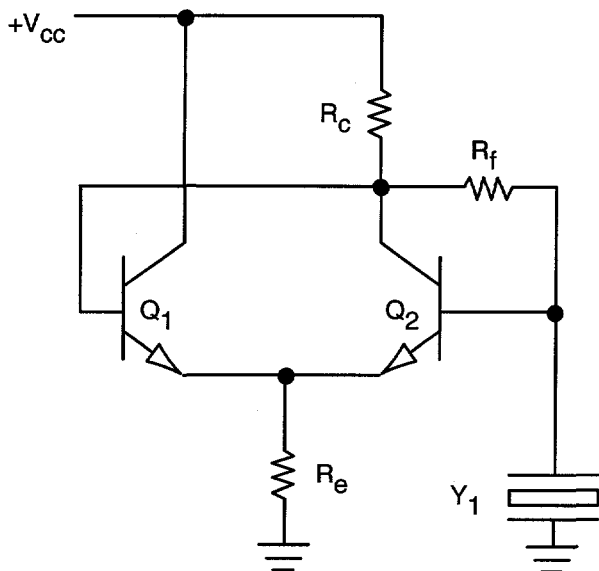
Figure 2. Differential-Amplifier Oscillator

R_{in} is determined by the following equations:

$$h = h_1 = h_2 = \frac{kT/q}{(1/2)\, I_e} \sim \frac{26mV}{(1/2)\, I_e} \text{ (at 25°C)} \quad (1)$$

$$R_{in} \sim R_f + R_c - \frac{R_f\, R_c}{2(h + r_e)} \quad (2)$$

This oscillator is a series resonant design in that the oscillator loop phase is 0° when the resonator is a real impedance. This condition is true near series resonance of the resonator.
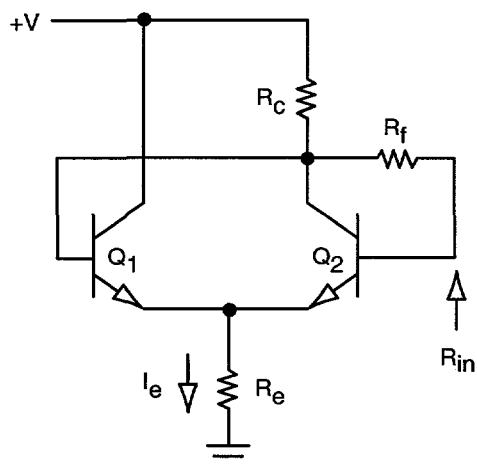

Figure 3. Oscillator Negative Resistance Model

Another way to look at the circuit is to break the loop at the base of Q_1 and look at the gain from the base of Q_1 to the collector of Q_2 with the resonator in the circuit and feedback resistor R_f connected from the collector to the base of Q_2. The gain function is controlled by the resonator only when there is significant feedback provided by R_f. If R_f is not in the circuit then the resonator impedance is divided by the transistor β and therefore is of little or no consequence in the loop[2]. R_f can be made relatively small to provide significant negative feedback for a very stable oscillator.

The larger $-R_{in}$ is (made relative to the resonator loss) the larger the amplitude of oscillation and the harmonics generated. The amplitude of oscillation will increase until the effective h of the transistor has increased and or output limiting has effectively driven $-R_{in}$ down to the magnitude of the resonator loss (R_m). Again, the differential amplifier transfer function provides the most ideal limiting function one can use in a self limiting design. One can also control the amplitude of oscillation by replacing R_e with voltage controlled current source.

The differential amplifier oscillator configuration can be realized at very high-frequencies because the circuit is non-inverting and the collector of Q_1 is ac grounded. This eliminates any Miller effect at the base of Q_1. Miller impedance at the base of Q_1 will adversely load the collector of Q_2 and significantly limit the frequency response and oscillator performance. The output of the oscillator will be taken from the collector of Q_2 but in a well controlled manner.

Another characteristic of the emitter-coupled pair design is that when driven to non-linearity a pseudo square-wave is generated. Since a square wave is made up of odd-harmonics so is the harmonic content of an over-driven emitter coupled pair. This attribute is exploited to more efficiently generate a tripled, or even a quintupled output frequency relative to the primary oscillation frequency. Overdriven single transistor designs generate all harmonics but produce the larger amplitudes on the even harmonics.

An example of a practical oscillator using the emitter coupled pair with negative feedback is shown in Figure 4.
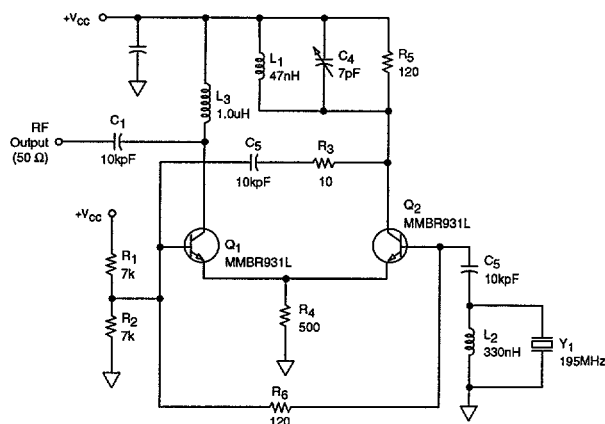

Figure 4. High-Frequency Differential Oscillator

This design uses R_6 as both a dc bias resistor and negative feedback, as in R_f from Figure 3. R_5 is the same as R_c in Figure 3. This design uses the tank circuit L_1 in parallel with C_4 chosen to be resonant at the desired crystal (Y_1) frequency. This tank provides two required functions: first, it allows the removal of undesired capacitance from the collector of Q_2 to ground allowing high frequency operation, secondly it helps to constrain the potential oscillation of the circuit to the resonator frequency (f_s) and reject undesirable L-C oscillations or undesired crystal modes.

The undesirable L-C oscillation frequencies will typically occur when high gain (low h) conditions exist or when the capacitance (C_0) or resistance (R_m) of the resonator are relatively large. The undesirable modes (typically relatively close to the desired mode of operation) can be suppressed and or eliminated by increasing the Q of the collector tank at Q_2 (by increasing C_4 and decreasing L_1, or increasing R_5) and adjusting L_2 to tune out the resonator shunt capacitance (C_0) at the desired frequency. If this oscillator is designed at relatively low frequency and at a fundamental resonator mode L_2 is not required.

The oscillator in Figure 4. was designed for 195 MHz operation with a 3rd overtone resonator. To determine the validity of equation (2) the circuit was measured to determine the values of R_c, R_f, r_e, and h at two operating points. R_c was effectively 90 Ω

(due to loss of the tank circuit in parallel with R_5), R_f was set equal to 120 Ω, r_e was assumed to be 3 Ω and the resonator loss measured (R_m) 35 Ω.

Figure 5. is a graph of the calculation, equation (2), of R_{in} versus transistor h. This graph should predict the point at which oscillation will start for a given resonator impedance. The calculation predicts that for the 35Ω resonator a transistor h of at most 19Ω would be required to start oscillation, and that an h of at most 22.5Ω would be required if the resonator had an R_m of 0 Ω. The measurements determined that the transistor h was actually 16.5 Ω for
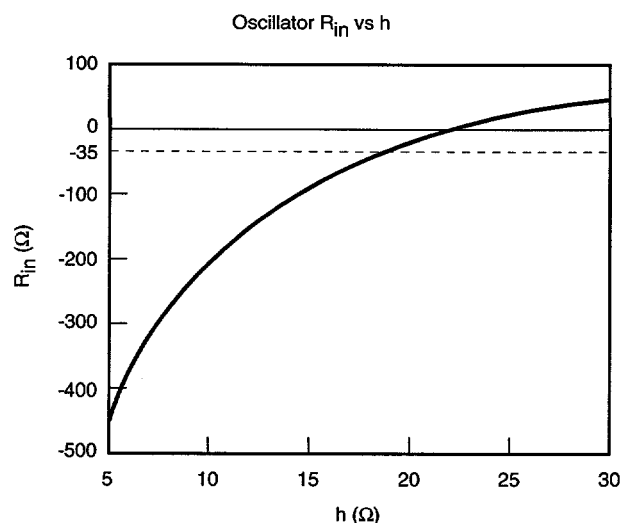

Figure 5. Negative Resistance Model Calculations

the oscillation (small signal) with the 35 Ω resonator and 20 Ω when the resonator was shorted out with a small wire. This error is well within both the measurement capability at this frequency and the simple model that equation (2) is derived from. Base-spreading resistance and internal transistor capacitances easily explain this discrepancy.

At low frequencies (<10 MHz) the transistors are more nearly ideal and equation (2) is nearly ideal. At high-frequencies if R_5 and R_6 are kept relatively small then the circuit will behave closer to the ideal. Another important aspect of the circuit in Figure 4. is how the output is take from the collector of Q_1. In this circuit the 50 Ω load is connected directly (L_3 is an RF choke) to the collector of Q_1. This is done to minimize the Miller effect at the base of Q_1 thus isolating the oscillator from the load.
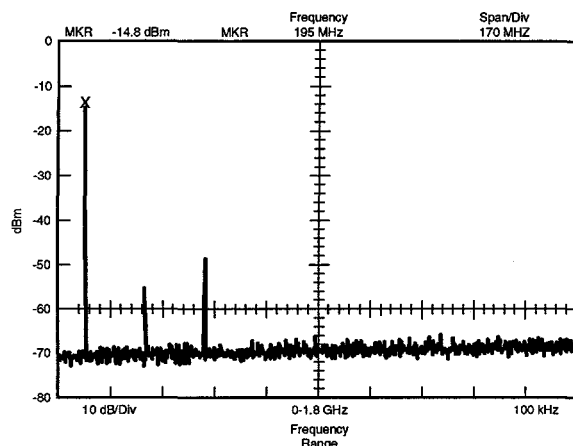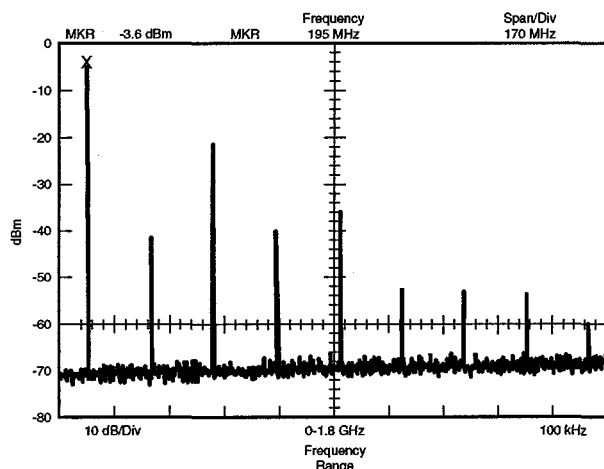
Figure 6. Oscillator Spectrum, R_{in} = -90Ω

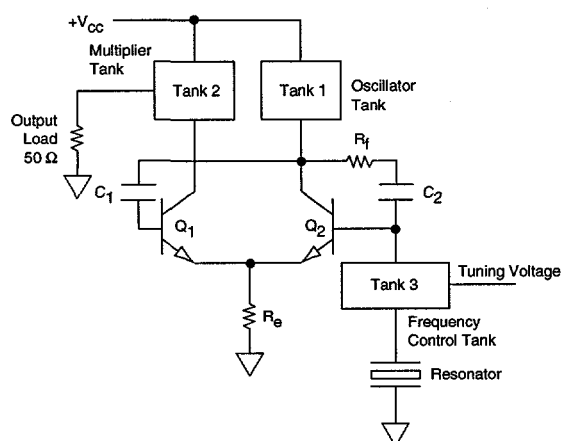Figure 7. Oscillator Spectrum, R_{in} = -330 Ω

Figure 8. High-Frequency Multiplier VCO

Frequency Multiplied VCO

The oscillator described generates significant odd-harmonics. The amplitude of the harmonics relative to the fundamental is strongly a function of the excess negative resistance (or excess gain) of the circuit.

Figures 6. and Figure 7. are the oscillator output spectrum for h = 15 and h = 7 respectively. From the graph in Figure 5. it can be seen that this corresponds to a R_{in} of approximately -90 Ω and -330 Ω. These spectra demonstrate that for relative efficiency a tripler design would be the best choice. The oscillator stability is not very dependent upon the level of overdrive in this circuit design but is primarily determined by resonator Q and the magnitude of the negative feedback. For this example R_f was set to a relatively low value of 120 Ω which provides significant negative feedback (via the resonator impedance given) thus increasing the circuit stability. The transfer function of the differential pair yields nearly linear performance over a large range of operating amplitude.

Figure 8. is a block diagram of a complete differential amplifier-oscillator with a built in tripler and voltage control. This VCO was designed for 585 MHz operation with a 195 MHz resonator. Tank 3 is series L-C combination where the C is a hyperabrupt varactor diode, Tank 1 is the oscillator tank and is used for the same purpose as the previous design example. Tank 2 is the frequency multiplying tank which provides a good impedance match at three times the oscillator frequency. Tank 2 also is designed to minimize any Miller effect at the base of Q_1 at the primary oscillation frequency.

These functions will be addressed separately and in greater detail. The negative feedback resistance R_f is from the collector to base of Q_2. This is equivalent to the previous design in that ac behavior of the two circuits are identical. C_1 and C_2 are large value dc blocking capacitors.

Figure 9. is a complete schematic of the VCO. This design includes voltage regulation of the collectors and bases of Q_1 and Q_2 via the low current band-gap devices CR_3 and CR_2 respectively.

Figure 10. is the schematic of Tank 2, the multiplier tank. L_2 in parallel with L_6 is series resonant with C_4 in parallel with the capacitance of the choke L_1 (of Figure 9.) This tank circuit shunts the funda-
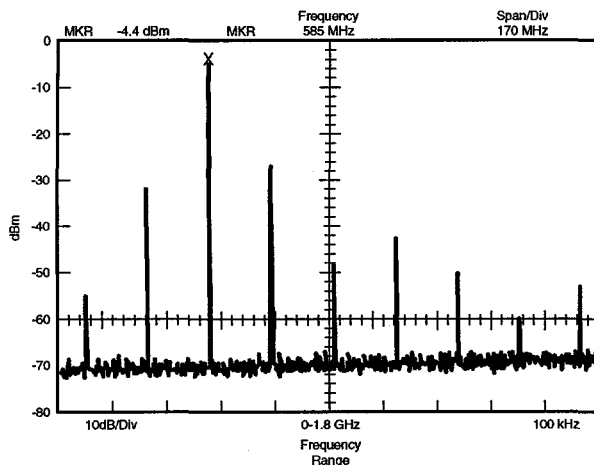
Figure 12. Oscillator-Multiplier Output Spectrum

f_s	195 MHz
Overtone	3rd
R_m	36 Ω
C_m	0.462 fF
L_m	1.44 mH
C_o	1.82 pF

Figure 14. 195 MHz Resonator Parameters

comb or cavity type filter if desired.

Tank 3 in Figure 8. uses a series L-C where the capacitance is a frequency linear tuning varactor which allows for a linear impedance (jΩ) versus varactor voltage. This tank is designed to be approximately series resonant at one half the desired control voltage range. This L-C combination creates nearly a linear impedance versus voltage. Therefore linear
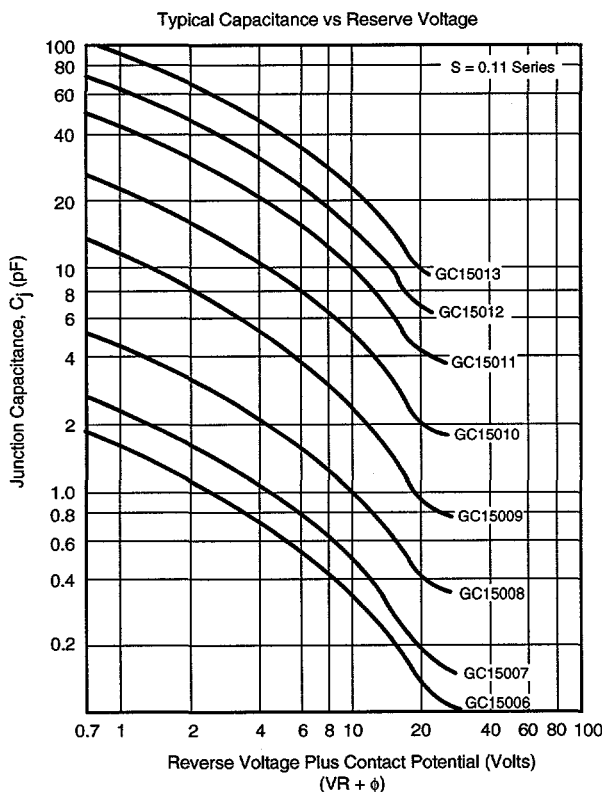
control is possible down to zero volts dc. The actual schematic of the resonator puulling network network is : L_7, L_8, CR_1, in series with the resonator Y_1. To allow the tuning network to linearly control frequency the resonator shunt capacitance must be removed, thus making the resonator impedance versus frequency linear. L_4 is chosen to resonate out the resonator and circuit-board capacitance from the resonator node to ground.

The varactor chosen was a Loral GC15008 which is approximately 2 pF at 4 volts. The varactor capacitance curves are shown in Figure 13. The total network was designed for maximum pullability while maintaining design robustness. The resonator was chosen for repeatability of design, low-phase noise and very low-aging. Typical resonator parameters are given in Figure 14. Figure 15. is a calculation of

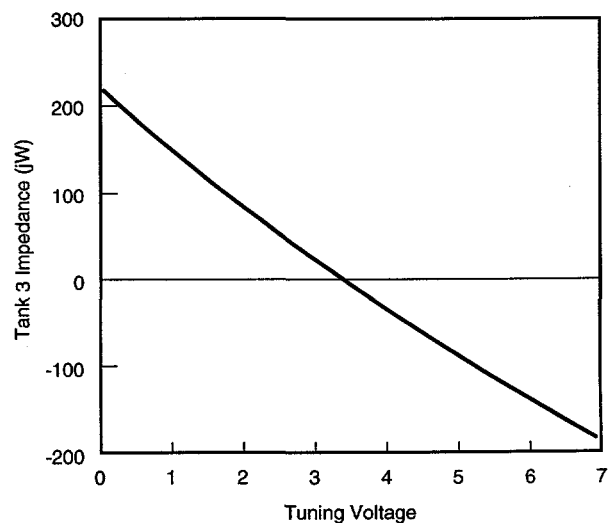Figure 13. Hyper-Abrupt Diode Characteristics

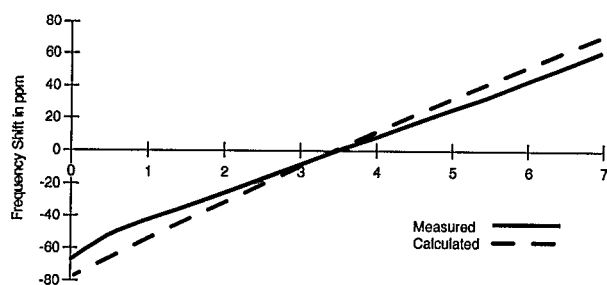Figure 15. Calculations of Tank 3 Impedance vs Tuning Voltage

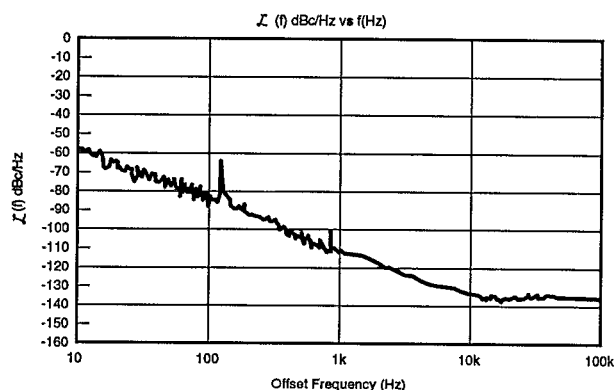Figure 16. VCO Frequency Shift vs Control Voltage

Figure 17. Typical Oscillator Phase-Noise, 585 MHz

the L-C (Tank 3) impedance versus varactor control voltage. This graph shows a high degree of linearity over approximately 400 jΩ of impedance change.

Figure 16. shows a measured and calculated frequency versus control voltage plot. The model used to calculate this response included component and circuit-board parasitic capacitances. The difference between the measured and calculated responses is probably due to unit to unit varactor variations in that the model used is based on the average varactor performance. The frequency pulling range is greatly effected by the C_m of the resonator which was specified as 0.5 fF +/- 0.15 fF. This range of C_m will yield a +/- 50 to +/- 70 ppm frequency pulling capability for the basic design tolerances. The power supply for this design was chosen to be 7 volts therefore the center-frequency control voltage is 3.5 volts. R_7 and R_{11} which correspond to R_c and R_f of the earlier design example are larger value resistors (relative to the first design example) to increase circuit

efficiency and harmonic generation at the expense of oscillator stability. The design draws a total of 9 mA at 7 volts. Without voltage regulation the oscillator had a frequency stability of approximately 2 ppm per volt. The oscillator itself draws approximately 6 mA. The load pushing is approximatelty +/- 5 ppm for a return loss of -10 dB.

Figure 17. is plot of the oscillator phase-noise versus offset frequency. This plot is typical but the design spread, due to resonator phase-noise inconsistencies and variability in Q, is within +/- 6 dB from this plot. The phase-noise of this unit is approximately -113 dBc/Hz at 1 kHz offset. The phase noise of the reference oscillator is primarily limiting the measurement at offset frequencies > 10 kHz.

The oscillator (Figure 9.) has components that may be required to limit the high-frequency response and thus decrease the possibility of undesired high-frequency modes of oscillation. C_5 can be a relatively low-value (0.5 pF) capacitor placed from the emitters of the differential amplifier to ground to limit the gain of the stage at very high (> 1 GHz) frequencies. Also it has been found that adding a small loss in series with the resonator will also help supress high frequency modes. In the oscillator in Figure 9. the varactor-inductor tuning network is lossy enough to provide high frequency damping; therefore, a resistor was not added as a dicrete component. The oscillator in Figure 4., if designed for high frequency operation with no series tuning network, may require a series resistor to be added to the resonator to suppress high frequency modes. These modes are primarily driven by the resonance of the resonator lead length resonanting with the resonator shunt capacitance and will generally be in the GHz range.

Experimental Oscillator

The oscillators described to this point use two transistors for the differential amplifier . For many applications this simple circuit is adequate. Referring to Figure. 8, if one desired significantly more negative feedback for improved oscillator stability then one would decrease R_f. Decreasing R_f significantly would simultaneously decrease the Q and effective collector impedance at Q_2. Although the design can function with low values of R_f it may at some point be
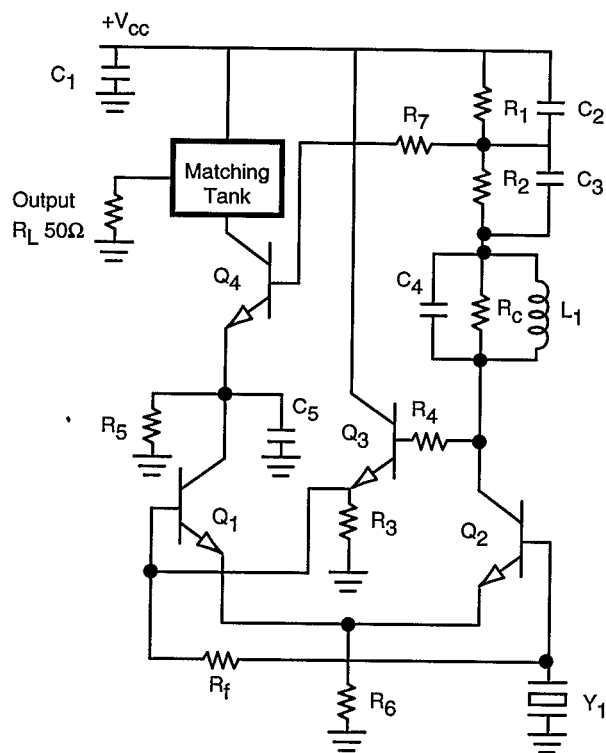
Figure 18. Experimental Differential-Amplifier Oscillator

oscillator frequency harmonic or nonharmonic to be matched to the desired load.

The negative resistance (R_{in}) of this oscillator is determined by the following equiation:

$$R_{in} \sim R_f - \frac{R_f R_c}{2(h + r_e)} \qquad (3)$$

Conclusions

Differential-amplifier oscillators have been shown to be a practical design topology for high-frequency designs. These oscillators can be voltage controlled with a series varactor-inductor-resonator circuit and can be designed for a high degree of tuning linearity. The odd harmonic generation of the differential amplifier configuration makes a tripler or quintupler design an attractive option when high-efficiency is desirable. These designs are relatively easy to analyze and realize at the high frequencies available with inverted-mesa resonators.

References

[1] A. Benjaminson, "Balanced Feedback Oscillators," in Proceedings of the 38th Annual Symposium On Frequency Control, 1984, pp. 327-333.

[2] K. O. Wessendorf, "The Lever Oscillator For Use In High Resistance Resonator Applications," in Proceedings Of The 1993 IEEE International Frequency Control Symposium, 1993, pp 711-717

[3] P. R. Gray and R.G. Meyer, Analysis and Design of Analog Integrated Circuits Second Edition. New York, John Wiley and Sons, 1984, ch.3, pp. 167-199

impractical to load the collector of Q_2 too heavily. Also, as stated earlier, it is desirable to eliminate the main oscillation component from the collector of Q_2 to minimize or eliminate Miller effects at the base of Q_1. The previous designs are either multipliers or poorly matched direct frequency outputs.

A derivative of the oscillator designs presented is given in Figure. 18. This design attempts to solve the above short-comings in a relatively elegant way. Q_3 and Q_4 have been added to the design together with bias and stabilizing resistors. Q_3 is simply an emitter follower used to provide a low output impedance from the collector of Q_2 while maintaining a high output impedance leg for the collector tank C_4, R_c, L_1. This dual use collector is ideal for design flexibility of the differential amplifier oscillator. As one can see Q_3 provides bias for Q_1 and also Q_2 through Rf. This arrangement is acceptable when Rf is small and thus has no significant dc drop across it. Q_4 is added to the collector leg of Q_2 as a cascode buffer amplifier. This arrangement allows a low impedance load for the collector of Q_1 thus minmizing Miller effects at Q_1. The matching tank at the collector of Q_4 allows the selection of any desired