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Space and Military Radiation Effects in Silicon-on-Insulator Devices

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Outline

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1.0 INTRODUCTION

Advantages in transient ionizing and single-event upset (SEU) radiation hardness of silicon-on-insulator (SOI) technology spurred much of its early development. Both of these advantages are a direct result of the reduced charge collection volume inherent to SOI technology. The fact that SOI transistor structures do not include parasitic n-p-n-p paths makes them immune to latchup. Even though considerable improvement in transient and single-event radiation hardness can be obtained by using SOI technology, there are some attributes of SOI devices and circuits that tend to limit their overall hardness. These attributes include the bipolar effect that can ultimately reduce the hardness of SOI ICs to SEU and transient ionizing radiation, and charge buildup in buried and sidewall oxides that can degrade the total-dose hardness of SOI devices. Nevertheless, high-performance SOI circuits can be fabricated that are hardened to both space and nuclear radiation environments, and radiation-hardened systems remain an active market for SOI devices.

In this short course segment, we review the effects of radiation on SOI MOS devices. At the end of each section, major differences in the radiation response of bulk-silicon devices are highlighted (throughout this review we refer to bulk-silicon devices as those devices fabricated either directly on a silicon substrate or on an epitaxial layer). By including a review of radiation effects on bulk-silicon devices, we are in a position to better appreciate and understand the advantages (and disadvantages) and possible applications of SOI devices for radiation-hardened systems.

We begin with a description of two major radiation environments: the natural space radiation environment and the environment associated with a nuclear weapon explosion. The mechanisms for heavy-ion induced SEU upset and hard errors are discussed next. Possible methods for improving the SEU hardness of both SOI and bulk-silicon devices are reviewed. We next cover the effects of total dose ionizing irradiation. The next topic covers the response of SOI and bulk-silicon devices to pulses of high dose rate, i.e., transient ionizing irradiation. We conclude with a very brief review of displacement damage effects. Because displacement damage primarily affects the lifetime of minority carriers, they are most important for bipolar and optoelectronic devices and are relatively unimportant for MOS devices.

2.0 RADIATION ENVIRONMENTS

2.1 Natural Space Radiation Environment

The concentration and types of particles in the natural space environment vary significantly with altitude and angle of inclination, recent solar activity, and amount of spacecraft shielding. As such, it is nearly impossible to define a "typical" space environment. Particles present in the earth's natural space radiation environment include 1) particles trapped by the earth's magnetic field (primarily electrons and protons), 2) galactic cosmic rays, and 3) solar
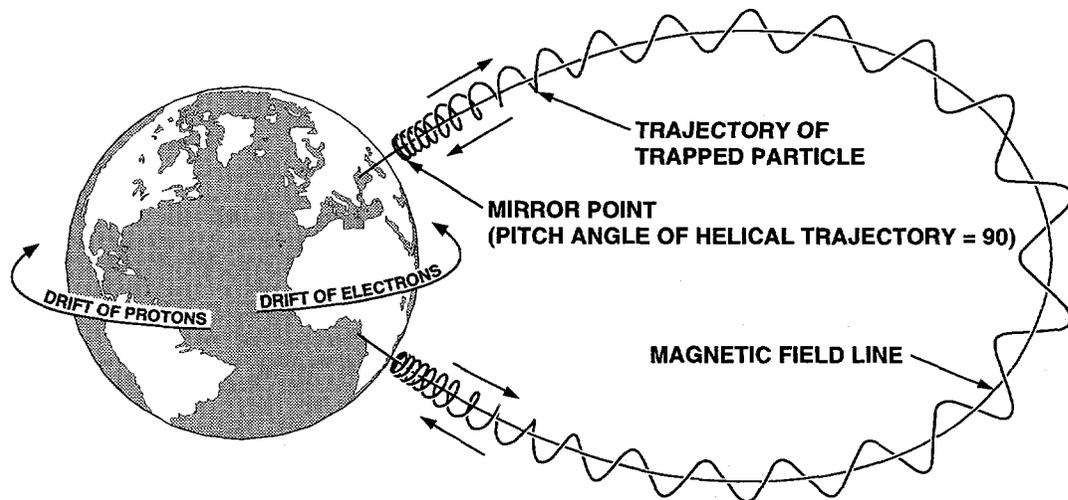
Figure 1: Motion of trapped particles in the earth's magnetosphere. (After Ref. 1)

cosmic rays. In this section, some of the general properties of the natural space environment are presented.

2.1.1 Particles Trapped by the Earth's Magnetic Field

The earth's magnetic field creates a geomagnetic cavity known as the magnetosphere [1]. The magnetic field lines trap low-energy charged particles. These trapped particles consist primarily of electrons and protons, although some heavy ions are also trapped. The trapped particles gyrate spirally around the magnetic field lines and are reflected back and forth between the poles where the fields are confined. The motion of the trapped particles is illustrated in Fig. 1 [1]. As charged particles gyrate along the magnetic field lines, they also drift around the earth with electrons drifting in an easterly direction and protons drifting in a westerly direction. The motion of charged particles forms bands (or domains) of electrons and protons around the earth and form the earth's radiation belts.

The boundaries of the domains at the equator are illustrated in Fig. 2 [1]. Distances are specified in earth radii (one earth radius is equal to 6380 km) referenced to the center of the earth, i.e., one earth radius is at the earth's surface. Because of the variation in the magnetic field lines with latitude, the boundaries of the domains vary with latitude (angle of inclination). Most satellites are operated in near-earth orbits at altitudes from slightly above 1 earth radius to 10 earth radii. Geosynchronous orbit (GEO) is at an altitude of approximately 35,800 km corresponding to approximately 6.6 earth radii. The domains can be divided into five regions. The trapped proton distribution exists primarily in regions one and two that extend from slightly above 1 earth radius to 3.8 earth radii. The distribution of proton flux as a function of energy and radial distance is given in Fig. 3 [1]. *[Flux is the rate at which particles impinge upon a unit surface area. It is normally given in units of particles/cm^2-s. The time integral of flux is fluence. Thus, fluence is equal to the total number of particles that impinge upon a unit surface area and it is normally given in units of particles/cm^2.]* Trapped protons can have energies as high as

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~3.8

~2.8   ~5.0   ~12.0

Region | **1** | **2** | **3** | **4** | **5**

1 2 3 4 5 6 7 8 9 10 11 12 13 14

Earth Radii

Solar Flare Protons

Trapped Protons

Outer Zone Electrons

Inner Zone Electrons

Synchronous

Inner Zone Electrons   Trapped Protons

Outer Zone Electrons   Solar Flare Protons
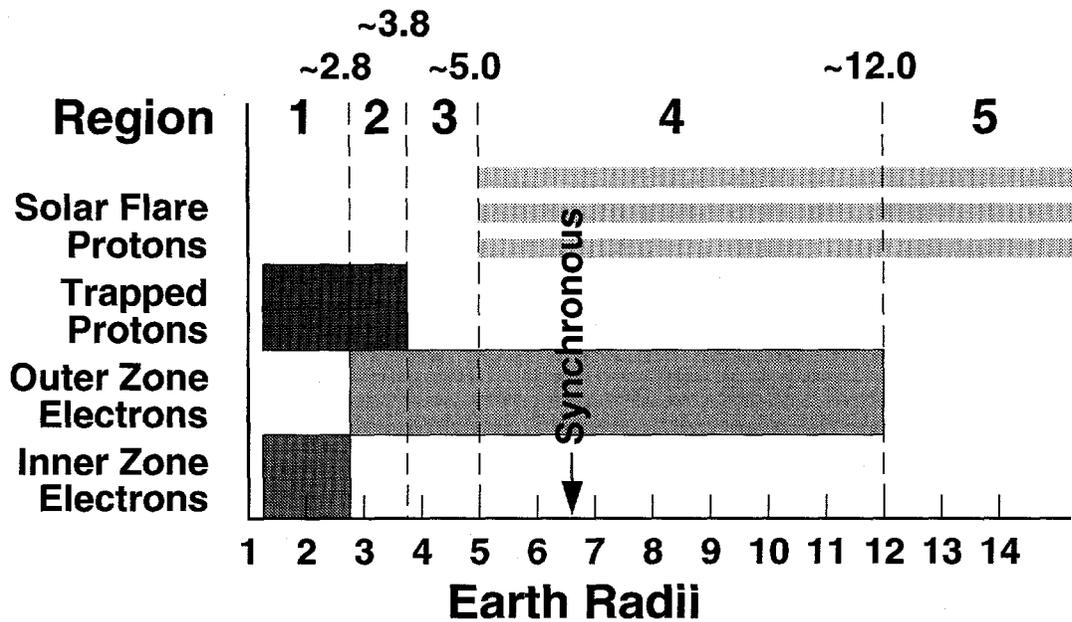
Figure 2: Boundaries of the domains for solar flare and trapped protons and outer and inner zone electrons. (After Ref. 1)

500 MeV [1]. Note that the altitude corresponding to the peak in flux decreases with proton energy. Protons with energies greater than 10 MeV primarily occupy regions one and two below 3.8 earth radii [1]. Typical spacecraft shielding attenuates protons with energies below 10 MeV [2]. Thus, the predominantly low-energy trapped protons present above 3.8 earth radii are normally ineffective in producing radiation-induced damage. For proton energies greater than 30 MeV, the highest proton flux occurs at about 1.5 earth radii. Protons originating from solar flares (discussed below) are present predominantly in regions four and five (Fig. 2) and extend from ~5 earth radii to beyond 14 earth radii.

Above the Atlantic Ocean centered off the coast of South America, the geomagnetic sphere dips toward the earth causing a region of increased proton flux at relatively low altitudes. This region is called the South Atlantic anomaly (SAA). In this region, the flux of protons with energies greater than 30 MeV can be as much as 10^4 times higher than in comparable altitudes over other regions of the earth. At higher altitudes the magnetic sphere is more uniform and the South Atlantic anomaly disappears [3].

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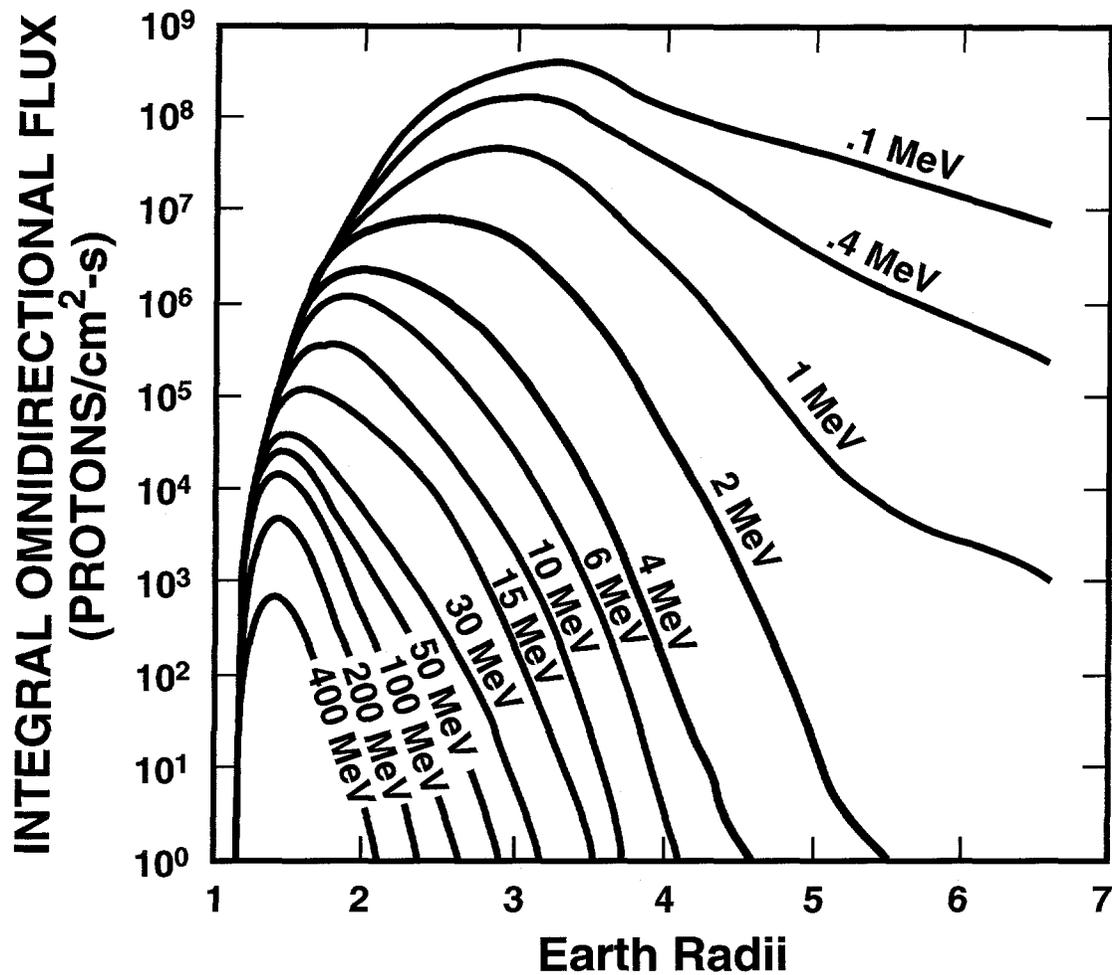
Figure 3: Distribution of proton flux as a function of energy and radial distance. (After Ref. 1)

Electrons are present predominantly in regions one to four and extend up to 12 earth radii [1]. The electron domain is divided into two zones, an inner zone extending to about 2.8 earth radii and an outer zone extending from 2.8 to 12 earth radii. The outer zone electrons have higher fluxes (~10 times) and energies than the inner zone electrons. For electrons with energies greater than 1 MeV, the peak in flux is located between 3 and 4 earth radii [4]. The maximum energy of trapped electrons is approximately 7 MeV in the outer zone; whereas, the maximum energy is less than 5 MeV for electrons in the inner zone [1]. At these energies electron interactions are unimportant for single-event effects, but must be considered in determining total-dose effects.

Fluxes of electrons and protons in particular orbits can be estimated from existing models. Two models that have been used to estimate proton and electron fluxes as a function of satellite orbit are AP8 [5] for protons and AE8 [6] for electrons. However, experimental data [7-9] suggest that recent solar flares have created a new proton belt and have enhanced the electron
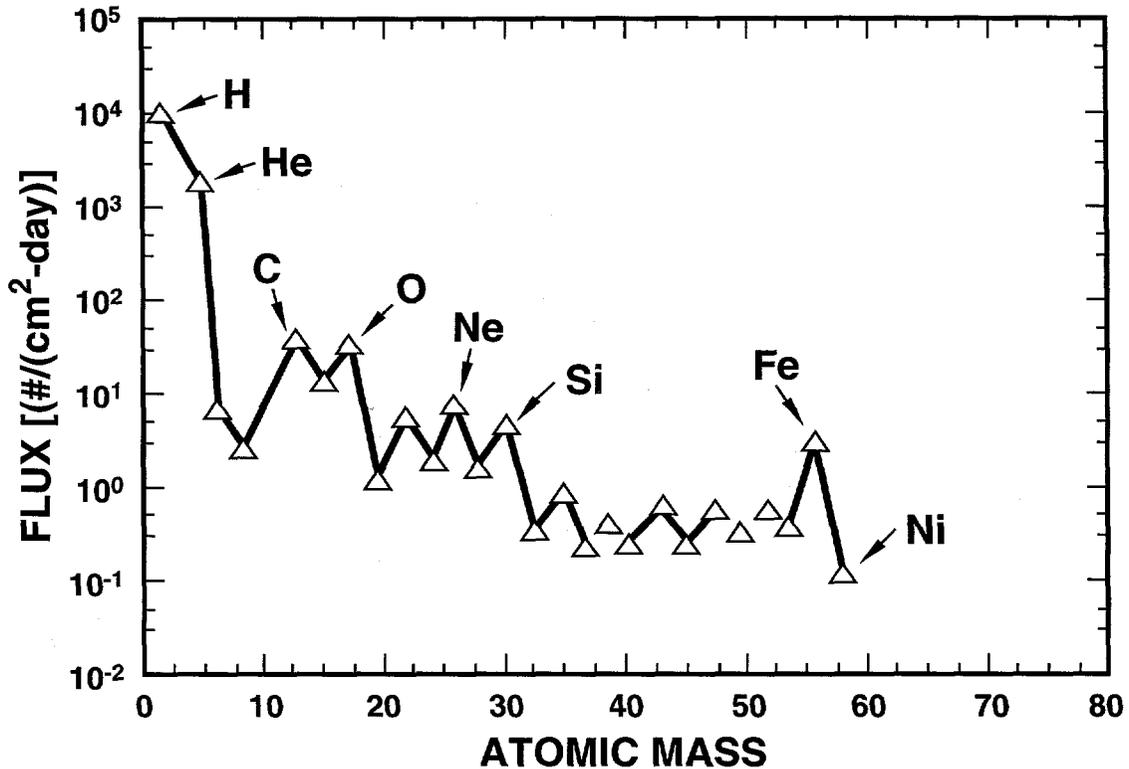
Figure 4: Flux of galactic cosmic ray particles for atomic masses up to 59. (After Refs. 2 and 10)

belts. These results indicate that the AP8 and AE8 models may significantly underestimate the concentration of protons and electrons, especially for orbits between 1.8 and 3 earth radii.

2.1.2 Galactic Cosmic Rays

Galactic cosmic rays originate from sources outside our solar system and are always present. In the absence of solar activity, cosmic radiation is composed entirely of galactic radiation. Outside of our solar system, the spectrum of galactic cosmic rays is believed to be uniform. Its composition as a function of atomic mass is given in Fig. 4 [2,10]. It consists mostly of protons (85%) and alpha particles (helium nuclei) (14%). Less than 1% of the galactic cosmic ray spectrum is composed of high-energy heavy ions. This is not an indication that heavy ions are not as important as protons in space radiation effects. As will be discussed below, heavy ions deposit more energy per unit depth in a material than protons, and can actually cause greater numbers of single-event effects. As illustrated in Fig. 4, the flux of protons is more than two orders of magnitude higher than the flux of either carbon or oxygen and approximately five orders of magnitude higher than the flux of nickel. The energy spectrum of galactic cosmic rays is given in Fig. 5 [11]. Note that the x-axis of Fig. 5 is given in units of MeV/nucleon. Thus, for carbon with 12 nucleons, the point at 100 MeV/nucleon on the x-axis corresponds to an energy of 1.2 GeV. For most ions, the flux peaks between 100 and 1000 MeV/nucleon. For carbon, the peak flux is at an energy of approximately 2.4 GeV. For protons and alpha particles, the energy

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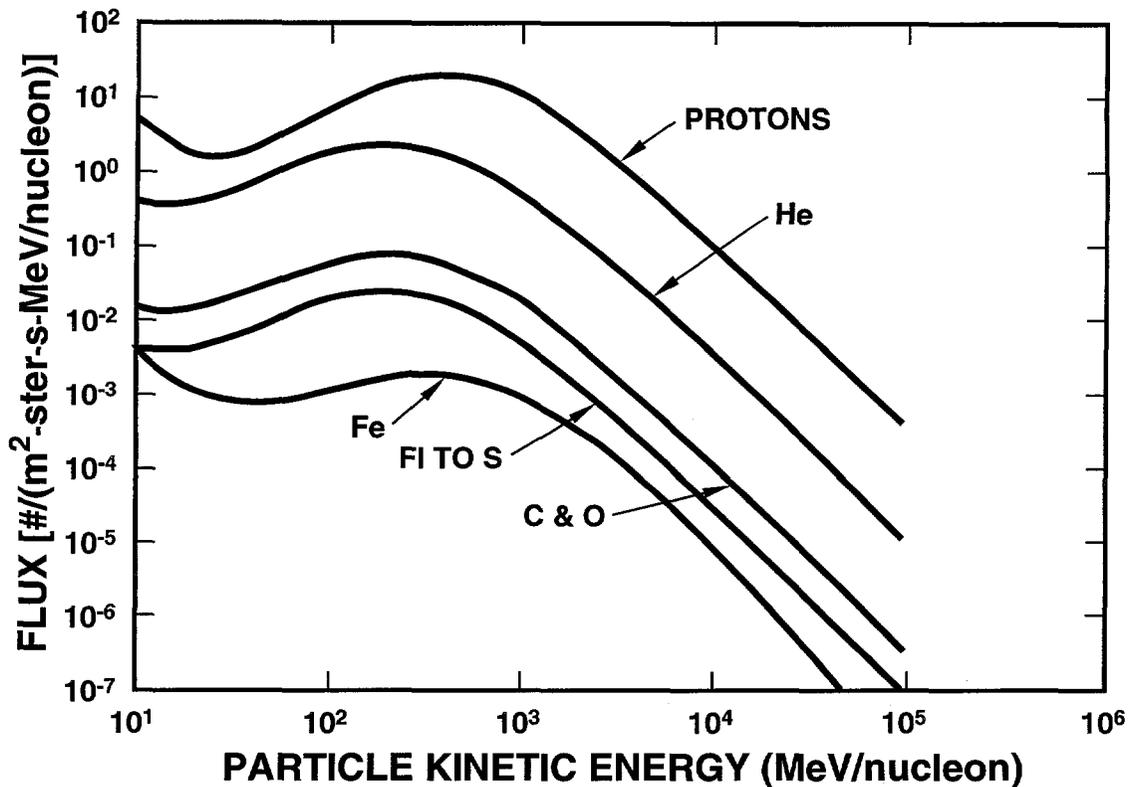
Figure 5: Energy spectrum of galactic cosmic rays. (After Ref. 11)

of the ion can be more than 100 GeV/nucleon. At these high energies, it is nearly impossible to shield electronics inside a spacecraft from cosmic rays.

At geosynchronous orbit (~35,800 km) the earth's magnetic field is weak enough, that for all practical purposes, it can be considered to have a negligible effect on the galactic cosmic ray spectrum [12]. However, as cosmic rays penetrate deeper into the magnetosphere, low-energy particles are attenuated, modifying the cosmic ray spectrum. Only the more energetic particles are able to penetrate the magnetosphere. The amount of geomagnetic shielding decreases with higher inclination orbits as the magnetic field lines converge near the poles.

2.1.3 Solar cosmic rays

The amount of solar cosmic rays is naturally dependent on the amount of solar activity. Solar flares are random in nature and account for a large part of all solar cosmic rays. After a solar flare occurs, particles begin to arrive near the earth within tens of minutes, peak in intensity within two hours to one day, and are gone within a few days to one week (except for some solar flare particles which are trapped in the earth's radiation belts). In a solar flare, energetic protons, alpha particles and heavy ions are emitted. In most solar flares the majority of emitted particles are protons (90-95%) and alpha particles. Heavy ions constitute only a small fraction of the emitted particles, and the number of heavy ions is normally insignificant compared to the background concentration of heavy ions from galactic cosmic rays. In a large solar flare the

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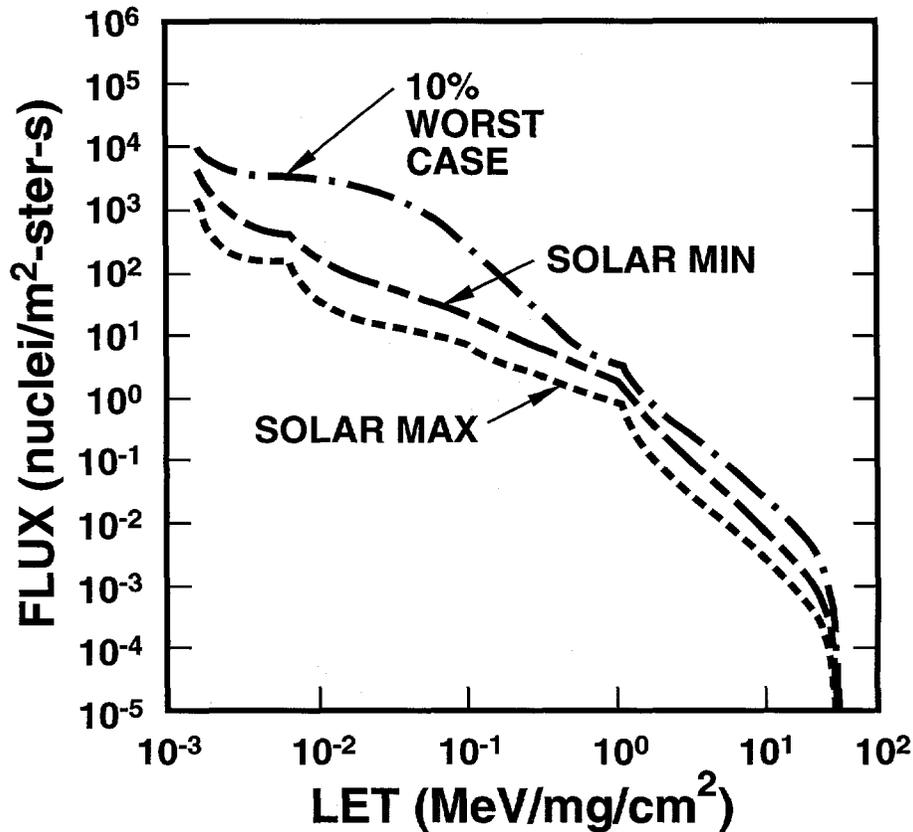
Figure 6: Flux of cosmic ray particles at solar maximum, at solar minimum, and for Adams' 10% worst-case environment. (After Ref. 15)

number of protons and alpha particles can be greatly enhanced ($\sim 10^4$ times) over the background galactic cosmic ray spectrum; whereas, the number of heavy ions for a large solar flare approaches up to ~50% of the background galactic cosmic concentration of heavy ions [13]. Associated with a solar flare is the solar wind or solar plasma. The solar wind usually arrives near the earth within one to two days after a solar flare [14]. As the solar wind strikes the magnetosphere, it can cause disturbances in the geomagnetic fields (geomagnetic storm), compressing them towards the earth. As a result, the solar wind can enhance the total dose that a device receives in a low-earth orbit.

Figure 6 [15] is a plot of the angular flux of galactic cosmic ray particles (both solar and galactic) during solar minimum and maximum inside a spacecraft in geosynchronous orbit with 25 mils of aluminum shielding as a function of linear energy transfer (LET). *[LET is the mass stopping power of cosmic rays and is given in the units of MeV/mg/cm^2. It is a measure of the amount of energy a particle transfers to a material per unit path length.]* The solar cycle peaks in intensity approximately every 11 years. Solar maximum refers to periods of maximum solar activity, and solar minimum refers to periods of minimum solar activity. The solar wind during periods of high solar activity reduces the galactic cosmic ray flux. Thus, the minimum in galactic cosmic ray flux occurs during solar maximum, and the maximum in galactic cosmic ray flux occurs during solar minimum. The flux at solar minimum describes the actual environment for
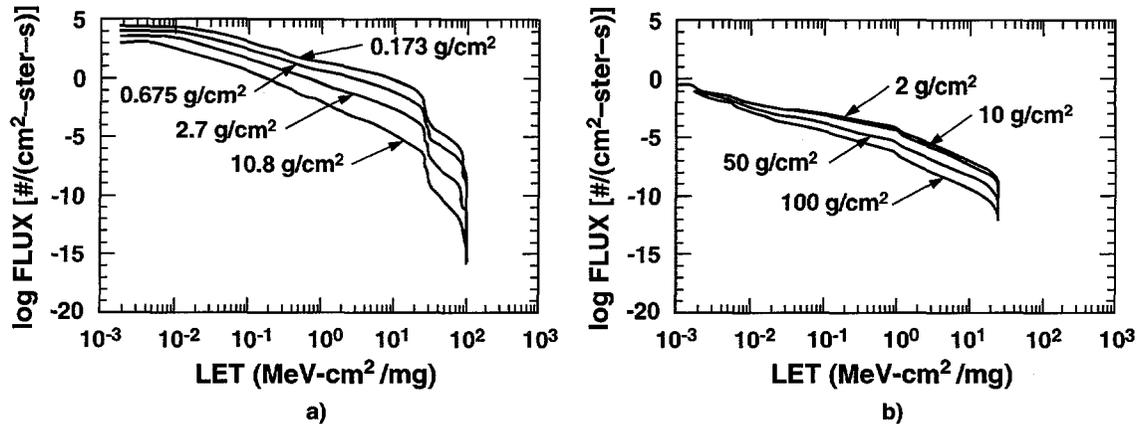
Figure 7: The effects of aluminum shielding on the attenuation of the flux from a large solar flare (a) and of the flux from the galactic cosmic ray spectrum (b) as a function of the LET of the incident particles. (After Ref. 16)

40% of the time. Also shown in Fig. 6 is the Adams' 10% worst-case environment. The actual environment is more intense than the Adams' 10% worst-case environment only 10% of the time. It includes contributions from both galactic and solar cosmic rays. This environment is often used in benchmarking the single-event upset hardness of electronic devices.

2.1.4 Radiation Environment Inside a Spacecraft

Thus far, we have explored the natural space radiation environment outside a spacecraft. To determine the effects of the natural space environment on electronics inside the spacecraft, the effects of shielding must be taken into account. Shielding not only modifies the radiation environment inside a spacecraft by altering the energy and concentration of incoming particles, but also can create secondary particles as the incoming particles pass through the shielding. For instance, bremsstrahlung radiation in the form of x rays is emitted as energetic electrons decelerate in the shielding. For modest amounts of shielding, the effects of shielding can be estimated by taking into account only the energy loss of particles as they pass through the shielding [15].

The amount of energy loss as a particle passes through shielding depends on the thickness of the material. Typical spacecraft shielding is in the range of 100 to 250 mils. Figure 7a [16] is a plot of flux for a large solar flare versus LET for aluminum thicknesses of 0.173 (25 mils) to 10.8 g/cm^2 (1570 mils). Note that increasing aluminum thickness results in decreasing solar flare flux for the relatively low-energy particles associated with a solar flare. However, the qualitative variation in flux with LET is relatively unaffected by the shielding. For LETs above 30 MeV-cm^2/mg, increasing the shielding thickness from 0.17 g/cm^2 to 10.8 g/cm^2 reduces the intensity of the spectrum by five orders of magnitude. The effect of spacecraft thickness on galactic cosmic ray flux is shown in Fig. 7b [16]. It takes much more shielding to reduce the intensity of galactic cosmic rays. Spacecraft thicknesses of aluminum from zero up to 10 g/cm^2 (1450 mils) only slightly affect the LET spectrum. By comparing Figs. 7a and 7b, we conclude that spacecraft shielding can attenuate the low-energy nuclei from a solar flare, but has little effect on the

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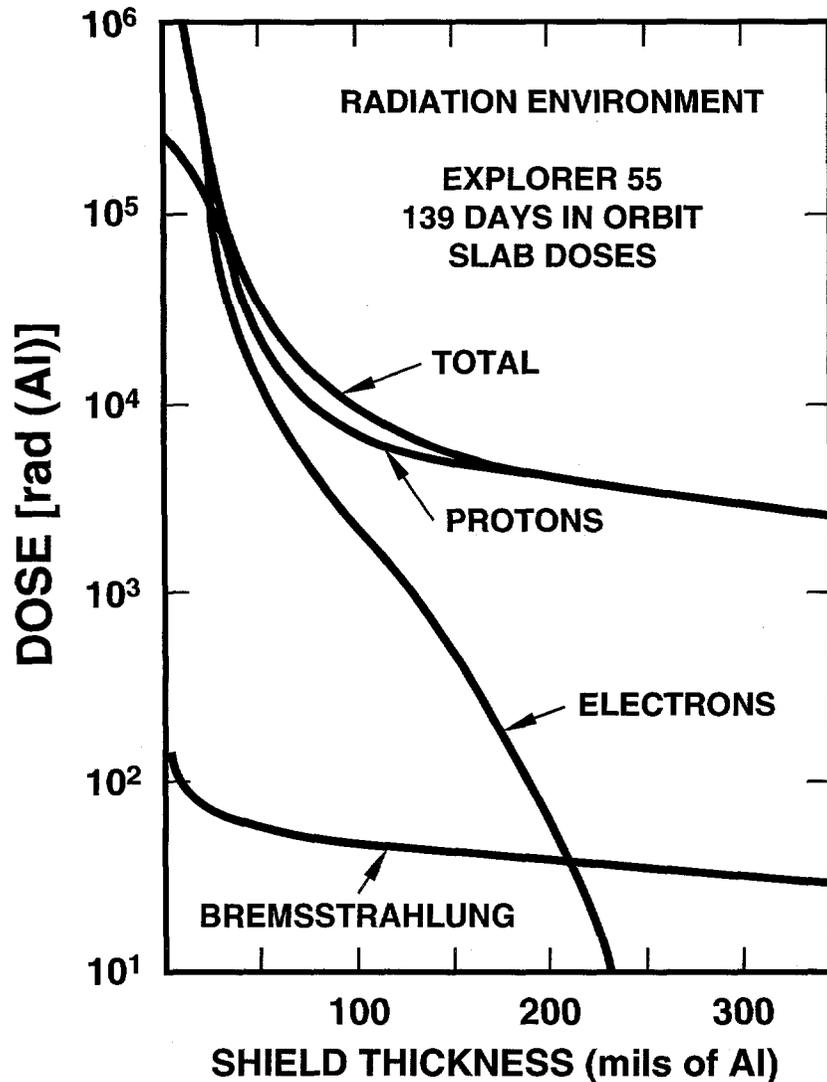
Figure 8: Contributions of protons, electrons, and bremsstrahlung to total dose as a function of aluminum shielding. The data were taken after a 139-day exposure during the Explorer 55 space mission. (After Ref. 17)

attenuation of nuclei in the galactic cosmic ray spectrum. Thus, for practical shielding thicknesses, additional shielding may prove effective against soft components of a solar flare environment, but is relatively ineffective in reducing the galactic cosmic ray spectrum [2].

Figure 8 [17] is a plot of the contribution of protons, electrons, and bremsstrahlung to the total dose received after a period of 139 days as a function of aluminum thickness measured aboard the Explorer 55 spacecraft [17]. The data were taken during a period of minimum solar activity. *[Note that the total dose is specified in units of rad(Al). A rad is defined as radiation absorbed dose. It is a measure of the amount of energy deposited in the material and is equal to 100 ergs of energy deposited per gram of material. The energy deposited in a device must be specified for the material of interest. Thus, for a MOS transistor, total dose is measured in units of rad(Si) or rad(SiO₂).]* For small aluminum thicknesses, both electrons and protons contribute to the total-absorbed dose. However, for aluminum thicknesses greater than ~150 mils, the

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electron contribution to the total dose is negligible. The contribution of bremsstrahlung radiation to the total absorbed dose is negligible for all aluminum thicknesses. Increasing the shielding thickness from 100 to 250 mils of aluminum decreases the proton dose by less than a factor of two. Although these data are for a specific satellite orbit, the trends indicated in Fig. 8 are typical for those of other orbits.

As is apparent from Figs. 2 and 3, the total dose that a device is exposed to in a space environment is highly dependent on the orbit. To determine the total dose, one must include contributions from both electrons and protons. The dose rate can vary over a wide range, from less than 10^{-6} to mid 10^{-3} rad(Si)/s. For a five year mission life, these dose rates correspond to a total-dose range of less than 1 krad(Si) to more than 5 Mrad(Si). For low-earth orbits at high inclination, 200 mils of aluminum shielding can limit the total proton dose to less than 1 krad(Si) per year [18]. Other orbits can result in total doses several orders of magnitude higher. At altitudes corresponding to roughly 1/2 the altitude at geosynchronous orbit (near worst case), the total dose that a device can receive inside a spacecraft with light shielding can approach 1 Mrad(Si) per year [1,19].

2.2   Nuclear Radiation Environment

Tremendous amounts of energy are released in a nuclear explosion. If a device (or electronic system) survives the thermal radiation and blast or shock induced by a nuclear weapon, it is still susceptible to failure or degradation due to the highly energetic particles released instantaneously as a direct result of the blast or over longer periods of time due to secondary processes [20]. These particles include low-energy x rays, high-energy gamma rays, and neutrons. The short time scales associated with a nuclear explosion can result in very high dose rate pulses of ionizing radiation that can generate large photocurrents in an IC leading to memory upset.

2.3   Laboratory Radiation Sources

A wide range of laboratory sources are available to characterize the response of electronic devices in space and nuclear radiation environments. For total-dose effects, these sources range from very high dose rate sources for characterizing device response in weapon environments to very low dose rate sources for investigating the basic mechanisms of radiation effects for simulating the total-dose response of electronic devices in the natural space environment. The most common laboratory sources are moderate dose rate Co-60 and x-ray sources. Co-60 sources emit gamma rays with a nominal energy of 1.25 MeV at dose rates up to 400 rad(Si)/s. The present U. S. military standard test guideline MIL-STD-883D, Method 1019.4 specifies that standard laboratory acceptance testing be performed at dose rates from 50 to 300 rad(Si)/s. Thus, Co-60 sources can normally meet these requirements. Another common type of laboratory source is the 10-keV x-ray source. Laboratory x-ray sources that can test unlidded package devices or devices on a wafer are available that can achieve dose rates from below 200 rad(Si)/s

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to above 3600 rad(Si)/s. The high dose rate of x-ray sources and the capability for testing at the wafer level allows for rapid feedback on radiation hardness during device fabrication [21].

Two high dose rate sources that can be used to investigate the total-dose and dose-rate response of electronic devices at short times after a pulse of radiation are electron linear accelerators (LINACs) and proton cyclotrons. Electron LINACs are pulse type sources with pulse widths ranging from less than 20 ns to more than 10 μs with energies from 10 MeV to more than 40 MeV. Dose rates greater than 10^{11} rad(Si)/s can be obtained from electron LINACs. Proton cyclotrons are quasi-continuous sources and can have dose rates as high as 1 Mrad(Si)/s with energies from around 40 MeV to greater than 200 MeV. They can also be operated in low current modes suitable for characterizing proton-induced single-event effects.

For simulating low dose rate total-dose effects, Co-60 and Cs-137 sources are available. Cs-137 sources emit gamma rays with a nominal energy of 0.66 MeV. Dose rates below 0.01 rad(Si)/s can be obtained from Cs-137 radiation sources.

There are a wide range of sources available for characterizing heavy-ion induced single-event effects. These sources vary widely in ion species, energy, and flux. Two often used sources in the U. S. are Brookhaven National Laboratories' Twin Tandem van de Graaff accelerator and Lawrence Berkeley Laboratories' 88-inch cyclotron. At the Brookhaven facility, ions are available, ranging from protons with energies of 30 MeV (maximum) and LETs of 0.02 MeV-cm^2/mg to gold with energies of 350 MeV and LETs of 81 MeV-cm^2/mg (in silicon at normal incidence and maximum energy). At Berkeley's facility, ions are available ranging from protons with energies of 60 MeV (maximum) and LETs of 0.009 MeV-cm^2/mg to bismuth with energies of 803 MeV and LETs of 95 MeV-cm^2/mg (in silicon at normal incidence and maximum energy). In addition to these facilities, other facilities are available in the U. S. and throughout the world for characterizing the single-event upset properties of electronic devices.

A number of neutron sources exist throughout the world. Two neutron sources at Sandia National Laboratories in Albuquerque, New Mexico, are the Annular Core Research Reactor (ACRR) and Sandia Pulse Reactor II (SPR-II). ACRR is a water reactor that uses a BeO-UO$_2$ fuel material enriched to 35% ^{235}U with 21.5 weight percent UO$_2$ and 78.5 weight percent BeO. Control rods are used to regulate the reactor. The reactor has a peak neutron flux (E>10 keV) of 5.7×10^{17} neutrons/cm^2-s. Associated with the neutron pulse is a gamma-ray pulse with a peak dose rate of 5.1×10^{8} rad(H$_2$O)/s. SPR-II is a fast-burst reactor containing a fuel element enriched to 93 percent ^{235}U alloyed to molybdenum. A burst rod is pneumatically moved between control rods to achieve high rates of reactivity. The peak neutron flux is 2×10^{19} neutrons/cm^2-s and has an associated gamma-ray pulse with a peak dose rate of 4.1×10^{9} rad(H$_2$O)/s.

3.0 SINGLE-EVENT PHENOMENA

One of the most detrimental effects of the natural space environment on electronics is single-event effects (SEE). Single-event effects were first postulated in 1962 by Wallmark and Marcus [22] and first observed in spacecraft electronics in 1975 by Binder, Smith, and Holman

[23]. In memory circuits, information is stored at nodes in a circuit. If a high-energy heavy ion strikes a circuit node, it can create sufficient charge in a transistor to change the state of the node and cause false information to be stored. This type of failure is a non-destructive or soft error and is known as a single-event upset (SEU). In addition to heavy ions, protons and neutrons can also cause single-event upset. A soft error can be corrected by reprogramming the circuit into its correct logic state or by restarting an algorithm in a central processing unit. The number of soft errors is normally specified in units of errors/bit-day. If the error rate is too large, it can result in performance degradation of a system and potentially mission failure.

A class of single-event effect that is not correctable by reprogramming is termed a hard error. Hard errors include single-event latchup (SEL), snapback (also called single transistor latch), burnout (SEB), and gate rupture (SEGR). If a hard error occurs, a circuit element can be physically damaged and the error cannot be corrected by reprogramming.

As device dimensions continue to shrink, less charge is stored on circuit nodes, and the energy required to change the state of a circuit node decreases. Hence, devices will become more vulnerable to single-event phenomena (SEP). Thus, as device dimensions continue to shrink, they will become more vulnerable to SEP. In fact, not only are commercial silicon circuits sensitive to radiation in the space environment, but they also are becoming more prone to upset due to cosmic-ray by-products and radioactive package contamination at the ground level.

In this section the mechanisms for single-event effects for SOI and bulk-silicon circuits are presented. Methods for hardening circuits to single-event effects are discussed.

3.1   SOI Technology

3.1.1   Mechanisms of Charge Collection

As a high-energy ion passes through a material, it loses energy by excitation and ionization of atoms, creating a very high density electron-hole plasma along the path of the ion [2]. The amount of energy that an ion deposits per unit depth in a material is given by its stopping power. The mass-stopping power is defined as the linear energy transfer, LET, and is given by

$$LET = \frac{1}{\rho} \frac{dE}{dx} \tag{1}$$

where ρ is the density of the material and $\frac{dE}{dx}$ is energy loss in the material per unit path length. LET has the units MeV-cm^2/mg. The integral of LET over path length gives the total deposited energy. Figure 9 [2] is a plot of stopping power (LET) for 2.5-MeV helium ions as a function of depth in silicon. The point of maximum stopping power is called the Bragg peak. The LET for a

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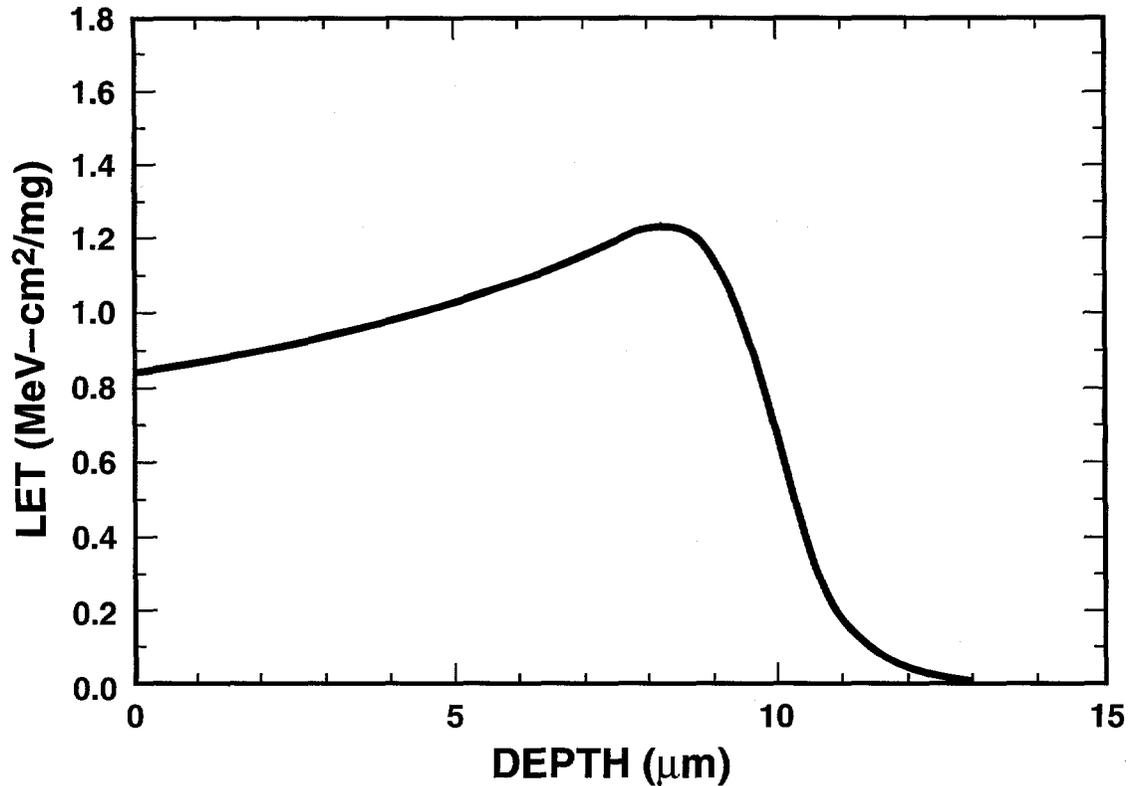
Figure 9: Stopping power (LET) versus depth for a 2.5 MeV helium ion in silicon. (After Ref. 2)

given ion depends on the target material and energy. Experimental and theoretical values of stopping power for most ions in several materials have been published by Northcliffe and Schilling [24] and Ziegler [25]. Stopping powers can be calculated for silicon, germanium, GaAs, and many compounds using the TRIM code [26] on most IBM compatible personal computers [2].

Protons cannot directly cause single-event upsets in most present-day silicon circuits. Instead, protons induce upset by dislodging atoms from their lattice sites or through nuclear interactions with lattice atoms. Because the resulting secondary particles (e.g., alpha particles or displaced atoms) have higher stopping powers, i.e., LET, the secondary particles can cause sufficient ionization to induce single-event upsets.

For single-event effects, an important parameter is the charge deposited in the material. The total deposited charge per unit path length in a particle track, Q_l, can be calculated from [27]

$$Q_l = \frac{1.6 \times 10^{-2} \cdot LET \cdot \rho}{E_p \cdot \cos\theta},$$ (2)
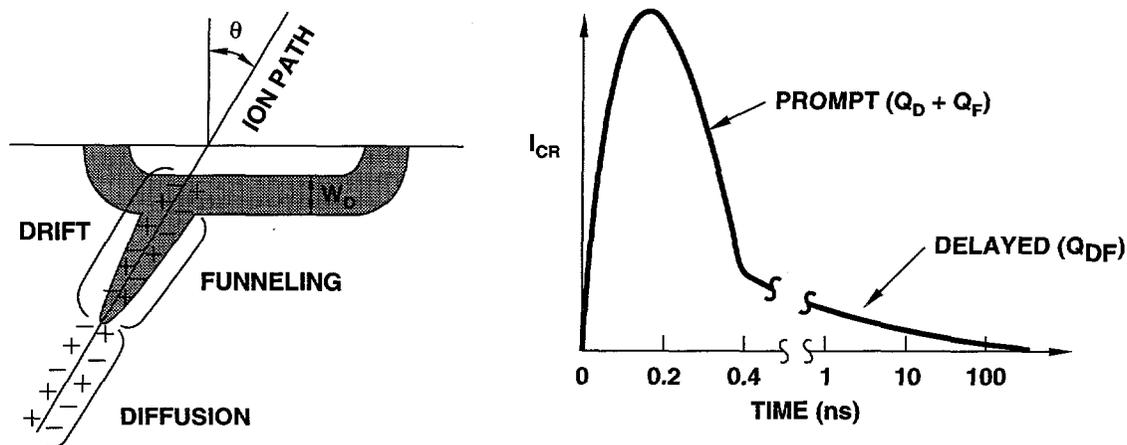
Figure 10: Schematic diagram and time dependence for charge collection by drift, funneling, and diffusion. (After Ref. 2)

where E_p is the electron-hole pair ionization energy (minimum energy required to create an electron-hole pair) given in units of eV, LET is in units of MeV-cm^2/mg, ρ is the density of the material in units of g/cm^3, θ is the angle of incidence, and Q_l is given in the units of pC/μm. For silicon, $E_p = 3.6$ eV and $\rho = 2.32$ g/cm^3. Thus, for a LET of 50-MeV-cm^2/mg, the charge deposited is approximately 0.5 pC/μm.

Immediately after an ion passes through a p-n junction, charge is collected at the electrodes by drift of carriers from within the depletion region. The drift of carriers to the electrodes occurs within hundreds of picoseconds after a heavy-ion strike. This is depicted as Q_D in Fig. 10 [2].

Diffusion of carriers to the edge of the junction depletion region contributes a another component to the collected charge. The diffusion of carriers takes much longer (up to hundreds of nanoseconds to microseconds) than the drift component. The diffusion of carriers is noted as Q_{DF} in Figure 10.

After a heavy-ion strike, only those carriers generated within the top silicon region will be collected by drift or diffusion. Because of the normally thin body layers used for SOI circuits, the number of carriers collected will be significantly less than for bulk-silicon circuits. Funneling effects (discussed below) that significantly increase the susceptibility of bulk-silicon circuits to SEU do not occur for SOI circuits. The reduced charge collection volume and the absence of funneling effects will significantly reduce the single-event error upset cross section for SOI ICs. This is the primary reason for the improved SEU hardness of SOI circuits compared to bulk-silicon circuits. To first order, the reduction of collection volume will not significantly impact the critical charge which is affected more by circuit design.

The SEU sensitivity of an IC is normally characterized by measuring the upset cross section versus ion LET. The upset cross section has units of cm^2. LET is varied by using different ions and by varying the angle of the incident ion beam normal to the device surface. By

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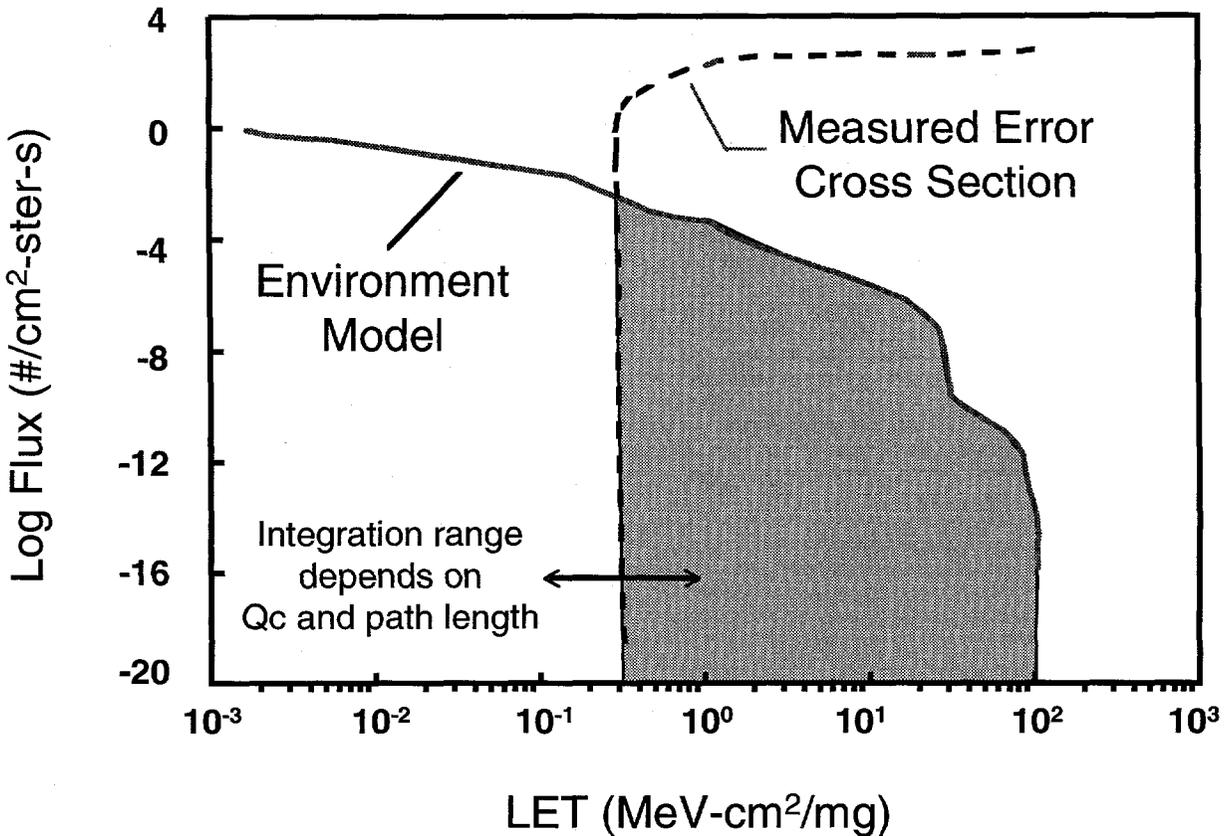
Figure 11: Measured upset error cross section and particle flux for a hypothetical space environment. The error rate is determined by convolving the environment model with the error cross section. (After Ref. 2)

varying the angle, more or less charge can be deposited per unit path length into the semiconductor. The upset cross section curve can be roughly characterized by an LET threshold and a saturation upset cross section. To determine the number of circuit errors that will result for a space mission, one must convolve the upset cross section curve with the heavy-ion versus LET spectrum for the orbit. This is illustrated in Fig. 11 [2]. The error rate (in units of errors/bit-day) is calculated by convolving the flux of particles in the environment with the upset cross section curve. It is equal to the shaded area in Fig. 11. As is apparent in the figure, an increase in LET threshold and/or a decrease in the upset saturation cross section will lead to a decrease in the error rate. The heavy-ion spectrum can be estimated using several different models. To compare device response, the Adams' 10% worst-case environment is often used as a reference.

One attribute that limits the SEU hardness of SOI technology is the bipolar effect. This effect is due to the floating body (not referenced to a specific potential) of SOI transistors. A bipolar effect occurs in SOI transistors as a heavy-ion strike injects majority carriers in the body region of a transistor [28]. Figure 12 is a schematic diagram of an SOI transistor with a body tie (discussed below) [28]. For this transistor layout, the injected charge must either recombine, be swept to the source junction, contribute to MOS channel charge, or exit through the distributed resistance of the body material to the source tie [28]. The latter current can lower the source-to-body potential causing minority-carrier injection from the source to the body where the injected

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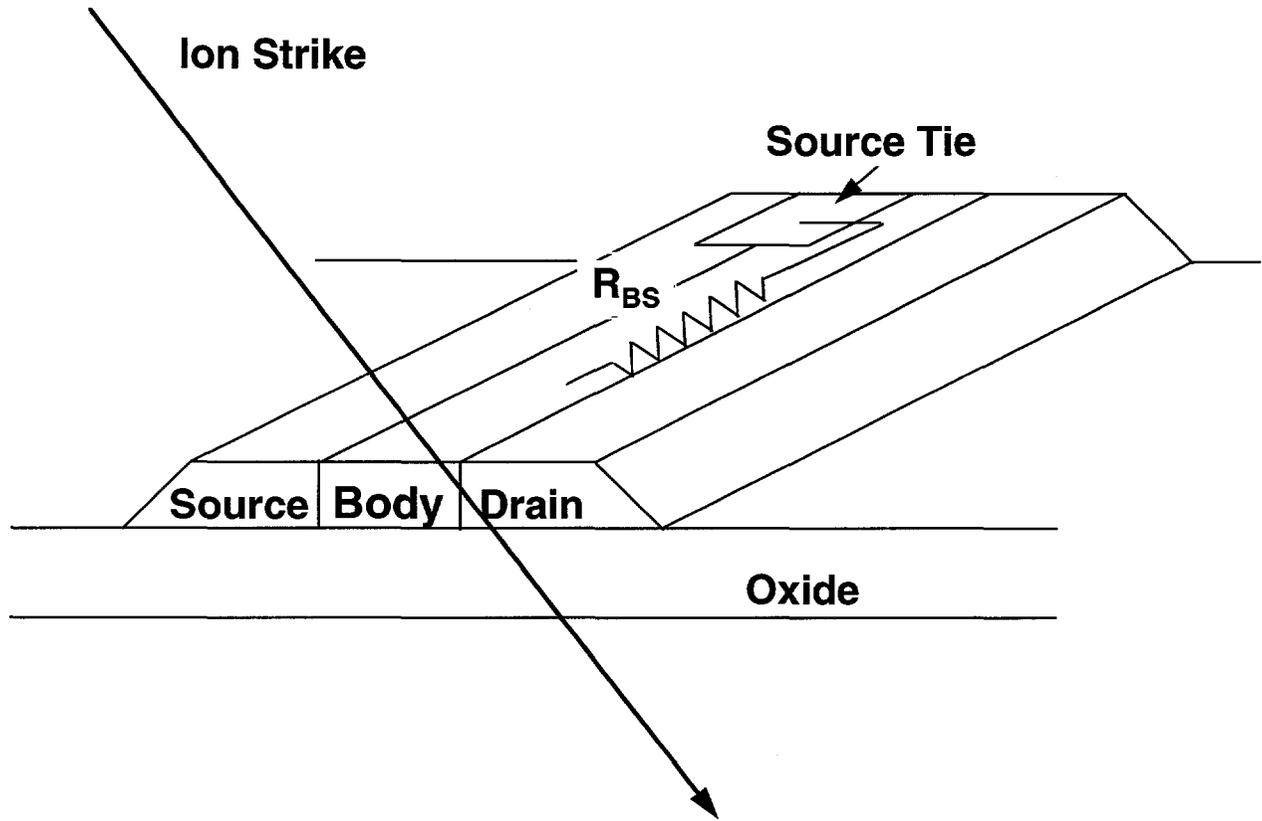
Figure 12: Schematic diagram of an SOI transistor with a body tie. (After Ref. 28)

carriers can be collected at the drain. This is analogous to minority carrier injection from the emitter-to-base region in a bipolar junction transistor. The bipolar current adds to (enhances) the charge collected by the normal drift of carriers generated by the ion strike. Once collected, the charge can lead to circuit upset.

The total charge collected at the drain, Q_D, including that contributed from the bipolar effect is equal to [29],

$$Q_D = (1 + \beta) \cdot Q_1 \cdot t_{Si}, \tag{3}$$

where β is the effective charge gain due to the bipolar effect, Q_1 is the charge deposited by the ion per unit path length given by Eq. 2, and t_{Si} is the thickness of the top silicon layer. The dependencies of β on gate length, L, and width, Z, are given by [29],

$$\beta \propto \frac{1}{L}, \tag{4}$$

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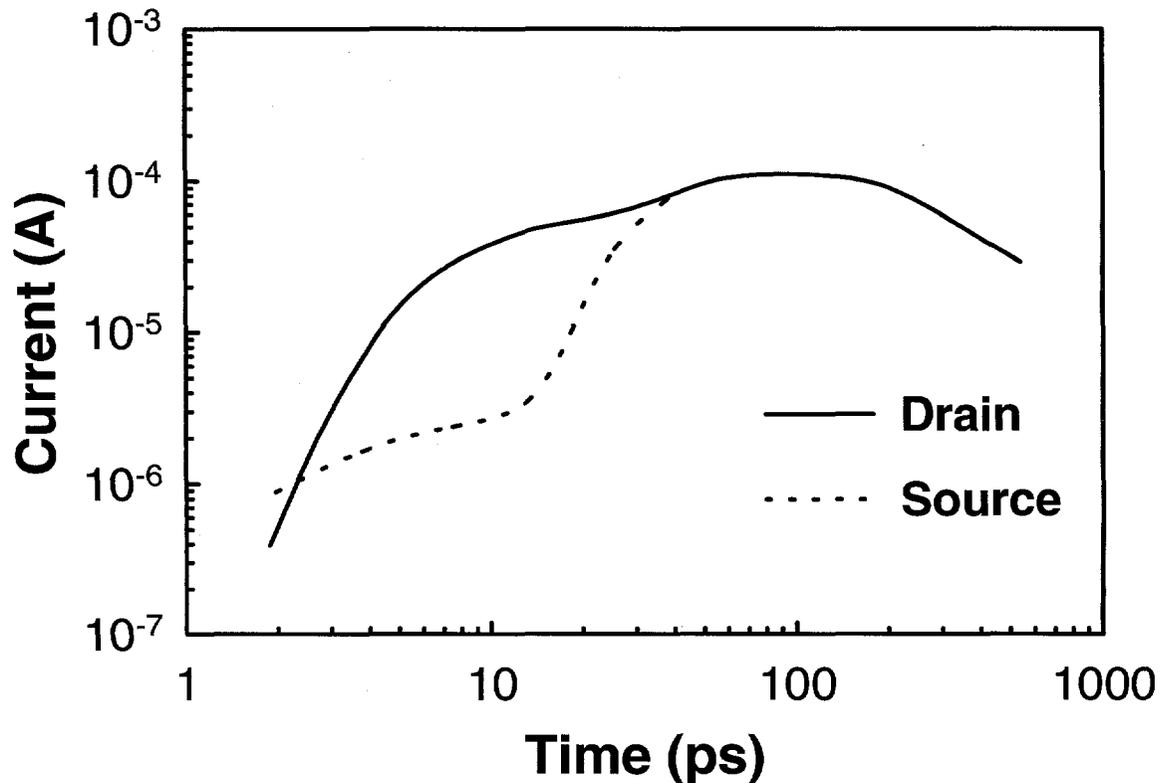
Figure 13: Simulated drain and source currents after a heavy-ion strike. The large increase in current at the source is due to the bipolar effect. (After Ref. 29)

and

$$\beta \propto (1 + 0.65 \cdot Z). \tag{5}$$

As noted from Eqs. 4 and 5, the bipolar gain increases as gate length decreases and gate width increases. Thus, as gate dimensions continue to decrease, the significance of the bipolar effect on SEU sensitivity will continue to increase. The bipolar effect also increases with decreasing doping concentration in the body [30].

The time dependence of the collected current has been modeled using 3D simulations [29] (using TMA's DIVINCI device simulator). Results of the simulations for a heavy-ion strike with a LET of 30 MeV/mg/cm^2 are shown in Fig. 13 [29]. This figure is a plot of the total collected current at the drain and the current injected at the source versus time. The initial increase in the collected drain current for times less than approximately 10 ps is due to the normal drift and diffusion of carriers generated directly by the heavy-ion strike. For times greater than ~10 ps, the current injected at the source begins to increase due to the bipolar effect causing

a corresponding increase in the current collected at the drain. The current due to the bipolar effect reaches a peak in approximately 100 ps.

A bipolar effect occurs for both partially- and fully-depleted circuits. Monte Carlo simulations of 0.25-μm fully-depleted transistor SOI circuits have suggested that the bipolar effect arises as excess electrons and holes are produced by a heavy-ion strike [31] in NMOS transistors in the off state. According to these simulations, the excess electrons are quickly collected at the drain and source contacts. The excess holes tend to accumulate in the channel initiating a bipolar transistor mechanism and electron flow from source to drain. The electron flow can discharge the output capacitance and cause transient upset.

The bipolar effect will cause a decrease in LET threshold and an increase in upset cross section. Despite the increase in SEU sensitivity due to the bipolar effect, fully-depleted 0.5-μm transistor SOI 256k SRAMs have been fabricated using commercial designs (without the use feedback resistors, body ties, or other design hardening techniques) with extremely good SEU immunity [32]. For these devices the LET threshold was determined to be 80 MeV/mg/cm^2 with an associated bit-error rate of 5×10^{-12} errors/bit-day assuming an Adams' 10% worst-case environment. These results indicate that for at least these gate lengths, exceptional SEU immunity can be obtained from fully-depleted SOI circuits without the use of performance degrading design hardening techniques.

3.1.2 Circuit Effects

In a digital circuit, an upset will occur if sufficient charge is collected at a node to change the logic state at the node and the node remains in the disturbed state long enough for the disturbance to propagate through the circuit. Therefore, the likelihood of an upset depends on both the amount and duration of collected charge. The minimum charge required to upset a memory bit is referred to as the critical charge. Critical charge decreases with feature size and is highly circuit dependent. Figure 14 is a plot of critical charge, Q_C, versus feature size, L, (e.g., gate length) for several technologies for a given circuit type [33]. As noted in Fig. 14, the critical charge does not change strongly with technology *including SOI*. This does not imply that SOI and bulk CMOS devices are equally susceptible to SEU. Because less charge is collected in SOI devices than for bulk-silicon devices, much more charge must be deposited in SOI devices in order to reach the critical charge. For the data of Fig. 14, the dependence of critical charge on feature size is given by,

$$Q_C = 0.023 \times L^2. \tag{6}$$

Thus for the circuits of Fig. 14, the critical charge is 6 fC for a feature size of 0.5 μm. Extrapolating the data to lower feature sizes, the critical charge is 0.5 fC for a feature size of 0.15 μm. *For the feature size of 0.15 μm, the critical charge can result from only 3,000 electrons.* Unless steps are taken to harden future technologies, they will be extremely sensitive
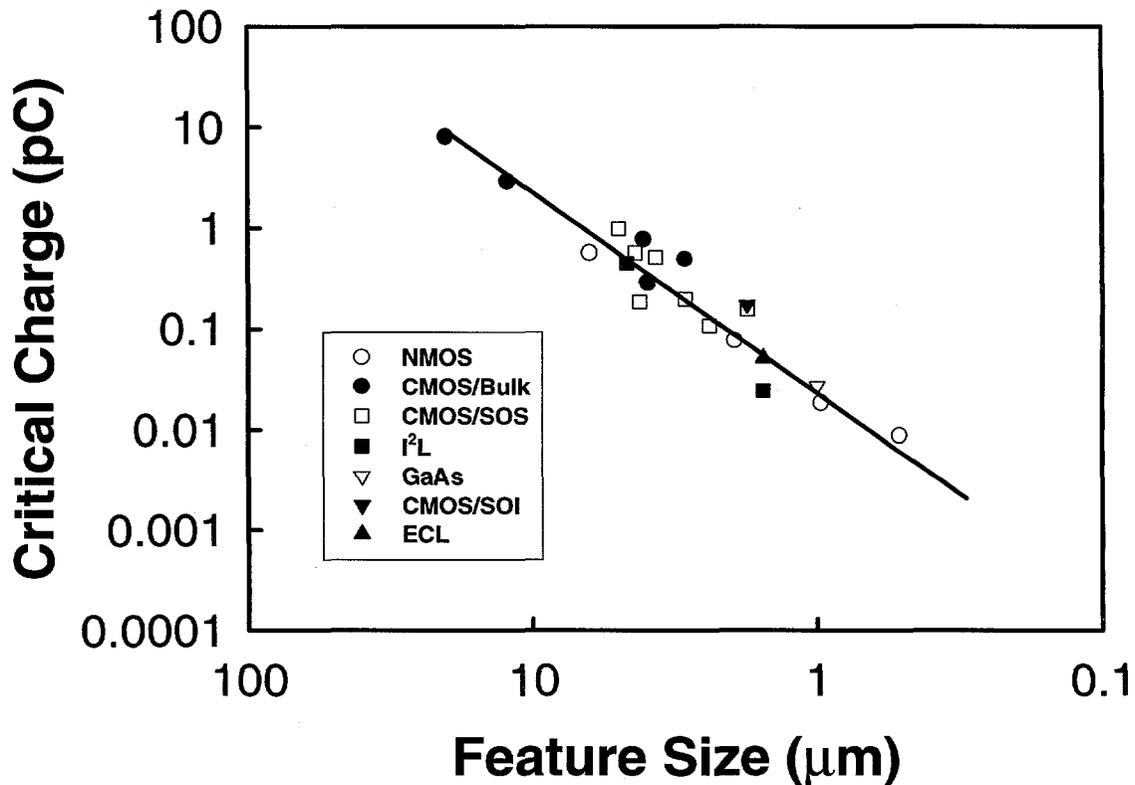
Figure 14: Critical charge versus feature size for several different technologies. (After Ref. 33)

to SEU in both space due to cosmic rays and on earth due to cosmic rays that penetrate the atmosphere and to neutrons created by cosmic ray interaction in the atmosphere.

For a DRAM, errors can result if information stored on a storage node (often a capacitor) is lost. The critical charge is the difference between the amount of charge stored on the node and the minimum charge that the sense amplifiers require to reliably read the stored data. Maximum charge collection will occur at the highest potential across a p-n junction. The depletion width and is proportional to the square root of voltage [2]. Consequently, nodes in a "1" state are most vulnerable to upset. Thus, an upset will occur if sufficient electrons are collected at the storage node to change the logic state from a "1" to a "0." No upset will occur for nodes at low potential (i.e., "0" logic state) [2]. Because DRAMs directly manipulate stored charge at a circuit node and are not dependent on the propagation of charge through a circuit, dynamic circuits are very susceptible to SEU. As device dimensions shrink and stored charge is reduced for normal operation, DRAMs will become more susceptible to SEU.
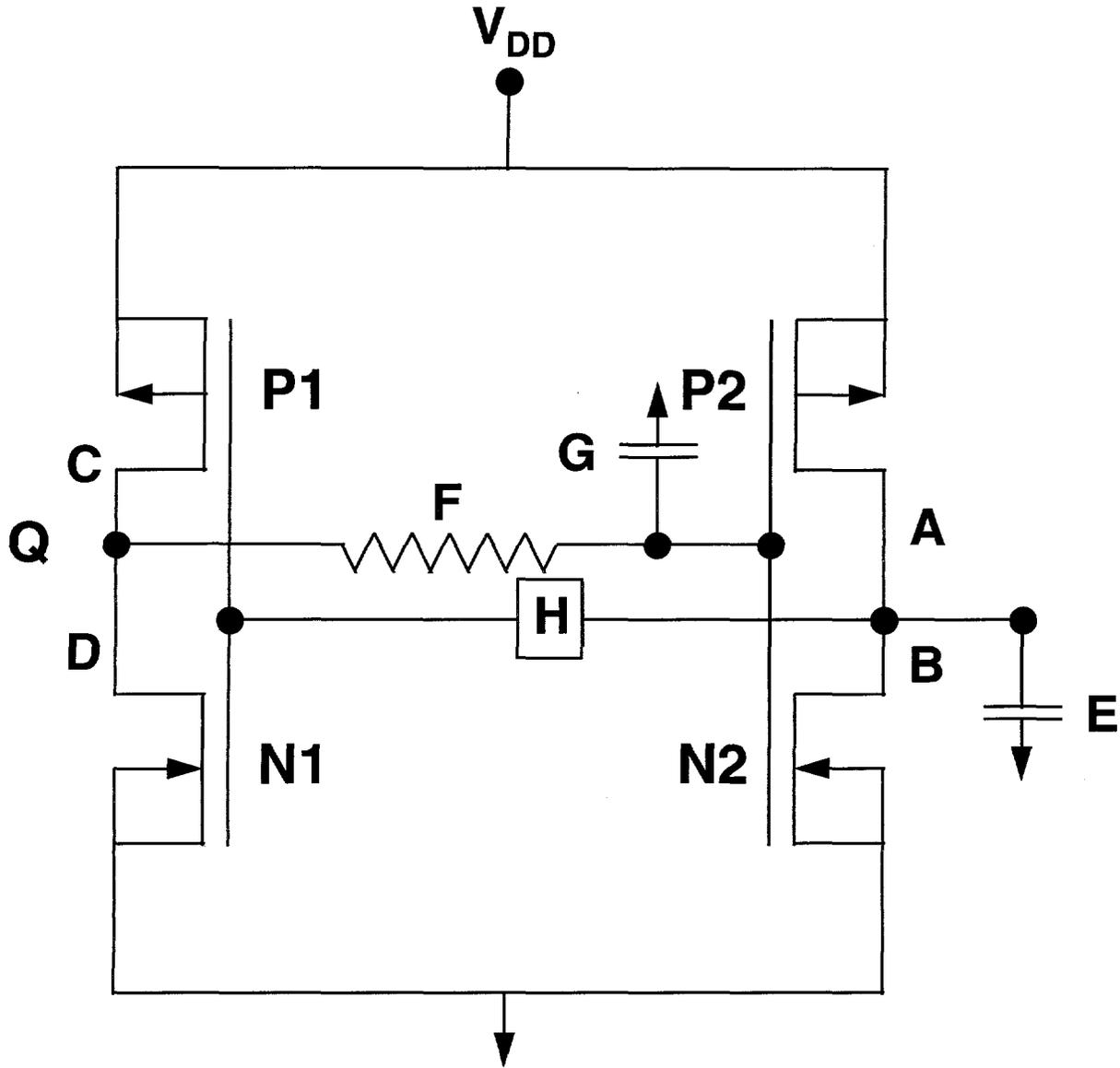
Figure 15: Six-transistor SRAM cell. (After Ref. 34)

For a static memory, whether or not an upset will occur will depend on whether or not excess charge at the struck node can be removed before the opposing inverter of the memory cell changes state. Figure 15 is a schematic diagram of a six-transistor SRAM cell [34]. Each series connection of n- and p-channel transistors forms an inverter whose input is the common gate, and whose output is the common drain. The output of each inverter is coupled to the input of the other inverter forming a bi-stable memory element. One scenario leading to an upset could be as follows [2]: If an ion strike occurs at the off-biased drain of transistor P1, a current spike will be observed at the storage node, Q, of the inverters formed by transistors N1 and P1. If charge is collected by the drain of P1 faster than it is removed by the unstruck n-channel transistor N1 (called the restoring transistor), the node voltage will rise to a diode voltage drop above V_{DD}.
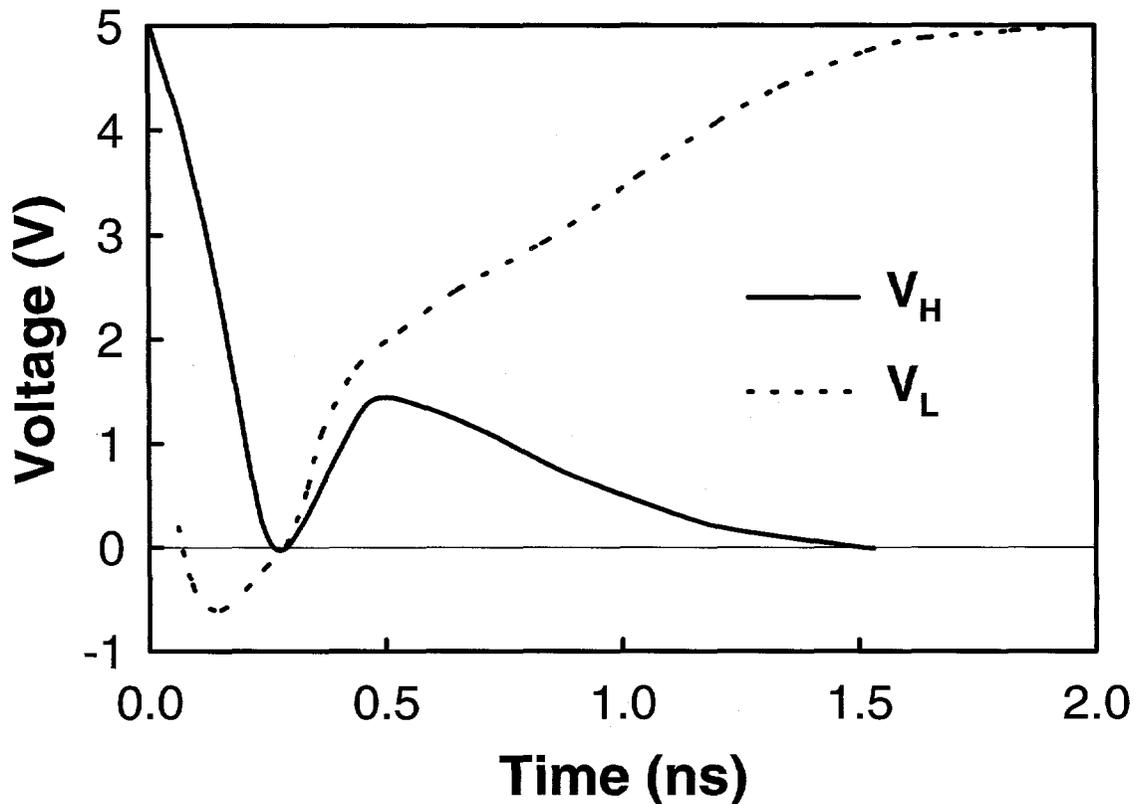
Figure 16: Simulated output high and low voltages in a six-transistor SRAM cell after a heavy-ion strike. (After Ref. 30)

Whether or not an upset occurs depends on the competing processes of removing excess charge at the struck node, and changing the state of the opposing inverter of the memory cell. The time required for the struck node to recover to one-half the voltage swing at the node is defined as the recovery time, t_R. The time required to switch the opposing inverter formed by transistors N2 and P2 is defined as the decoupling time, t_{DC}. If t_R is greater than t_{DC}, upset will occur. Because the maximum charge collection occurs at the highest potential across a p-n junction, the off-biased drain regions (biased at V_{DD}) of an SRAM memory cell are the most sensitive nodes to heavy-ion induced upset [2].

The time dependence of the output high, V_H, and low, V_L, voltage levels in a six-transistor memory cell (Fig. 16) have been modeled using a SPICE compatible electrical simulator [29]. Figure 16 shows the transient voltages for a heavy-ion strike at the drain of an SOI NMOS transistor. An upset will occur when $V_H \leq V_L$.

Figure 17 is a plot of the charge deposited by the ion (not including gain enhancement), Q_{ion}, necessary to upset a 6-T SRAM cell versus carrier lifetime as estimated by SPICE
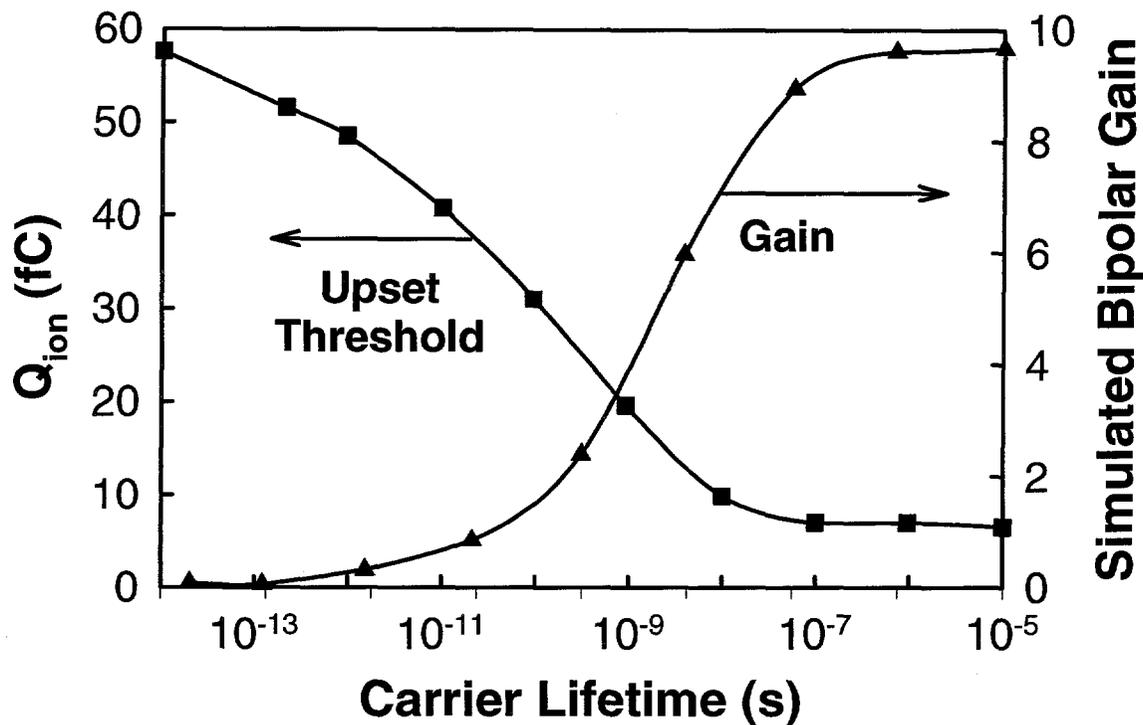
Figure 17: Simulated critical deposited charge by an ion in order to cause upset and bipolar gain versus carrier lifetime. Note that as the bipolar gain increases the critical ion charge decreases. (After Ref. 35)

simulations [35]. Note that, for bipolar charge enhancement, Q_{ion} is not equal to the critical charge. Also plotted in Fig. 17 is the bipolar gain for $V_{BE} = 1$ V. For carrier lifetimes above 10 ns, the gain is relatively insensitive to carrier lifetime, but as the lifetime decreases, the gain rapidly decreases. As the bipolar gain decreases, more charge must be deposited by the ion in order to cause circuit upset.

3.1.3   SEU Hardening

Circuits can be hardened to SEU at several different levels using many different techniques. For instance circuits can be hardened at the system, circuit, and transistor level. There are two general methods for hardening circuits at the circuit and/or transistor level: 1) approaches reducing the amount charge collection from a given hit, requiring a larger charge to be deposited before upset will occur, and 2) approaches increasing the critical charge of sensitive nodes of a circuit, thereby requiring a larger charge to be collected before the circuit will experience upset [34]. SOI technology is an example of an approach that reduces the amount of charge collection.
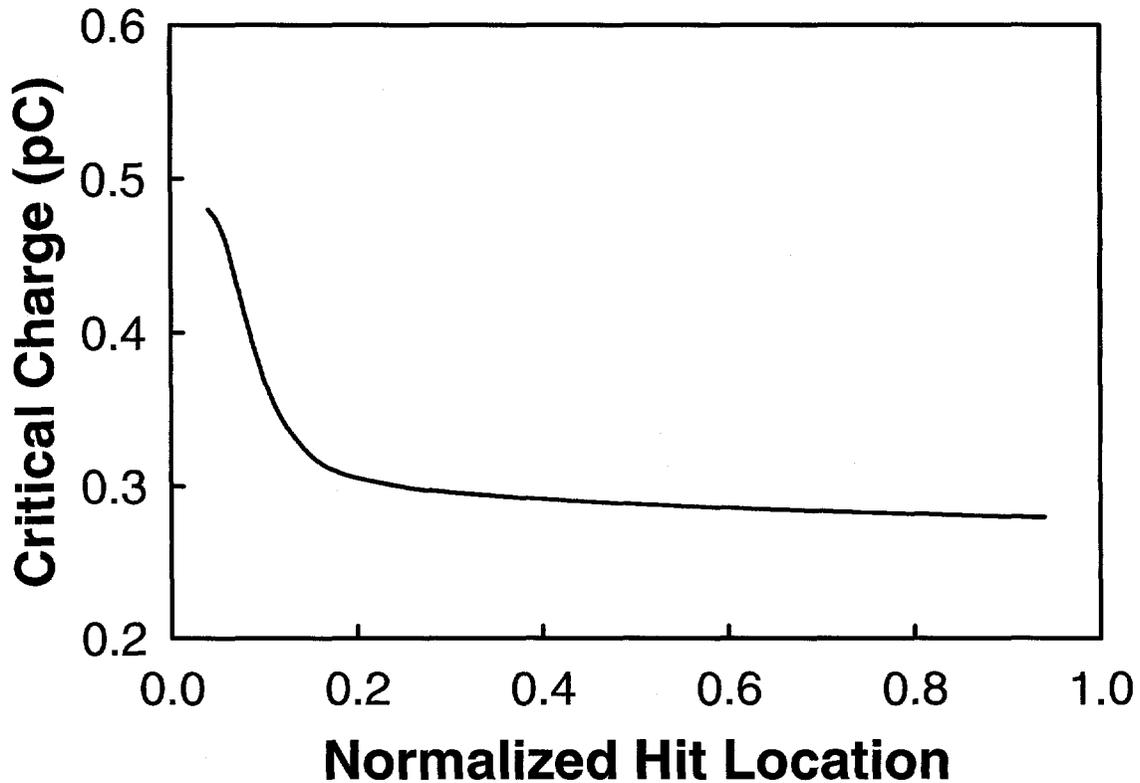
Figure 18: Simulated critical charge versus location of the heavy-ion strike relative to location along the width of the transistor. "1.0" corresponds to the transistor width. The body tie is located at "0". (After Ref. 28)

Approaches used to reduce the critical charge of sensitive nodes of a circuit are most important for bulk-silicon circuits and are discussed in detail in Section 3.2.2 below. One technique used to increase the SEU hardness of SOI circuits is the use of feedback resistors and/or capacitors.

Improvements in SEU hardness can also be obtained by reducing the bipolar gain effect. The most common technique used for reducing the bipolar effect in partially-depleted transistor circuits is the use of body ties. Although body ties can suppress the bipolar effect, they cannot completely eliminate it. The ability of body ties to suppress the bipolar effect depends strongly on the location of the body tie in relation to the ion strike. The farther the ion strike is from the body tie, the larger the effect of the parasitic bipolar transistor [28,36,37]. Figure 18 is a plot of the critical charge versus normalized location ("1" corresponds to the transistor width) of the ion strike simulated by varying the distributed body resistance [28]. For ion strikes close to the body tie, the critical charge is a maximum (least sensitive to SEU) and decreases rapidly as the location of the ion strike gets father from the body tie (most sensitive to SEU).
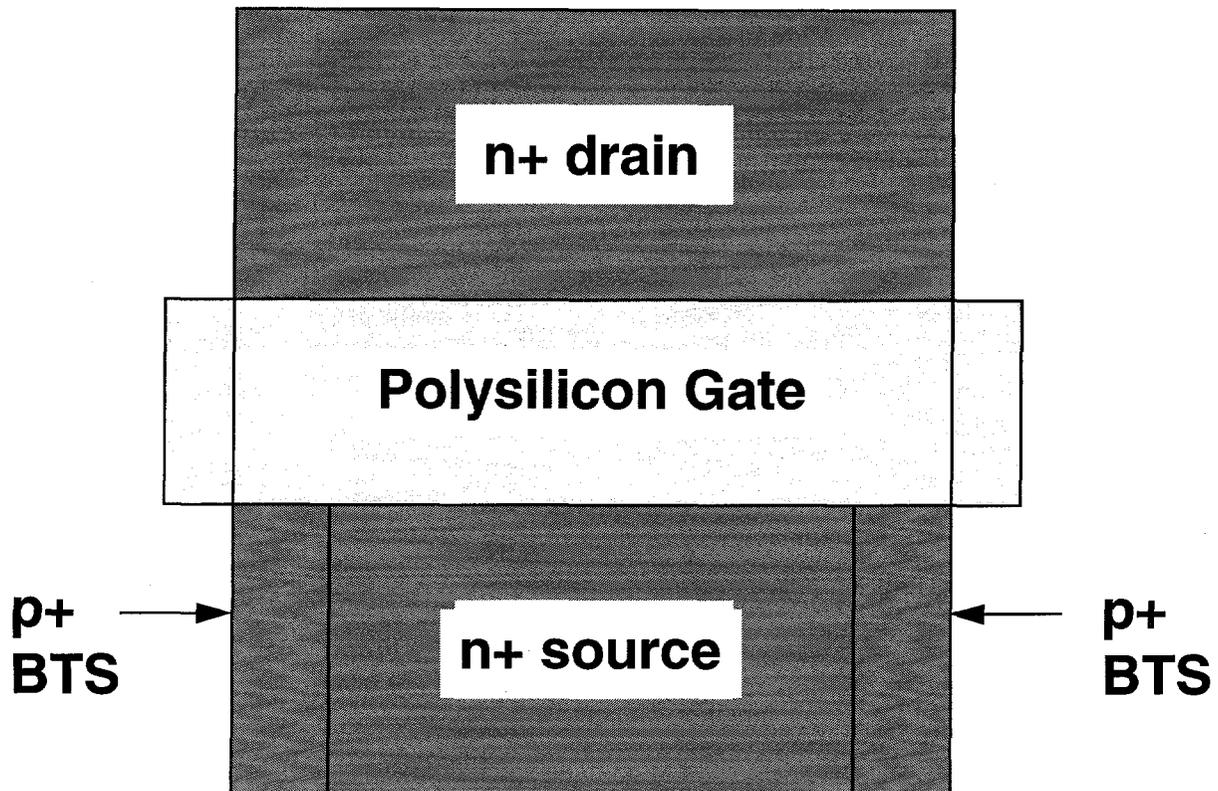
Figure 19: Example of a body tie used for SEU hardening. (After Ref. 36)

An example of a body-tie used for the design of a partially-depleted 256k SRAM circuit (1-μm feature size) is shown in Fig. 19 for an n-channel transistor [36]. For the example shown, the body tie is a p+ source/drain diffusion that contacts the p- body region. A silicide process connects the p+ body tie to the n+ source. The body tie helps to reduce the bipolar effect, but because of distributed series resistance from the contact to portions of the body node cannot completely eliminate it. Figure 20 is a plot of the upset cross section for a 32kx8 SRAM using body ties similar to that in Fig. 19 and using partially-depleted transistors [36]. This circuit also uses a gated resistor/transistor in the cross-coupling feedback circuit of the SRAM to provide both resistance and cross coupling (Miller) capacitance to obtain a high level of resistance to upset over a wide temperature range [36]. This feedback network provides good SEU protection, but does not severely degrade the memory write time (about 10% increase over the SRAM minimum write pulse time) or increase cell area [36]. Data are shown for temperatures of 25 and 125°C. The upset cross section did not saturate for the highest LET (163 MeV/mg/cm^2) examined. Assuming an Adams' 10% worst-case environment, the error rate for this IC is estimated to be between 3×10^{-11} and 5.1×10^{-12} errors/bit-day.

Another technique that can be used for reducing the bipolar effect is to reduce the carrier lifetime in the channel region [30,35,38]. Germanium implantation has been suggested as a method for hardening fully-depleted transistors without significantly affecting the front-channel mobility (less than 4% degradation) [38]. Silicon interstitials are generated as the front-channel is implanted with germanium at energies between 120 and 150 keV. Substantial strain is created
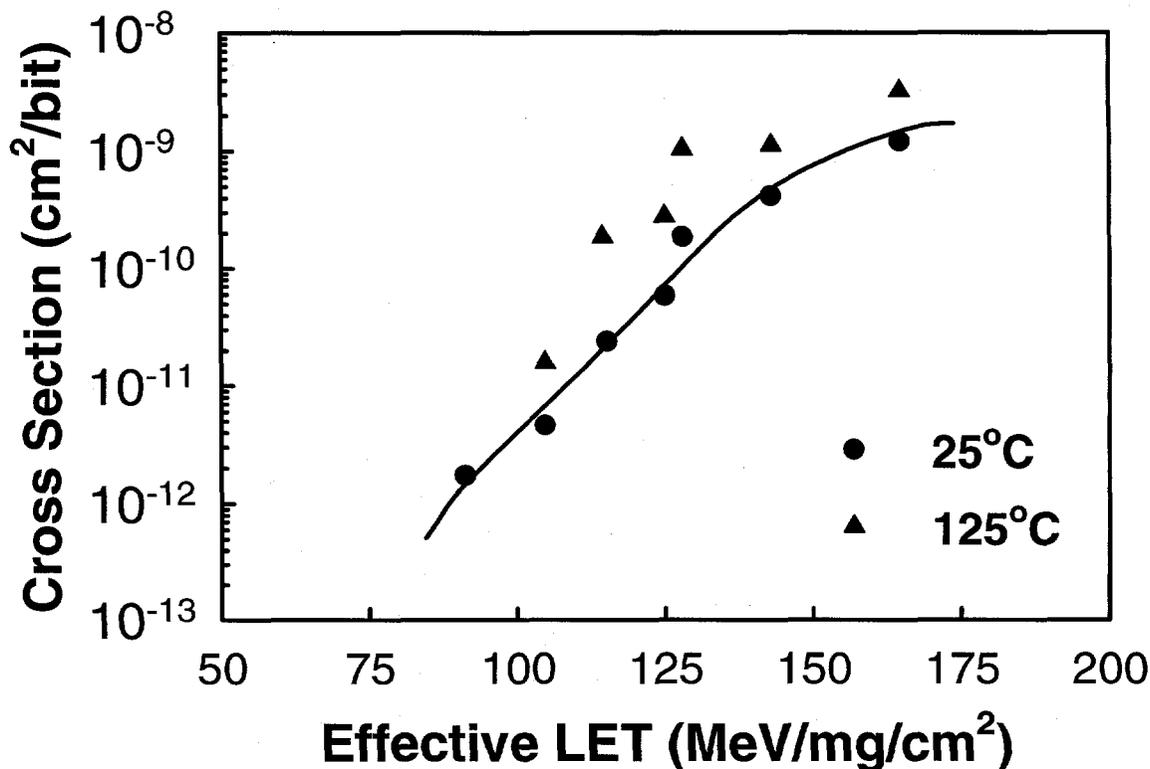
Figure 20: Upset cross section for a 32kx8 SRAM with partially-depleted transistors and body ties for SEU hardening. (After Ref. 36)

resulting in threading dislocations in the silicon between the germanium-implant end-of-range and the buried oxide. The germanium dopants and silicon structural defects act as recombination centers that will reduce the minority carrier lifetime and thus, reduce the bipolar effect. In addition, they also reduce the back-channel mobility and increase the back-channel threshold voltage by pinning the back-channel Fermi level. This will help to suppress radiation-induced back-channel leakage current [38]. For some transistors, the parasitic bipolar gain has been reduced from ~35 to less than 0.7 by implanting with germanium [38].

3.1.4 Hard Errors

Two mechanisms that can cause hard errors in SOI circuits are single-event snapback and single-event gate rupture. Because of the absence of four layer n-p-n-p paths and multiple layer structures, SOI ICs are immune to single-event latchup and burnout.

3.1.4.1 Single-Event Snapback

Snapback (also referred to as single-transistor latch) can occur for partially-depleted SOI transistor circuits [39-41] and is enhanced by the bipolar effect. A steady-state concentration of holes can exist in the body that keeps the source-body (emitter-base) junction forward biased [39]. The hole concentration will depend on the amount of charge generated by impact ionization at the drain and the number that recombine at the source junction. Single-transistor latch occurs only for ON transistors [29]. In the ON condition electron-hole pairs are generated by impact ionization at the drain junction. Holes drift through the body and the source-to-body potential. After an ion strike, additional electrons transport to the drain, further increasing the drain current. This in turn causes more holes to be generated by impact ionization which can transport to the source and further turn on the source-to-body junction. As more electrons are injected, positive feedback is established, and the transistor latches [29]. Snapback has also been predicted for fully-depleted transistor circuits [40], but has not yet been observed [39].

3.1.4.2 Single-Event Gate Rupture

A single-event gate rupture can occur as a single heavy ion passes through a gate oxide. SEGR occurs only at high oxide electric fields, such as those during a write or clear operation in a nonvolatile SRAM or E^2PROM [2,42,43]. It was first observed [42,43] for metal nitride oxide semiconductor (MNOS) dielectrics used for memory applications. In later works, SEGR was observed in power MOSFETs and MOS transistors [44].

SEGR is caused by the combination of the applied electric field and the energy deposited by the ion [44]. As an ion passes through a gate oxide it forms a highly conducting plasma path between the silicon substrate and the gate contact [2,43,44]. With an electric field across the oxide, charge will flow along the plasma path depositing energy in the oxide. If the energy is high enough, it can cause localized heating of the dielectric and potentially a thermal runaway condition. If thermal runaway occurs, the local temperatures along the plasma will be high enough to cause thermal diffusion of the gate material, cause the dielectric to melt, and evaporate overlying conductive materials [2,44]. The resistance of the initial ion track is inversely proportional to the ion LET. If the LET is increased, resistance is lowered and the required voltage across the device to sustain conduction is reduced [44].

For thermal SiO_2 oxides with the incident ion normal to the surface, the critical electric field, E_{cr}, for SEGR is given by [44,45]

$$E_{cr} = \frac{41}{(LET)^{1/2}} x10^6 \ V \ / \ cm. \tag{7}$$

For a 180 MeV Ge ion with an LET of 36.8 MeV-cm^2/mg, this gives a critical electric field of approximately 6.7 MV/cm. Typical intrinsic breakdown electric field strengths for a thermal gate oxide are in the range of 10 MV/cm [45]. Thus, the critical electric field for SEGR is roughly

67% of the intrinsic breakdown electric field strength under these conditions. In addition to depending on the oxide electric field and LET, the failure threshold also depends on the incident angle of the ion strike.

For a memory transistor, the probability of a SEGR will depend on the time that the device is in a write, clear, or other high-electric field mode of operation. For a number of nonvolatile memory applications this may be only a small percentage of the total operation time. Clearly the probability of a SEGR is highly dependent on the system application.

3.2 Bulk-Silicon Technology

Charge is collected by both drift and diffusion in bulk-silicon devices similar to that for SOI devices. However, SOI ICs are in general significantly harder to SEU than bulk-silicon ICs because of the reduced collection volume and the absence of funneling effects. In this section, we review SEU effects in bulk-silicon technology.

3.2.1 Mechanisms for Charge Collection

For bulk-silicon devices, the amount of charge that is collected by drift of carriers within the depletion region can be greatly enhanced by *field funneling* (noted as Q_F in Fig. 10). Funneling was first proposed by Hsieh, et al. [46,47], in 1981. The density of the electron-hole plasma (10^{18} to 10^{21} cm^{-3}) created by the ion strike is considerably greater than the doping concentration of typical p-n junctions [48]. The high concentrations of electrons and holes in the plasma will distort the original depletion region of the junction into a cylinder which follows the path of the ion [2,46-49]. As a consequence, the extended junction field region creates a *funnel region* that extends down into the substrate as depicted in Fig. 10 [2,46-50]. The electric fields within the funnel region will cause carriers to be collected rapidly by drift to the electrodes. The funnel will exist as long as the concentration of electron-hole pairs in the plasma created by the ion strike is large compared to the doping concentration of the substrate. The temporal peak of collected current from the drift of carriers by field funneling corresponds roughly to the dielectric relaxation time [49]. The dielectric relaxation time, τ_D, is the characteristic time it takes for a solid to respond to charge imbalance [51]. It is given by $\tau_D = \varepsilon/\sigma$, where ε is the permittivity and σ is the conductivity of the material. For silicon substrates with a doping concentration of 10^{15} cm^{-3}, τ_D is approximately 14 ps, and the potential spreading of the funnel reaches a maximum in approximately 25 ps [49]. For silicon devices, the amount of charge that is collected by drift is greatly enhanced by the funnel region, increasing the sensitivity of silicon ICs to single-event upset.

A mechanism that has been suggested to result in enhanced charge collection is the ion shunt mechanism [52-54]. This mechanism is applicable to silicon devices with multiple p-n structures (e.g., silicon bipolar and CMOS transistors). The ion-shunt mechanism is illustrated in Fig. 21 [53]. As depicted in Fig. 21, a heavy-ion passes through an n$^+$-p-n-n$^+$ junction and deposits charge along the ion track. The high density of charge created by the ion is initially
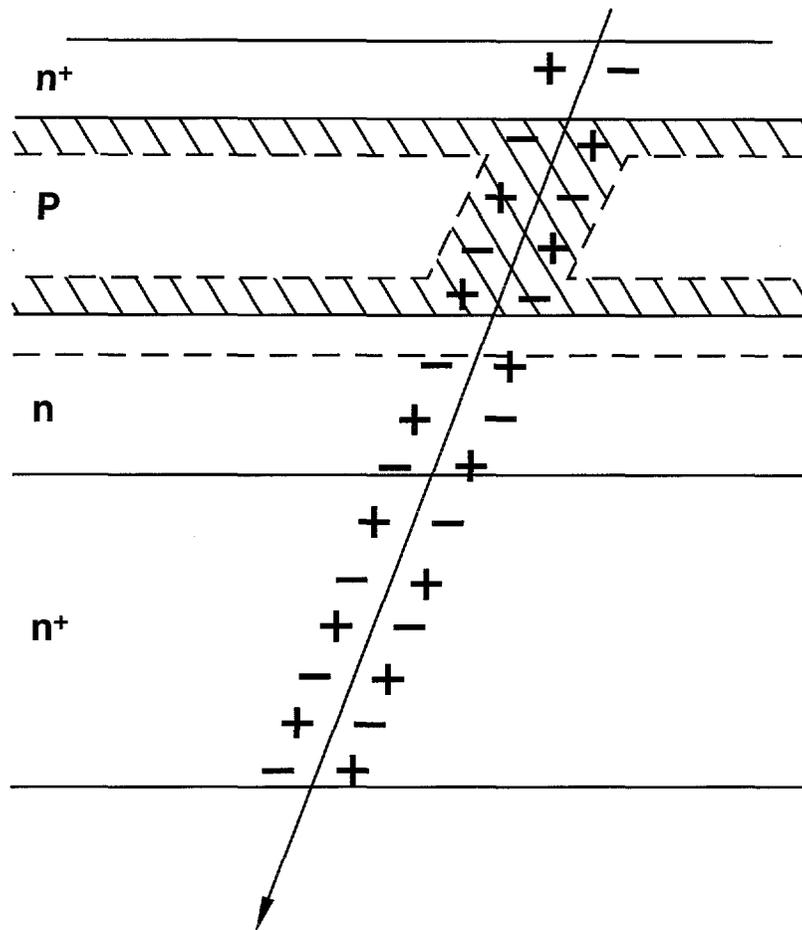
Figure 21: Schematic diagram of a heavy ion penetrating an n^+-p-n-n^+ junction. The cross-hatched regions correspond to the n-p junction depletion regions. (After Ref. 53)

considerably larger than the background concentration of the n and p layers. The charge deposited by the ion effectively shorts together the bottom and top n^+ layers. If a potential field exists between the electrodes, charge will flow between the n^+ layers and a single-event upset can result. Note that, for this mechanism to occur, the ion track must penetrate both n^+ regions. The amount of charge collected by the ion shunt mechanism will increase with the LET of the incident ion [54], and in some cases can be more than that deposited by the ion [54]. The effect of the ion-shunt mechanism on the single-event upset sensitivity will depend on the device structure and operating conditions.

3.2.2   SEU Hardening

To hardened bulk-silicon circuits to SEU, techniques that increase the critical charge of sensitive nodes are employed. All of these approaches result in some type of performance penalty. A table listing several types of approaches that have been suggested for hardening bulks-silicon circuits is given in Table 1 [34].

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Table 1: SEU hardening approaches for bulk-silicon ICs. (After Ref. **Error! Bookmark not defined.**)

Increase Critical Charge
Increase Nodal Capacitance
Transistor sizing
Doping concentration and profile
Added capacitors
Increase Feedback Time Constant
Feedback resistance
Capacitance
Decouple Nodes
Drain diodes
Circuit elements
Decrease Recovery Time Constant
Transistor sizing

A number of techniques are available for increasing the critical charge of sensitive nodes. Increasing the nodal capacitance at a critical circuit node will decrease the voltage swing ($\Delta V = \Delta Q/C$) by the collected charge, thereby making it less likely that the induced charge will lead to an upset. A simple technique for increasing the capacitance is to increase the area of transistor drains at sensitive nodes (e.g., points A, B, C, and D for the SRAM circuit of Fig. 15). This approach can cause some increase in circuit area and decrease in fabrication yield (fewer devices per wafer). Because of this, increasing the drain size is not a viable approach for high-density memories. Similar to other approaches that increase the area of a sensitive node, increasing the drain size will also increase the sensitive area of the circuit. However, in most cases the improvement in SEU hardness caused by the increase in critical charge outweighs the reduction in SEU hardness due to increased sensitive area.

Capacitance at sensitive nodes can also be increased by adding a capacitor directly to the node (e.g., point E for the SRAM circuit of Fig. 15) or to alter the doping concentration and/or profile at the junction area of sensitive drains. Both of these techniques could require a change in the baseline process used to fabricate the circuits and degrade the circuit performance. Adding a capacitor will also increase the circuit area.

One of the most popular approaches for increasing the critical charge is to increase the feedback time constant of a memory element by adding a resistor or capacitor in the feedback loop (e.g., at points F or G in the SRAM circuit of Fig. 15). This approach works by increasing the decoupling time by increasing the RC time constant of the feedback path between the storage node Q and the opposing inverter. In effect, by increasing the delay time, sufficient charge can be dissipated by the restoring transistor, decreasing the potential at the storage node, before the cell resets leading to an upset. This approach will affect circuit performance parameters (e.g., minimum write time for a memory). The resistance of the feedback resistor (normally formed by implanting a polysilicon connector) will decrease as temperature is increased. Therefore, increasing temperature will make the circuit less protected against SEU. Adding a feedback resistor may or may not affect circuit area depending on cell design and layout. In lieu of a feedback resistor, a capacitor inserted between the storage node and the opposite transistor can also be used to increase the RC time constant of the feedback path.

The effective critical charge may also be increased by decoupling the hit node from the feedback node in a memory element by inserting resistors in the drain legs of the inverters (e.g.,
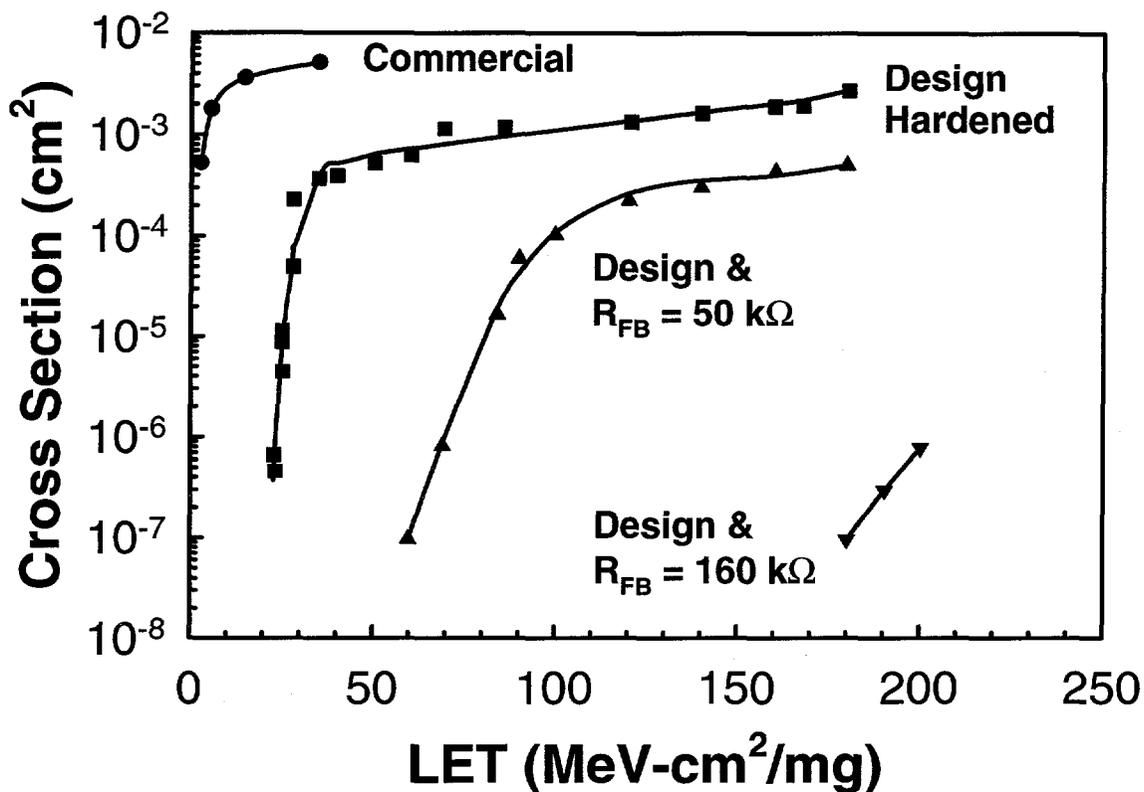
Figure 22: Error upset cross section curves for a commercial and several versions of a hardened microprocessor. (After Ref. 56)

at points A, B, C, and D in Fig. 15), inserting diodes in series with the drains (e.g., at points A and C in Fig. 15), or placing additional active circuit elements in the feedback path (e.g., at point H in Fig. 15). One final method for increasing the critical charge is to decrease the time constant for the hit node to recover to its original state. One simple method for accomplishing this is to increase the drive of transistors that restore the node to its pre-hit state by increasing the width of restoring transistors. This also increases the drain capacitance which further hardens the circuit element. The primary drawback to this approach is that it increases cell size.

To reduce the amount of charge collected at sensitive nodes of a circuit, techniques using different substrates have been suggested. Most of these techniques are aimed at reducing the amount of charge collected by charge funneling. One common technique is to use a thin epitaxial layer on a heavily doped substrate [48]. Other techniques such as increasing the doping concentration under junction areas by tailoring the doping profile or using a well structure (i.e., p-well or n-well) also have been proposed [55].

The improvements in SEU hardness that can be achieved using some of the approaches described above to increase the critical charge are illustrated in Fig. 22 [56]. This figure is a plot
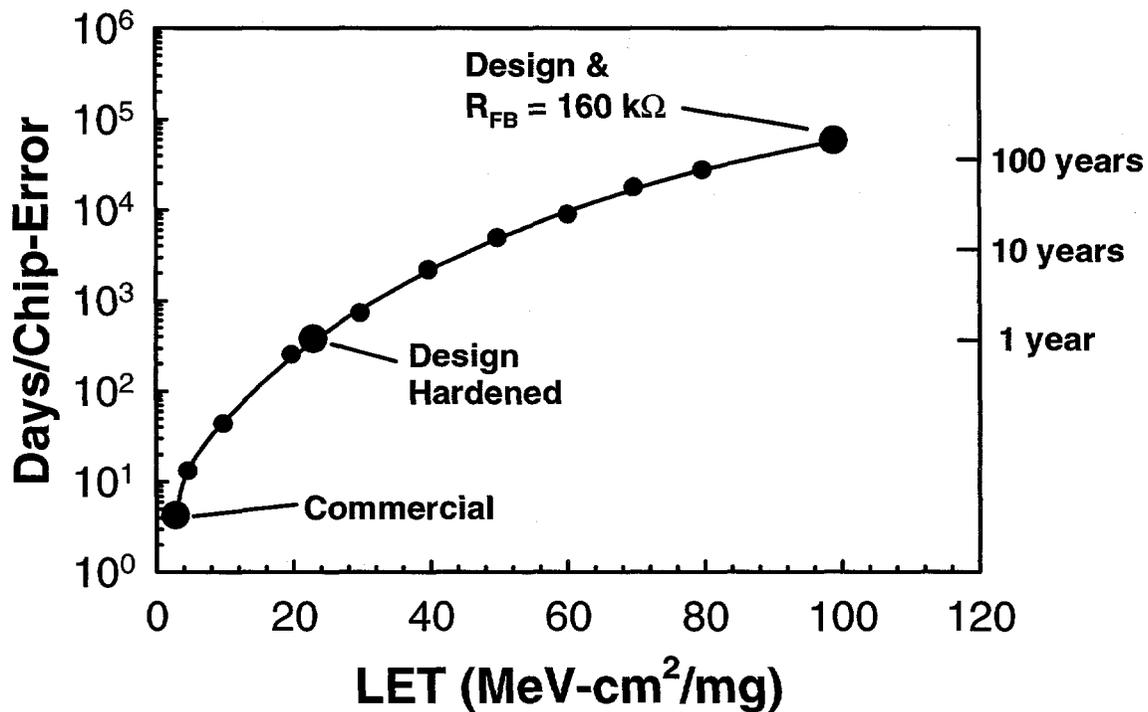
Figure 23: Error rates for the microprocessors of Figure 20. (After Ref. 56)

of the upset cross section versus LET for several versions of a 16-bit microprocessor (SA3300) and a commercial equivalent. The LET upset threshold is about 3 MeV-cm^2/mg for the commercial microprocessor. This is typical of commercial bulk-silicon ICs. Improvements in the SEU hardness were made by incorporating design enhancements and by using feedback resistors. The design enhancements consisted of using oversized transistors to increase the drive of transistor restoring nodes. By using oversized transistors, excess charge can more readily be removed before an upset occurs. All dynamic circuit elements requiring periodic refresh were replaced with CMOS circuit elements. The design enhancements (with a feedback resistance of 3.6 kΩ) resulted in an LET threshold of 23 MeV-cm^2/mg. Increasing the feedback resistance to 50 and 160 kΩ significantly increased the LET threshold The increase in LET threshold translates directly to a decrease in the bit-error rate. Figure 23 is a plot of the bit-error rate for the same ICs for a geosynchronous orbit for a spacecraft with 25 mils of aluminum shielding for an Adams' 10% worst-case environment [56]. For the commercial microprocessors, one error will occur approximately every 3 days. Using design and resistor (160 kΩ) hardened techniques, one error will occur approximately every 100 years. Unfortunately, the improvements in SEU hardness were at the sacrifice of performance, with substantial increases in write time.

**Figure 24:** A cross section of a CMOS technology on an n-type substrate. Parasitic bipolar transistors form an SCR that is subject to latchup. (After Ref. 57)

3.2.3 Hard Errors

Single-event snapback and single-event gate rupture can also cause hard errors in bulk-silicon devices. Because bulk-silicon devices may include four layer p-n-p-n and multiple layer structures, they are also susceptible to single-event latchup and single-event burnout.

3.2.3.1 Single-Event Latchup

Single-event latchup (SEL) can be caused by a heavy-ion strike in silicon ICs with parasitic four layer n-p-n-p paths. SEL is triggered by excess current in the base of either a parasitic pnp or npn transistor following a heavy-ion strike. Latchup creates a low-resistance path from power supply to ground that can cause destructive burnout. A cross section of a CMOS IC illustrating parasitic four-layer p-n-p-n paths is shown in Fig. 24 [57,58]. One scenario that can lead to latchup is as follows [2]: A heavy ion-strike can trigger excess current in the base of the lateral pnp transistor. It will deposit charge and create a current that can flow through the substrate resistance. If the voltage drop across the substrate resistance is large enough, it can forward bias the lateral pnp transistor and holes can be injected into the substrate. Some of these holes will be collected by the p-well where they will provide base drive to the npn transistor. This results in a regenerative feedback loop, and if the feedback loop has a gain greater than unity, latchup will occur. Latchup is triggered on the order of hundreds of nanoseconds, and can cause destructive burnout on the order of hundreds of microseconds [59]. A typical I-V characteristic for latchup is shown in Fig. 25 [57]. The holding voltage for latchup is typically on the order of 1 V. Thus, unless the power supply voltage is interrupted, the low-resistance path from the power supply to ground will be maintained.

Figure 25: Typical I-V characteristics for latchup. (After Ref. 58)

The holding current, I_h, for latchup is given by [60]

$$I_h = \frac{I_W \beta_p (\beta_n + 1) + I_s \beta_n (\beta_p + 1)}{\beta_p \beta_n - 1},$$ (8)

where β_n (β_p) is the current gain of the parasitic npn (pnp) transistor and I_W (I_S) is the current through well (substrate) resistance R_W (R_S). To avoid latchup, the holding current can be raised by reducing all or some combination of β_n, β_p, R_S, or R_W.

An effective method for reducing the susceptibility of bulk-silicon ICs to latchup is the use of expitaxial buried layers (e.g., a low resistivity n-type substrate in conjunction with an n-type expitaxial layer [61,62]). The low resistivity substrate lowers the lateral resistance and increases the lateral current required for latchup initiation and reduces the current gain of the parasitic transistor increasing the latchup threshold [61]. This method works for reducing latchup due to heavy-ion strikes and due to high dose rate transient irradiation. It is often possible to make the holding voltage larger than the operating voltage of the circuit making

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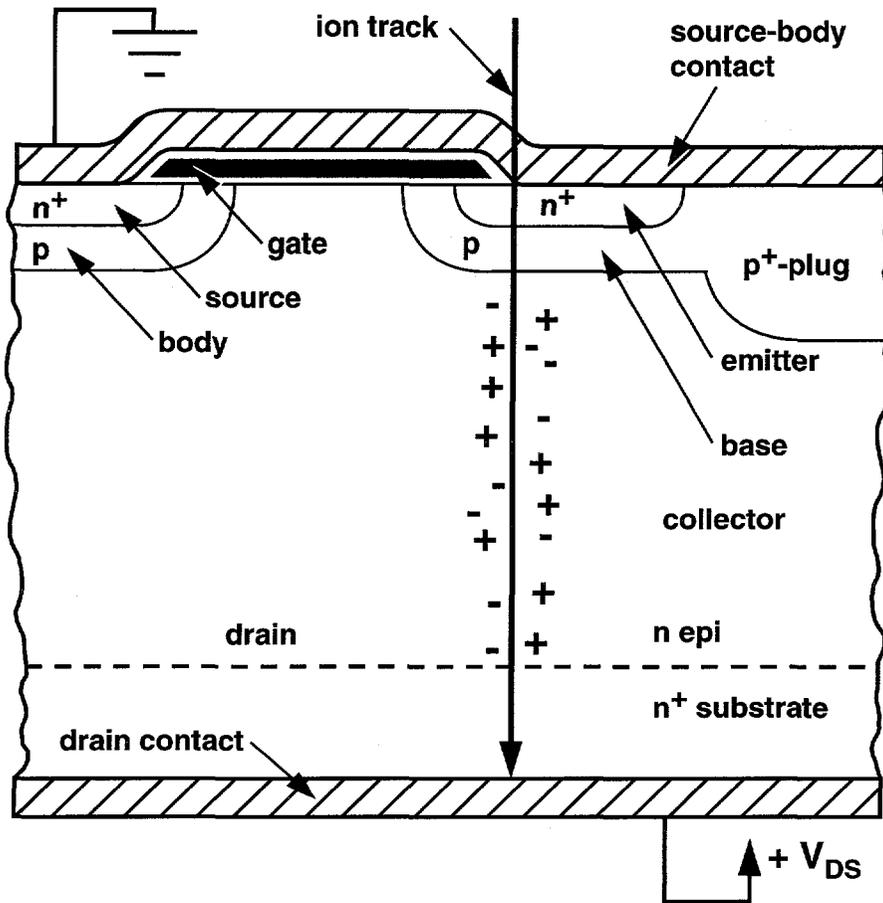
Figure 26: Cross-section of a power MOSFET. (After Ref. 69)

latchup impossible under normal operating conditions. Another method that has been used to reduce the susceptibility of CMOS ICs to latchup is neutron irradiation. This will cause displacement damage that can reduce the lifetime of minority carriers and reduce the current gain of the parasitic transistors.

3.2.3.2 Single-Event Burnout

Single-event burnout can cause permanent damage to bipolar power transistors and to power MOSFETs [63-70]. A cross-section of a power MOSFET is shown in Fig. 26 [69]. Note that the structure of a power MOSFET is much different than for a standard MOSFET. The substrate of a power MOSFET acts as the drain. The channel (body) and source regions are formed by a double diffusion. Inherent to this process is a bipolar npn transistor (for the n-channel power MOSFET of Fig. 26) with the drain acting as the collector, the channel region as the base, and the source as the emitter. For normal operation a positive bias on the gate allows electrons to flow from the source to drain near the surface. The bipolar junction is always biased in the OFF mode during normal operation by shorting the source to the channel at the surface of the device. If a heavy ion strikes the parasitic transistor, as shown in Fig. 26, the charge deposited by the ion strike will cause current to flow in the base region and it will raise the local

potential of the emitter-base junction. If the current flow is high enough, it can forward bias the emitter-base junction. At this point the parasitic transistor turns ON. After the parasitic bipolar transistor is turned ON, second breakdown of the bipolar junction transistor can occur. This second breakdown has been referred to as current-induced avalanche [68]. In addition to increased electron injection from the emitter to the base, the avalanche breakdown will also cause holes to flow from the collector to the base. Depending on the current density during current-induced avalanche (and the current supply of the external circuit), the current induced in the parasitic transistor by the heavy ion will either dissipate with no device degradation or will regeneratively increase until (in absence of current limiting elements) the device is destroyed [2,68].

Experimental results [64] have shown that there is a threshold for the drain-to-source voltage, V_{DS}, in order for SEB to occur. This threshold has been referred to as the failure-threshold voltage (V_{Fth}). If V_{DS} is below the failure-threshold voltage, the heavy-ion strike causes a small prompt photocurrent lasting for approximately 5 ns. Observation of the prompt signal is normally an indication that V_{DS} is close to the failure-threshold voltage. As V_{DS} exceeds V_{Fth} burnout can occur, and the drain-to-source current increases dramatically. If the current is below a critical value, burnout will not destroy the device. However, if the current is sufficiently high, SEB will destroy the device. The voltage level at which a device is destroyed is highly device dependent and can vary from 22 to 90% of the rated breakdown voltage for an n-channel transistor [64]. Breakdown voltages for a power MOSFET can vary widely, from less than 80 V to more than 500 V. Thus, the range of V_{DS} required to initiate burnout can vary from less than 20 V to hundreds of volts. The closer V_{DS} is to V_{Fth}, the lower the current density of the ion strike is in order to initiate burnout [64].

The failure-threshold voltage has also been found to depend on the LET of the incident ion [64]. As the ion LET is increased, it generates higher current densities along its path. A lower voltage is required to sustain current-avalanche breakdown as the ion current density is increased [68]. Thus, the failure-threshold voltage decreases as LET increases, consistent with experimental results [64]. Increasing temperature has been found [69] to decrease the susceptibility of power MOSFETs to SEB by lowering the avalanche multiplication factor.

Several methods for reducing or eliminating SEB have been proposed [63]. These include 1) using pnp transistors to utilize the lower ionization coefficients of holes, 2) using graded junctions to increase the length of the silicon region over which the voltage is dropped, and 3) using current limiting (inductance, resistance, or both) to prevent the simultaneous high-current, high-voltage condition.

4.0 TOTAL-DOSE EFFECTS

Total dose ionizing irradiation can affect a SOI transistor by creating charge in the oxide and at the silicon/oxide interfaces for gate oxides, field or sidewall oxides, and buried oxides. The increased charge can change the threshold voltage (either positive or negative), decrease carrier mobility and n-channel transistor current drive, and cause increases in leakage current,

increases in timing delays, and potentially IC failure. In this section, we discuss the effects of total-dose irradiation on SOI transistors.

4.1   Photon Interactions

As a gamma ray, proton, electron, neutron, or other high-energy particle impinges on the surface of a material, it can interact with the material creating many electron-hole pairs and defects within the material. The manner in which radiation interacts with solid material depends on the type, kinetic energy, mass, and charge state of the incoming particle and the mass, atomic number, and density of the target material. Ionization of the target material occurs for photons, electrons, protons, and energetic heavy ions. Photons interact with material through three different processes, namely the photoelectric (or fluorescent) effect, the Compton effect, and pair production [50,71]. For each of these processes, the primary result of the interaction is the creation of energetic secondary electrons. The process by which a photon will interact with a material depends on the photon energy and material atomic mass. Photons incident on silicon in the energy range of ~0.1 to 10 MeV will interact primarily by Compton scattering.

As high-energy electrons (or holes) are created by photon interactions, they can also ionize atoms creating additional electron-hole pairs. As long as the energies of the electrons and holes generated are higher than the minimum energy required to create an electron-hole pair (~3.6 eV for Si and 17 eV for SiO_2 [50,72,73]), they can continue to generate electron-hole pairs. In this manner, a single, high enough energy incident photon, electron, or proton can create thousands (up to millions) of electron-hole pairs. These electron-hole pairs are the cause of radiation-induced degradation in MOS devices.

4.2   Gate oxide

In an ionizing radiation environment, electron-hole pairs will be generated uniformly throughout the oxide. The generated carriers induce the buildup of charge which can lead to device degradation. Although the amount of damage can be quite different, the fundamental processes for the radiation-induced degradation of gate oxides are similar in nature to that for SOI buried oxides and sidewall and field-oxides. Because of this, in this section we will present a detailed overview of radiation effects in gate oxides.

4.2.1   Oxide- and Interface-Trap Charge

The mechanisms that cause radiation-induced charge in thermal oxides are depicted in Fig 27. [50]. Figure 27 is a plot of an MOS band diagram for a positively applied gate bias. Immediately after irradiation, electrons will rapidly drift (within picoseconds [74,75]) toward the gate and holes will drift toward the Si/SiO_2 interface. However, even before the electrons leave the oxide, some fraction will recombine with holes. The fraction of electron-hole pairs that escape recombination is the electron-hole yield. The amount of initial recombination is highly
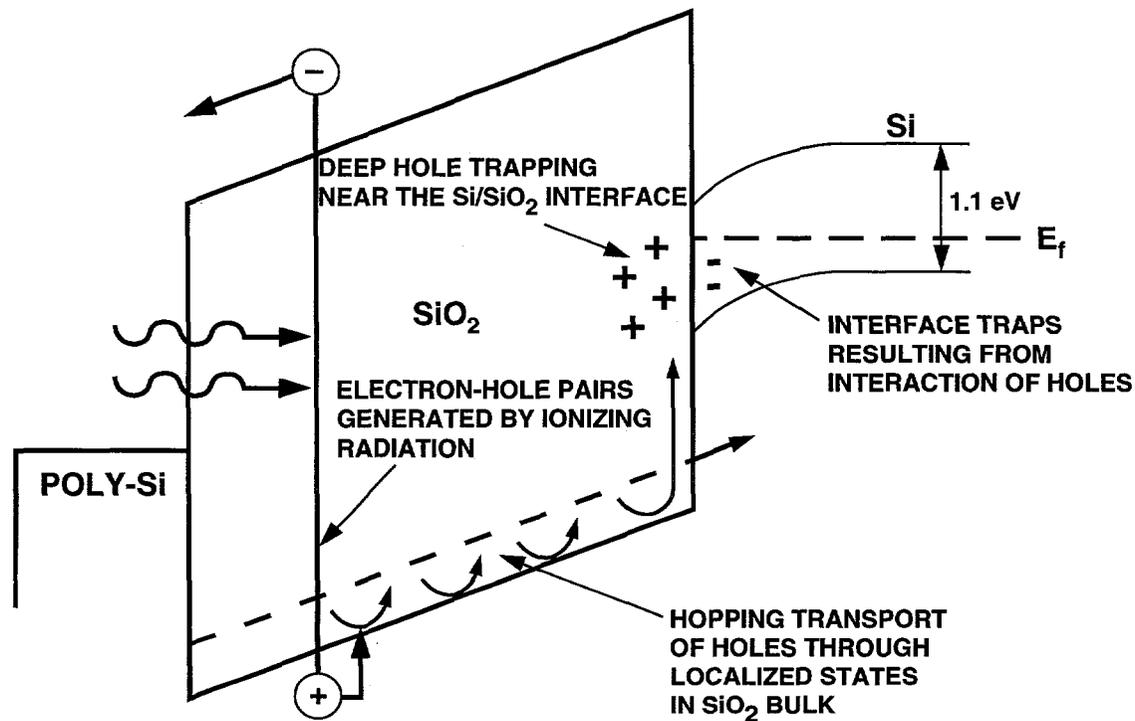
Figure 27: Band diagram of an MOS device with a positive gate bias. Illustrated are the main processes for radiation-induced charge generation. (After Ref. 50)

dependent on the electric field in the oxide and the energy and type of incident particle [50,76,77]. For low electric fields, the amount of initial recombination can be very high. Thus, for thick field oxides or buried oxides, the amount of initial recombination can be significantly more than for gate oxides under normal bias conditions.

Those holes which escape initial recombination will transport through the oxide toward either the Si/SiO$_2$ or gate/SiO$_2$ interface depending on the polarity of the applied field. Holes transport in thermal oxides by hopping between localized states in the oxide via polaron motion [50,78,79]. Polaron hopping makes hole transport dispersive (causing hole transport to occur over many decades in time after a radiation pulse) and highly temperature and oxide thickness dependent [50,78,79]. The time for holes to transport through a thermal oxide follows approximately a t_{ox}^4 thickness dependence [80]. At room temperature, for a thick 96.5 nm thermal oxide at an electric field of 3 MV/cm, the time for ~50% of the radiation-induced holes to transport through the oxide is roughly 10^{-4} s [81].

As holes approach the interface, some fraction of the holes will be trapped, forming net positive oxide-trap charge for both p- and n-channel transistors. The fraction of holes that are trapped is governed by the trapping efficiency near the interface which is highly device fabrication dependent, with only a few percent of the holes trapped for radiation-hardened oxides to as much as 50 to 100% for non-hardened oxides. Large concentrations of oxide-trapped charge will cause large negative threshold-voltage shifts in n-channel transistors driving them towards depletion mode. This can cause large increases in leakage current in an IC. Immediately

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after oxide-trapped charge is created it begins to be neutralized by tunneling of electrons from the silicon into oxide traps [82-87] and the thermal emission of electrons from the oxide valence band into oxide traps [82-85]. This causes a logarithmic decrease in oxide-trapped charge with time. The rate of neutralization is highly dependent on the spatial and energy distribution of the traps in the oxide, each of which can depend on processing conditions. For a number of hardened technologies, a relatively high rate of neutralization has been observed, while for several commercial technologies little or no neutralization was observed [82]. Because of the neutralization of oxide charge with time, the effects of oxide-trapped charge on IC response are often most important for short times following a pulse of irradiation (e.g., military weapon environments), although in some cases oxide-trapped charge can also affect device response at long times.

Hydrogen ions are also released as holes *hop* through the oxide or as they are trapped near the Si/SiO$_2$ interface. The hydrogen ions can drift to the Si/SiO$_2$ interface where they may react to form interface traps. Interface traps exist within the silicon band gap at the interface. Because of their location at the interface, the charge of an interface trap can be changed easily by applying an external bias. Interface traps can be positive, neutral, or negative. Traps in the lower portion of the band gap are predominantly donors, i.e., if the Fermi level at the interface is below the trap energy level, the trap *donates* an electron to the silicon. In this case, the trap is positively charged. A p-channel transistor at threshold samples primarily interface traps in the lower region of the band gap. Therefore, for a p-channel transistor, interface traps are predominantly positive, causing negative threshold-voltage shifts. Conversely, traps in the upper portion of the band gap are predominantly acceptors, i.e., if the Fermi level is above the trap energy level, the trap *accepts* an electron from the silicon. In this case, the trap is negatively charged. An n-channel transistor at threshold samples interface traps predominantly in the upper region of the band gap. Therefore, for an n-channel transistor, interface traps are predominantly negative, causing positive threshold-voltage shifts. At midgap, interface-trap charge is approximately neutral [88-91]. Because oxide-trap charge is positive for both p- and n-channel transistors, oxide-trap charge and interface-trap charge compensate each other for n-channel transistors and add together for p-channel transistors.

An increase in the number of interface traps will reduce carrier mobility. The degradation in mobility with interface-trap charge follows the general relationship [92,93],

$$\mu = \frac{\mu_0}{1 + \alpha \cdot \Delta N_{it}}, \tag{9}$$

where μ_0 is the preirradiation mobility and α is a constant. This equation is often referred to as the Sun-Plummer relation [94], which was derived for the change in mobility due to preirradiation fixed oxide charge. Equation 9 has been found to be valid under most conditions, except for short times (<0.1 s) after a pulse of irradiation [95]. At early times after irradiation (~0.01 s), there can be a significant concentration of oxide-trap charge close to the Si/SiO$_2$ interface which can affect, and in some cases dominate, the degradation in mobility. However, as the electron tunneling front moves into the oxide, neutralizing oxide charge close to the

interface, the importance of charged hole traps on mobility becomes increasingly less [95]. Other work [96-98] has suggested that, for some technologies, Eq. 9 must be modified to include oxide-trap charge scattering even for long times after irradiation.

Interface-trap buildup occurs on time frames much slower than oxide-trap charge buildup. Interface-trap buildup can take thousands of seconds to saturate after a pulse of ionizing irradiation. Unlike oxide-trap charge, interface-trap charge does not anneal at room temperature. These properties make interface-trap charge effects very important for low dose-rate applications, e.g., space. For an n-channel transistor, interface traps affect device performance primarily through an increase in threshold voltage and a decrease in channel mobility. Both of these degradation mechanisms tend to reduce the drive current of ON transistors, leading to increases in timing parameters of an IC.

4.2.2 Effects of Oxide-Trapped and Interface Trapped Charge on Device Response

The total threshold-voltage shift for a transistor is the sum of the threshold-voltage shifts due to oxide-trap and interface-trap charge, i.e.,

$$\Delta V_{th} = \Delta V_{ot} + \Delta V_{it} \ . \tag{10}$$

ΔV_{th} is given by

$$\Delta V_{th} = \frac{-1}{C_{ox} t_{ox}} \int_0^{t_{ox}} \rho(x) x \, dx \ , \tag{11}$$

where $\rho(x)$ is the charge distribution of radiation-induced charge. It includes contributions from both radiation-induced oxide-trap and interface-trap charge. Note the change in sign between the charge distribution and the threshold-voltage shift. For positive charge, the threshold-voltage shift is negative; conversely, for a negative charge, the threshold-voltage shift is positive. Thus, for devices where oxide-trap charge dominates, the threshold-voltage shift will be negative.

At high dose rates and short times, little neutralization of oxide-trap charge will occur and ΔV_{ot} can be large and negative. Conversely, interface-trap charge at high dose rates and short times will have had insufficient time to build up and ΔV_{it} is normally small. Thus, at high dose rates and short times for either n- or p-channel transistors the threshold-voltage shift can be large and negative. For an n-channel transistor, large negative threshold-voltage shifts will significantly increase the drain-to-source leakage current, which in will turn cause significant increases in IC static supply leakage current, I_{DD}, leading to potential IC failure. Thus, for short times after a pulse of radiation, device response is normally dominated by large increases in oxide-trapped charge.

At moderate dose rates, some neutralization of oxide-trap charge will take place and some buildup of interface traps will also occur. Thus, for this case, both ΔV_{ot} and ΔV_{it} can be large. For an n-channel transistor, ΔV_{ot} and ΔV_{it} tend to compensate each other. Therefore, at moderate dose rates, even though the individual components (ΔV_{ot} and ΔV_{it}) of the threshold-voltage shift can be large, the net threshold-voltage shift for an n-channel transistor can be small and the failure level of an IC may be relatively high.

For the long times associated with low-dose-rate irradiations, a large fraction of the oxide-trap charge in hardened transistors will be neutralized during irradiation. Thus, ΔV_{ot} is normally small. In contrast, the long times associated with low-dose-rate irradiations allow for interface-trap buildup to saturate. This results in a positive increase in threshold voltage in n-channel transistors and a decrease in carrier mobility which tend to reduce the current drive of a transistor and can lead to timing related failures for an IC.

No differences in radiation hardness are expected for gate oxides grown on bulk-silicon or SOI substrates. Indeed, previous work showed similar radiation-induced threshold-voltage shifts for gate oxides grown on bulk-silicon and SIMOX and bonded SOI substrates [99].

4.2.3   Gate-Oxide Hardening

One process condition that has a large effect on gate-oxide radiation hardness is gate-oxide thickness. Fortunately, as the thickness of the gate oxide decreases, its radiation hardness increases. Figure 28 is a plot of the threshold-voltage shifts due to interface-trap and oxide-trapped charge for dry and steam grown (wet) oxides. The concentrations of both types of charge decrease with slightly less than a t_{ox}^2 thickness dependence ($\sim t_{ox}^{-1.5}$ to $t_{ox}^{-1.8}$). For very thin oxides (<20 nm), there is evidence that the amount of radiation-induced oxide-trap charge decreases with an even faster dependence on oxide thickness [100]. Because of the improvement in hardness with decreasing thickness, there is no inherent reason for gate oxides in advanced commercial technologies not to be extremely radiation hard.

In addition to oxide thickness, other process conditions can affect hardness. High-temperature anneals can significantly degrade device hardness due to the creation of oxygen vacancies in the oxide. Figure 29 is a plot of ΔV_{ot} for capacitors annealed in nitrogen at temperatures from 800 to 950°C and irradiated to 1 Mrad(SiO_2) [101]. Anneal temperatures above 875° result in significant increases in ΔV_{ot}. Nitrogen anneals over the same temperature range have a much smaller affect on ΔV_{it}. However, annealing in ambients containing hydrogen after depositing the gate material (e.g., polysilicon or metal) can significantly increase the amount radiation-induced interface-trap charge. Figure 30 is a plot of ΔV_{it} for capacitors annealed in varying amounts of hydrogen after deposition of the polysilicon gate and irradiated to 100 krad(SiO_2) [102]. Capacitor A was exposed to the least amount of hydrogen and capacitor C was exposed to the greatest amount of hydrogen. Increasing the amount of hydrogen used in processing resulted in increasing concentrations of interface-trap charge. Thus, to optimize hardness, process temperatures after gate oxidation should be kept at or below 850°C (except
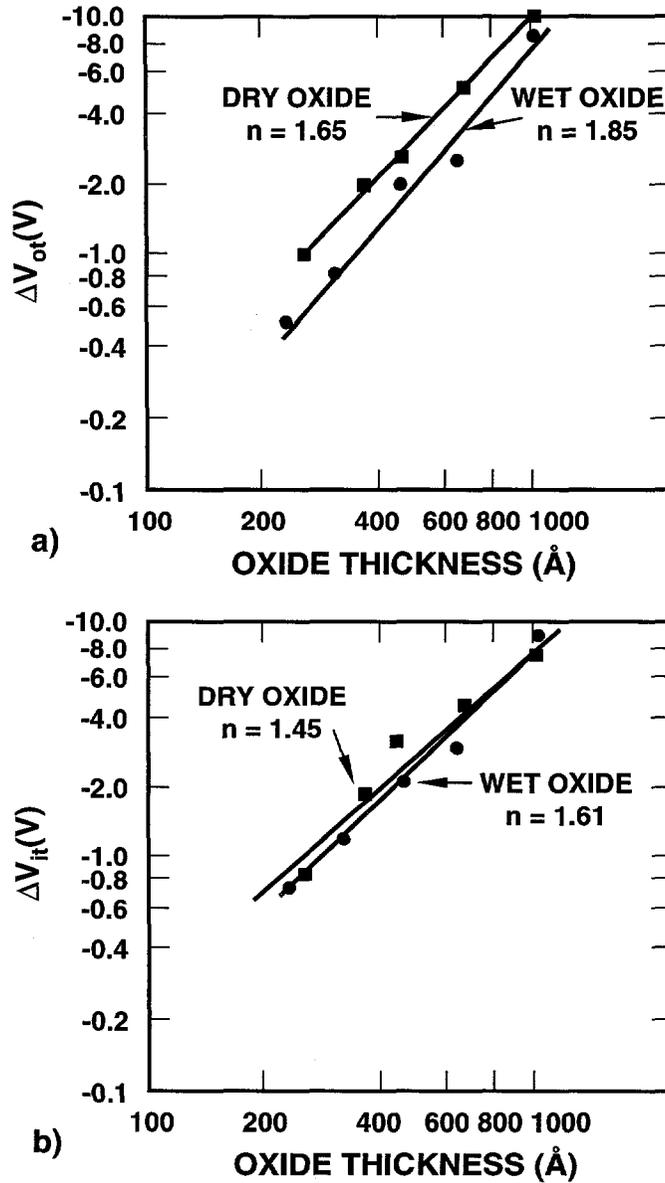
Figure 28: The dependence of the threshold-voltage shift due to oxide-trap and interface-trap charge on oxide thickness.

perhaps for a few brief rapid thermal anneals) and ambients containing hydrogen should be avoided.

4.2.4 Microscopic Defects

A powerful tool for investigating the microscopic nature of defects in oxides is electron paramagnetic resonance (EPR) or electron spin resonance (ESR) [103]. In EPR, the energy associated with the intrinsic angular momentum (spin) of an electron is measured. Spin is quantized with quantum number 1/2, i.e., it can have only two orientations with respect to the
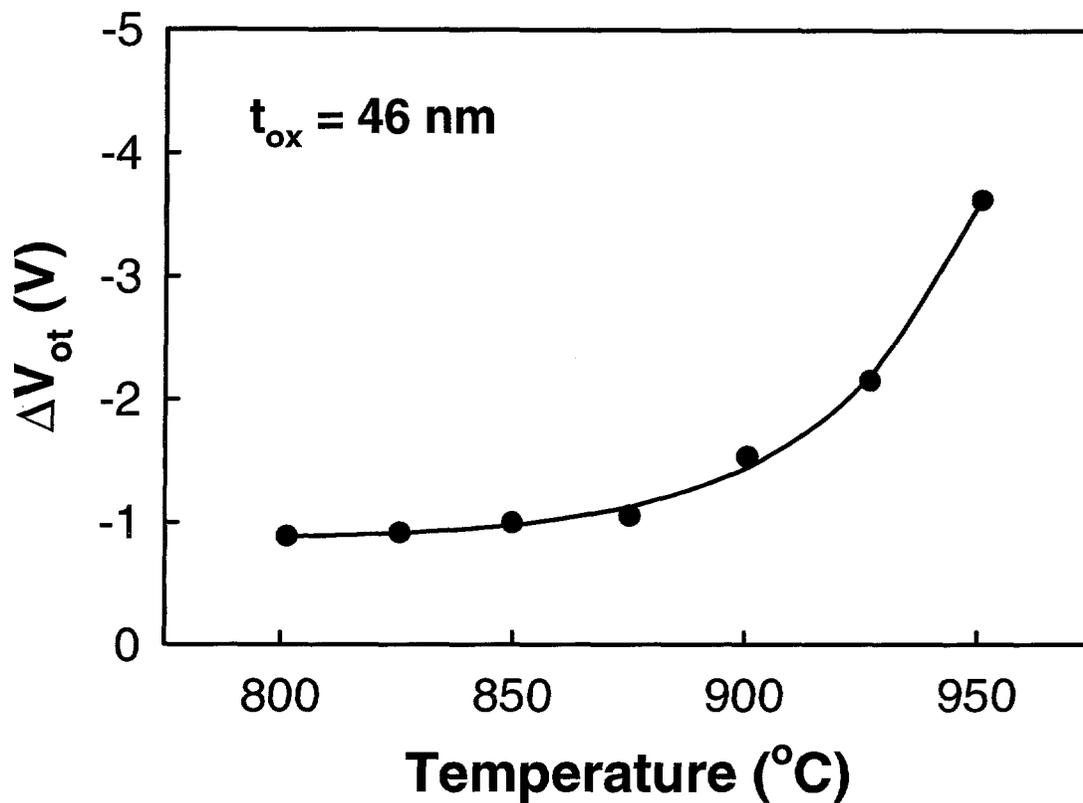
Figure 29: The effect of anneal temperature on radiation-induced oxide-trapped charge. (After Ref. 101)

axis of an applied magnetic field. The difference in energy between two states with different spin is given by $E = h\nu = g\beta H$, where ν is the microwave frequency, H is the magnetic field strength, β is the Bohr magneton ($\beta = eh/4\pi mc$), and g is a dimensionless tensor which gives information on the amount of splitting, characteristic of the atom or ion, and information regarding the symmetry of the defect. In an electron paramagnetic resonance system, the sample under test is placed in a microwave cavity and a DC magnetic field is applied. The magnetic field is varied. If a point is reached where the microwave energy, $h\nu$, is equal to $g\beta H$, an unpaired electron can resonate between the two energy levels. Measurement of the resonance absorption point gives information on the g-value or tensor. Note that the atom or ion must be paramagnetic, i.e., have an unpaired electron or electrons, in order to observe a resonance absorption (EPR signal). If the atom or ion is diamagnetic, i.e., it has no net electronic magnetic moment, an EPR signal will not be measured.
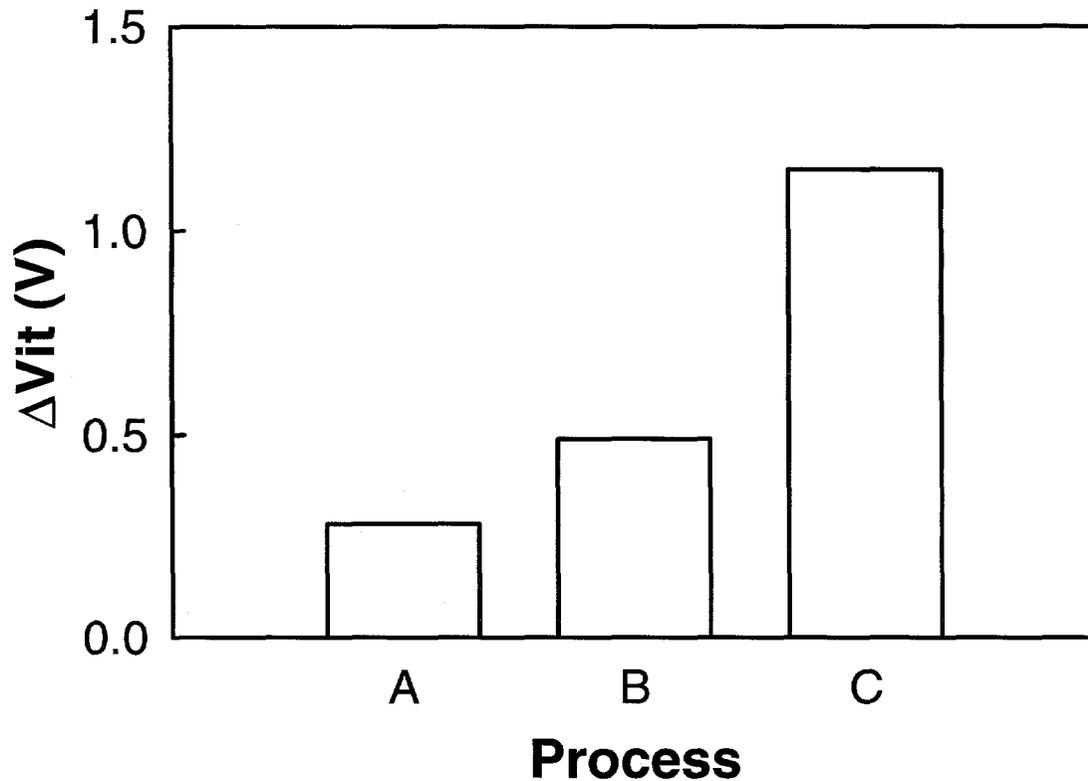
**Figure 30:** Effect of hydrogen on radiation-induced interface-trap buildup. Capacitor A was exposed to the least amount of hydrogen during processing (in high-temperature anneals) and Capacitor C was exposed to the most amount of hydrogen. (After Ref. 102)

A number of defects have been identified in irradiated thermal oxides. The most important of the defects identified by EPR in irradiated thermal oxides is the E' center [104-108]. At least nine variations of the E' center have been identified in either thermally grown oxides or in bulk crystalline or fused oxides. Most E' centers are characterized by an unpaired electron highly localized on a silicon atom bonded to three oxygen atoms. The chemical notation for the generic E' center is given by $\uparrow$Si$\equiv$O$_3$ or $\bullet$Si$\equiv$O$_3$. (The combination Si$\equiv$O$_3$ indicates a silicon atom bonded to three oxygen atoms and an arrow, $\uparrow$ or $\bullet$, represents an unpaired electron that will have a net magnetic moment, resulting in an EPR center). One of the more common types of E' centers identified in thermally grown oxides is the E'$_\gamma$ center. The chemical notation for the E'$_\gamma$ center is given by O$_3\equiv$Si$\bullet$ $^+$Si$\equiv$O$_3$. The E'$_\gamma$ center is a trivalent silicon atom bonded to three oxygen atoms. It becomes paramagnetic and positively charged when a radiation-induced hole becomes trapped at the vacancy site of a missing oxygen atom. It is identified by an EPR signal with a zero crossing at g = 2.0005. For thermal oxides, the precursor state exists prior to irradiation. (This is not necessarily true for bulk crystalline oxides [104].) It occurs naturally, usually in greatest density close to the Si/SiO$_2$ interface due to the lattice mismatch between the

silicon substrate and the oxide (which may be an indication of an incomplete oxidation process) or due to out-diffusion of oxygen out of the oxide and into the silicon [109].

Three other types of E' centers identified in irradiated thermal oxides are the E'$_\delta$ [110] and the 74-G [111-113] and 10.4-G doublets [113]. The E'$_\delta$ center likely results from capturing a hole at a silicon interstitial/oxygen vacancy complex. It is identified spectroscopically by differing g-tensors than the E'$_\gamma$. The E'$_\delta$ center also anneals at lower temperatures than the E'$_\gamma$ center [114]. Like the E'$_\gamma$ center, the E'$_\delta$ center has a positive paramagnetic charge state. The 74-G and 10.4-G doublets are hydrogen-associated E' centers [111-113]. The structure of the 74-G doublet has been determined to be an unpaired spin on a silicon atom bonded to two oxygen atoms and one hydrogen atom. Its chemical notation is given by $H-Si=O_2\bullet\ ^+Si\equiv O_3$. It has a positive paramagnetic charge state. In order to observe the 74-G doublet, thermal oxides must be irradiated to very high radiation levels ($\sim 10^8$ rad) [112], or exposed to hydrogen following irradiation [113]. Lenahan and Dressendorfer [105] showed a correlation between the E' center and radiation-induced positive charge (oxide-trap charge) for some thermal oxides. Using etch-back measurements, they also found the same spatial distribution in the oxide for the number of E' centers as for the number of oxide-trap charge. Most of the E' centers and oxide-trap charge were determined to be located close to the Si/SiO_2 interface (within 10 nm for a 1100 nm thick oxide). However, this correlation does not appear to be true in general for all oxides. As will be shown below, recent works on thick SIMOX [115,116] and BESOI [114] buried oxides and on other thermally grown gate oxides [114] showed no correlation between the number of E' centers and oxide-trap charge.

The microscopic structure of the radiation-induced interface-trap defect center has been identified as a P_b defect [105-108,117,118]. A P_b center is a trivalent silicon defect site [119-121], similar to the E' center except that the P_b center is back bonded by three silicon atoms. The chemical notation for the P_b center is $\bullet Si\equiv Si_3$. In (100) silicon, two distinct types of P_b centers have been identified preirradiation [122,123]. These centers are noted P_{b0} and P_{b1}.

4.3   Field and Sidewall Oxides

The structure of a SOI IC includes either a thick field oxide or a thin sidewall oxide. Even though the radiation hardness of commercial gate oxides may improve as the IC industry tends towards ultra-thin oxides, field or sidewall oxides of advanced commercial SOI technologies can be very soft to ionizing irradiation. (Field oxides for bulk-silicon technologies also can be very soft to ionizing irradiation.) A relatively small dose in a field or sidewall oxide (~ 10 krad(Si) for many commercial devices) can induce sufficient charge to cause IC failure.

4.3.1   Effects of Field and Sidewall Oxides on Device Response

A cross section of a mesa-etched SOI transistor illustrating the sidewall oxide is shown in Fig. 31 [124]. Thin sidewall oxides occur for transistors isolated by mesa etching. The sidewall oxide exists as the gate oxide extends over the edges of the silicon island and forms a parasitic
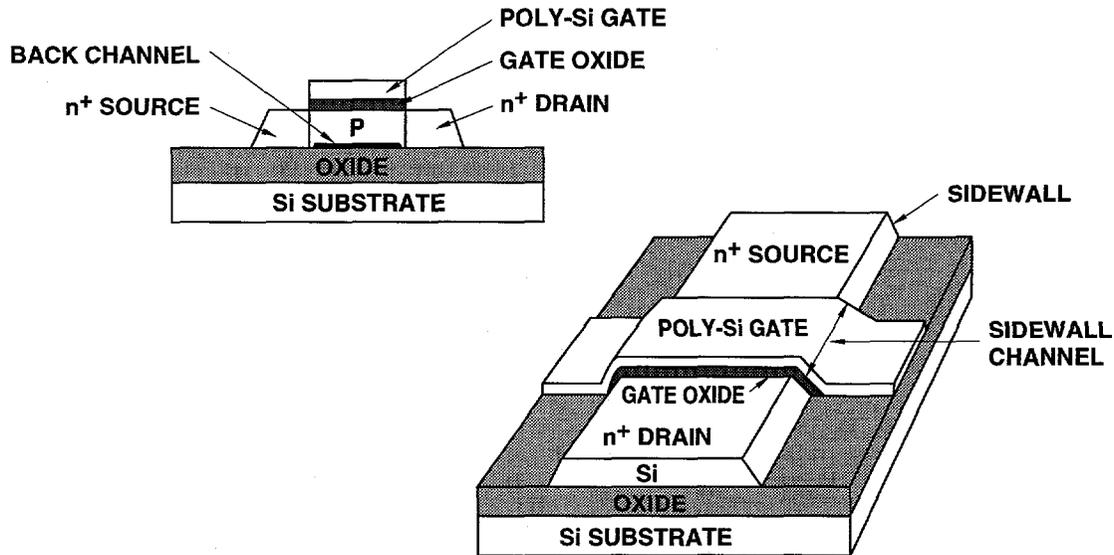
Figure 31: Cross-sections of a silicon-on-insulator transistor (SOI). (After Ref. 124)

transistor in parallel with the top transistor (similar to that for thick field oxides). In some cases, the sidewall oxide is less radiation tolerant than the top oxide and can greatly increase the top oxide transistor leakage current. The positive charge generated in the oxide as a result of irradiation can invert p-type surfaces. Thus, the effects of irradiation on sidewall leakage are only important for n-channel transistors. The sidewall oxide induced leakage forms a shoulder in the MOS transistor I-V curve as illustrated in Fig. 32 [125]. (Figure 32 was actually taken from an MOS transistor fabricated on a silicon-on-sapphire (SOS) substrate. However, an MOS transistor fabricated in a SOI substrate has the same qualitative nature for sidewall and back-channel leakage current.) Plotted in Fig. 32 are the drain-to-source leakage current versus gate-to source voltage curves for an n-channel gate-oxide transistor before and after irradiation. The sidewall-oxide leakage significantly adds to the drain-to-source current at zero gate voltage. Thus, the sidewall-oxide leakage prevents the transistor from being completely turned off. This will greatly add to the static supply leakage current of an IC.

If transistors are not mesa etched, they usually are isolated using field oxides. Field oxides are much thicker than gate oxides. Unlike gate oxides, which are routinely grown by thermal oxidation, field oxides are produced using a wide variety of growth and deposition techniques. Thus, the trapping properties of a field oxide may be poorly controlled and can be considerably different than for a gate oxide.

A cross-section of a typical commercial field oxide is shown in Fig. 33 [126]. The threshold voltages of parasitic field oxide transistors (~10 to >30 V) are initially much larger than that for gate-oxide transistors. As radiation-induced oxide charge builds up in a field oxide, it causes the threshold voltage of the field oxide to tend to go toward depletion mode for field oxides over a p substrate (equivalent to an n-channel field oxide transistor). If the buildup of charge is large enough, excessive leakage current can flow from the source to drain of the gate-oxide transistors and between transistors. The excess leakage current is identical in nature to that for sidewall-oxide leakage as illustrated in Fig. 32.
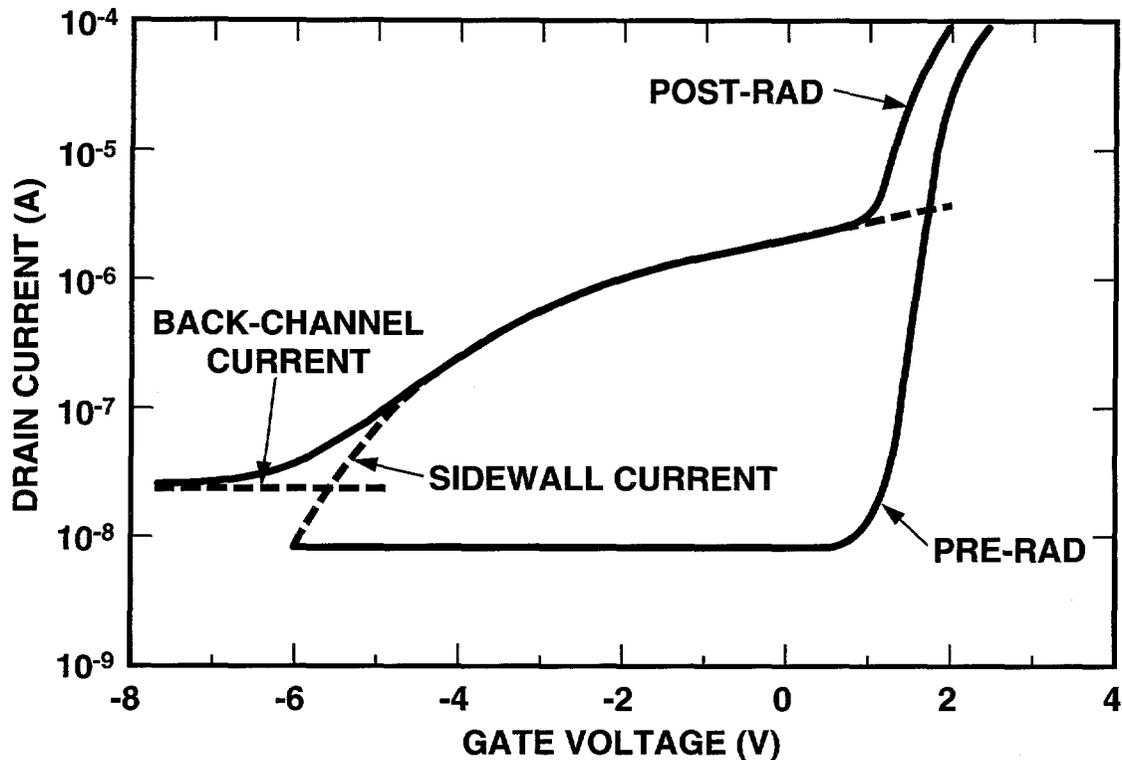
Figure 32: I-V curves for a gate oxide transistor on a silicon-on-sapphire substrate. Illustrated are the contributions of back-channel and sidewall leakage to the leakage current. (After Ref. 125)

4.3.2 Field and Sidewall Oxide Hardening

One method that can completely eliminate field or sidewall oxide leakage current is to use closed geometry (or edgeless) transistors. For these transistors, the gate does not terminate at an edge where leakage can occur. The major drawback to this method is increased transistor size and may not be viable for extremely dense circuits.

A technique that has been used to reduce sidewall leakage current is to heavily dope the sidewall by selective implantation. This raises the threshold voltage of the parasitic sidewall transistor, reducing its importance to the radiation response [124,127-129]. A similar technique has been used to reduce the effects of field oxide leakage. Implanting a p+ guard band around the edges of an n-channel transistor will greatly increase the threshold voltage of the parasitic field oxide transistor at the gate edge and reduce the importance of the field oxide. Unfortunately, p+ guard bands greatly increase the area of a transistor (even more so than for closed geometry transistors).

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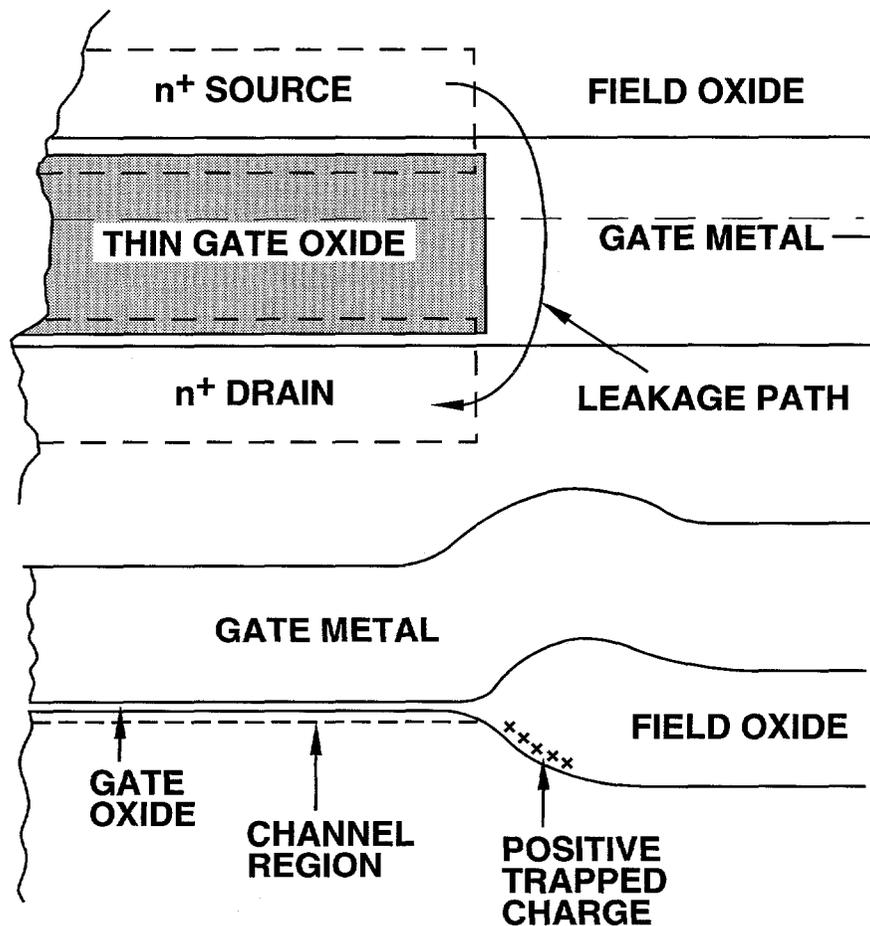
Figure 33: Cross-section of a parasitic field oxide transistor showing the primary leakage current paths. (After Ref. 126)

4.4 Buried Oxides

4.4.1 Effects of Buried Oxides on Leakage Current

The buried oxide inherent to an SOI transistor is the major difference in the total-dose response between bulk-silicon and SOI technologies. Ionizing radiation induces the buildup of net positive charge in the buried oxide near the silicon/buried oxide interface and interface traps at the interface. The radiation-induced charge can invert the bottom surface of the silicon channel forming a conducting channel (back channel) between the source and the drain of the transistor. If the channel is partially depleted, the gate bias of the MOS transistor has only a weak effect on the back-channel leakage current. Thus, for partially-depleted channels, the buried oxide causes a fixed increase in leakage current which is relatively independent of gate bias as illustrated in Fig. 32. For fully-depleted transistors, the back-channel leakage is strongly affected by gate bias.

50
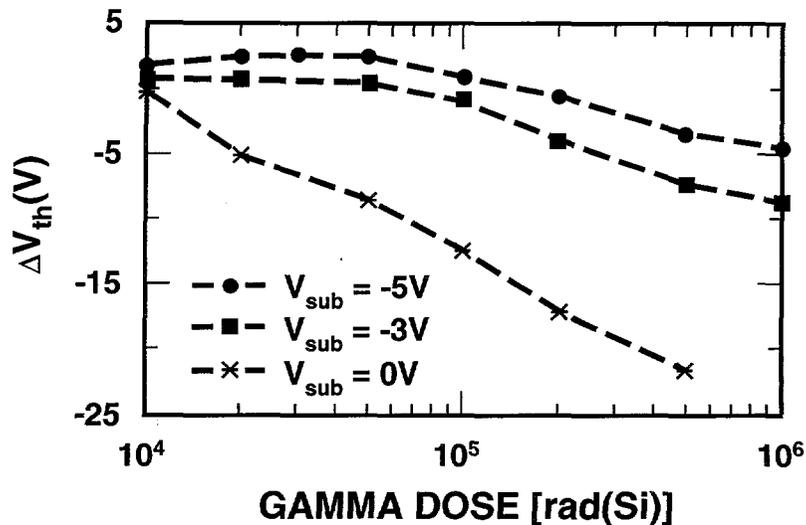
Figure 34: Back-channel transistor threshold-voltage shift versus dose for varying substrate biases. (After Ref. 131)

The bias on the bottom substrate can strongly affect the radiation response [130,131]. By applying a negative bias to the bottom substrate, holes generated in oxide during irradiation will preferentially drift toward the back electrode, reducing the charge accumulated at the surface of the silicon channel/buried oxide interface, thus reducing the back-channel leakage current. This is illustrated in Fig. 34 [131] where the back-channel threshold-voltage shift is plotted versus dose for n-channel transistors. (Note from Fig. 31 that, if the SOI transistor structure is flipped upside down, the transistor still looks like an MOS capacitor with the substrate as the gate electrode. This is often referred to as a back-channel transistor.) The data of Fig. 34 were taken from SIMOX SOI transistors with the front (top) channel transistor biased in accumulation to separate the effects of the front- and back-channel transistors. For an n-channel transistor (p-type island), a large negative threshold-voltage shift of the back channel will invert the bottom surface of the channel leading to leakage current. The negative threshold-voltage shift for n-channel back channel transistors is greatly suppressed by applying a large negative substrate bias, which will lead to a reduction in back-channel leakage current.

The radiation response of buried oxides has been found to be highly dependent on the fabrication process [132,133]. SIMOX buried oxides are fabricated by implanting substrates with oxygen at high dose levels and energies. As such, it is natural to expect that the oxide may include numerous implant related defects throughout the buried oxide that can trap radiation-generated charge. Previous work [133-137] has shown that up to 100% of the radiation-generated holes are trapped in the bulk of the oxide at deep trap sites close to their point of origin. This is in contrast to thermal oxides where a smaller fraction (~3% for hardened oxides) of the radiation-generated holes are trapped near the Si/SiO_2 interface. Once trapped, some of the holes are slowly neutralized by electrons by thermal detrapping at room temperature [133-137]. No significant transport of holes through the buried oxide at room temperature has been observed [133,135,138] for SIMOX buried oxides fabricated using normal process conditions [138]. However, for SIMOX buried oxides receiving a supplemental oxygen implant and a low

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temperature anneal, photocurrents have been observed indicating the transport of radiation-induced charge carriers through the oxide [138]. In addition to hole trapping, electrons are also trapped throughout the bulk of the buried oxide [133,135,139,140], especially at low-field regions [135]. Most of the trapped electrons are thermally detrapped within <1 s after a pulse of irradiation. After the electrons are detrapped, the resultant charge is due to a high concentration of trapped holes causing large negative threshold-voltage shifts of the buried oxide. The concentration of electron traps can be altered by subjecting SIMOX oxides to a supplemental oxygen implant. Recent work has shown that in some cases, the amount of electron trapping can be significantly reduced [141-143] and the amount of hole trapping in the bulk of the buried oxide can be decreased [142,143] for supplemental implanted substrates. The amount of charge trapping has been determined to follow less than a square-law thickness dependence for normal device bias conditions (low fields in the buried oxide) [144].

BESOI buried oxides are fabricated by bonding together two thermal oxides. As long as the bonding process does not degrade the properties of the thermal oxides, BESOI buried oxides should look more like standard thermal oxides than SIMOX buried oxides [133,145,146]. Only moderate hole trapping in the bulk of BESOI buried oxides has been observed [132]. Most of the electrons and holes move through BESOI oxides and a significant fraction of the holes are trapped near the Si/SiO_2 interfaces [146]. Some electron trapping also can occur, presumably at the bond interface [132]. High-temperature annealing reduces the concentration of electron traps, but increases the number of hole traps in the bulk of the oxide [132]. However, BESOI oxides (and thermal oxides with a polysilicon cap) annealed at high temperatures (>1100°C) behave very similar to SIMOX oxides [137] and exhibit radiation-induced deep hole and shallow electron traps distributed throughout the buried oxide. The fact that BESOI oxides can be more characteristic of thermal oxides suggests that techniques used to hardened thermal oxides may be more successfully applied to BESOI oxides than to SIMOX oxides [146].

Fully-depleted transistor circuits are much more sensitive to radiation-induced oxide charge buildup in the buried oxide and interface-trap buildup at the top buried oxide/silicon interface. Positive oxide-charge buildup in the buried oxide will tend to deplete the back-channel interface and decrease the front-channel threshold voltage. This decrease in threshold voltage will cause a decrease in threshold voltage of the front-channel gate oxide in addition to that caused by radiation-induced positive charge buildup in the gate oxide. It will also cause increased back-channel leakage current.

Neglecting interface-trap buildup and assuming the substrate is grounded, the radiation-induced threshold-voltage shifts of the front, ΔV_{tf}, and back-gate, ΔV_{tb}, transistors can be modeled as [147,148],

$$\Delta V_{tf} = \Delta V_{tfo} + k_1 \Delta V_{tbo}, \tag{12}$$

$$\Delta V_{tb} = \Delta V_{tbo} + k_2 \Delta V_{tfo}, \tag{13}$$

where ΔV_{tfo} and ΔV_{tbo} are the threshold voltage shifts due to oxide-trapped charge buildup in the front- and back-gate transistors, respectively, and k_1 and k_2 are coupling coefficients given by,

$$k_1 = \frac{C_{ox2}C_{Si} / C_{ox1}}{C_{Si} + C_{ox2}}, \qquad (14)$$

$$k_2 = \frac{C_{ox1}C_{Si} / C_{ox2}}{C_{Si} + C_{ox1}}, \qquad (15)$$

where C_{Si} is the fully-depleted silicon capacitance, C_{ox1} is the front-gate oxide capacitance, and C_{ox2} is the buried oxide capacitance.

For normal CMOS inverter and transmission gate bias conditions, the worst-case bias conditions for both partially and fully-depleted transistors are those for nMOS transmission gates in the pass-gate configuration [148].

Preliminary work on BESOI wafers has shown hardness levels of 100 krad(Si) [32]. (Using hardening techniques for isolation field oxides, total-dose hardness levels in excess of 1 Mrad(Si) have been demonstrated [149].) Combining the SEU hardness with BESOI buried oxides (and hardened SIMOX oxides), it should be possible to fabricate SOI ICs using commercial designs that can survive most space requirements.

4.4.2 Buried Oxides - Microscopic Defects

Several microscopic defects have been identified using EPR in SOI buried layers. These defects play a role in instabilities in the buried oxides in radiation environments. The SOI technology most extensively studied is SIMOX technology. In SIMOX material all of the defects in the buried oxide are due to excess silicon indicating that the post-implantation, high temperature anneal step used to form the buried oxide is the source of the defects [114]. The primary defect identified by EPR in SIMOX material is the E'$_\gamma$ center [115,116,150-154] similar to that for gate oxides. However, in contrast to gate oxides, the variation in the number of E'$_\gamma$ centers does not track with the variation in positive charge in the buried oxide. Thus, E'$_\gamma$ centers are not the primary source of radiation-induced oxide-trap charge [115,116]. The concentration of E' centers has been coupled to electron trap sites in the buried oxide in which a substantial fraction of the E' centers are positive and compensated by trapped negative charge [155]. In addition to the E'$_\gamma$ center, several other types of defect centers have been identified. One of these is a relatively new class of defect center which has been categorized as a delocalized spin center [153,154,156]. The defect center is delocalized in the sense that the unpaired electron is not associated with any one particular atom. Both E'$_\gamma$ and delocalized spin centers have also been identified in BESOI material [157]. The delocalized spin center in BESOI material was found to be hydrogen related [158]. In BESOI material, the radiation-induced EPR centers are located

near the bonded interface [114]. Therefore, the bonded interface is a potential hole-trap site and may lead to radiation-induced back-channel leakage. In addition, to the defects in BESOI buried oxides, EPR has also identified a new oxygen-related donor defect in the silicon substrate near the bottom Si/SiO$_2$ interface [158]. The donors appear to result from the nonoxidizing anneal during the bonding process. These donors are also present in SIMOX material [159] and may change the doping concentrations of the substrates.

4.4.3 Techniques for Reducing Back-Channel Leakage

One method that can be used to eliminate back-channel effects is the use of gate-all-around transistors [160]. In these transistors, the gate oxide completely surrounds the body region (both top and bottom) and no back-channel exists.

As discussed above, some SIMOX implant and anneal conditions can lead to reduced radiation-induced charge generation and, therefore, less back-channel leakage current. For instance, buried oxides formed using supplemental [141-143] and multiple [161] implant and anneals show less radiation-induced degradation than buried oxides formed with a single implant. Both the number of radiation-induced interface traps and the concentration of oxide-trapped charge was significantly reduced for buried oxides formed using multiple implants [161]. Lowering the oxygen implant dose and nitrogen implantation have also been suggested [162] as methods for hardening SIMOX buried oxides. For the nitrogen annealed buried oxides, the improvement in hardness has been attributed to the formation of an interfacial oxynitride layer [162].

In addition in techniques for hardening the buried oxide other techniques have been suggested for minimizing back-channel leakage current. A heavily doped layer near the back-gate interface can minimize back-channel leakage current [163]. A deep boron implant has been used in n-channel transistors to reduce back-channel leakage currents [164,165]. If available, a -5 V bias applied to the substrate can minimize back-channel leakage of n-channel transistors without affecting the performance of p-channel transistors [166] as shown in Fig. 34.

A deep germanium implant (as used to reduce parasitic bipolar gain effects to improve SEU performance, see Section 3.1.3) can be used to minimize back-channel leakage current. A deep germanium implant will create defects in the body region near the back-channel. These defect centers will reduce the back-channel mobility and increase the back-channel threshold voltage by pinning the back-channel Fermi level. This will help to suppress radiation-induced back-channel leakage current for fully-depleted transistors [167].

5.0 HIGH DOSE RATE TRANSIENT EFFECTS

High dose rate pulses of ionizing irradiation produce many electron-hole pairs in a short period of time. The concentration of radiation-induced electrons and holes can be many times greater than the doping concentrations in the silicon. Photocurrents will be generated that may

cause temporary loss of stored information or disrupt functional operation of an IC (dose rate upset) or in some cases cause permanent damage to a device. In this section, we review high dose rate transient ionizing radiation effects on SOI MOS circuits and differences between the response of SOI and bulk-silicon ICs.

5.1   SOI Device Response

In many regards, the response of an IC to a high dose rate pulse of ionizing radiation is similar to the response of an IC to a heavy-ion strike. However, there are some major differences. A heavy-ion strike produces charge over a very narrow region in the device; whereas, a pulse of radiation produces charge uniformly throughout the device. The time scales are also considerably different. The time scale for charge collection induced by a heavy-ion strike is generally much shorter than device response. In contrast, a pulse of irradiation normally generates photocurrents that occur over a much longer time period and the photocurrents can exist for relatively long times as compared to device response times. The current density generated by a pulse of ionizing irradiation also is normally much lower in magnitude than for a heavy-ion strike.

As mentioned in Section 4.1, a single high-energy gamma ray, proton, or electron can generate thousands or even millions of electron hole pairs. Once generated, the electrons and holes can be collected at a device junction or circuit node where they can contribute to a photocurrent. The transport of electrons and holes normally occurs due to either the drift of carriers under the influence of an electric field or diffusion of carriers due to carrier-concentration gradients. The drift of carriers occurs within short times after a pulse of radiation (within hundreds of picoseconds). The drift contribution of photocurrent occurs primarily for carriers generated within the depletion region of a p-n junction. It has often been referred to as the prompt component of photocurrent. Diffusion of carriers takes place over much longer time periods than for the drift of carriers and has often been referred to as the delayed component of photocurrent. Carriers generated within approximately one diffusion length of a p-n junction can contribute to the diffusion component. The diffusion of carriers occurs over much longer time periods (up to hundreds of nanoseconds to microseconds) than the drift component. Once carriers transport to within the depletion region of a p-n junction by diffusion, they will be rapidly collected by drift.

The two most common mechanisms by which a transient radiation pulse can cause upset of a memory cell are rail-span collapse and local photocurrent induced upset [168-170]. Local photocurrents add together and flow through the power supply bus lines to the bias supplies. Because of the finite resistance of the power supply lines, the photocurrent will produce a voltage drop along the power supply bus lines. As a result, the bias voltage at individual circuit elements will be lower than the bias supply voltage. If the voltage drop is large enough, an upset of the memory can occur. This has been referred to as rail-span collapse [169,170]. In an SRAM cell, local photocurrents can cause upset by charging the p-channel drains of both halves of the memory cell [168]. If the potential at the drains become sufficiently close an upset will occur. P-channel transistors normally result in greater charging than n-channel transistors because p-

channel transistors normally are larger in area [168]. If circuits are designed to minimize rail-span collapse, local photocurrents often dominate circuit upset [168].

Other mechanisms can also cause memory upset. As discussed in Section 4.2, at short times after a pulse of irradiation, holes generated in the oxide can produce large negative threshold-voltage shifts for both p-channel and n-channel transistors. These large threshold-voltage shifts in some cases can cause IC failure. Another mechanism for upset is lateral voltage drops induced by the large local photocurrents. Because of lateral resistances along the surface of the device, photocurrents will induce voltage drops along the surface. If these voltage drops are large enough, circuit upset can occur.

The carriers collected by diffusion or drift will contribute to a local photocurrent, e.g., the photocurrent for a single p-n junction. The magnitudes of local photocurrents generated by a transient pulse of ionizing irradiation are roughly proportional to p-n junction area. Because SOI transistors are built on an insulating layer (as opposed to an n- or p-well), the magnitudes of local photocurrents are significantly lower and upset levels are order of magnitudes higher for SOI ICs than for bulk-silicon ICs. The absence of four layer p-n-p-n paths makes SOI ICs immune to transient latchup.

However, parasitic bipolar gain effects limit the transient upset hardness of SOI ICs. The parasitic bipolar gain mechanisms for transient pulse effects are similar to those for SEU effects (discussed above). As a result, transient upset tests show larger photocurrents than predicted from volumetric photocurrents generated in the active region [164]. These larger photocurrents were attributed to the bipolar effect. Parasitic bipolar gain effects on the dose rate response of a SOI transistor are illustrated in Fig. 35 [171]. This curve was determined by SPICE simulations for a partially-depleted transistor with a body tie. For dose rates below ~5x10^{11} rad(Si)/s the drain current increases linearly with dose rate. As the dose rate is increased above ~5x10^{11} rad(Si)/s, the drain current increases rapidly with dose rate. This is a result of parasitic bipolar gain effects. At very high dose rates, the increase in drain current with dose rate becomes lower due to high injection effects. At these dose rates the minority carrier concentration becomes comparable to the majority carrier concentration and the body doping is effectively reduced. This causes a reduction in the parasitic bipolar gain.

Nevertheless, very high transient upset levels have been observed for SOI ICs [164,172]. Figure 36 is a plot of the number of upsets versus dose rate for a 4k SRAM for pulse widths of 13 and 70 ns [172]. Upsets were detected at dose rates of 7.7x10^{10} rad(Si)/s and above with 13 ns pulse widths and at dose rates of 4.2x10^{10} rad(Si)/s and above with pulse widths of 70 ns. These results were obtained without the use of body ties or other techniques for minimizing the bipolar effect. The dose rates for circuit upset for these SOI circuits are more than two orders magnitude higher than for similar bulk-silicon circuits.
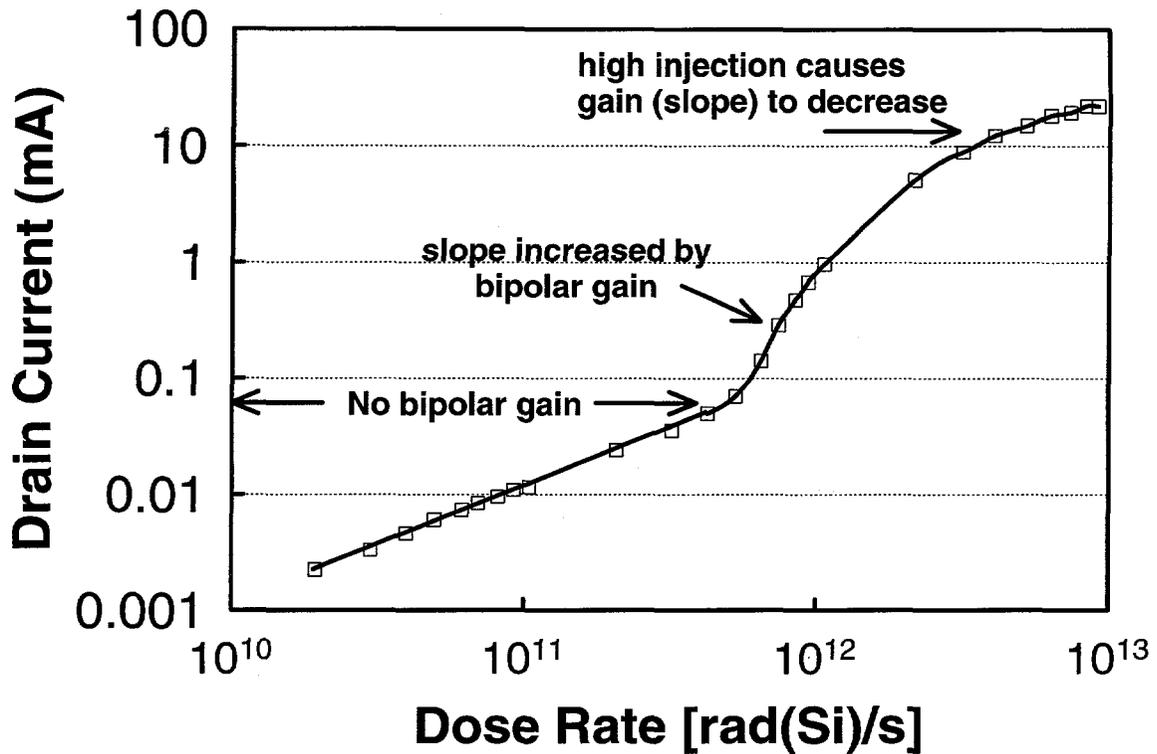
Figure 35: Simulated increase in drain current with dose rate for a SOI partially-depleted transistor. (After Ref. 171)

5.2 Hardening SOI ICs to Dose-Rate Upset

Techniques for improving the hardness of SOI ICs to transient radiation effects are centered around techniques for reducing parasitic bipolar gain effects. The most common method to harden SOI ICs is to use body ties [35,163,171,173]. The use of body ties was discussed in Section 3.1.3. In fact, body ties are more effective at reducing or eliminating parasitic bipolar gain effects for transient pulses of ionizing radiation than they are for reducing parasitic bipolar gain effects for heavy-ion strikes [35]. For dose rates important for nuclear weapon effects, the charge induced by a pulse of radiation has only a small effect on carrier lifetime or conductivity. Hence, the body resistance and bipolar gain are only slightly affected by conductivity modulation [35].

Another method proposed for reducing the parasitic bipolar gain effect is to reduce the carrier lifetime in the body region. For example, neutron irradiation [163] has been proposed as a method for improving the transient upset hardness of SOI devices. Neutron irradiation causes displacement damage (discussed in Section 6 below) that will result in deep level traps and a reduction in carrier lifetime. Proper adjustment of lightly doped drain [163] and source
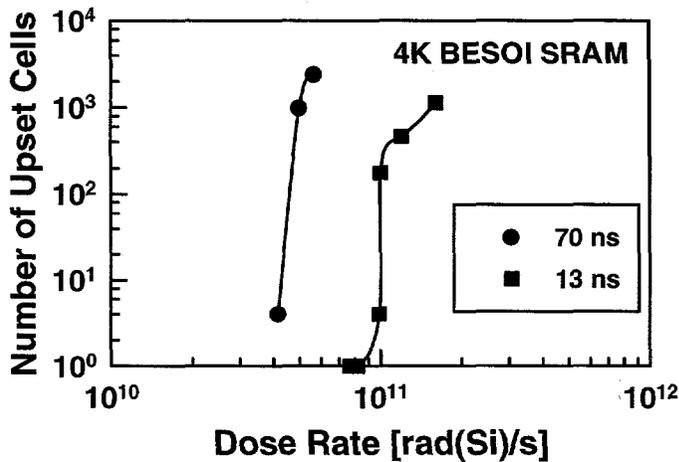
Figure 36: Transient upset levels for a SOI 4k SRAM. (After Ref. 172)

structures [174] can also reduce the bipolar effect by reducing the amount of impact ionization [163] at the drain and increasing the recombination rate of carriers near the source [174].

5.3 Upset Mechanisms in Bulk-Silicon Devices

Figure 37 illustrates possible junctions where photocurrents can be collected in a typical CMOS inverter [175]. Any area that includes a p-n junction accessible to either the drift or diffusion of carriers will contribute to the photocurrent. Because electrons and holes are generated throughout the semiconductor, the collected photocurrent will be approximately proportional to the junction area. Thus, for the p-n junctions illustrated in Fig. 37, the largest contributor to the photocurrent will be the p-well to n-epi junction (nonexistent in SOI ICs). The local photocurrents add to together creating large photocurrents along power supply rails. The large local photocurrents generated at p- and n-well to substrate junctions and rail-span collapse will result in low transient upset levels for bulk-silicon ICs.

The high photocurrents caused by a high-dose rate pulse of ionizing irradiation can trigger latchup in silicon CMOS ICs and other silicon ICs with four-layer p-n-p-n paths. The mechanisms for generating latchup are similar to those for generating latchup due to a heavy-ion strike discussed above.

Gold doping [176] and neutron irradiation [177] have been suggested as means for reducing the minority carrier lifetime and lowering the bipolar current gains of parasitic transistors. For small geometry transistors these methods become less effective [178]. Using heavily doped substrates with an epitaxial layer reduces latchup susceptibility by shunting the substrate resistance and raising the holding current to either a level beyond the capability of the power supply or to the region of current gain fall-off with collector current such that regeneration cannot occur [178,179].

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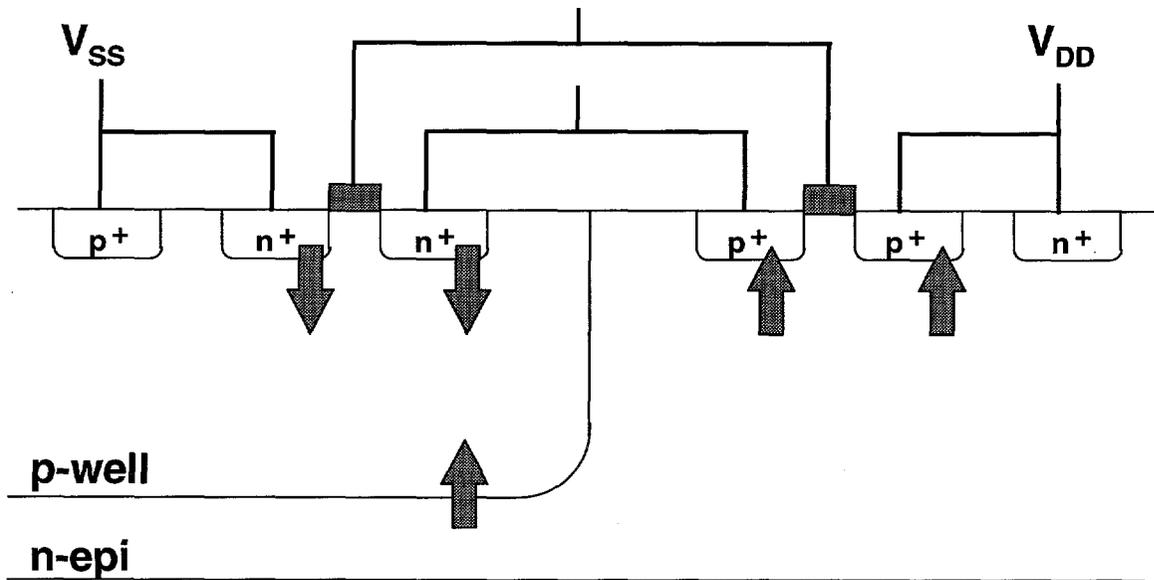
Figure 37: Cross section of a CMOS inverter illustrating possible paths for photocurrent generation. (After Ref. 175)

6.0 DISPLACEMENT EFFECTS

In this section, we give a very brief overview of the basics of displacement damage in materials. In addition to ionization effects, high-energy protons and neutrons can also cause displacement damage in silicon and other semiconductor materials [50,180-182]. As a high-energy proton or neutron collides with an atom, the atom will recoil from its lattice site. If the energy transferred to the atom is high enough, the atom can be knocked free from its lattice site to an interstitial site. The minimum energy required to knock an atom free of its lattice site is called the displacement threshold energy. As the atom is displaced from its original position it leaves behind a vacancy. The combination of the interstitial atom and its vacancy is called a Frenkel pair. If the displaced atom has sufficient energy it can in turn displace other atoms. Thus, for very high energy recoils a defect cascade can be created with large defect clusters. A typical distribution of clusters produced by a 50-keV silicon recoil atom is illustrated in Fig. 38 [180]. As the primary silicon atom travels through the silicon, it knocks free other atoms and it is in turn reflected, altering its path. Towards the ends of the paths of the reflected atoms (and the primary atom) large clusters of defects may be formed (terminal clusters). About 90% of the displaced atom and vacancy pairs recombine within a minute after irradiation at room temperature.
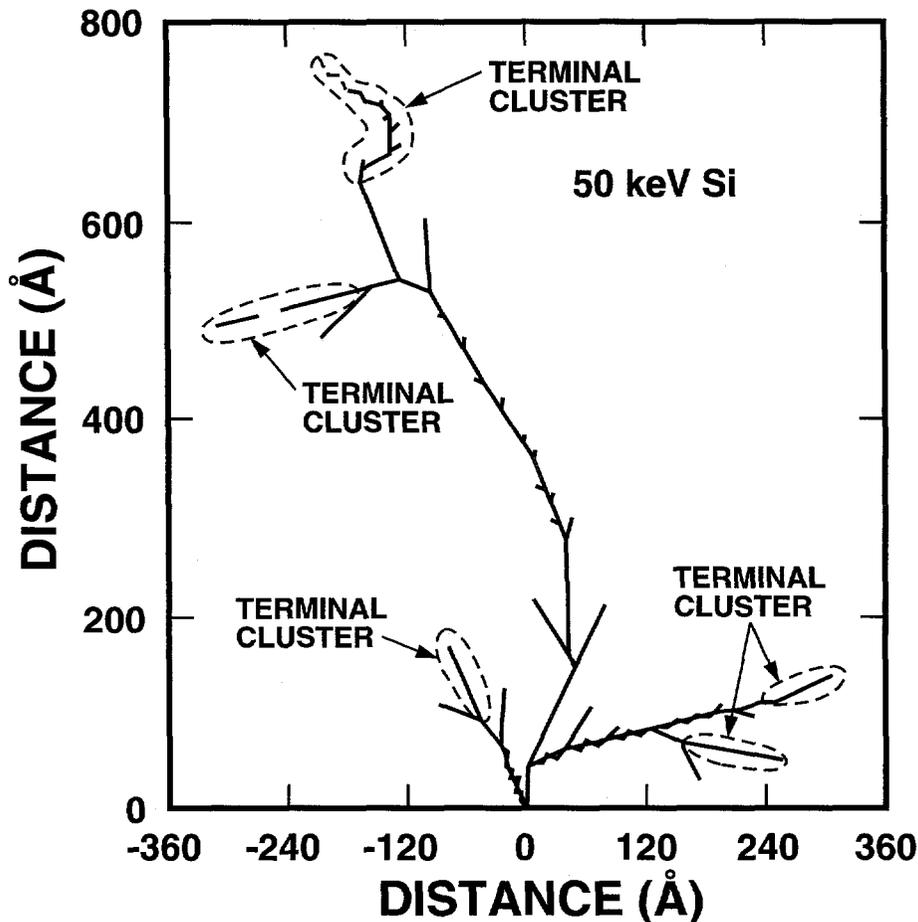
Figure 38: Defect cascade created by a 50-keV silicon recoil atom. (After Ref. 180)

The primary effect of displacement damage is the creation of deep and shallow level traps in the material [180-182]. The shallow level traps can compensate majority carriers and cause carrier removal. Deep level traps can act as generation, recombination, or trapping centers. These centers can decrease the minority carrier lifetime, increase the thermal generation rate of electron-hole pairs, and reduce the mobility of carriers. As a result, displacement damage is a concern primarily for minority carrier (e.g., bipolar transistors) and optoelectronic devices. It is relatively unimportant for MOS transistors.

7.0 APPLICATIONS

As discussed above, the major radiation-hardness advantage of SOI technology results from the reduced charge collection volume. This leads to orders of magnitude improvements in transient ionizing radiation hardness and reduced sensitivity to single-event upset due to heavy-ions. Latchup will not occur for SOI ICs under any condition. Bulk-silicon circuits can be made hard to heavy-ion strikes (both upset and latchup) if circuit performance is compromised. For instance, feedback resistors can make bulk-silicon ICs hard to all practical space environments at
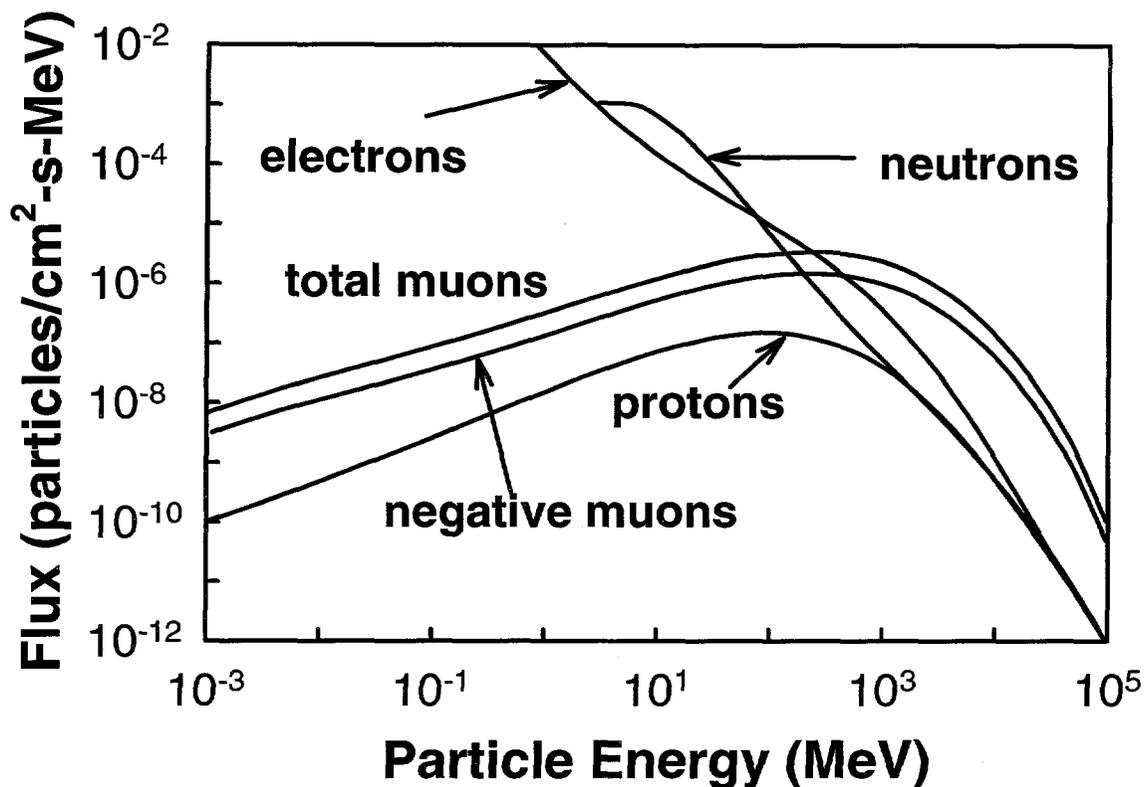
Figure 39: Energy spectrum of cosmic particles at sea level. (After Ref. 181)

the expense of increased timing delays. As such, two large application areas for SOI ICs are space and nuclear weapon environments requiring high-performance (e.g., speed and low power) ICs.

One example of system errors that could have been avoided in a space system if SOI ICs were used is the Hubble telescope [183]. Information used to control fine focusing in the Hubble telescope is stored in silicon bipolar SRAMs. Each time that the telescope passes over the South Atlantic Anomaly, these parts upset at a very high rate due to high fluxes of protons. The problem has now been circumvented by scrubing (performing error correction) on a more frequent basis.

Another harsh environment that can benefit from the hardness advantages of SOI circuits is that of high-energy particle accelerators. The development of supercolliders (e.g., CERN) requires electronics that can survive total doses from 10 to 100 Mrad(SiO$_2$). Devices also must be able to survive without upset or latchup the heavy particle jets and secondary cascades associated with the accelerators. The heavy particle jets and secondary cascades are similar to the cosmic ray heavy ions. SOI ICs have been made using closed geometry transistors and body

ties that can survive total doses up to 100 Mrad(SiO_2) [184]. SOI technology also provides these devices with good SEU immunity.

In addition to being susceptible to soft errors due to cosmic rays in the space environment, advanced silicon ICs also will be susceptible to single-event upset on earth and in low altitude aircraft due to cosmic rays that penetrate the earth's atmosphere and due to energetic particles emitted from other sources. For example, it is well known that the alumina of ceramic packages, gold bond wires, and other materials common to IC packages contain trace amounts of ^{238}U [185]. As ^{238}U spontaneously decays to a stable isotope it emits an alpha particle. Alpha particles can have LETs high enough to cause SEU in commercial ICs. If the alpha particles are generated outside the IC substrate, they can be effectively attenuated using polyimide or other insulating coatings on the IC. These problems can be reduced or mitigated by using SOI technology.

Cosmic rays at the earth's surface consist primarily of neutrons, protons, electrons, and muons (an unstable elementary particle with a mass of about 207 times that of an electron). The flux of these particles at about 40° north geomagnetic latitude for particle energies from 1 keV to 10^5 MeV is shown in Fig. 39 [186]. Those particles most important for SEU are protons and neutrons. Shielding of these particles is normally not practical. The LETs of both neutrons and protons are too small to directly cause SEU in present-day ICs. However, both neutrons and protons can generate secondary particles (e.g., alpha particles) by nuclear interactions with LETs high-enough to cause SEU. If the secondary particles are generated in the IC, they can lead directly to SEU. One source of alpha particles within an IC is the nuclear interaction of boron with cosmic ray neutrons [187]. Boron is commonly used in many IC processes. If ^{10}B (~19.9% abundance in naturally occurring boron) absorbs a thermal neutron, it can emit an alpha particle with an energy of 1 MeV [187]. The flux of alpha particles generated by the nuclear interaction of ^{10}B and cosmic-ray neutrons is estimated to be 0.02 alpha particles/hr-cm^2. Assuming typical doping densities and geometries used in a DRAM, the collected charge was estimated to be 65 fC over a 5-μm range for alpha particles [187]. Obviously, by reducing the amount of boron used in processing, the number of alpha particles generated can be reduced. These data indicate that advanced bulk-silicon ICs potentially may be susceptible to SEU failure from a number of sources in ground-based systems. Thus, unless steps are taken to mitigate or reduce these effects (such as using SOI technology), the reliability of future bulk-silicon ICs may be significantly degraded.

Even though the flux of cosmic rays is orders of magnitude lower at an altitude of 30,000 feet than it is at an altitude of 65,000 feet, neutrons (and secondary protons) have also been observed to cause upset in aircraft avionics [188,189]. Neutrons and secondary protons are the primary cosmic ray products responsible for causing upset in aircraft microelectronics.

Therefore, the improved single-event upset hardness not only results in application areas for high-performance SOI ICs for space and nuclear environments, but it also results in application areas for *all* future advanced high-performance ICs, regardless of where they are used. It is expected that as device dimensions continue to be reduced and circuit complexities continue to increase, the importance of SEU on device reliability will become a major area of

concern and technologies like SOI will be required to meet the reliability requirements for future technologies.

8.0 SUMMARY

We have covered the basic mechanisms of radiation effects on SOI and bulk-silicon MOS device performance in the natural space and nuclear radiation environments. The natural space and nuclear radiation environment can cause significant damage to spacecraft electronics. These environments can cause degradation through total-dose ionizing radiation damage, single-event related soft and hard errors, transient upset, and displacement damage.

Heavy-ions in the space environment can cause both soft and hard errors. Four types of hard errors for bulk-silicon ICs are single-event latchup, single-event snapback, single-event burnout, and single-event gate rupture. Because of the large charge collection depths for bulk-silicon ICs, they are very prone to single-event upset. The upset susceptibility will continue to get worse as device dimensions continue to decrease. Techniques for hardening bulk-silicon ICs result in performance penalties. The reduced charge collection volume of SOI ICs leads to significant improvements in SEU hardness as compared to that for bulk-silicon ICs. Excellent SEU hardness for SOI ICs have been obtained without the use of hardening techniques that degrade IC performance. However, parasitic bipolar effects can limit their SEU hardness. Because SOI ICs do not contain four layer n-p-n-n paths and multiple layer structures, single-event latchup and single-event burnout do not occur for SOI ICs.

The mechanisms for total-dose ionizing radiation effects in SOI ICs are similar to those for bulk-silicon ICs. However, the buried oxide adds an extra degree of complexity in hardening SOI ICs to total dose. Techniques are available to harden both SOI and bulk-silicon ICs to total dose. SOI ICs with closed geometry transistors have been fabricated with hardness levels up to 100 Mrad(SiO_2).

The reduction in charge collection volume also leads to orders of magnitude increases in the transient ionizing radiation upset levels for SOI ICs over bulk-silicon ICs. For bulk-silicon ICs, the transient dose rate hardness is limited by large p-n junctions that can generate large photocurrents leading to low transient upset levels and device latchup. Parasitic bipolar gain effects also limit the transient upset hardness of SOI ICs. However, SOI ICs can be hardened to transient upset with the use of body ties and other methods that reduce the parasitic bipolar effect.

The improved transient and SEU hardness of SOI ICs make them attractive for applications requiring high-performance ICs capable of withstanding the harsh space or nuclear radiation environment. As device dimensions continue to decrease and circuit complexities continue to increase, future advanced bulk-silicon ICs in ground-based and aircraft systems may also be prone to reliability problems caused by SEU from cosmic ray particles penetrating the earth's atmosphere and due to energetic particles generated in packaging and other materials.

Thus, SOI technology may see increased use in order to minimize the effects of SEU on advanced technologies.

Acknowledgments

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