Multi-Channel SiPM Readout ASIC with Digital Interface

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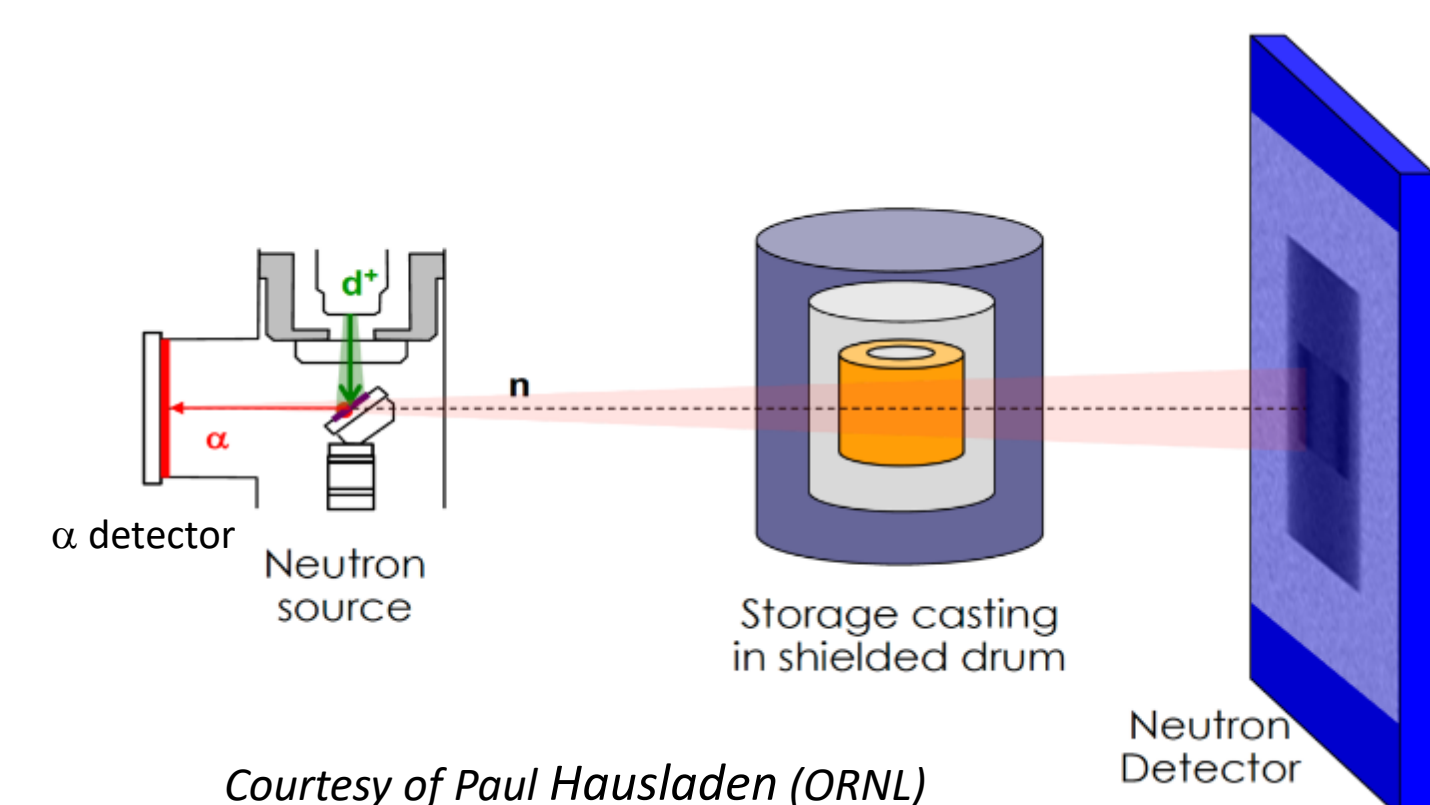LBNL[1], SNL[2]

Goals and Objectives

Develop a custom Application-Specific Integrated Circuit (ASIC) that, when used with commercially available Silicon Photomultiplier (SiPM) sensors, will enable new fieldable radiation detectors with significantly reduced size, weight, and power than currently available.
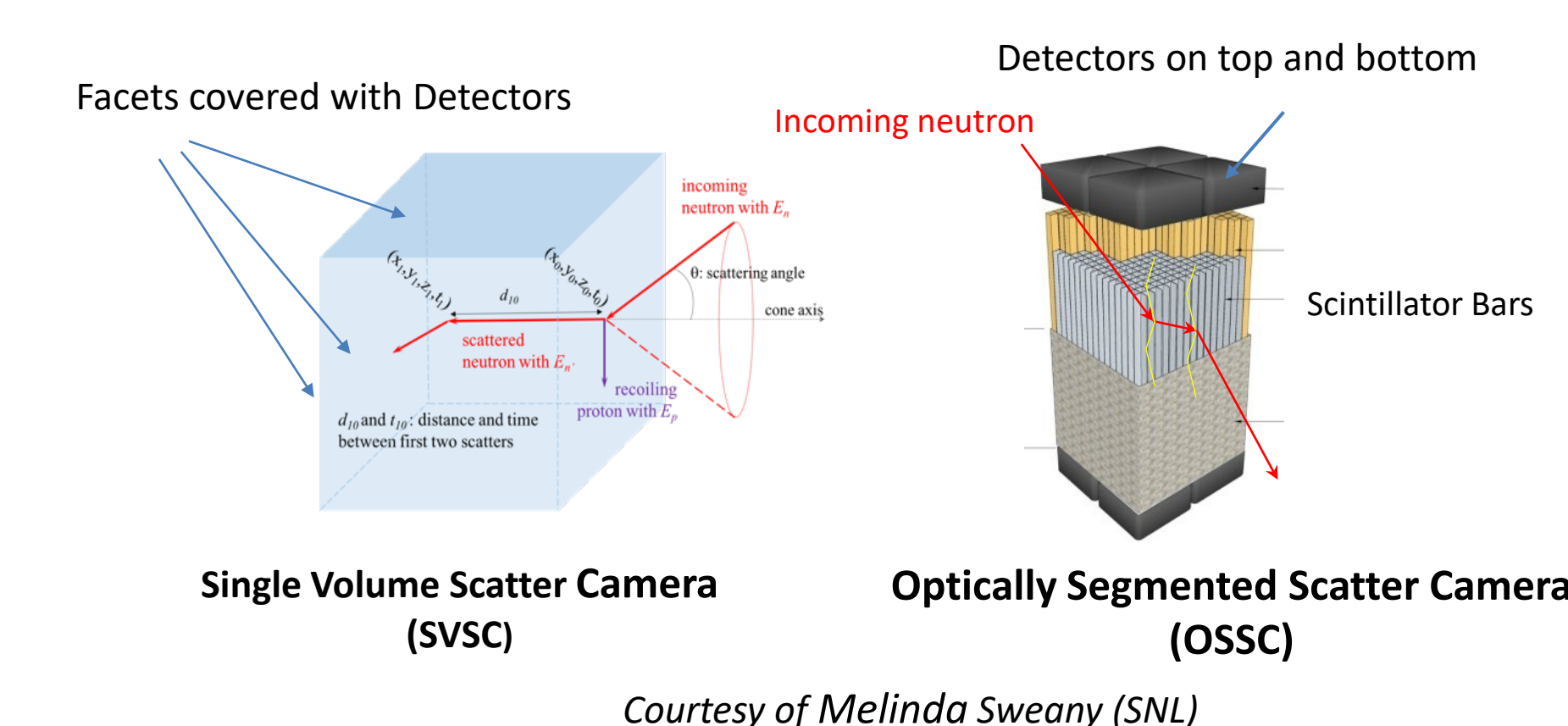
Introduction

Potential end-use applications were identified in a prior, dedicated ASIC scoping study.

We target four core applications:
▶ Neutron Radiography and Associated Particle Imaging (API)

Courtesy of Paul Hausladen (ORNL)

▶ Single Volume Scatter Camera
  ▪ Monolithic geometry readout
  ▪ Optically segmented geometry readout

Single Volume Scatter Camera (SVSC)   Optically Segmented Scatter Camera (OSSC)
Courtesy of Melinda Sweany (SNL)

Requirements

Requirements for the ASIC, along with the driving application, are given in Table 1,

Specification	Value	Apps
SiPM Interface		
Number of channels	64	All
Detector Capacitance/ch	4.2 nF	API
Bias tuning range/ch	none	All
Energy and Pulse Shape Measurement		
Discriminate n/g	Yes	Rad../API/OSSC
Measure single PE events	Yes	SVSC
Accuracy	> of 1 PE or 1%	Radiography
RMS noise	<1 PE	All
Dynamic Range	$1-10^5$ PE	Radiography
Time Measurement		
Accuracy	200 ps	SVSC / OSSC
Resolution	100 ps	SVSC / OSSC
Range	1us	SVSC / OSSC
Trigger Requirements		
Trigger thresholds	Global with <1PE resolution	ALL
Dead Time	<150ns /trig chan	Radiography / API
Average Trig Rate/ ch	450K CPS	API Particle
System Interface		
Interface	analog or digital	ALL
Power Dissipation/ ch	1 mW	SVSC / OSSC

Table 1. ASIC Specifications

Design Approach

The ASIC will provide a simple interface to the system. Architecture shown in Figure 1.

▶ Serial (SPI) interface for app configuration and status
▶ 125 MHz reference clock to be provided by the system
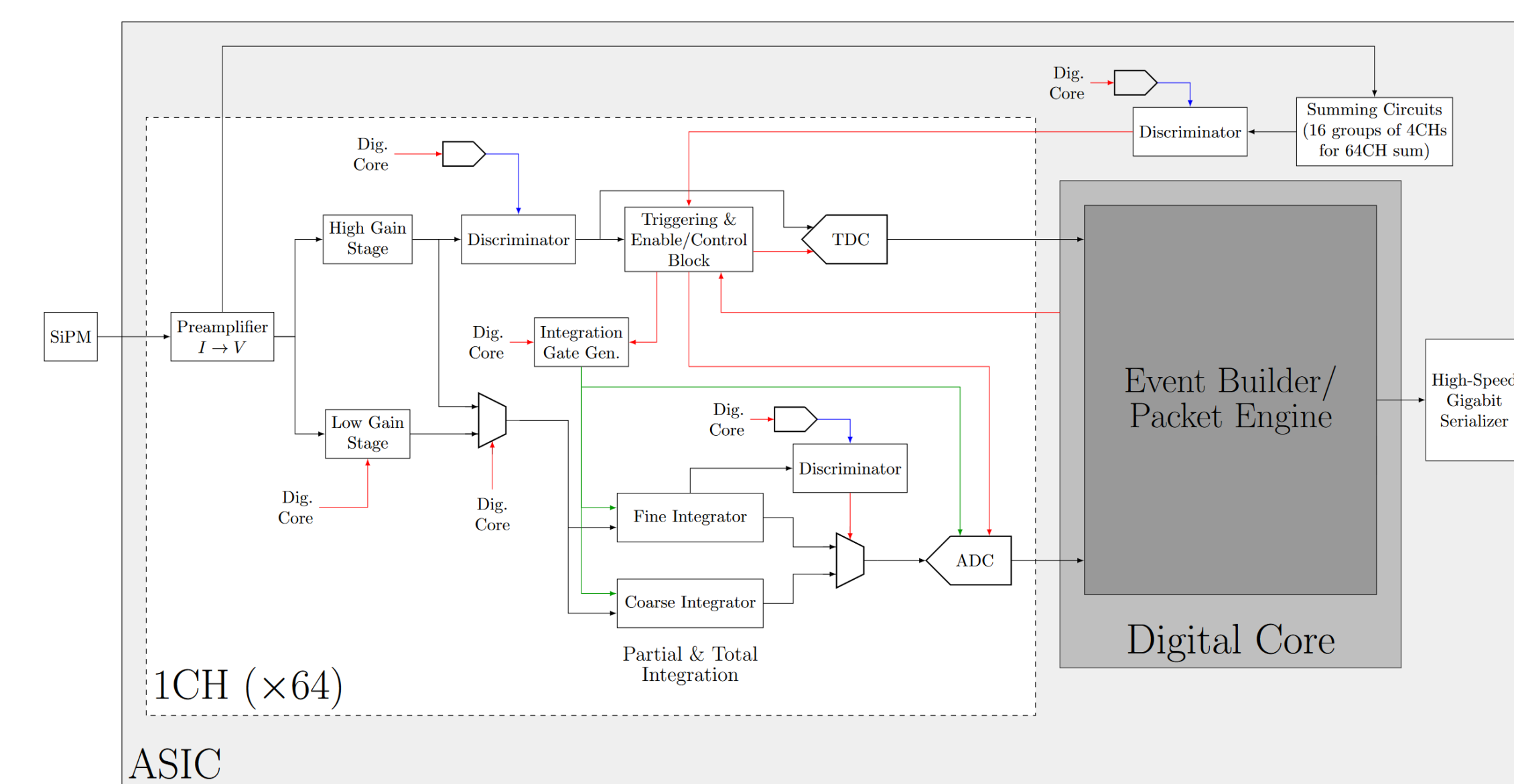▶ 1.25 GBPS serial data link from the ASIC to the system

Figure 1: ASIC Architecture

▶ Packetized Event Data
  ▪ Energy, Time Tag, neutron/gamma pulse shape discrimination (PSD)
  ▪ The PSD/pileup tagging engine will allow for identifying hits as either neutron or gamma while monitoring for pileup events.
▶ Flexible Triggering and coincidence options
  ▪ 4 triggering modes implement custom trigger requirements per application
▶ 64 channel SiPM interface will support a variety of commercially available common cathode SiPMs and scintillators

▶ Energy and PSD measurements will be implemented with variable-time and gain integration
  ▪ Wide dynamic range and 1 PE accuracy at low end necessitates using a high gain and low gain integrator in parallel
▶ Two-threshold Discriminator
  ▪ Low-threshold used as time-tagging fiducial
  ▪ High-threshold used for dark count or low energy event discrimination

▶ Scatter Camera inter-chip coincidence supported as seen in Figure 2
  ▪ (a) system level coincidence for single PE event reduction
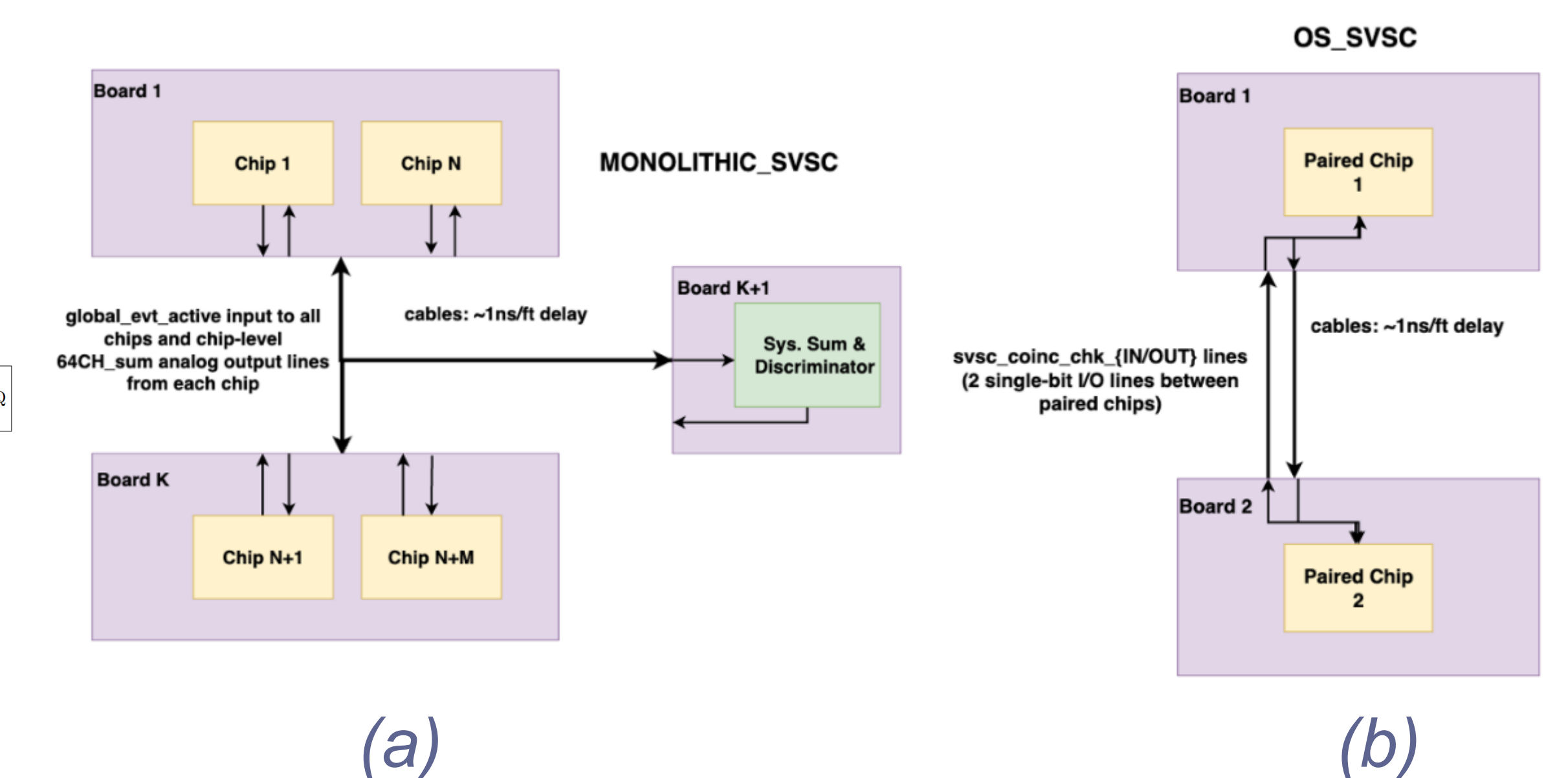 ▪ (b) Paired top and bottom ASIC coincidence for optically segmented scatter camera false event reduction

Figure 2: (a) System and (b) Paired Chip Coincidence

Schedule

Task	FY24				FY25				FY26			
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Requirements Definition												
ASIC Conceptual Design and requirements flow down												
ASIC Design												
ASIC Preliminary Design												
Conceptual Design Review				X								
ASIC Detailed Design and simulation												
Critical Design Review							X					
Fabricate Rev 1 - 65nm process												
Rev 1 ASIC Test and Evaluation												
ASIC Rev2												
Incorporate lessons learned												
Fabricate Rev 2 - 65nm process												
ASIC Test and Evaluation Rev 2												
Incorporate lessons learned												
Fabrication												
Test and Evaluation												
Final Report												X

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