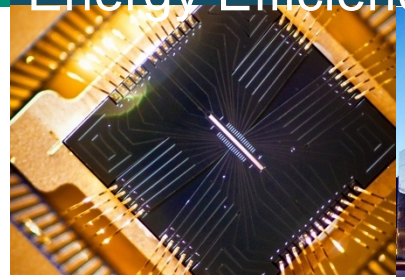
SAND2024-06396C

Sandia National Laboratories

Pathfinding Process Development for the Realization of Atomic Precision Advanced Manufacturing (APAM)-Based Vertical Tunneling Field Effect Transistors for Enhanced Energy Efficiency



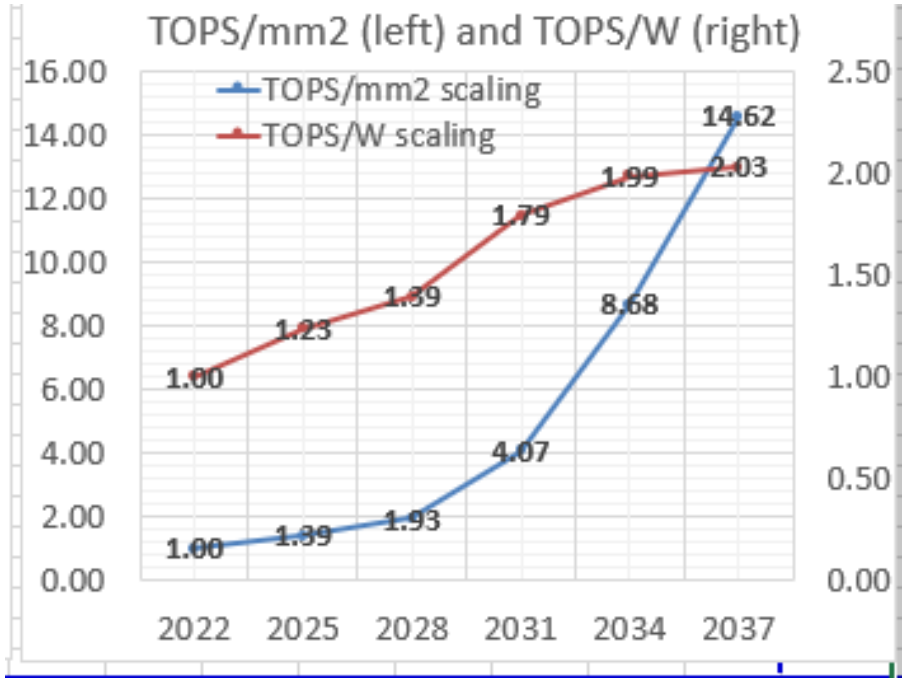
Evan M. Anderson, *Christopher R. Allemang, Christopher Arose, Tzu-Ming Lu, Scott W. Schmucker, Thomas R. Sheridan, Jeffrey A. Ivie, DeAnna M. Campbell, Ashlyn P. Vigil, Alisha G. Hawkins, Philip A. Gamache, Xujiao Gao, Thomas A. Weingartner, Shashank Misra*

Sandia National Laboratories is a multimission laboratory managed and operated by National Technology & Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.

U.S. DEPARTMENT OF ENERGY NNSA

Why TFETs? End of Dennard scaling & the Boltzmann limit

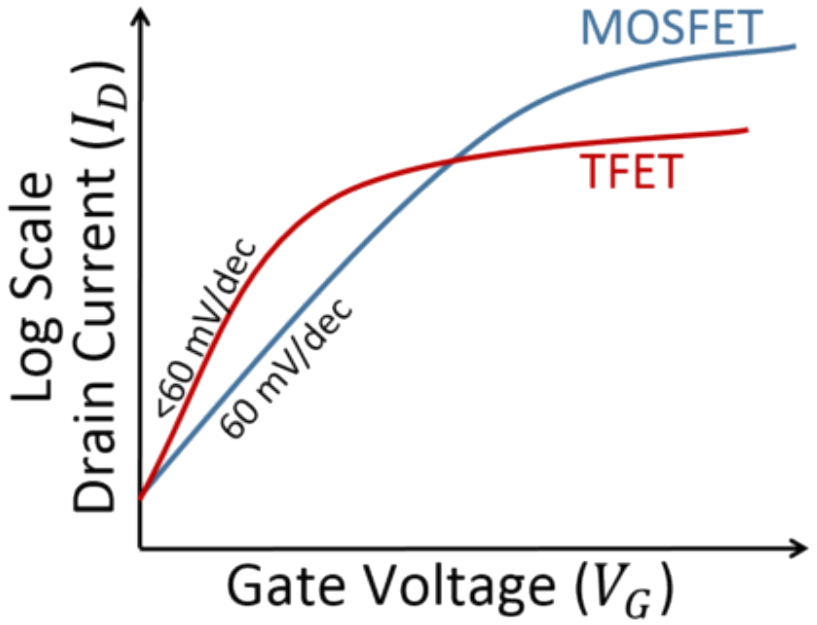
What does transistor scaling get you?



IRDS 2022

Dennard scaling (1975-2005): 500x increase in perf/watt
Transition (2005-2022): decreasing perf/watt improvement
Post Dennard (2022-2037): 2x increase in perf/watt

Dennard scaling requires a constant electric field

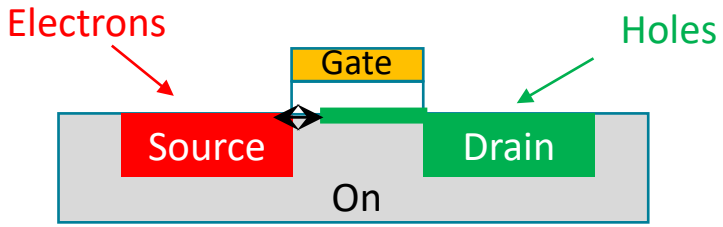


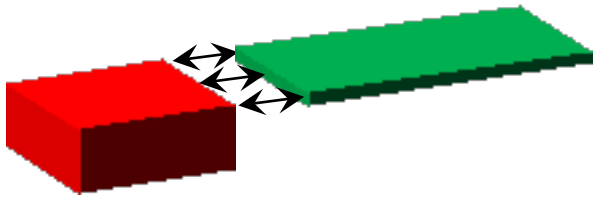
We are close to the theoretical limit for MOSFET energy efficiency

Tunnel field effect transistors (TFETs) may provide a path to lower voltage operation, but have not lived up to their promise in practice

Why are vertical TFETs interesting?

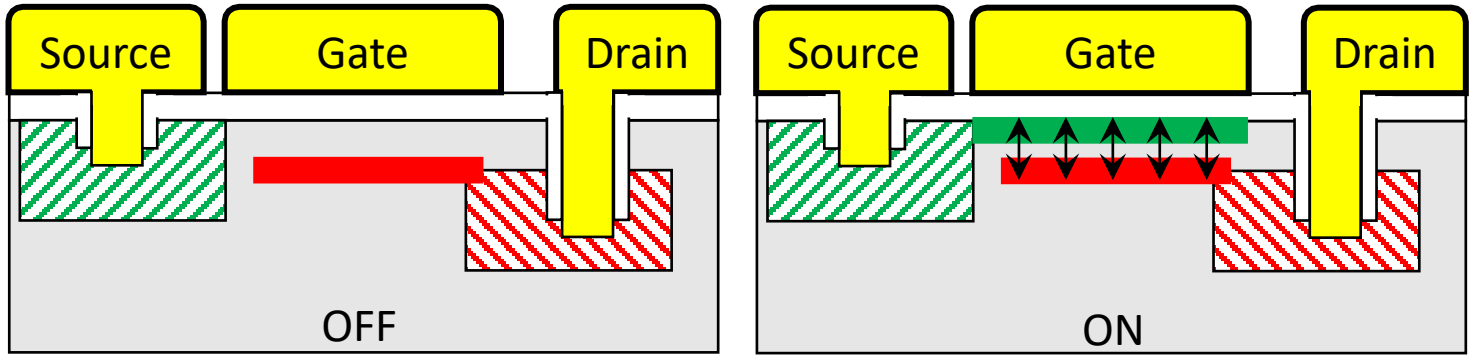
Traditional TFET

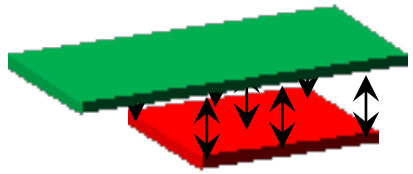




Current scales with linear dimension
Manufacturing limitation to subthreshold slope

Vertical geometry





Current scales with area, like a diode
Quantum limitation to subthreshold slope

Vertical TFET solves problems with current density

→ Important to understand process variability from epitaxy through fabrication

How does atomic precision advanced manufacturing work?

APAM flow

Oxide

Ex situ prep

Ward, Appl. Phys. Lett. (2017)

T ~ 1000° C

In situ clean

H termination

Patterning

PH_3 incorp.

T < 400° C

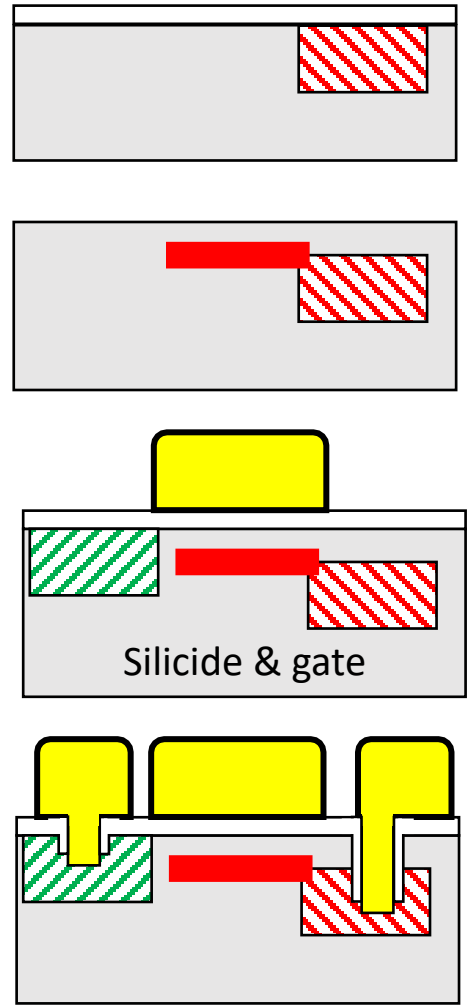
Si capping

Normal doping:
Dopant donates electron to silicon

VB

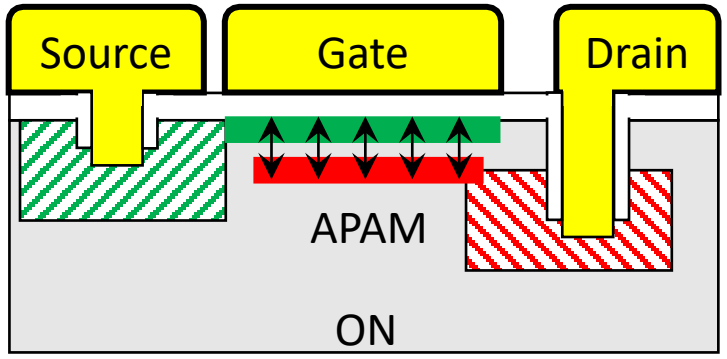
Ultra-doping:
dopant potentials overlap significantly

TFET flow

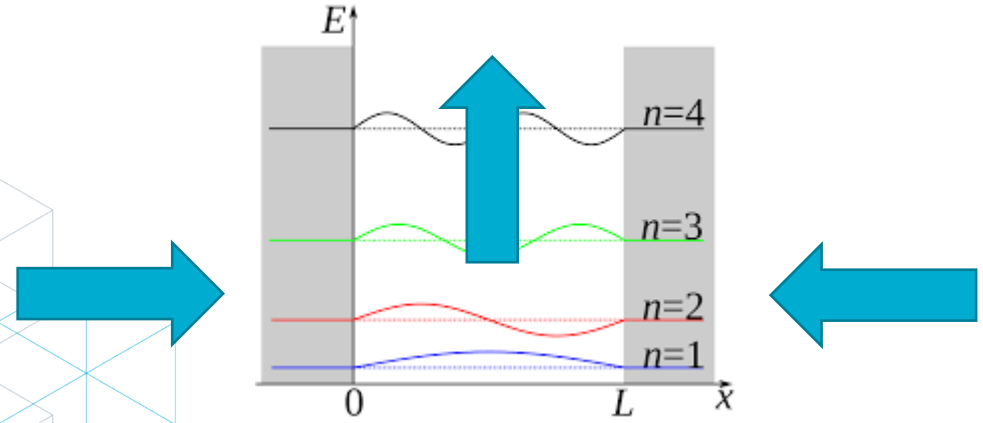


APAM produces atomic-scale abruptness, ultra-high n-type carrier density, confinement → all needed for VTFET to function

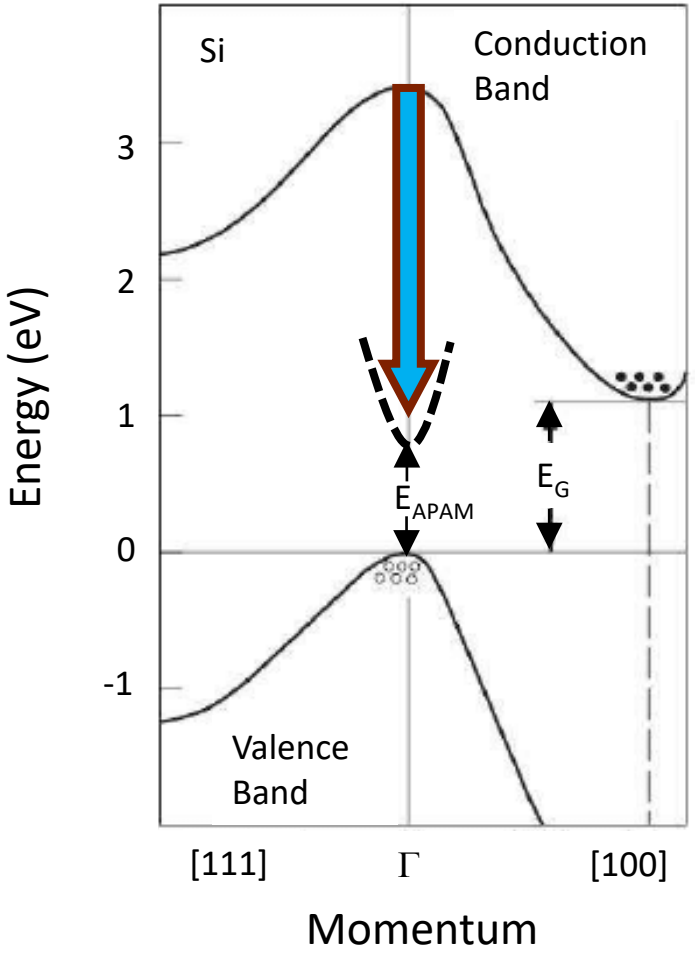
Band-to-band Epitaxial Area tunneling TransistorS (BEATS)



→ Should not deplete when gate field increases



→ Size quantization should be irrelevant

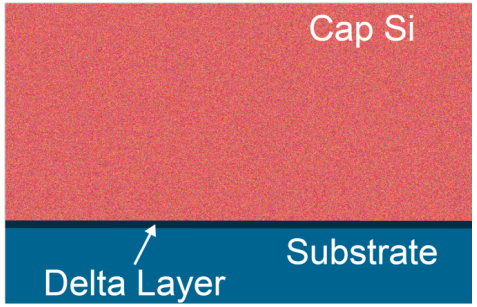


→ Many sub-bands occupied, not just heaviest ones (least tunneling)

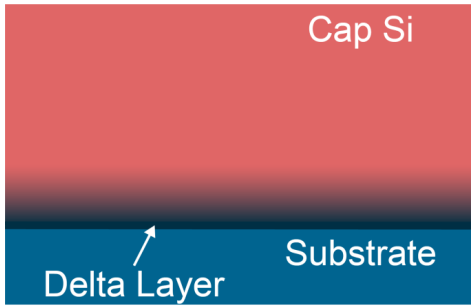
Tunnelling process is sensitive to the thickness and quality of Si above the APAM layer

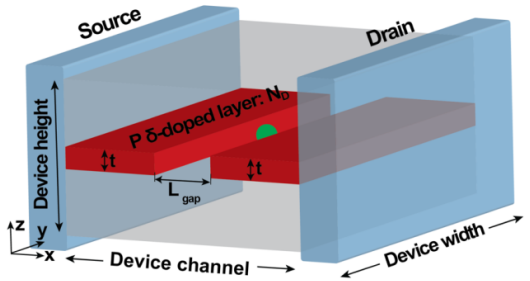
Epi Silicon Layer Growth Condition Tradeoffs

Lowest Temperature Growth



Higher Temperature Growth

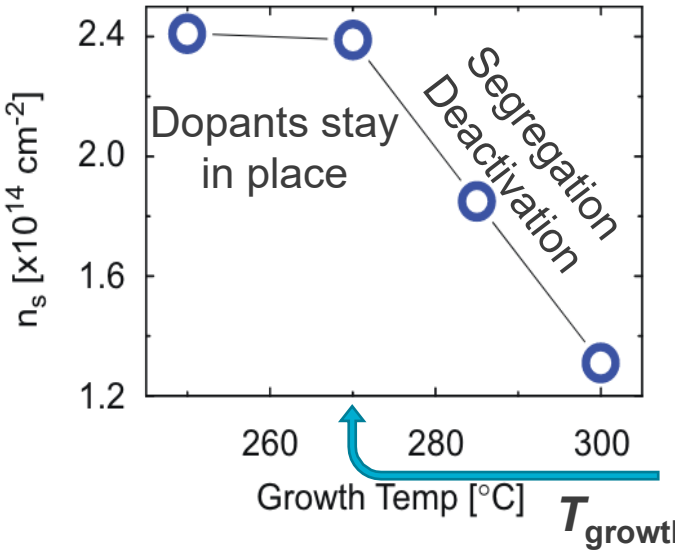




Single charged impurity may change current by order of magnitude

[*J. P. Mendez et al.*, Phys. Rev. Appl., 2023]

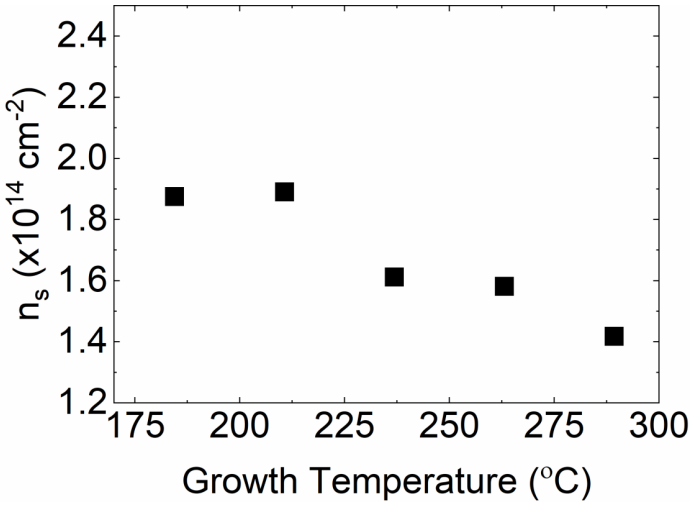
Literature Data



$T_{growth,max}$ ~270ºC

[*S. R. McKibbin et al.*, Physica E, 2010]

Our Data

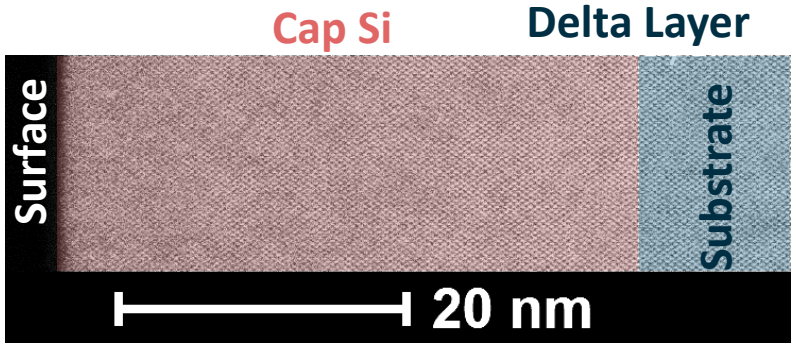


Variation between research groups and tradeoff between dopant stability and cap layer quality

Challenges and Approach to Studying Quality of Cap Si

Challenges:

Transmission Electron Microscopy



Does not provide information about electronic quality

Delta Layer Measurements

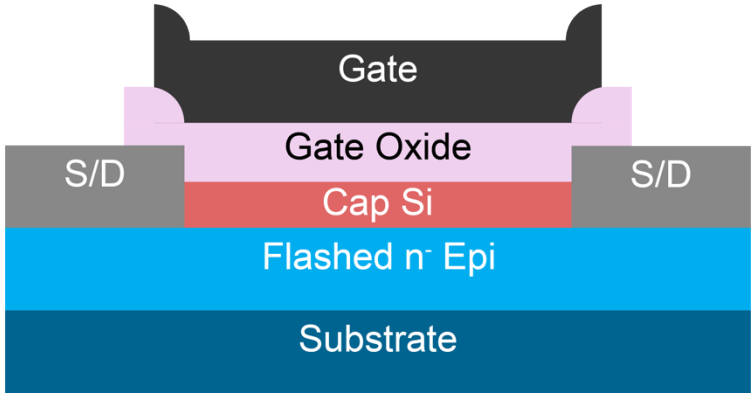
Weak Localization Thickness (nm)	SIMS Thickness (nm)
0.85 ± 0.04	~3

[*J. A. Hagmann et al.*, Applied Physics Letters, 2018]

Dominated by delta layer

Approach:

PMOS without delta layer

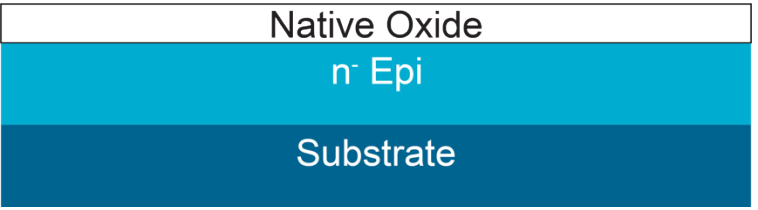


Requires:

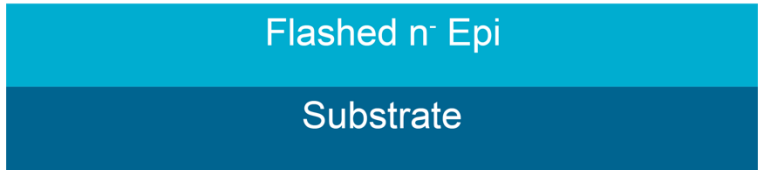
- Compatible gate stack
- Compatible ohmic contacts

Transistor may allow simple electronic qualification of cap Si

PMOS Process for APAM



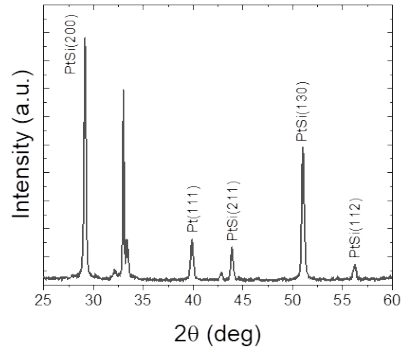
0) Starting material



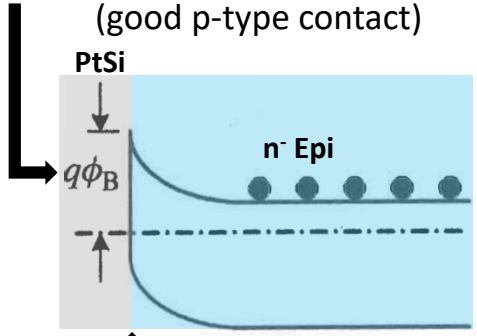
1) Flash clean in UHV

2) Epitaxial Si cap growth (10 nm)

XRD after 20 min 400ºC Anneal in Argon

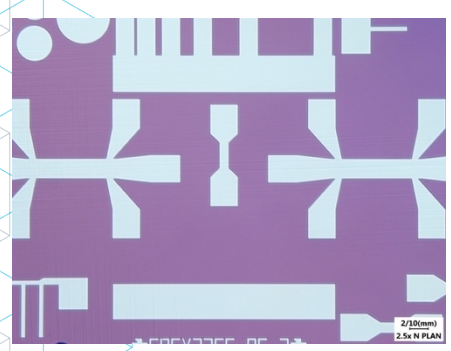


0.81 eV Barrier to conduction band
(good p-type contact)

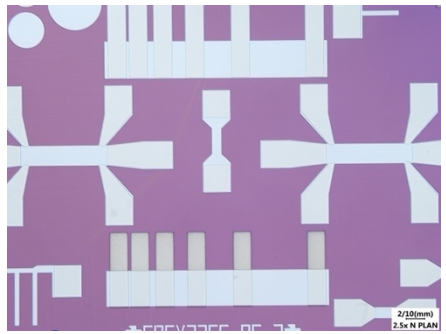


~1 Ideality factor
(good interface)

3) Mesa etch and field oxide

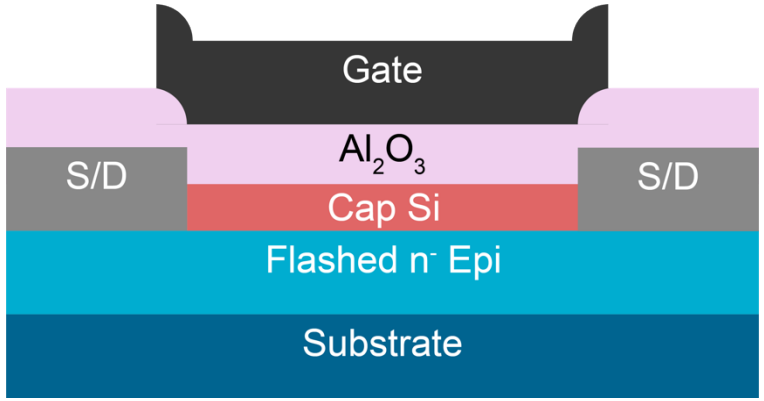


4) Silicide contacts

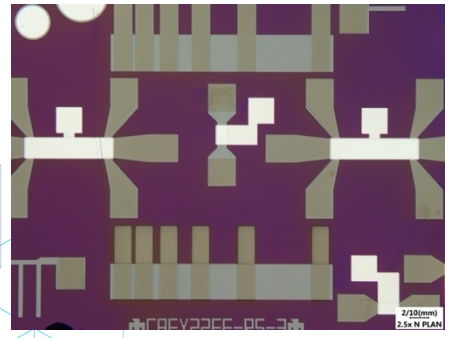


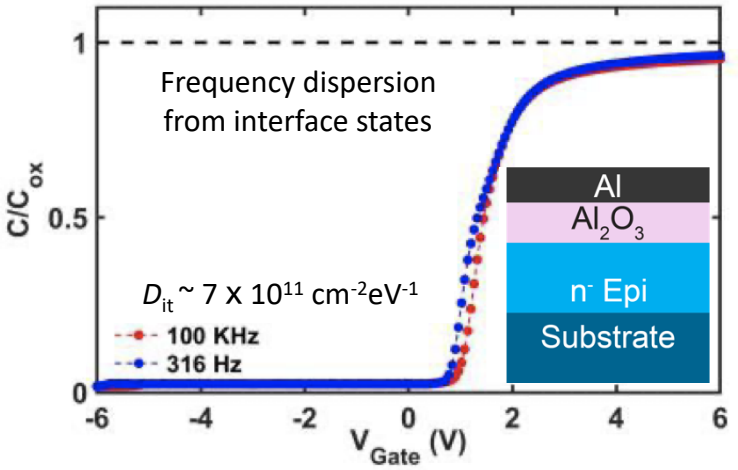
Adapted from [D. K. Schroder, Semiconductor Material and Device Characterization, 2006]

PMOS Process

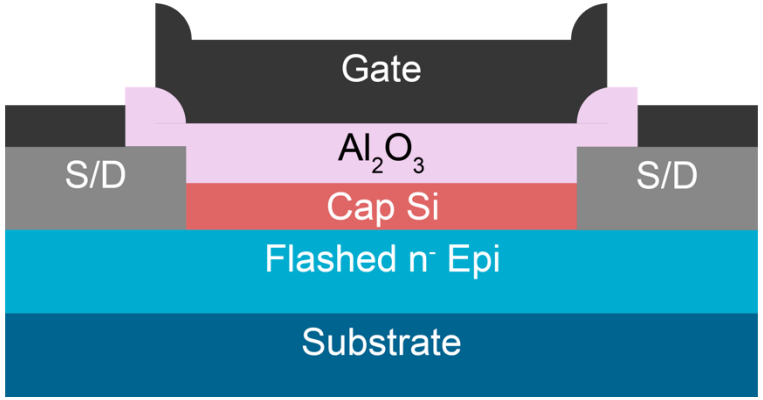


5) Gate stack

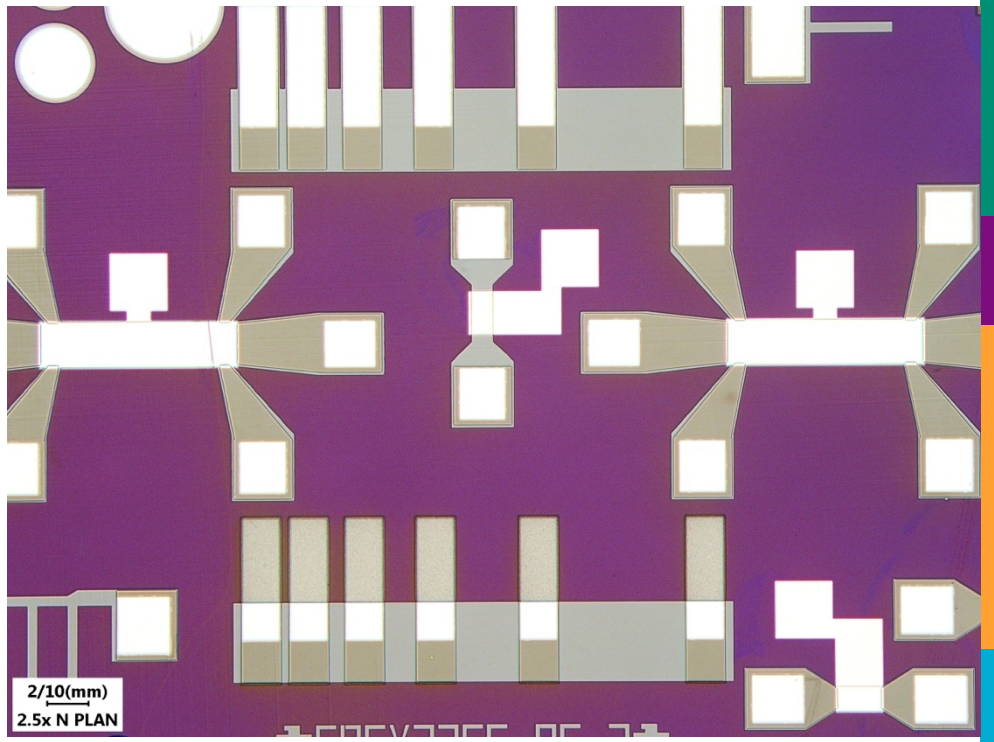




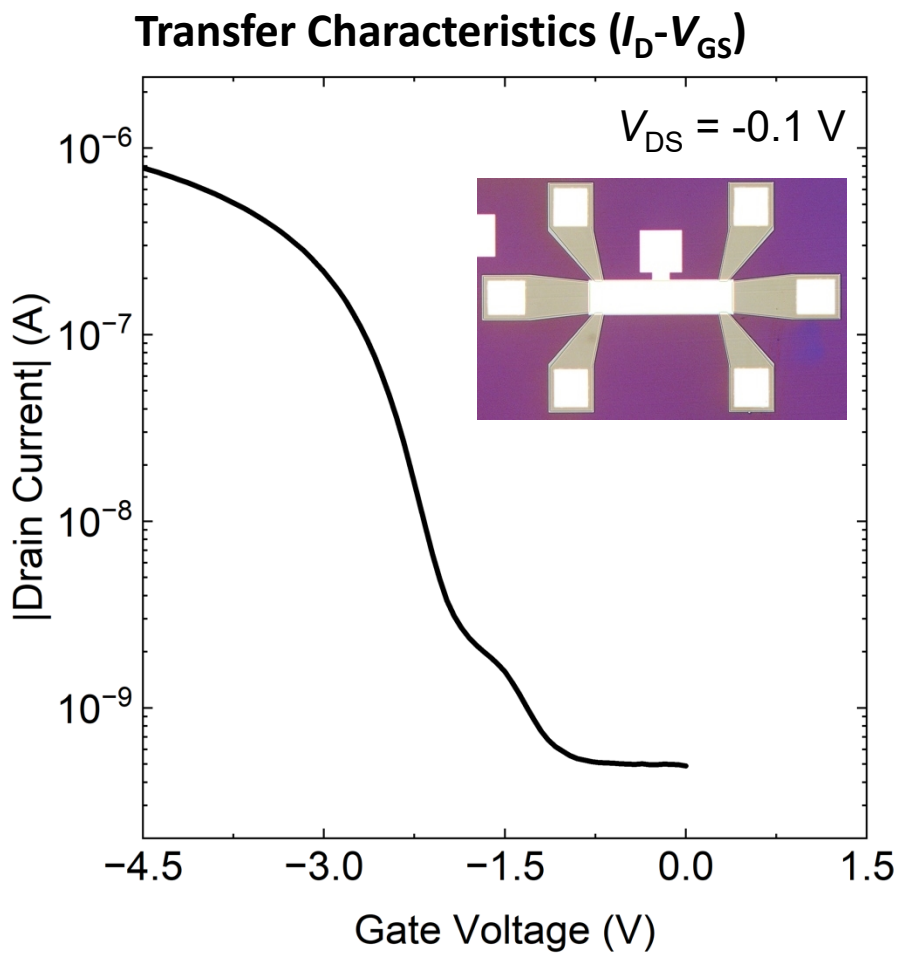
Adapted from [*T.-M. Lu et al.*, Silicon Nanoelectronics Workshop, 2021]

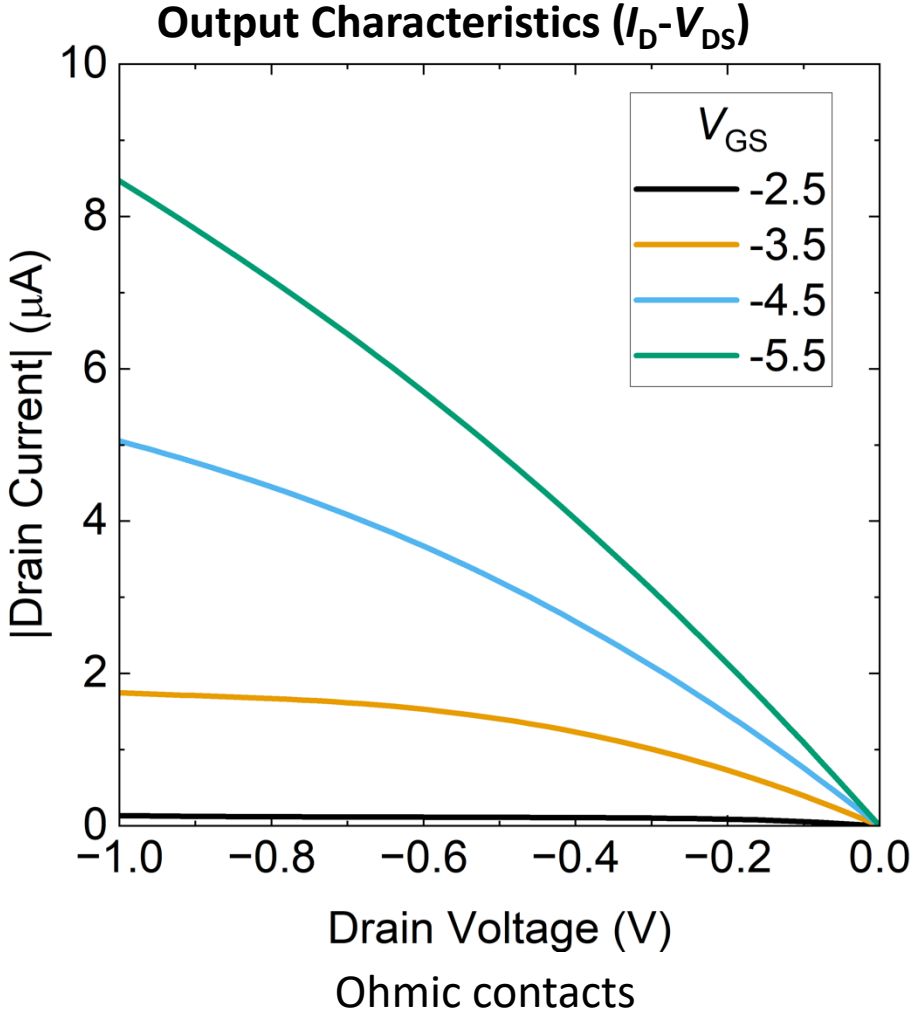


6) Via and bond pads



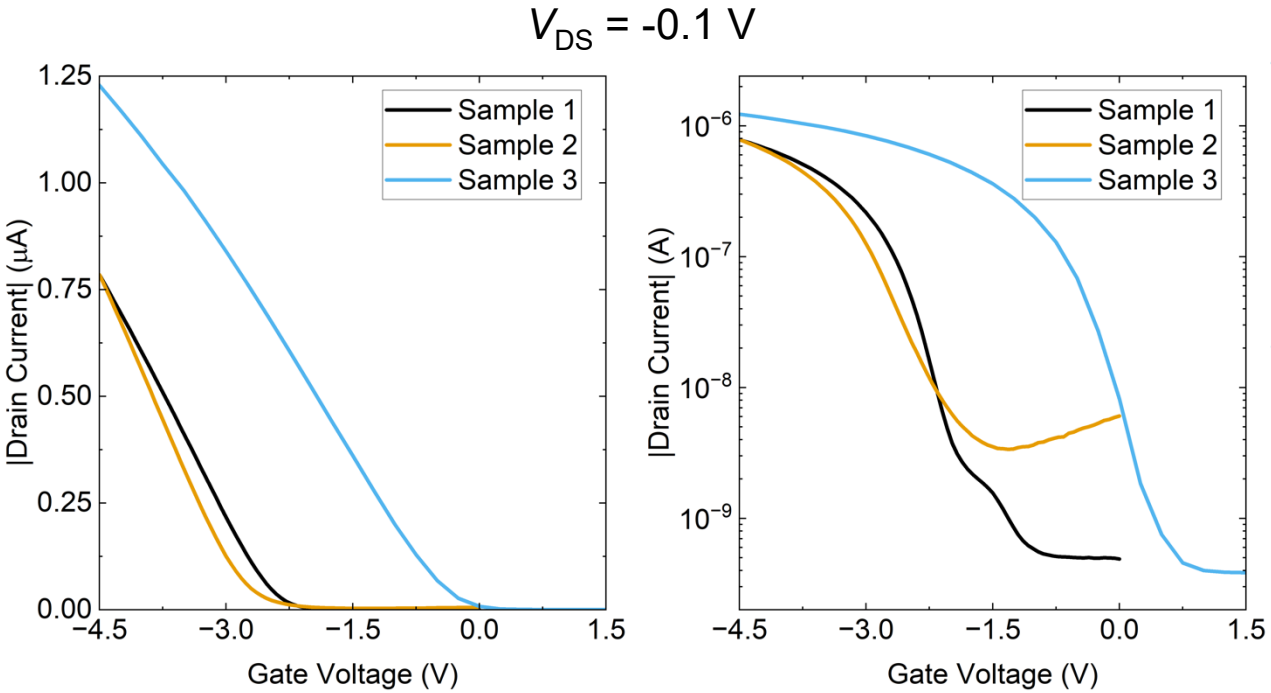
First Room Temperature PMOS in Epi Si





With functioning PMOS transistors, can we learn anything about the APAM cap Si?

Sample Characteristics

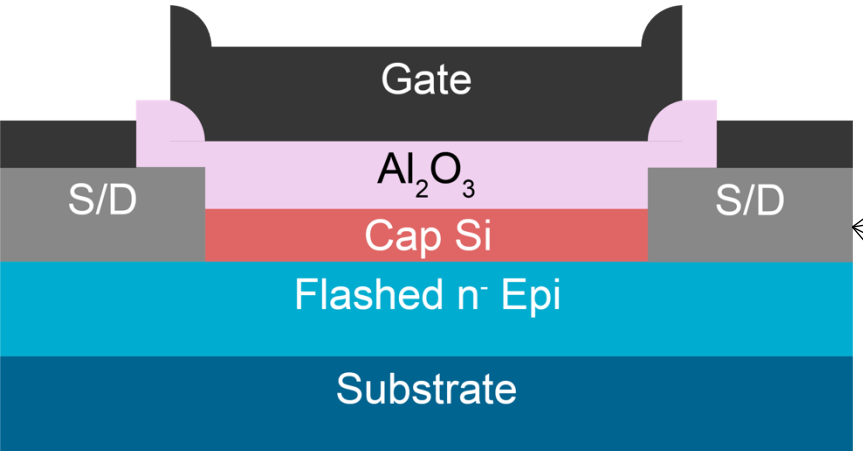


	$\mu_{FE,lin}$ ($cm^2V^{-1}s^{-1}$)	V_t (V)	SS ($mV\ dec^{-1}$)	$\lvert I_{off}\rvert$ (nA)
Sample 1	72	-2.4	396	0.49
Sample 2	83	-2.7	680	6.80
Sample 3	90	-0.6	492	0.41

- Field effect mobility – how well can the carriers move through the semiconductor and near the surface?
- Threshold voltage – at what gate voltage does the device turn on?
- Subthreshold swing – how fast does the device transition from off to on?
- Off current – how much current is flowing in the off state?

Large sample to sample or run to run variation may dominate intentional changes.

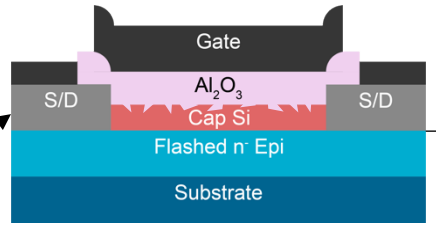
Potential Sources of Variation from Microfabrication



Potential Variations

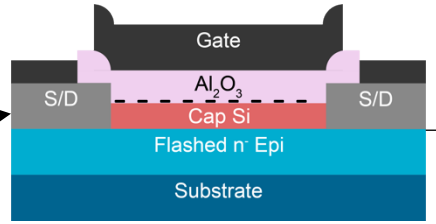
Potential Impacts

Interface Roughness



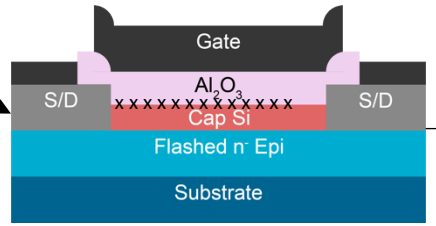
Field effect mobility

Fixed Charge



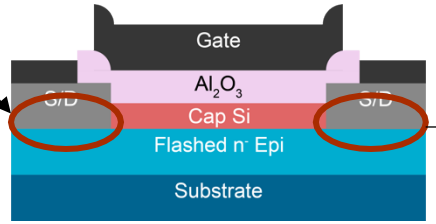
Field effect mobility
Threshold voltage

Interface States



Field effect mobility
Subthreshold swing

Contact Properties

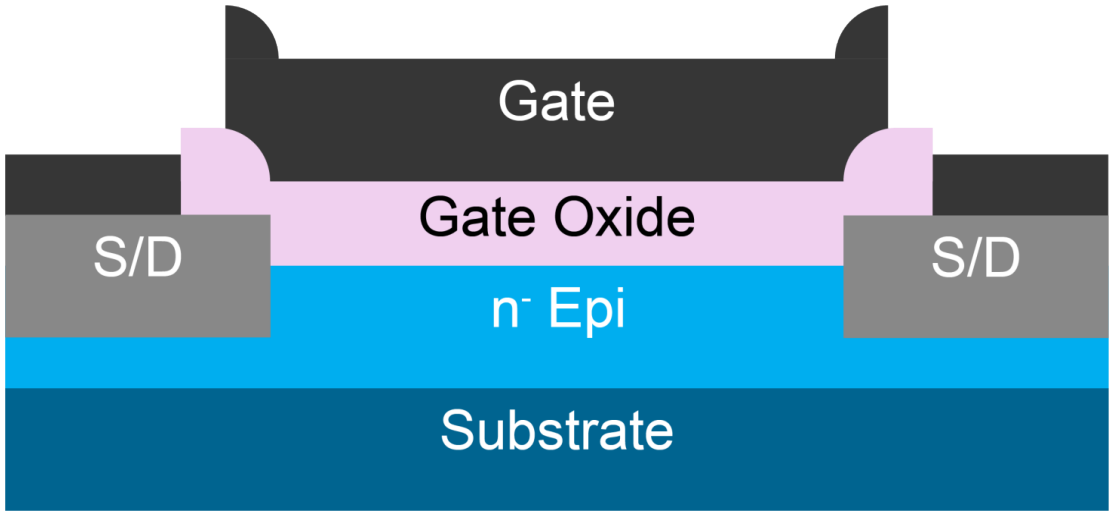


Off current

Need confidence in each to eliminate microfabrication as source of variation.

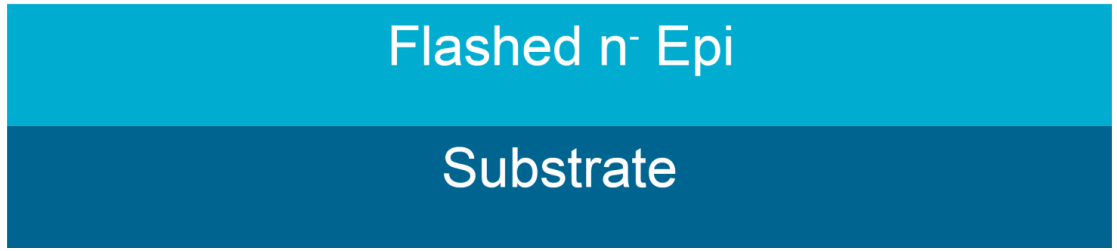
Next Steps

Verify with Starting Material

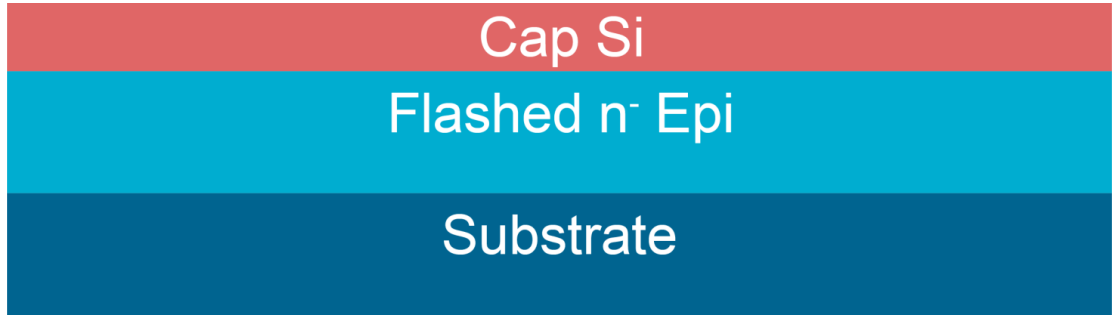


- Similar variation → evaluate process
- Minimal variation → next step

Evaluate Epi Cap Process Material for Variation



- Material characterization
- PMOS
  - Minimal variation → next layer



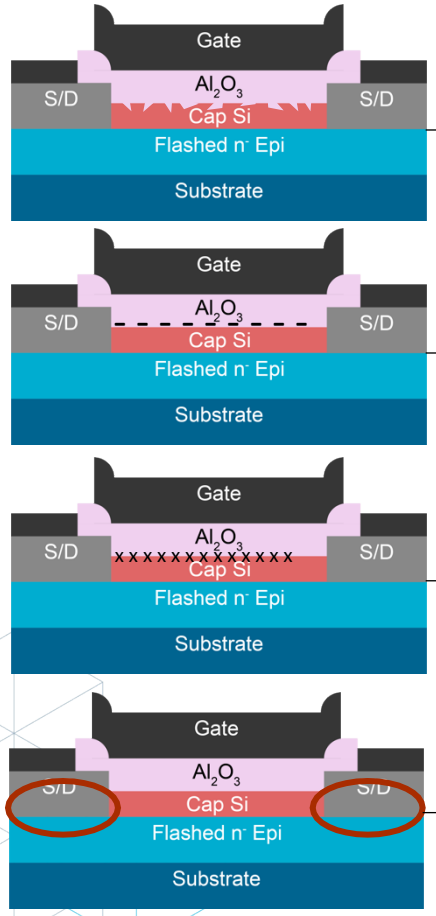
- Material characterization

Address variation once source is discovered, then study intentional changes and relate to TFET

Conclusions

Multiple sources of device variability exist that impact the realization of a vertical TFET with SS <60 mV/decade

Potential Fab Variations



Potential Impacts

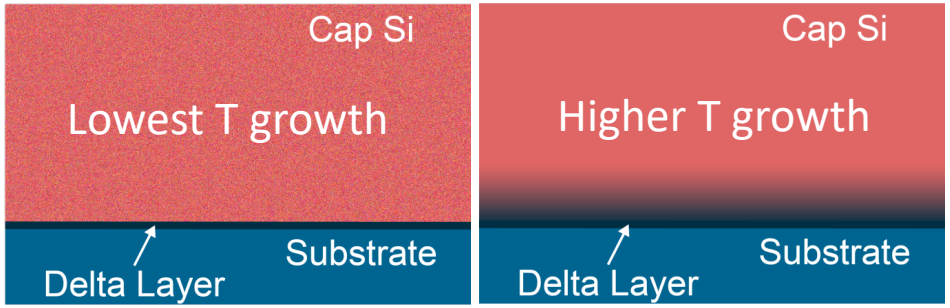
Interface Roughness → Field effect mobility

Fixed Charge → Field effect mobility, Threshold voltage

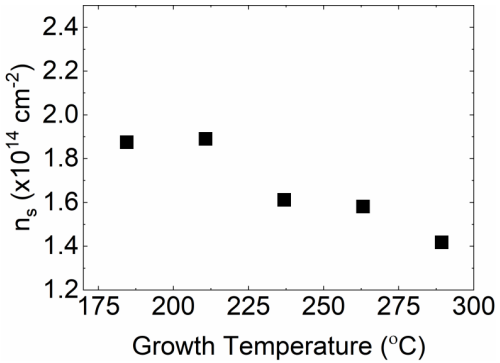
Interface States → Field effect mobility, Subthreshold swing

Contact Properties → Off current

Epitaxial Variations



Dopant Segregation



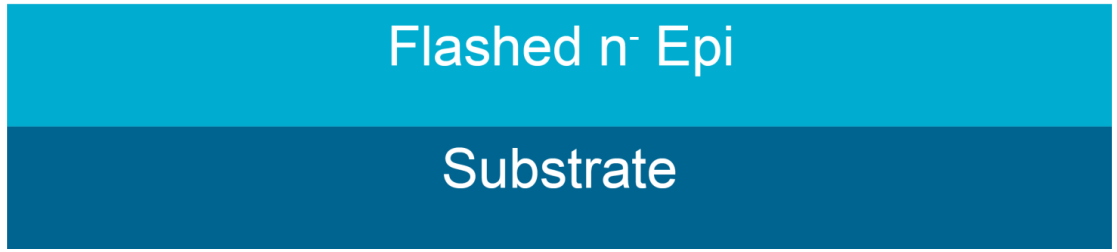
With working PMOS, can now test and eliminate sources of variability ahead of realizing a vertical TFET with APAM

This work was supported by the Laboratory Directed Research and Development Program at Sandia National Laboratories and was performed, in part, at the Center for Integrated Nanotechnologies, a U.S. DOE, Office of Basic Energy Sciences user facility. Sandia National Laboratories is a multimission laboratory managed and operated by National Technology & Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.

Backup slides

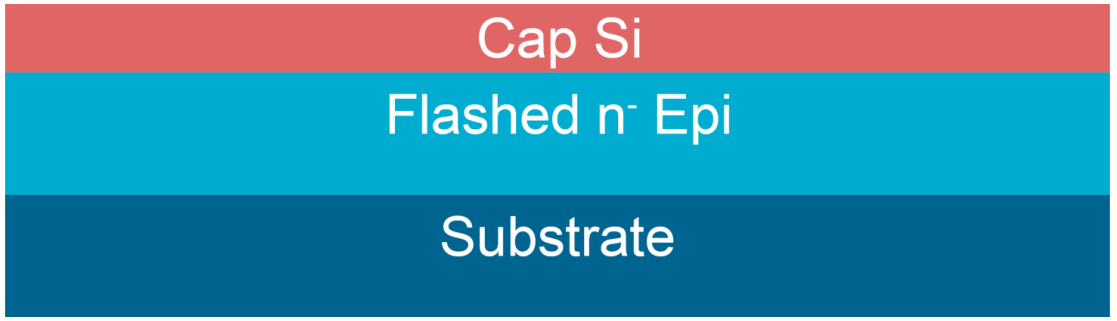
Potential Sources of Variation from Epi Cap Process

UHV Flash



- Flash unintentionally diffuses boron into the epi layer
- Changes in doping could change:
  - Threshold voltage
  - Off current

Epi Cap Silicon Growth

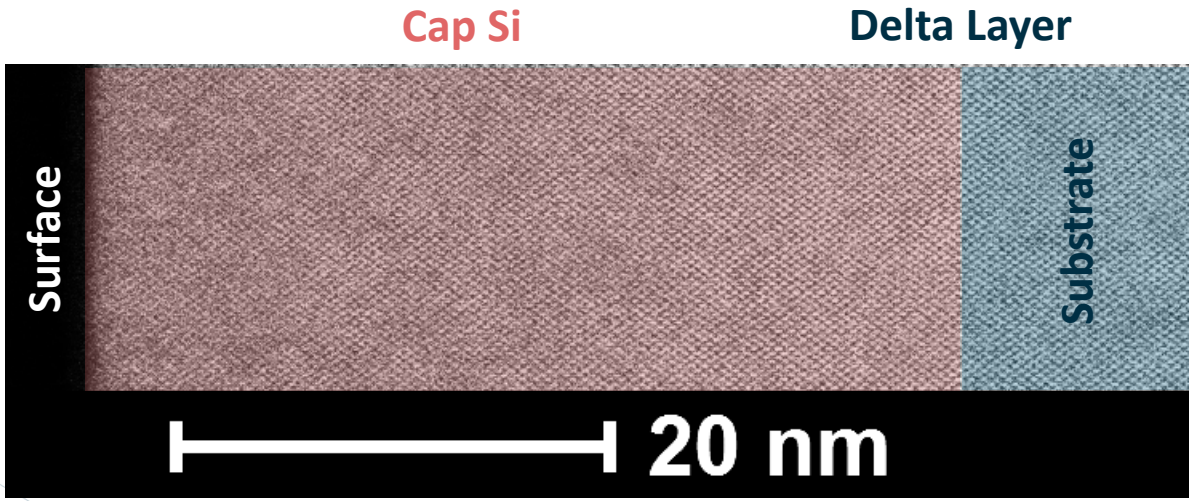


- The epi cap Si grows with defects/dopants
- Changes in doping could change:
  - Threshold voltage
  - Off current
- Changes in defects could change:
  - Field effect mobility
  - Subthreshold swing

These potential sources of variation may also impact tunnelling from a delta layer

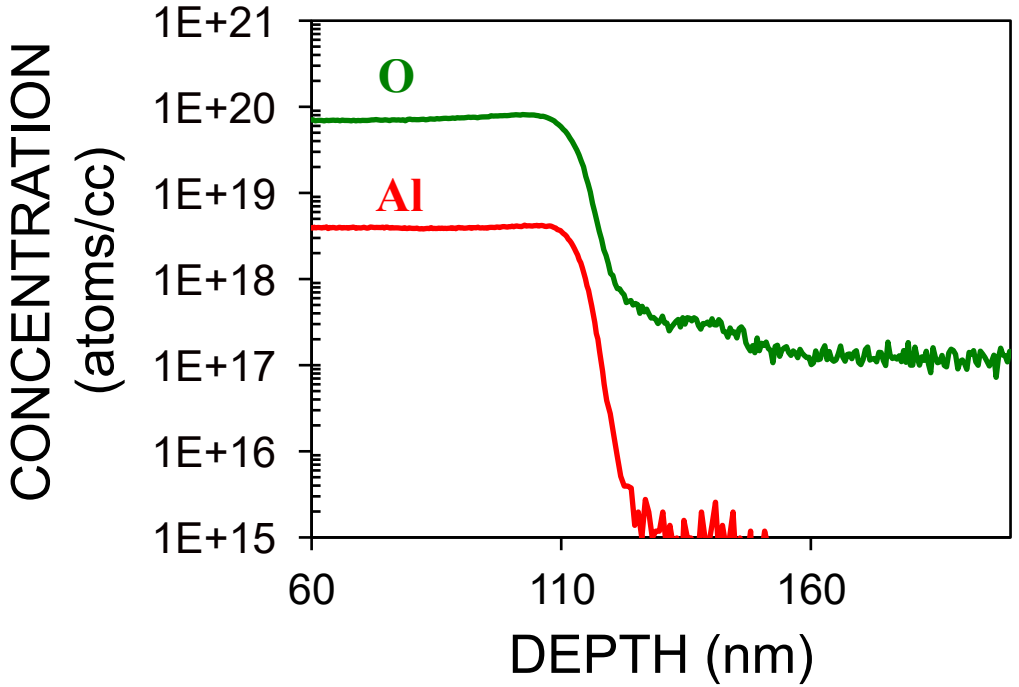
Low Temperature Growth Defects

Tunneling Electron Microscopy



Cap Si becomes amorphous towards surface

Secondary Ion Mass Spectroscopy Depth Profile



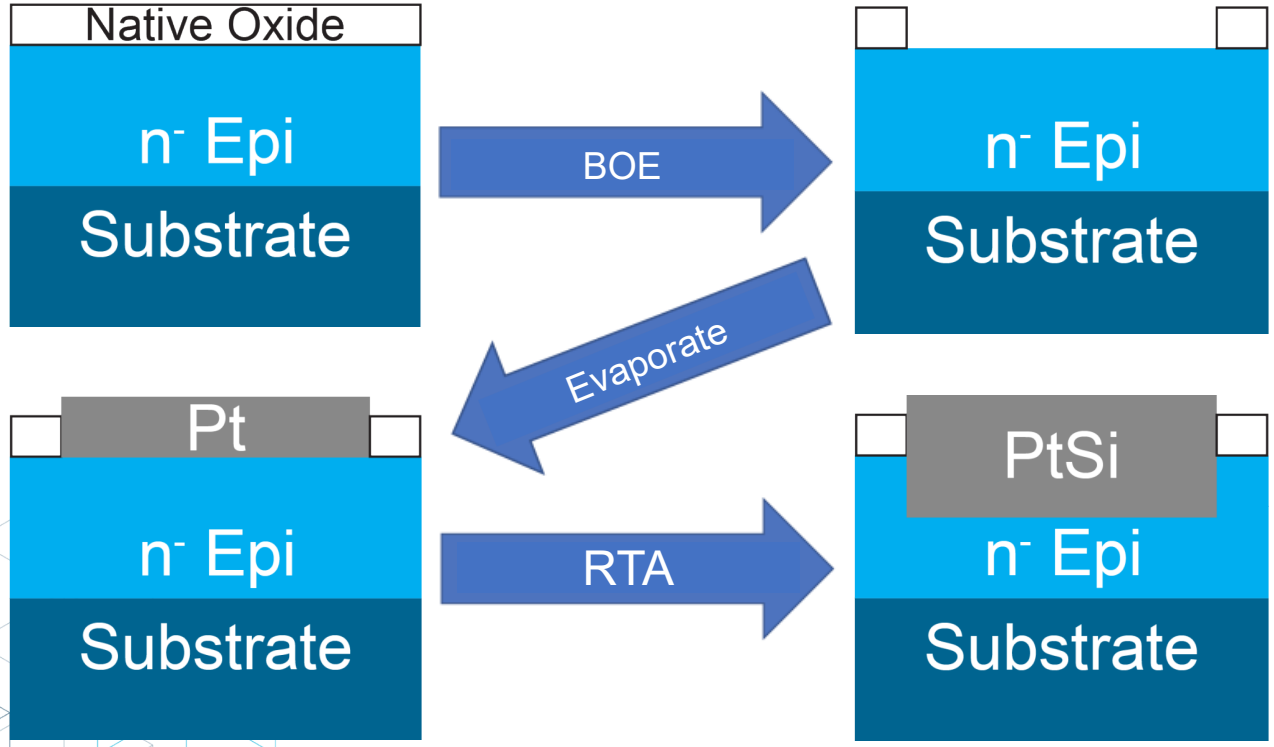
[*E. M. Anderson et al.*, Journal of Physics: Materials, 2020]

Al and O incorporated into Si cap

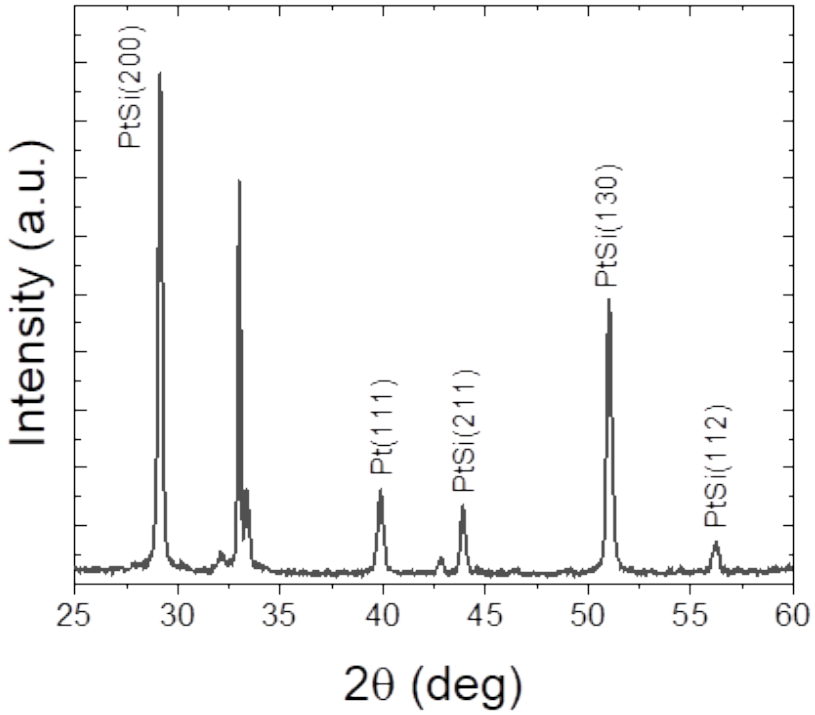
Low temperature growth = defective cap layer

Compatible Ohmic Contact Process

Platinum Silicide Process Flow



XRD after 20 min 400ºC Anneal in Argon

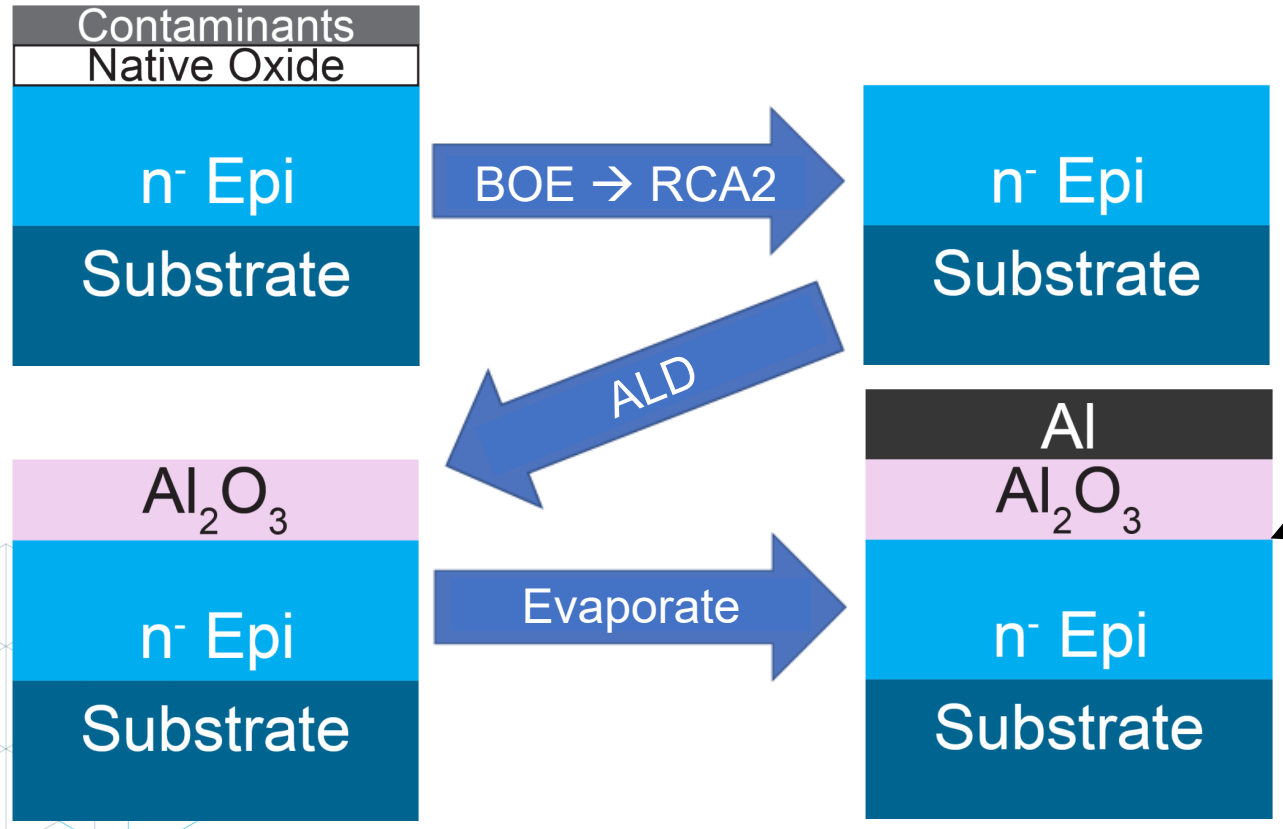


Pt silicide formed

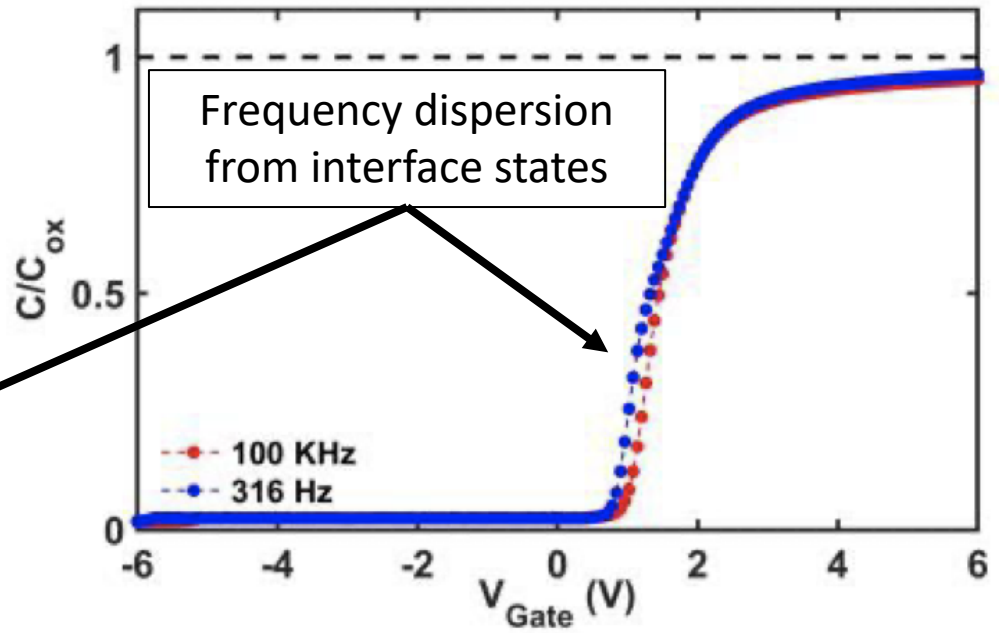
Silicide formation within thermal budget

APAM Compatible Gate Stack

Gate Stack Process Flow



Multifrequency Capacitance-Voltage



D_{it} ~ 7 x 10^{11} $cm^{-2}eV^{-1}$

Adapted from [*T.-M. Lu et al.*, Silicon Nanoelectronics Workshop, 2021]

APAM compatible ALD gate stack process with good interface

Boron Concentration after Flash