SAND2024-07911C

Sandia National Laboratories

Mitigation of Reverse Leakage Current and Charge Trapping in GaN Schottky Barrier Diodes

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EMC 2024

June 26th, 2024

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Overview

- GaN Schottky diodes have potential use in **high-power** and **fast-switching** applications.
- **Decrease perimeter leakage and hysteretic charging effects with passivation processes.**
- 10µm **MOCVD n-GaN (~1E16cm^{-3})** on 110µm n+-GaN substrate ~(1E18cm^{-3})
- Anode diameters **250µm, 500µm, 750µm** to study perimeter vs bulk leakage
- Repeat treatments of 5 min UV/O3 at 200C and 5 min in 49% HF around anode.

Table 1: Passivation treatments for wafers in this study. Average leakage current density for 250µm devices and hysteresis voltage, V_{hys}, for 750µm devices.

Wafer	Passivation Treatment	J_{leak} at -100V (µA/cm^2)	V_{hys} (V)
A-1	20min 50C downstream plasma ash in O_2 atm	316	N/A
A-2	**1**x (UV/O3 +HF) + UV/O3	0.316	240
B	**3**x (UV/O3 +HF) + UV/O3	0.148	519
C-1	**3**x (UV/O3 +HF) + UV/O3	0.032	N/A
C-2	**5**x (UV/O3 +HF) + UV/O3	0.032	N/A

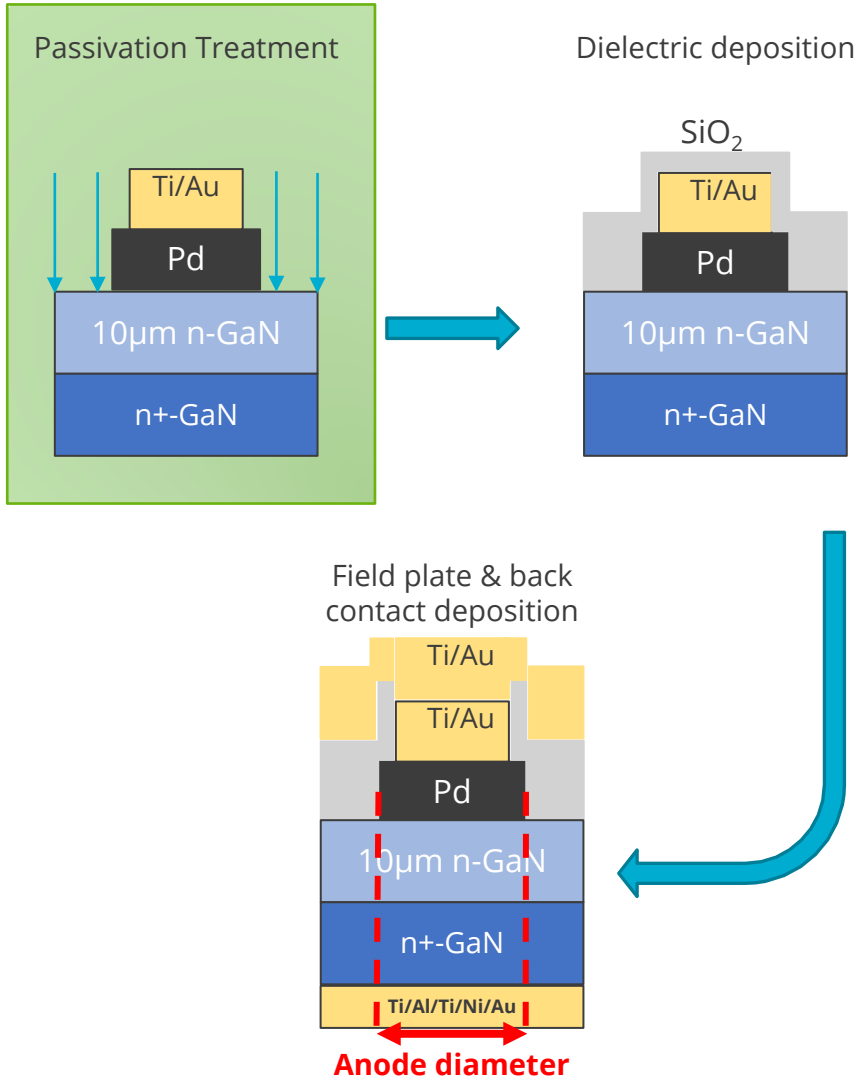

Fig. 1: Process flow and cross-sectional view for Pd-GaN Schottky diode.

Results: Leakage Current Reduction

Wafer A-1 & Wafer A-2 Post-Treatment Results

Wafer A-1
50C Plasma Ash

Wafer A-2
1x (UV/O3 +HF) + UV/O3

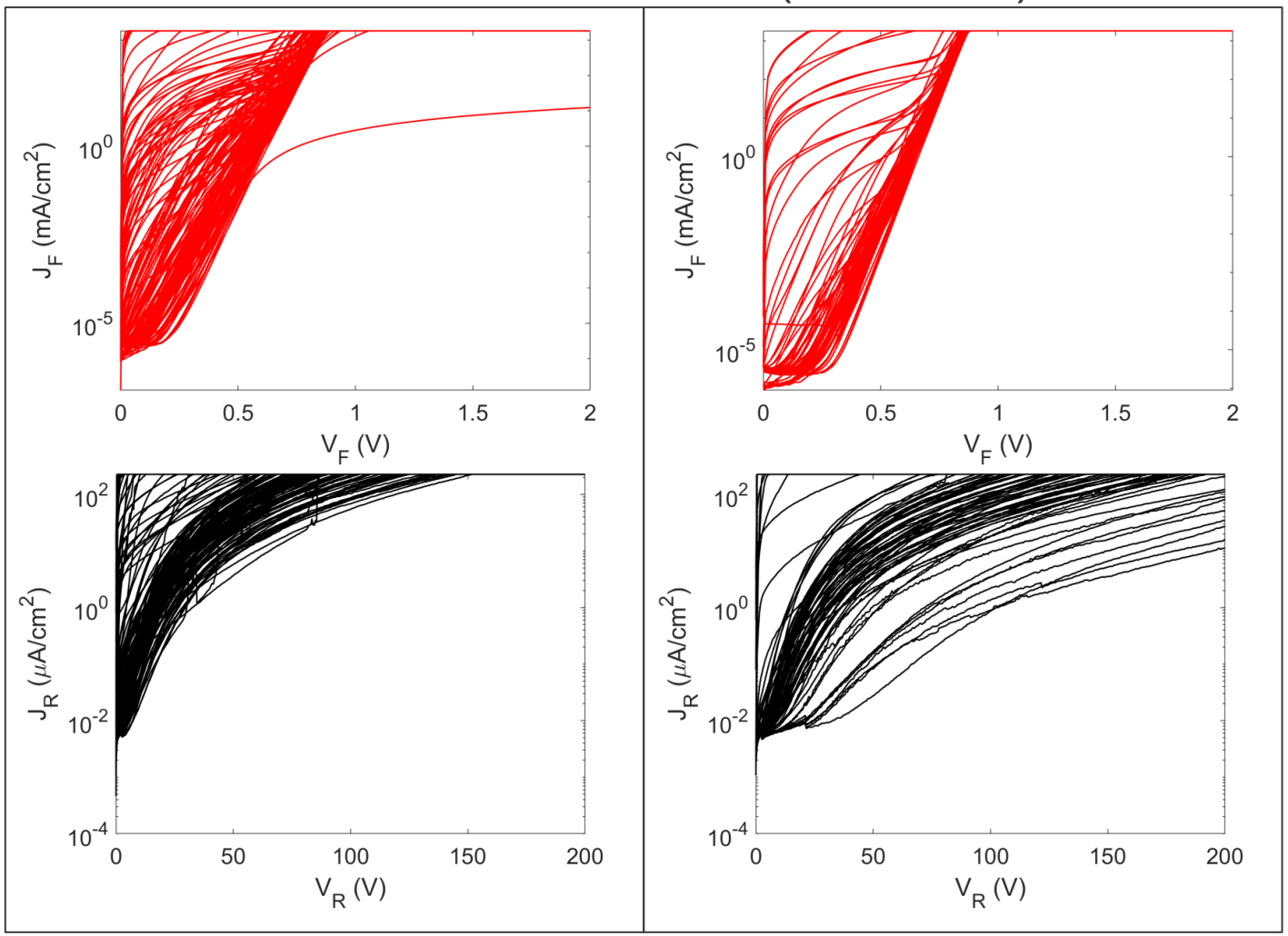

Fig. 2: FB (top) and RB (bottom) I-V curves for wafer A-1 (left) & A-2 (right) (750um devices).

- Wafers A-1 and A-2 quarters from same wafer
- Wafer A-2 shows **improvement of both FB and RB**.

Table 2: Comparison of average values for all device sizes.

Wafer	A-1	A-2	A-1:A-2
η	1.23	1.14	**1.08**
J_{leak} at 100mV (mA/cm^2)	22.5	8.97	**2.51**
J_{leak} at -100V (μA/cm^2)	250	97.7	**2.56**
Yield	50%	81%	**0.62**

Wafer A-1 & A-2: Current Density at -100V vs Anode Size

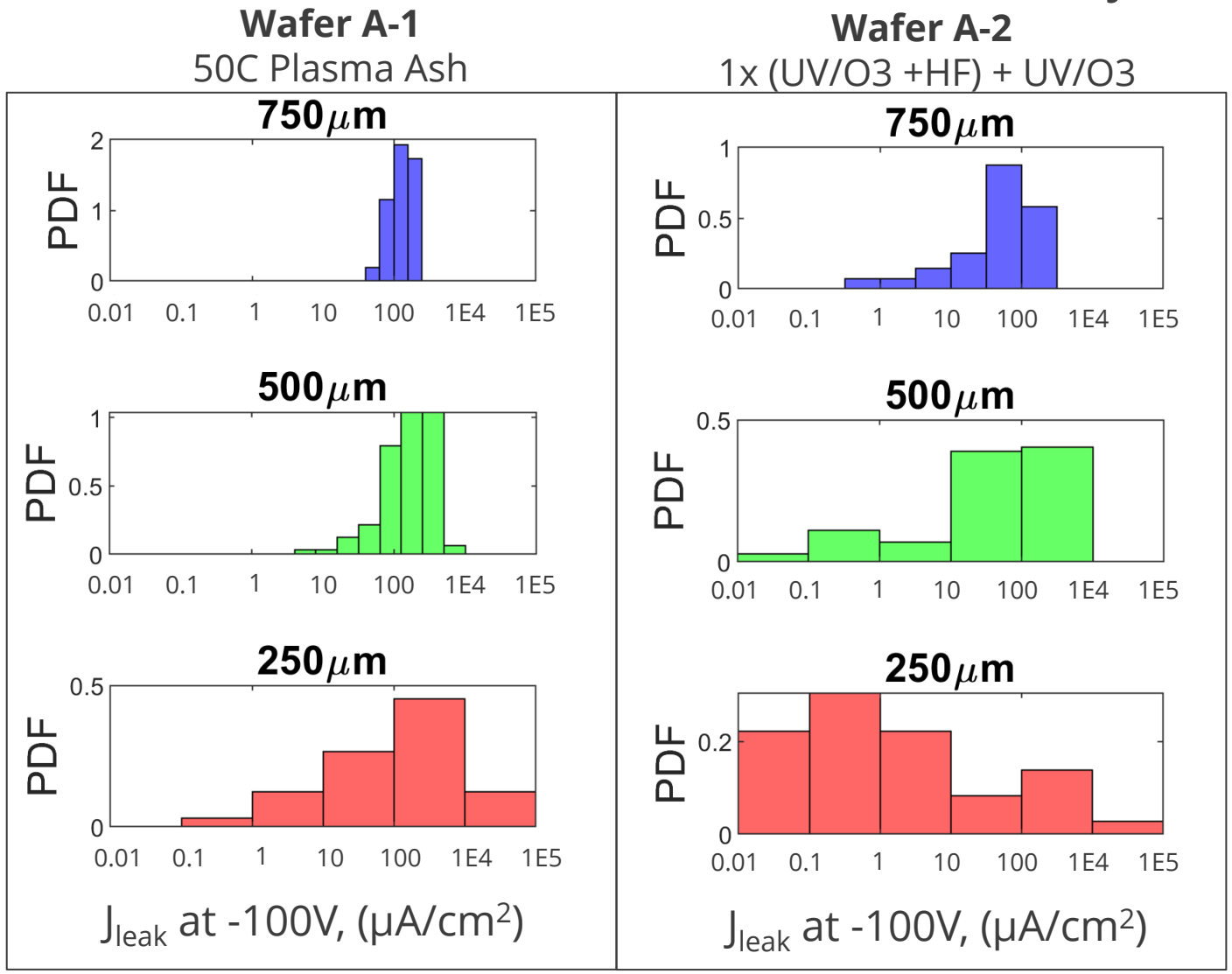

Fig. 3: Box chart and histogram for J_{leak} at -100V for different anode sizes.

- Wafer A-2 1 shows improvement by a factor of about 2 for 750um and 500um devices.
- **Improvement of 1000x** for 250um devices.
- Wafer A-1: **Perimeter leakage dominates**
- Wafer A-2: **Bimodal**. Bulk or perimeter leakage. **Leakage depends on size.**

Table 3: Locations of largest histogram peak for each device size. P2/P1 is the ratio of the peaks.

Wafer	A-1	A-2	A-1:A-2
750um peak (μA/cm²)	126	56.2	2.24
500um peak (μA/cm²)	252	100	2.52
250um peak (μA/cm²)	316	0.316	**1000**

Current Density for multiple UV/O3+HF treatments

- Multiple repeats of UV/O3+HF reduces leakage further
- Another **10x reduction** in leakage in 250um devices with 3x repeats
- Bimodal statistics observed in Wafer B 750um devices
- **More than 3x repeats does not improve performance further**

Table 4: Locations of largest histogram peak for each device size.

Wafer	A-1	A-2	B	C-1	C-2
Passivation Treatment	Plasma Ash	**1**x (UV/O3 +HF) + UV/O3	**3**x (UV/O3 +HF) + UV/O3	**3**x (UV/O3 +HF) + UV/O3	**5**x (UV/O3 +HF) + UV/O3
750um peak ($\mu A/cm^2$)	126	56.2	178	3.16	5.62
500um peak ($\mu A/cm^2$)	252	100	5.62	0.562	1
250um peak ($\mu A/cm^2$)	316	0.316	0.148	**0.032**	0.032

Results: Reduction of Charging Effects

Hysteretic Charging Effect in Pd/GaN diode

- FB & RB current increases after certain RB voltage, $\mathbf{V_{hys}}$.
- Appears as parallel conduction path
- Increase in current recovers after hours
- If held at V_{hys}, early breakdown occurs at device perimeter.
- V_{hys} is sensitive to surface treatments.

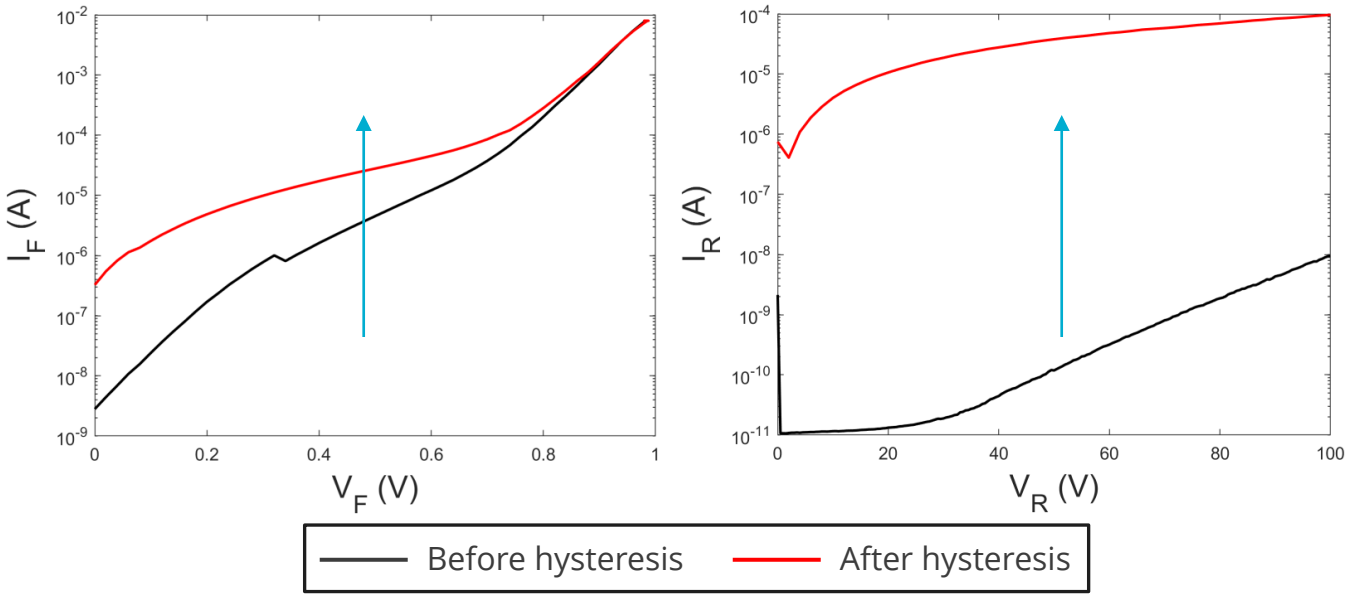

Fig. 4: (left) FB IV and (right) RB IV before and after hysteresis is triggered.

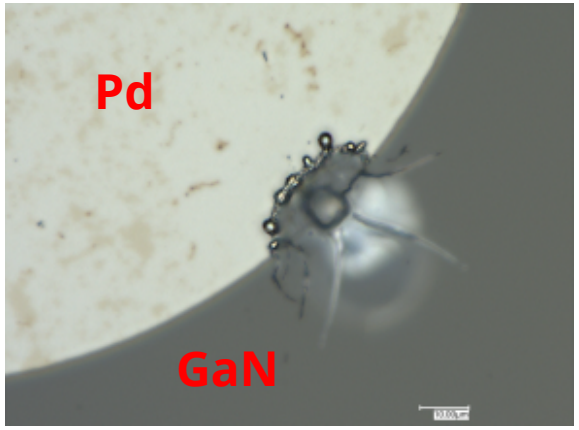

Fig. 5: Early breakdown when device is held at V_{hys}.

Effect on Charge Trappings

- UV/O3+HF treatments **increase V_{hys}**
- Average V_{hys} on A-2 increases from **130V to 240V** after passivation
- 3x UV/O3 + HF increases V_{hys} to **519V**
- Smaller devices tend to have higher V_{hys} with more variability.
- **Charge trapping is likely caused by surface defect with low density.**

Wafer	Passivation Treatment
A-2	1x (UV/O3 +HF) + UV/O3
B	3x (UV/O3 +HF) + UV/O3

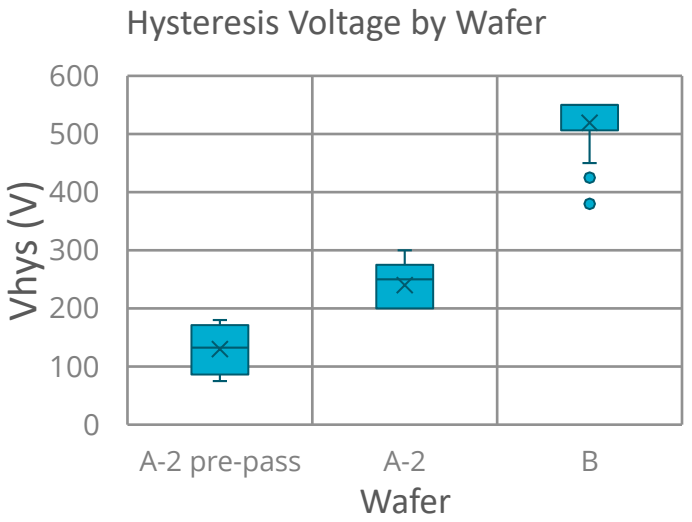

Fig. 6: Hysteresis voltages for each wafer.

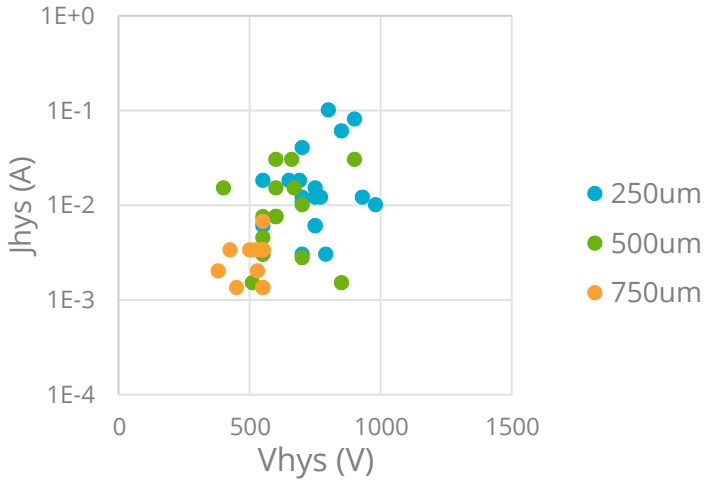

Fig. 7: Hysteresis current density vs voltages by anode size for wafer B.

Conclusions

- (UV/O3 + HF)+UV/O3 treatment has been shown to reduce RB leakage current density by a **factor of 1E4**.
- Best results: **3x repeats of 5 min UV/O3 at 200C and 5 min 49% HF follow by an additional 5 min UV/O3 at 200C**.
- Eliminates perimeter leakage for some devices.
- Mitigates surface defect that causes current hysteresis and early breakdown – V_{hys} increased from **130V to 519V**.
- **Possible Mechanisms**:
  - Passivating surface states through dense GaO growth
  - Removal of surface contaminants
- **Future work**:
  - Identify cause of large improvement in smaller devices
  - Modify UV/O3+HF treatment to further reduce reverse bias leakage

Questions and Comments