SAND2024-09345C

Impact of 12nm FinFET Technology Variations on TID Effects: A Comparative Study of GF 12LP and 12LP+ at the Transistor Level

Aldo I. Vidana[1], Nathaniel A. Dodds[1], R. Nathan Nowlin[1], Phil J. Oldiges[1], Keshab R. Sapkota[1], Trace M. Wallace[1,3], Brian M. Dodd[1], Jenny Xiong[1], Jeffrey S. Kauppila[2], Lloyd W. Massengill[2], Aymeric Privat[3], and Hugh J. Barnaby[3]

[1]Sandia National Laboratories, Albuquerque, NM, USA, [2]Reliable MicroSystems, Franklin, TN, USA, [3]Arizona State University, Tempe, AZ, USA

ABSTRACT

We compare the measured TID responses of GlobalFoundries 12LP and 12LP+ 12nm FinFET technologies. Differences in their TID response are attributed to certain expected differences between the physical parameters of these two processes.

MOTIVATION & OBJECTIVE

- Sandia National Laboratories' TID tests on GF 12LP showed higher threshold voltages and fewer fins enhance TID tolerance [1]
- GF's 12LP+ offers 20% better performance, 40% less power usage, and 15% improved logic area scaling, with a dual work-function gate [2], [3]
- This study expands TID analysis to all threshold voltages and fin counts, comparing 12LP and 12LP+
- Comparing 12LP and 12LP+ helps evaluate their use in radiation environments and the impact of process differences on TID tolerance

EXPERIMENTAL DETAILS

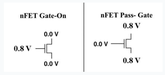
Transistor Test Structures

12LP & 12LP+ n-type FinFETs with min L_G

Threshold Voltage (VT)	*Fins per Transistor*	*# of Devices Tested*
Super-Low (SLVT)	1 | 2 | 3 | 4 | 12 | 20 | 40	10
Low (LVT)	1 | 2 | 3 | 4 | 12 | 20 | 40	10
Regular (RVT)	1 | 2 | 3 | 4 | 12 | 20 | 40	10
High (HVT)	1 | 2 | 3 | 4 | 12 | 20 | 40	10

Experimental Set-Up

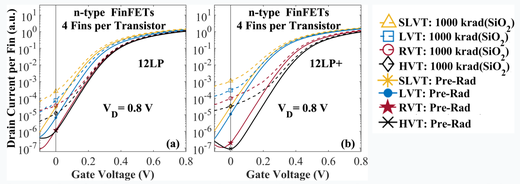
Irradiation Bias Conditions



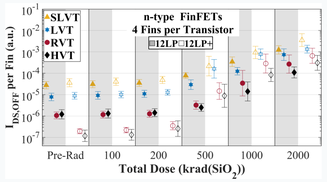
- **Transistors were irradiated at the wafer-level across many sites with an ARACOR 10 keV X-ray source**
- **Measurements and irradiation bias were done with a B1500A semiconductor analyzer and B2200A switch matrix**
- **P-type transistors showed negligible TID degradation up to 2Mrad(SiO_2)**
- **Gate- On showed slightly higher TID degradation in n-type transistors**

MAIN RESULTS

TID induced leakage currents dependence on process threshold voltage (VT)

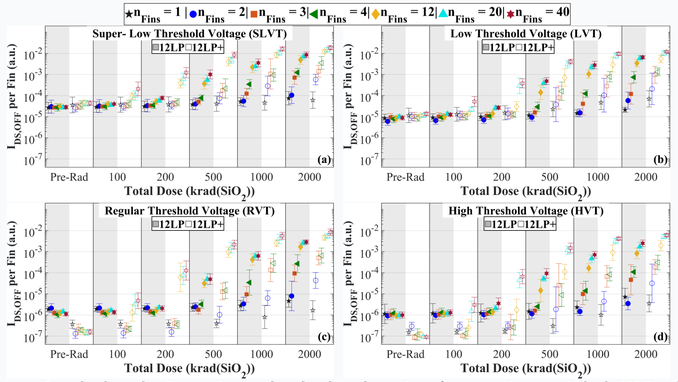


- Data indicates that for both 12LP (a) and 12LP+ (b), RVT and HVT transistors exhibit lower $I_{DS,OFF}$ pre- and post-radiation compared to LVT and SLVT transistors
- SLVT and LVT transistors in both technologies display similar pre-radiation $I_{DS,OFF}$ and measured threshold voltages (V_{TH})
- RVT and HVT transistors in 12LP+ show lower pre-radiation $I_{DS,OFF}$ and higher V_{TH} than those in 12LP



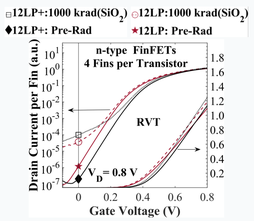
- General trend in both technologies shows that the pre-radiation order of $I_{DS,OFF}$ across the four VTs is maintained as the leakage currents increase due to TID
- In 12LP+ technology the $I_{DS,OFF}$ is observed to increase more rapidly with TID exposure than in 12LP

TID induced leakage currents dependence on number of fins per transistor

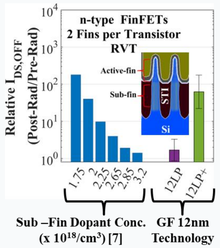


- Results consistently show that $I_{DS,OFF}$ rises as dose levels and transistor fin counts increase in both 12LP and 12LP+ technologies (even though the currents plotted have been divided by the number of fins per transistor)
- Transistors with 4 fins (or fewer) per transistor, which are more commonly used in digital applications, show the least sensitivity to dose effects
- Transistors with up to 40 fins per transistor, which may be used in custom analog or mixed-signal designs, or I/O drivers, exhibit significantly higher increases in $I_{DS,OFF}$

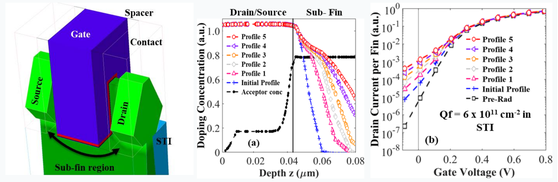
TID MECHANISMS 12LP VS. 12LP+



Dual MGWF and Lower Doping in 12LP+



Source/Drain (S/D) Doping Profiles



- Possible changes in 12LP+ compared to 12LP:
- Implementation of dual metal gate work functions (MGWFs), and lower channel doping to tune VT of transistors
- Deeper heavily-doped S/D regions to improve $I_{DS,ON}$ [4],[5]
- Optimization of fin geometric aspect ratios, such as fin width and height → smaller fin widths are more sensitive to TID induced $I_{DS,OFF}$ degradation [6]

- Devices with lower body or sub-fin doping have worse TID degradation [7]
- 12LP+ likely has lower sub-fin doping than 12LP, making it more prone to sub-fin parasitic inversion from drain to source post TID exposure

- Transistors were simulated with different S/D doping profiles below the drain/source region through the sub-fin region (z-axis)
- An increase in the off-state drain current is observed when the doping profile extends farther into the sub-fun region after introducing charge (Qf) in the STI
- If S/D doping profiles are deeper in 12LP+ than in 12LP, then this could help explain the greater susceptibility of 12LP+ to TID

CONCLUSIONS

- We compared TID responses between GF 12LP and 12LP+ 12nm bulk FinFET technologies at the transistor level
- 12LP+ devices with fewer than 4 fins per transistor, which are more commonly used in digital applications, showed high TID tolerance up to 200 krad(SiO_2) for all VT variants
- 12LP+ transistors show lower absolute leakage currents than 12LP in RVT/HVT devices with fewer than 4 fins, up to 200 krad(SiO_2)
- Beyond 500 krad(SiO2), absolute leakage currents of both 12LP and 12LP+ are comparable, but 12LP+ showed higher relative (pre-rad/post-rad) increases in leakage currents, indicating higher TID sensitivity
- This larger sensitivity in 12LP+ might be attributed to the dual MGWFs, reduced halo doping, deeper S/D doping profiles, and/or narrower fins of 12LP+ compared to those of 12LP
- TID hardening in GF12LP+ can be significantly improved by using parallel transistor designs with four fins or fewer

REFERENCES

[1] A. Vidana et al., "The Effects of Threshold Voltage and Number of Fins per Transistor on the TID Response of GF 12LP Technology," IEEE Transactions on Nuclear Science, 2024

[2] GlobalFoundries, "gf.com," 2021. [Online]. Available: https://gf.com/wp-content/uploads/2021/12/GF21-12LP-12LPFinFet-0628_0.pdf

[3] M. Togo et al., "Multiple Workfunction High Performance FinFETs for Ultra-low Voltage Operation," in 2018 IEEE Symposium on VLSI Technology, Honolulu, HI, Jun 2018

[4] H.-C. Lo et al., "Performance boost using spacer-confined cavity for advanced FinFET technology," Semiconductor Science and Technology, vol. 34, no. 1, p. 015012, Dec 2018

[5] H. C. Lo et al., "A 12nm FinFET Technology Featuring 2nd Generation FinFET for Low Power and High Performance Applications," in 2018 IEEE Symposium on VLSI Technology, Honolulu, HI, Jun 2018

[6] I. Chatterjee et al., "Geometry Dependence of Total-Dose Effects in Bulk FinFETs," IEEE Transactions on Nuclear Science, vol. 61, no. 6, pp. 2951-2958, Dec 2014

[7] T. Wallace et al., "Layout Dependence of Total Ionizing Dose Effects on 12-nm Bulk FinFET," IEEE Transactions on Nuclear Science, vol. 70, no. 4, pp. 620-626, Nov 2023

Sandia National Laboratories is a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE–NA0003525.