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RELIABILITY OF WIDE-BANDGAP POWER ELECTRONICS: DEVICES TO SYSTEMS

Presentation ID 902

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August 7, 2024

SAND No. SAND2024-10046C

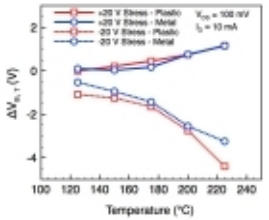
ACKNOWLEDGEMENT

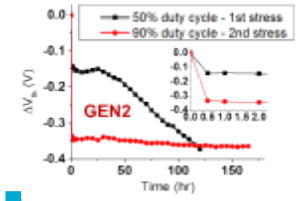
This material is based upon work supported by the U.S. Department of Energy, Office of Electricity (OE), Energy Storage Division.

PROGRAM HISTORICAL HIGHLIGHTS

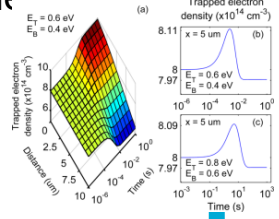
Suggested reliability improvements for components, software, and operation of Silicon Power Corporation's Solid-State Current Limiter

Characterized and evaluated commercial SiC MOSFETs, including the impacts of bias, temperature, packaging, and AC gate stress on reliability





Created a physics-based model for GaN HEMTs linking defect properties to device design



Characterized switching of vertical GaN PiN diodes using double-pulse test circuit

Constructed half-bridge hard-switching test circuit

2009

2024

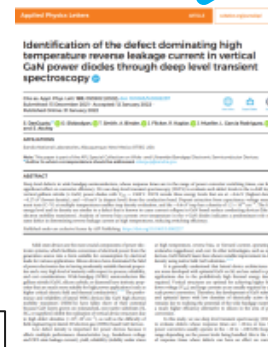
Developed and documented a general process for analyzing the reliability of any power electronics system

Developed models for SiC threshold voltage instability, and identified the free-wheeling diode ideality factor as a potential screening metric for threshold voltage shifts

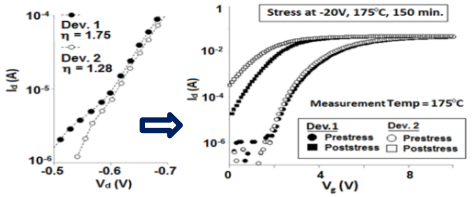
Developed an easy to use method that can be used by circuit designers to evaluate the reliability of commercial SiC MOSFETs

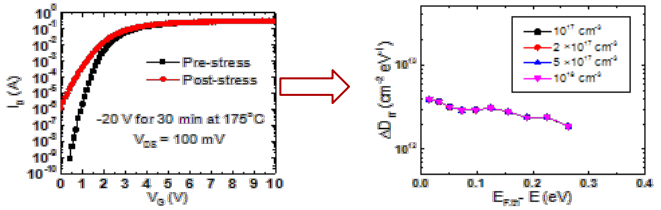
JEDEC

Participating in JEDEC WBG reliability working group



Over 30 papers and presentations over the course of the project





Leading ITRW materials and devices working group

Applied Physics Letters journal article selected as Editor's Pick

Serving as an unbiased evaluator of reliability to the WBG power electronics community, ranging from static device testing to in-circuit dynamic evaluation

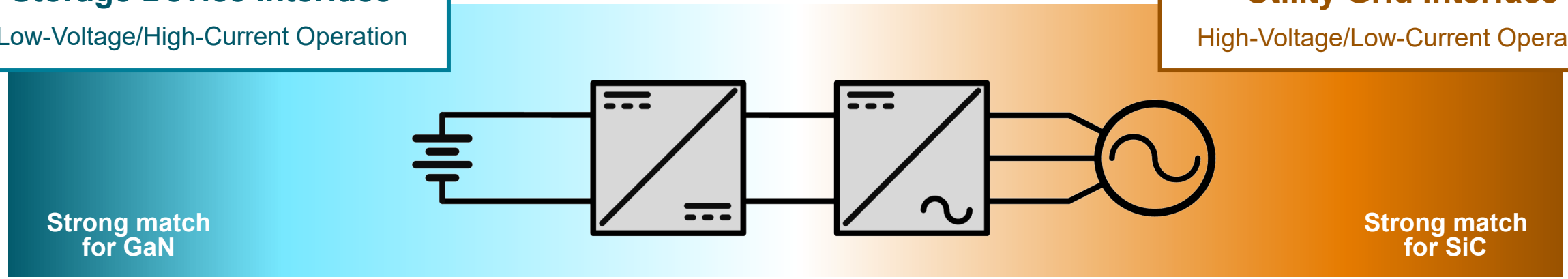
PROJECT MOTIVATION AND GOALS

Storage Device Interface

Low-Voltage/High-Current Operation

Utility Grid Interface

High-Voltage/Low-Current Operation



Power conversion system operating requirements are diverse – no single technology serves all needs.

All candidate solutions must provide exceptionally high reliability.

Program Goals:	**Identify semiconductor technologies best suited to all needs of energy storage**
	Understand device performance and reliability in realistic operating conditions
	Evaluate new devices' circuit- and system-level impact potential

PRIOR WORK: REPETITIVE DOUBLE-PULSE TESTING

Mission-Profile Based Reliability

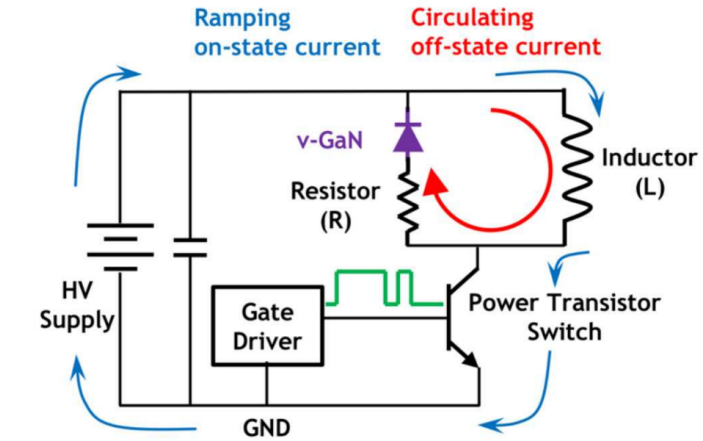
- Device reliability is influenced by its mission profile, which includes specific operating parameters and environmental stressors.

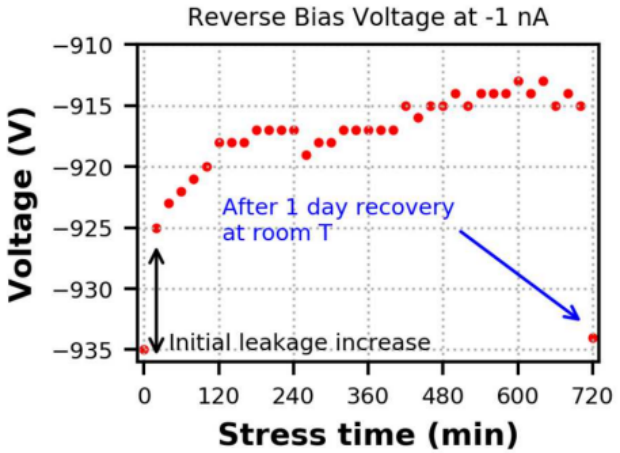
Value of Data from Practical Application Testing

- Translates device-level characterization to system-level performance improvements.
- Provides immediate utility for system integration, design optimization, and better monitoring of device and system integrity.
- Enhances lifetime estimates and maintenance scheduling.

Repetitive double-pulse testing (RDPT)

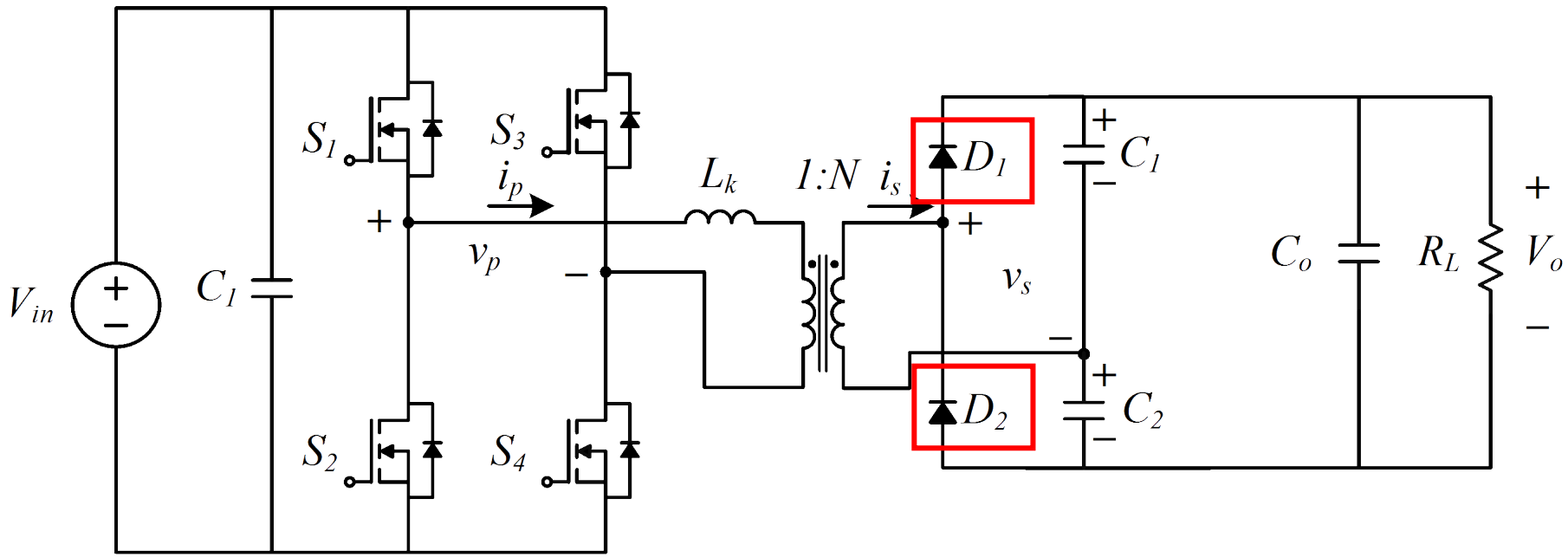
- RDPT simplifies mission profile emulation for various technologies but cannot fully replicate real-world conditions.
- V-GaN diodes were stressed in 20 min intervals. The reverse and forward I/V characteristics were taken using a Keysight B1505 Power Device Analyzer.
- Experiments were performed for a total of 720 min at 500, 750, and 1000 V with 0.2% duty cycle.





Slobodyan, O., Smith, T., Flicker, Jack, Sandoval, S., Matthews, C., Heukelom, M., Kaplar, R., & Atcitty, Stan. (2018). Hard-switching reliability studies of 1200 V vertical GaN PiN diodes. MRS Communications. 8. 1-5. 10.1557/mrc.2018.204.

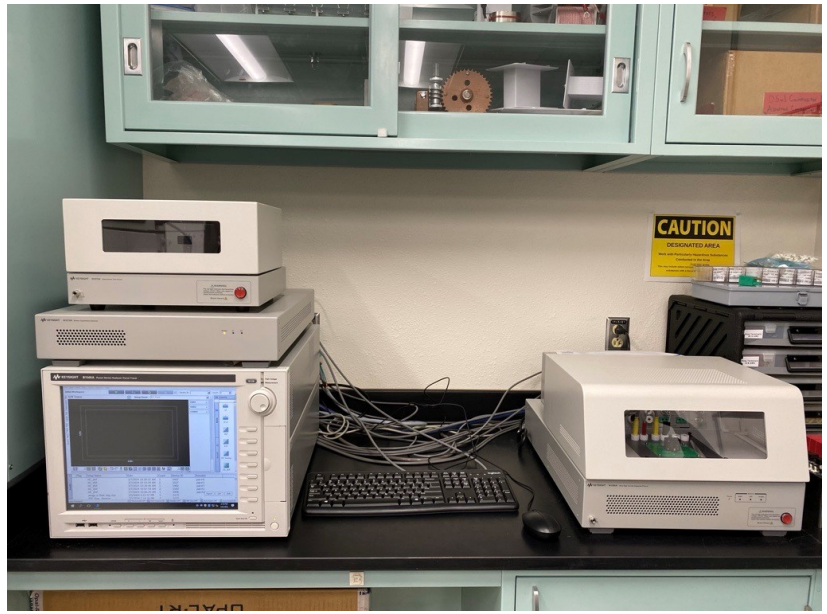
FULL-BRIDGE VOLTAGE DOUBLER CONVERTER TOPOLOGY



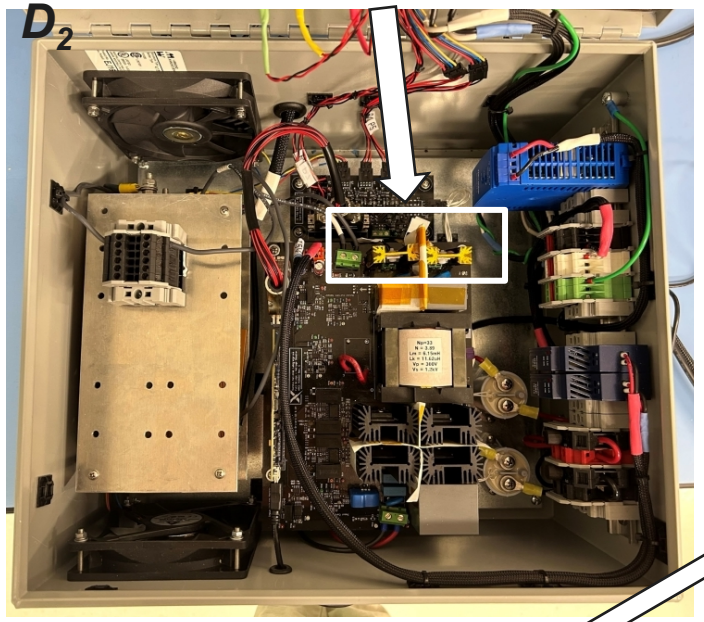
Method can be applied generally to new WBG technologies

- The Full-Bridge Voltage Doubler (FBVD) converter was designed and built to stress the v-GaN diodes under practical circuit conditions.
- The FBVD provides a reverse bias voltage across the diodes that is predictable and absent of high-frequency voltage disturbances.
- More than 3 dozen sample pairs of v-GaN diodes were stressed at 500, 700, and 900 V with an average current of 1 A using the FBVD converter operating at 100 kHz.
- After 1 hr of converter operation, the diodes were removed from the circuit and the reverse and forward I/V curves were extracted. The total stress process was set to 6 hrs for each diode pair.

EXPERIMENTAL SETUP

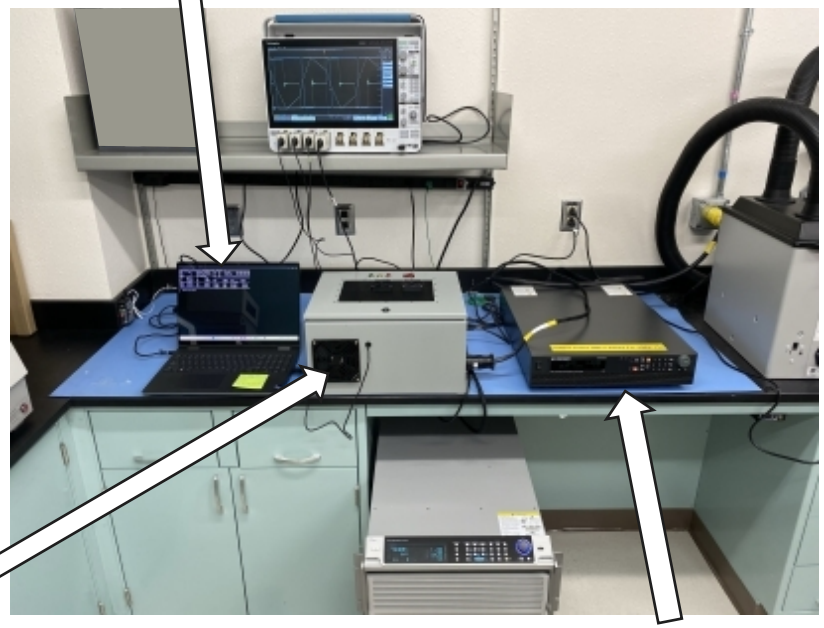


B1505 Power Device Analyzer Setup



Devices under test D_1 and D_2

Safety Enclosure



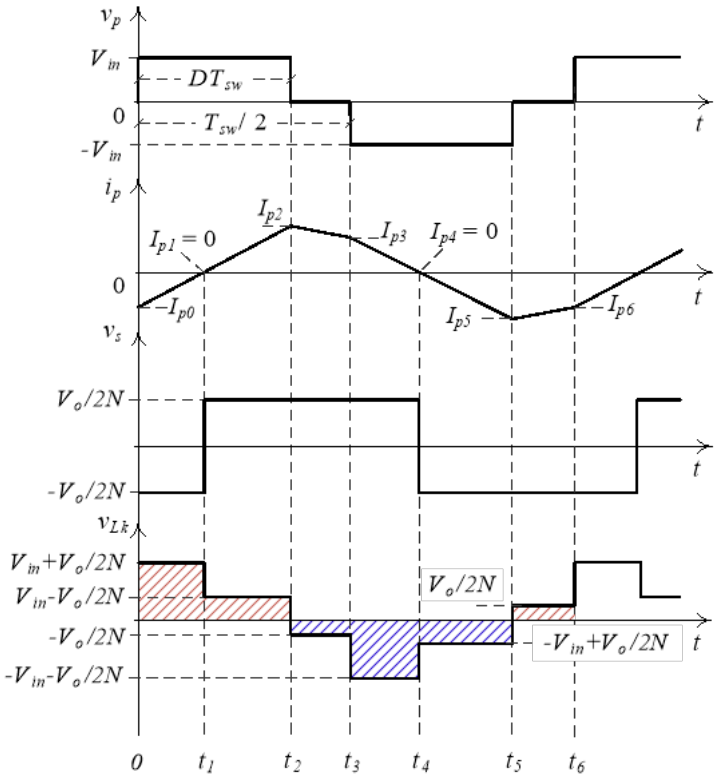
Comms/Data Logging

Electronic Load

DC Power Supply

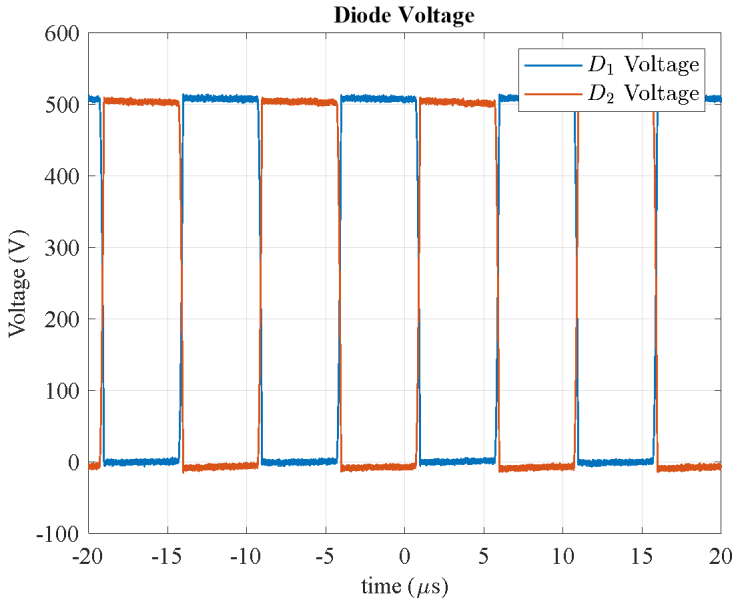
- The reliability/stress testing of the v-GaN diodes is done within the custom-built safety enclosure, which has multiple layers of protection for the device and user.
- The safety enclosure is inserted into the larger test setup that consists of a DC power supply, electronic load, oscilloscope, laptop, and B1505 power device analyzer.

DIODE IN-CIRCUIT STRESS WAVEFORMS



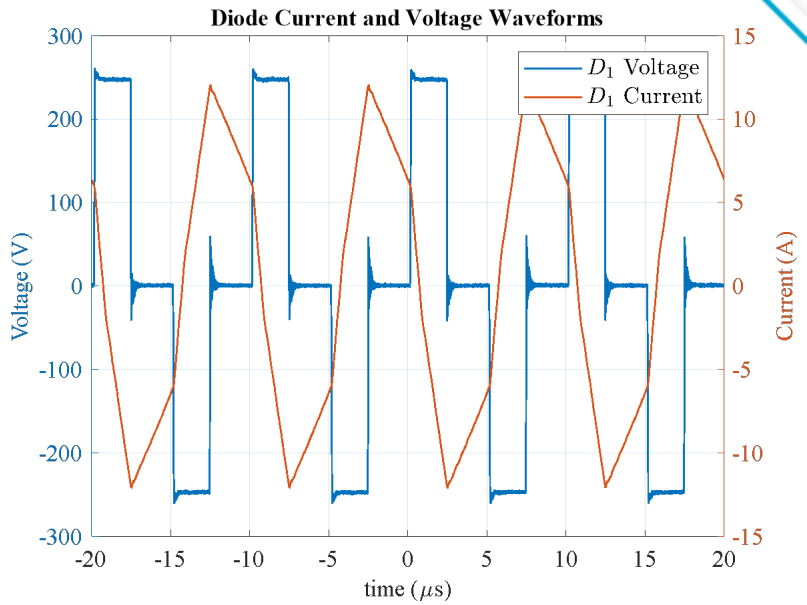
Time interval breakdown

- Theoretical waveforms showing the operation of the circuit in CC mode.



In-circuit diode voltage measurement

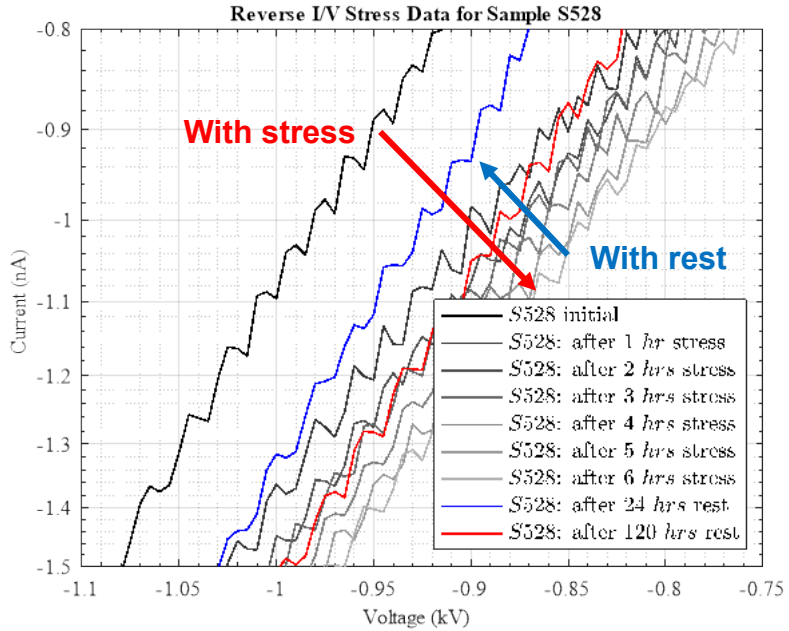
- Voltage waveforms captured for the 500 V stress test of D_1 and D_2.

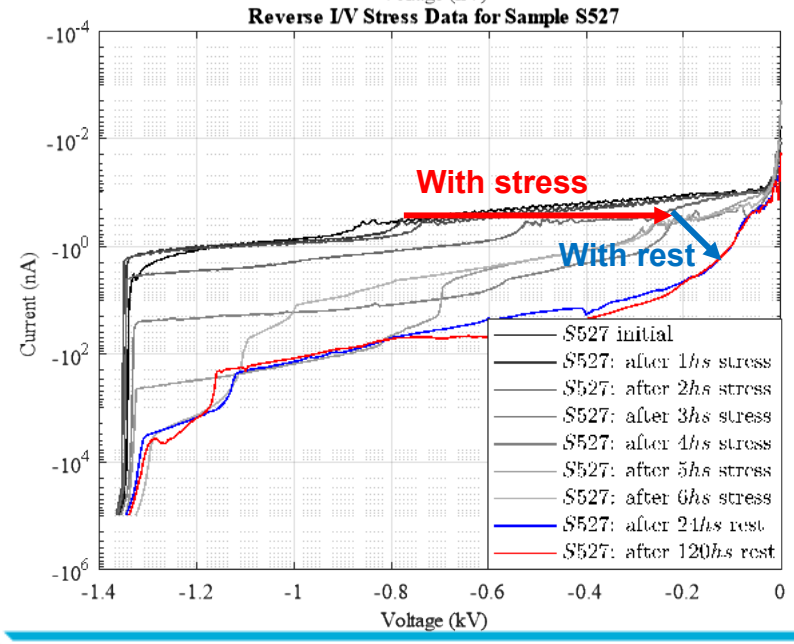


Transformer primary voltage and current

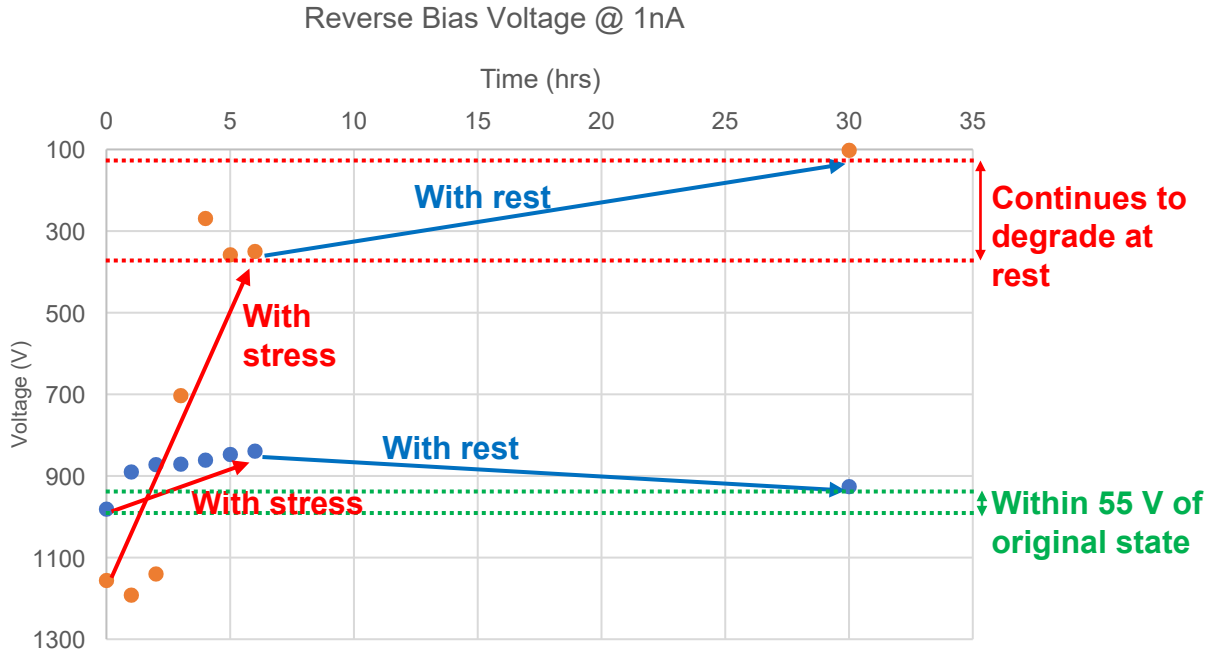
- Transformer current shows proper CC mode of operation for the 500 V stress test.

RESULTS FROM REVERSE I/V CURVES AFTER 6 HRS STRESS

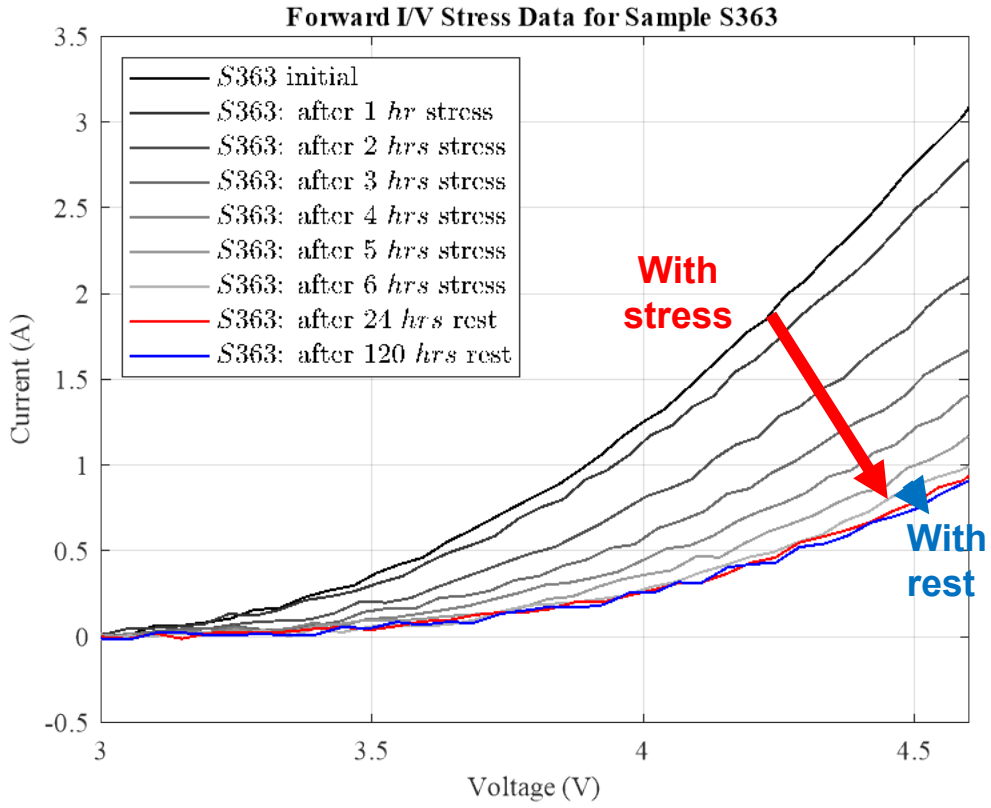


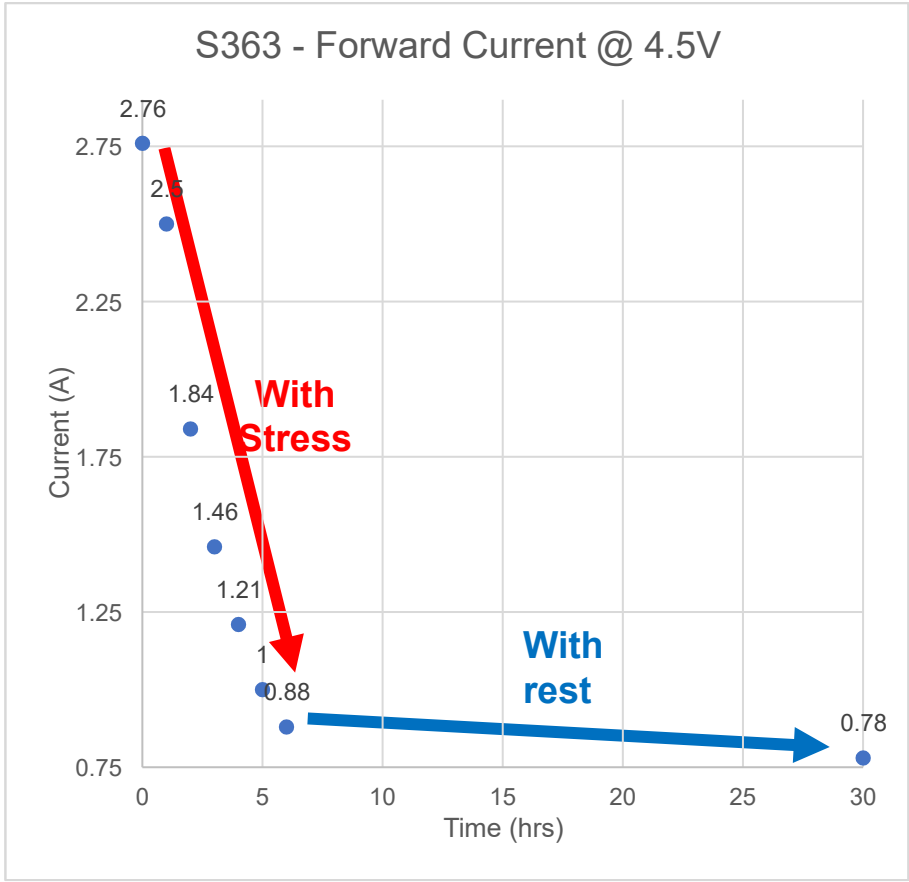


- The previous RDPT experiment results where the v-GaN diode showed degradation and recovery after rest were replicated in some, although not all, of the tests.
- Other v-GaN devices showed major degradation during stress, and kept degrading even after being at rest.
- The two different behaviors could be due to process variations, and the test can be used as a screen to identity devices that will perform poorly in a power converter.



RESULTS FROM FORWARD I/V CURVES AFTER 6 HRS STRESS





- The forward characterization showed that the devices did not recover even when the reverse characterization of the device showed some recovery, and in some cases the degradation continued even during rest.
- This result was consistent throughout every voltage level in every pair of diodes that were tested.
- Suggests a different root cause than for the reverse-bias degradation, probably not related to charge trapping due to lack of recovery after stress.

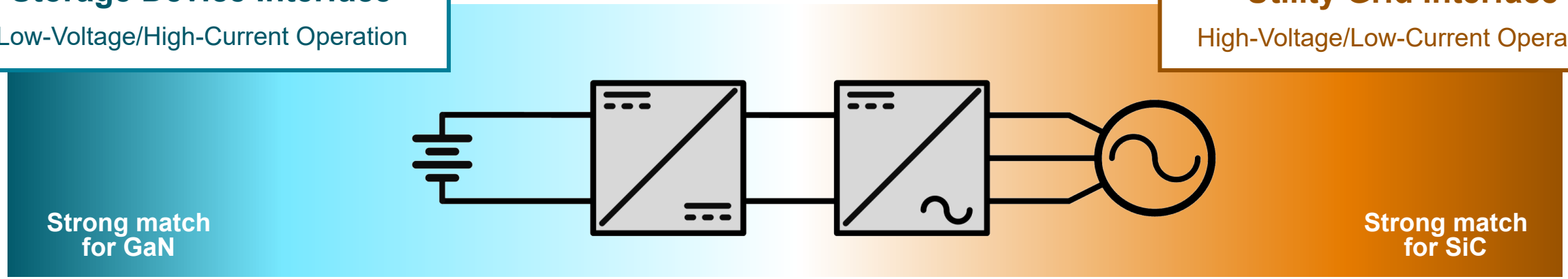
SIC MOSFET STRESS TESTING

Storage Device Interface

Low-Voltage/High-Current Operation

Utility Grid Interface

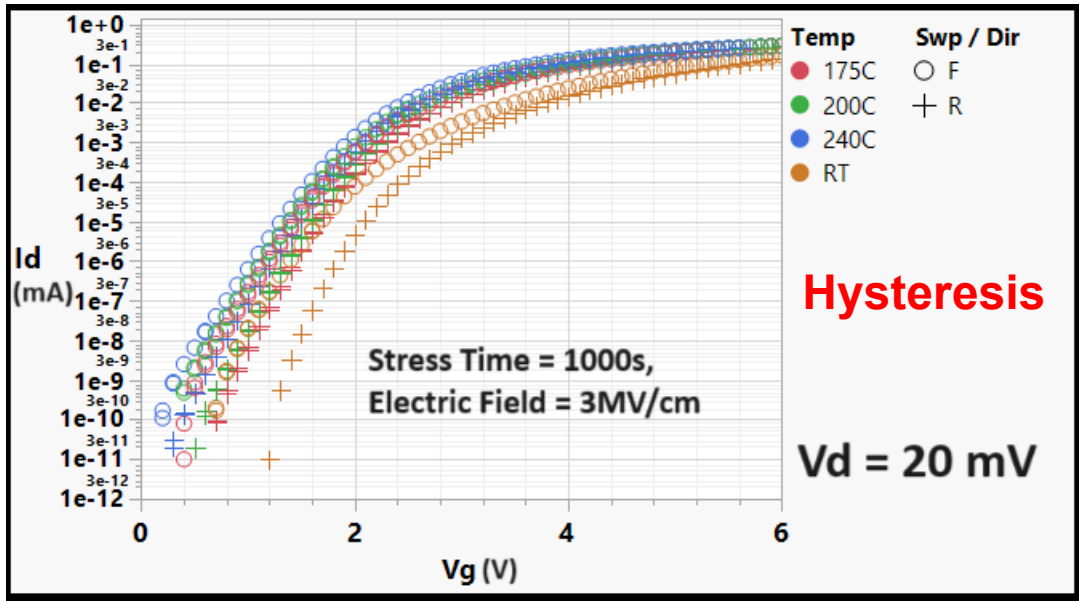
High-Voltage/Low-Current Operation

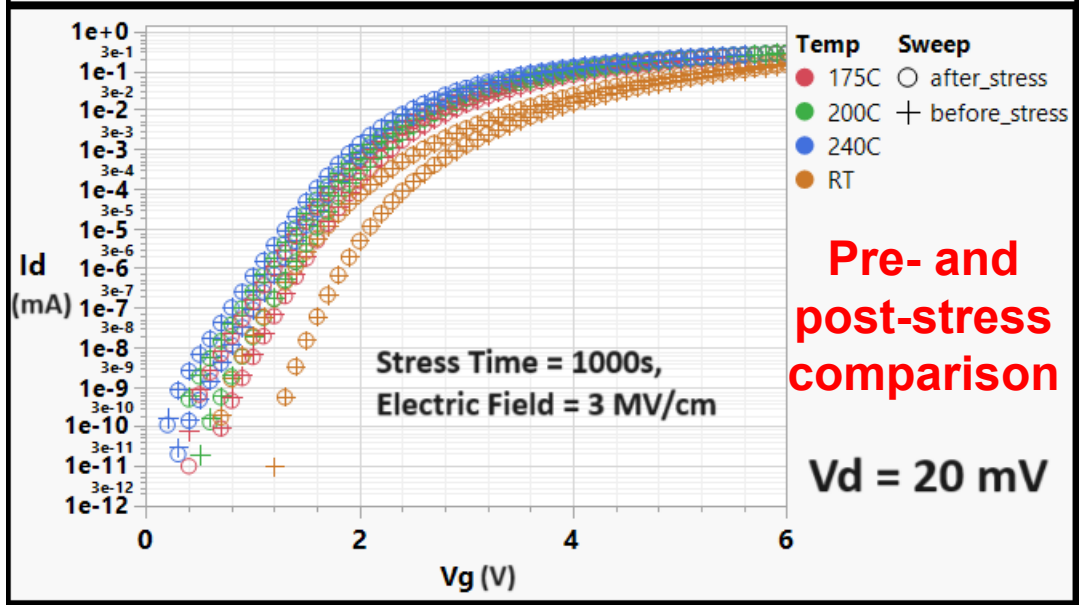


- **GaN is a strong match for the low-voltage/high-current requirements at the battery interface, motivating the studies just described.**
- **SiC is well-matched to the high-voltage/low-current grid interface, with gate oxide integrity being the main degradation factor for SiC MOSFETs.**
- **This motivates current work on bias-temperature stability evaluation and comparison between old and new generations of SiC MOSFETs.**

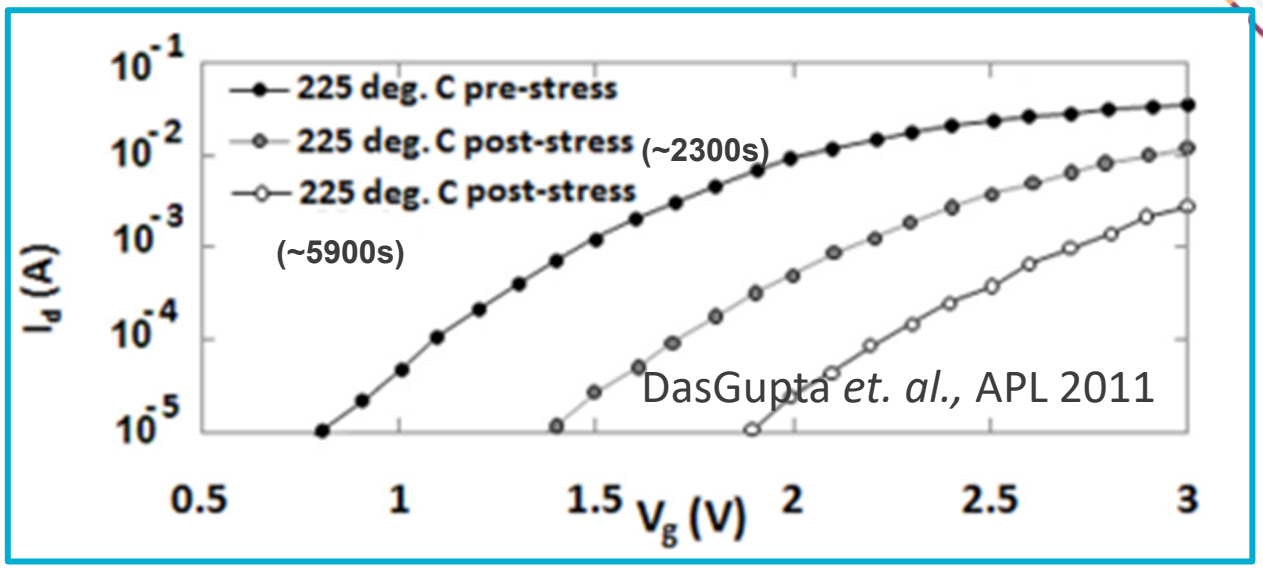
SIC MOSFET BIAS-TEMPERATURE STRESS DATA

Present Generation (2020)





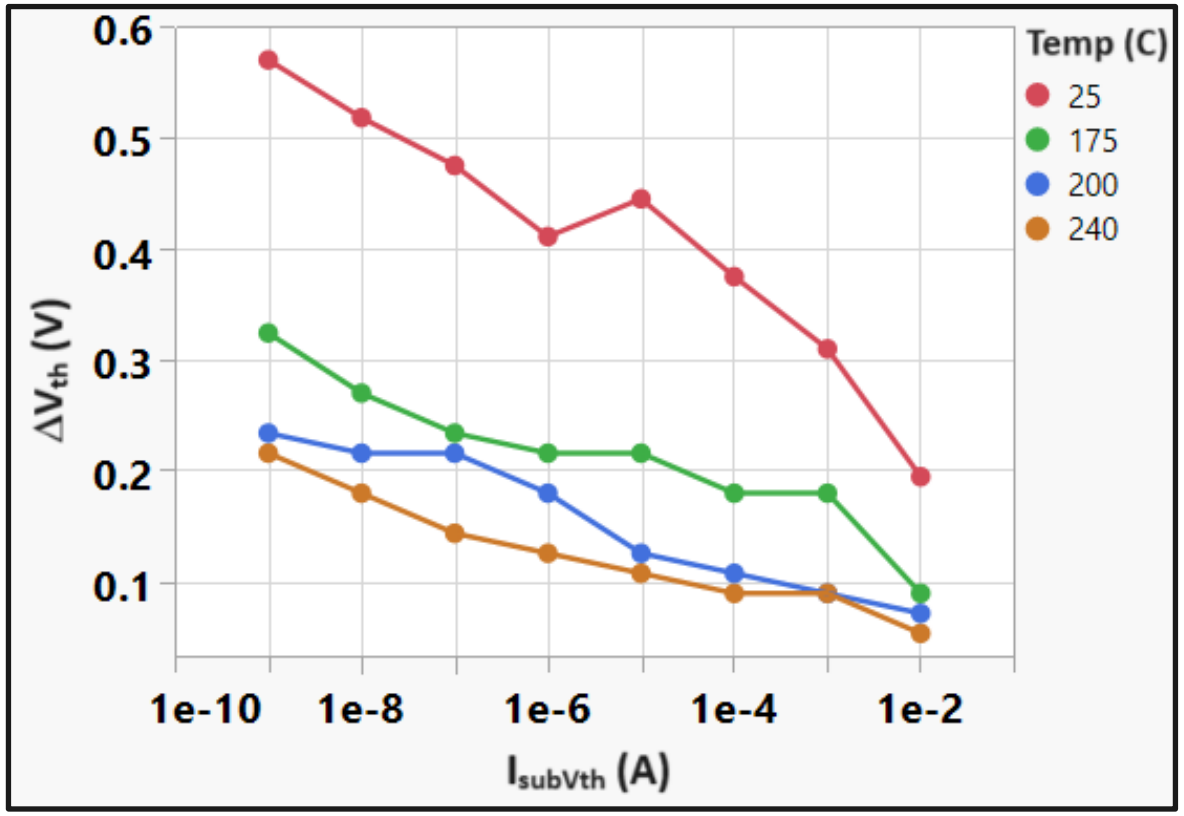
1st Generation (2011)

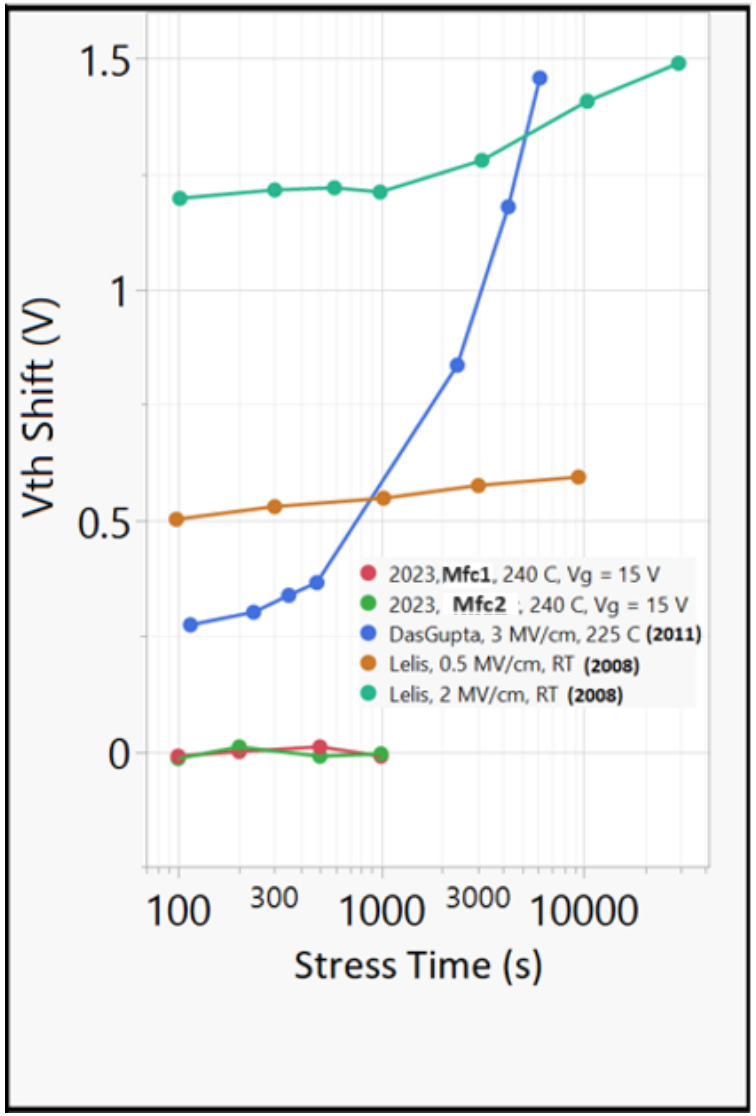


- 1st generation of SiC MOSFETs with SiO_2 gate oxide showed monotonic V_{th} shift.
  - Started at ~150°C and increased with temperature and DC stress time.
  - V_{th} shift was ~0.7 V at 225°C after1000 s of stress.
  - The shift was ~ 0.6 V from oxide trapping and ~0.1 V from interface trapping.
- Present MOSFETs show *no V_{th} shift or drive current loss up to 240 °C.*

However, they exhibit a pronounced hysteresis, which is larger at low temperature and reduces with increasing temperature.

1ST-GENERATION VS PRESENT-GENERATION OXIDES: HYSTERESIS VS V_{TH} SHIFT





- Hysteresis in present-generation MOSFETs is ~0.6 V at low current, ~0.2 V near V_{th} at room temperature, *decreases with temperature* reducing to ~0.2 V at low current, and ~0.05 V near V_{th} at 240°C.
- V_{th} shift in 1st-generation oxides was ~0.7 V at 225°C, 100 s stress.
- The subthreshold swing is comparable in the 2 generations.

Therefore, overall bias-temperature instability is improved at high temperature and degraded at low temperature in present-generation SiC MOSFETs

1ST-GENERATION VS PRESENT-GENERATION OXIDES: HYSTERESIS VS V_{TH} SHIFT TABLE

Feature	1st Generation	Current
Oxide trapping, Vth/drive current shift	Monotnoic, starts at 150°C, increases with temperature and stress time, Vth shift is ~0.6 V at 225°C and 1000 s stress	None up to 240°C
Interface trapping, Vth/drive current shift	Monotnoic, starts at 150°C, increases with temperature and stress time, Vth shift is ~0.1 V at 225°C and 1000 s stress	None up to 240°C
Hysteresis	None	~0.6 V at low current, ~0.2 V near Vth at room temperature, *decreasing with temperature* and reducing to ~0.2 V at low current and ~0.05 V near Vth at 240°C
Sub Vth Swing	kT/q + ~180 mV from interface traps (~ 2 orders of magnitude below threshold current)	kT/q + ~180 mV from interface traps (~ 2 orders of magnitude below threshold current)

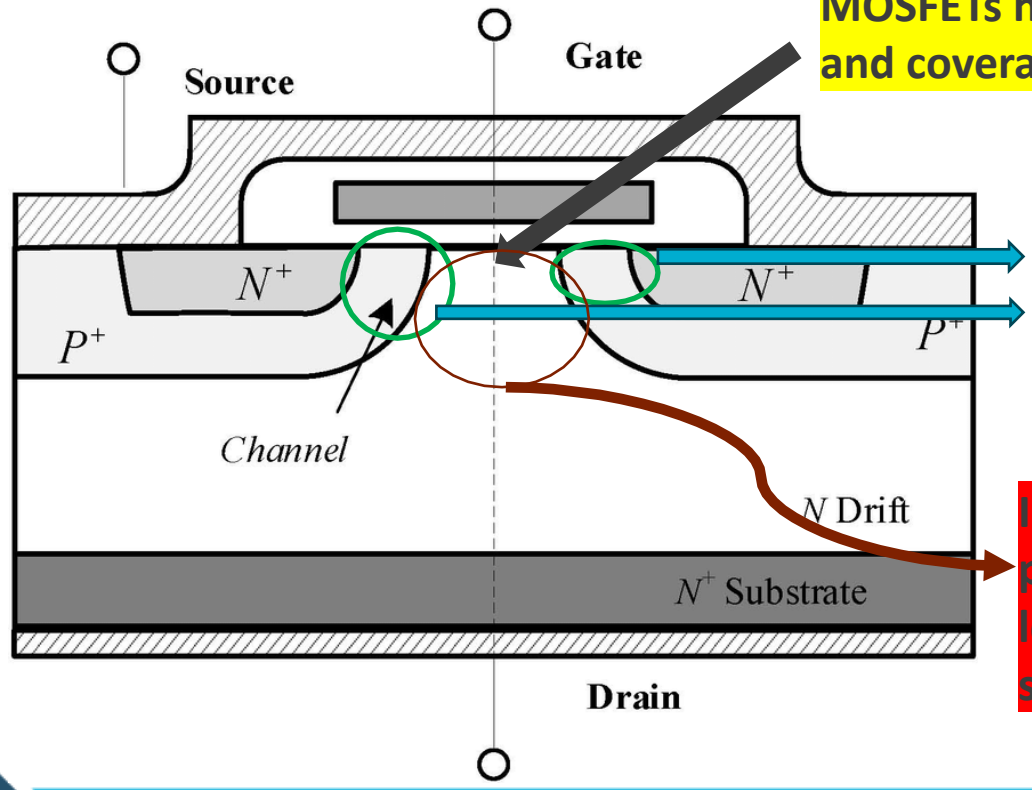
HYSTERESIS IN PRESENT-GENERATION OXIDES: POSSIBLE MECHANISM

Key Observations:

i) No change in drive current; *change is entirely in the subthreshold conduction regime.*

ii) Hysteresis is high at low temperature, reduces at high temperature.

Both observations are more suggestive of a floating body effect rather than trapping in the oxide over the channel



MOSFETs have higher electron density and *might have* poor oxide quality and coverage in the n-region away from channel

Lower e density, better coverage and quality in channel, no trapping, no change to drive current

In epi drift layer region, potential could shift leading to reduction in subthreshold current

Subthreshold current $I_D = I_{D0}e^{VGS/kT}$

$I_{D,\ pre\ trapping} = I_{D0}e^{VGS/kT}$

$I_{D,\ post\ trapping} = I_{D0}e^{(VGS - \Delta Vtrap)/kT}$

$$I_{D,\ pre\ trapping}/I_{D,\ post\ trapping} = e^{\Delta Vtrap/kT}$$

Indicates that subthreshold conduction degradation reduces with increasing temperature, consistent with observations

CONCLUSIONS

- **Using a GaN exemplar case, we have established a process that allows us to evaluate the validity of new WBG device technologies from electrical characterization metrics, to switching characteristics, to integration and validation of operation in practical in-circuit environments.**
- **This process allows us to understand the performance, reliability, and overall potential of new technologies with unbiased "third party testing", and will also help us to understand where they can be optimally utilized.**
- **This process of preliminary validation of new WBG technologies is crucial to the power electronics connected to ESS, which can optimally make use of both GaN for low-voltage/high-current and SiC for high-voltage/low-current.**
- **DC testing of present-generation SiC MOSFETs indicates far superior gate oxide reliability compared to 1st-generation devices; next step is to conduct switch-mode testing, similar to the GaN case.**

Questions?

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Stan Atcitty: satcitt@sandia.gov