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Lawrence Livermore National Laboratory

(U) CONTRACT SOW, UCD RadHard Collaboration

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Disclaimer

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(U) STATEMENT OF WORK, UCD RadHard Collaboration

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1. OVERVIEW

The following subcontract engages UC Davis (UCD) to collaborate with Lawrence Livermore National Laboratory (LLNL) on the design and analysis of microelectronic circuits (macrocells). As part of the proposed statement of work UCD will be given access to information that is export controlled. Within this statement of work UCD is to acquire and install any applicable foundry PDK(s) and collaborate with LLNL on the design of new macrocells and assist in making improvements to existing macrocells as well as the design of ASICs using collections of macrocells. The intent is to increase the application space of the existing LLNL macrocell library and demonstrate the use of the macrocell library, including new designs, by making reference design ASICs.

2. PROGRAM MANAGEMENT

2.1. Program Manager (PM)

The Subcontractor shall perform program management required for program execution and coordination between the Subcontractor and LLNS.

2.2. Program Controls (PC)

The Subcontractor shall perform program planning and control execution required for program execution in support of this effort between the Subcontractor and LLNS.

2.3. Project Engineering (PE)

The Subcontractor shall perform project engineering required for program execution and coordination including technical coordination between the Subcontractor and LLNS. The Subcontractor shall provide reports and Technical Interchange Meeting (TIM) presentations with schedule updates and shall support TIMs and coordination meetings as stated in the Subcontract.

2.4. Schedule

The Subcontractor shall provide a detailed schedule for this development effort with target specifications in accordance with the Subcontract and Additional Requirements and provisions for Fabrications clause in the Subcontract.

2.5. Program Updates

The Subcontractor shall hold regular meetings to provide LLNS with program updates, these are to nominally be held on a weekly or monthly basis as needed. As part of the program update meetings the subcontractor shall provide summary slides on programmatic and technical status.

2.6. Gate Reviews

Key program design gate reviews and program test gate reviews, where indicated, shall be coordinated by the Subcontractor who shall provide at least 30 calendar days' notice prior to scheduling the program gate reviews formally to allow adequate time for LLNS to prepare an attendance list and coordinate a date.

2.7. Contract Execution

This subcontract may be separated into multiple tasks with a scope of work for each explicitly defined. On initial execution of the subcontract LLNS would agree to execute one or more of the tasks. Any remaining tasks are to be considered as options that would not be committed to upon the initial execution of the subcontract but would be committed to as part of one or more contract modifications. This allows LLNS to manage the funding spend rate for the contract and manage risk as the development proceeds.

3. DEFINITION OF TASKS

3.1. Microelectronic Macrocell Design

The subcontractor shall support several activities defined below as part of this collaboration. Specific deliverables are defined that are associated with the general support activities and/or specific macrocell designs.

3.1.1. Programmatic Deliverables

In addition to task specific deliverables, the following programmatic deliverables shall be provided monthly:

- An excel spreadsheet that contains the following rows:
  - The authorized contract execution amount per month including all months since contract execution.
  - The amount invoiced per month including all months since contract execution.
  - The up-to-date anticipated invoice amounts for the entire period of performance of the contract by month.
  - The difference between the authorized contract amount and the anticipated invoice amount by month. This is a critical metric in managing the flow rate of funds and it has been very helpful for LLNL subcontractors to help manage this.
- PPT slides capturing recent accomplishments and next steps.

3.1.2. Supported Activities

Subcontractor shall perform and deliver the following:

1. The subcontractor shall identify a team that can perform analog and mixed signal ASIC design under export control compliance and host a presentation by LLNL that covers the macrocell based ASIC design workflow developed by LLNL in collaboration with Honeywell.
2. The subcontractor shall create a workspace that facilitates ASIC design and test while ensuring a high-level of ESD and foreign object debris (FOD) protection as well as assurance of export control.
3. The subcontractor shall procure and install the Honeywell S150 PDK and corresponding Cadence/Siemens ASIC design tools onto a high-performance computer while ensuring export control.
4. The following list of designs is intended to represent individual design efforts that may be executed individually. Upon mutual agreement and execution of each design effort, the subcontractor shall:

a. Participate in a kickoff meeting to review design intent and any associated documentation. After the kickoff meeting, the subcontract shall provide a report containing proposed development direction and preliminary schedule.
b. Document, present, and provide weekly design progress, design changes, simulations and test results, and any other related information.
c. Provide a final report including detailed explanation of final design. This final report shall include native source files including schematic, symbol, layout, and other design files.

3.1.3. List Of Designs

In the list that follows, a brief description of the design effort and associated scope of work is included to assist with estimating level of effort and costing.

1. Switched Mode Power Supply
    a. LLNL will provide a fully functional and tested SMPS controller design. Using this base design, modify the design to include one of more of the following:
        i. Add capability for higher output current utilizing multiple phases.
        ii. Increase conversion efficiency using radiation hardened MOS devices for power switches.
        iii. Investigate co-packaging critical components like the inductor and power switches into a single multichip module (MCM).
        iv. Power sequencing control.
2. Capacitive Sensing
    a. LLNL will provide a fully functional and tested capacitive sensing ASIC design. Using this base design, modify the design to include one of more of the following:
        i. Increase time constant and precision of accelerometer circuitry by exploring different bias networks and signal conditioning.
3. Displacement Sensing
    a. LLNL will provide a circuit that has an output dependent on space between a coil inductor and conductive barrier. Using this base design, modify the design to include one of more of the following:
        i. Review existing design.
        ii. Verify performance in testing.
        iii. Suggest design improvements.
4. Constant Current Piezo Accelerometer Front End
    a. The subcontractor shall use the existing macrocell library and create a circuit to both supply a constant current to a constant current accelerometer and condition the output of the accelerometer for ADC readout. This design includes:

i. Constant current supply and signal conditioning design using the existing macrocell library and primitives.
ii. Simulate the design.
iii. Perform the layout of the ASIC to be ready for fabrication.

4. APPENDIX

4.1. Acronyms

ADC – Analog to Digital Converter

AFE – Analog Front End

ASIC – Application Specific Integrated Circuit

BEOL – Back End of Line

CDR – Critical Design Review

Chiplet – An ASIC building block fabricated on a standalone die that is untested and delivered in either bare die or packaged form.

CMOS – Complementary Metal Oxide Semiconductor

CTR – Critical Test Review

CUI – Controlled Unclassified Information

DAC – Digital to Analog Converter

DRU – Dose Rate Upset

DRS – Dose Rate Survivability

EM Parts - These Engineering Model packaged parts receive three-temperature testing and get a more detailed inspection, leak/seal test, and a limited dynamic burn-in.

FEOL – Front End of Line

Flight Parts - These parts get QML Q-equivalent or V-equivalent testing and screening.

GPOTA – General Purpose Operational Transconductance Amplifier

IC – Integrated Circuit

KPP – Key Performance Parameter

LLNS – Lawrence Livermore National Security, LLC

Macrocells – ASIC library elements that constitute design building blocks. The macrocells are to be hierarchical design blocks that can quickly be reused, including both schematic and layout. Macrocell testing is limited to bench testing of samples. Delivery of die and packaged die will use untested die and untested packaged die respectively.

MEMS – Micro Electro-Mechanical System

MIMCAP – Metal-Insulator-Metal Capacitor

MRAM – Magnetoresistive Random Access Memory

N – Neutron

NDD – Neutron Displacement Damage

NED – Nuclear Event Detector

NVM – Non-Volatile Memory

P – Proton

PC – Program Controls

PDR – Preliminary Design Review

PE – Project Engineering

PM – Program Management

POD Die – Die tested at wafer level that are first off the line. These die support initial assessment towards evaluating Proof of Design. Die will be tested and may or may not pass all parameters.

POD Parts - Parts that are first off the line and receive packaged-part electrical testing at -55C, +25C, and +125C. These parts support initial assessment towards evaluating Proof of Design. Burn-in will not be performed and no screening of the die will be performed. PODs will be tested and may or may not pass all parameters.

S150HA-M – SOI CMOS (S) 150nm (150) Radiation-Hardened (H) ASIC flow (A) with MIMCAP (-M)

SEE – Single Event Effects

SOI – Silicon On Insulator

TID – Total Ionizing Dose

TRL – Technology Readiness Level

QCI – Quality Conformance Inspection

QM – Quality Management

QML – Qualified Manufacturers List

QSPI – Quad Serial Peripheral Interface

4.2. Definition of Deliverable Content

4.2.1. Design Details

Detailed Design deliverables shall include the following information where applicable:

- Native source design format
  - Example formats include Synopsys, Vivado, Altium, Cadence, CREO (2D and 3D formats)
- For source schematics, the following content shall be included:
  - Circuit topology
  - Connectivity
  - Inputs
  - Outputs
  - Transistors used, with widths, lengths, and type
  - Passive elements with parametric values
  - Top-Level Layout, e.g., in GDSII format
  - VHDL

4.2.2. Procurement Documentation

Procurement Documentation deliverables shall include the necessary documentation to perform repeated fabrication and assembly.

4.2.3. Reports

Report deliverables shall include the below content as applicable and be formatted in both Word and PowerPoint format.

1. Executive Summary
2. Requirements Summary
3. Performance and Specifications Summary
4. Electrical Characteristics
5. Design Approach Summary
6. Design Environment Summary
7. Functional Description
8. Functional Block Diagram
9. Test Bench Summary
10. Simulation conditions Summary
11. Key selected simulation results
12. High-Level Low-Resolution Layout, e.g., in GDSII format
13. Layout dimensions
14. Process Layer summary
15. Pad Ring Definition
16. Pad Assignments
17. Package Outline
18. Package Summary
19. Pin Assignments
20. Radiation Test Plans
21. Reliability Test Plans
22. Conclusions
23. Next Steps