Inverse Segmented Motor Drive Using Dual ANPC Inverters for Common-mode Voltage and Neutral-Point Current Cancellation

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***Abstract*—This article proposes an inverse segmented motor drive (SgMD) utilizing dual active neutral point clamped (ANPC) inverters. In the proposed configuration, the neutral point current and common-mode (CM) voltage is topologically canceled, achieving zero total neutral point current and CM voltage under ideal conditions. Also, the zero total neutral point current minimizes the neutral point voltage imbalance in ANPC inverters. The mechanisms behind neutral point current and CM voltage cancellation in the proposed inverse SgMD are first introduced. The modifications to the motor windings for implementing the inverse SgMD are explained, showing that a standard motor can be readily adapted for the proposed configuration. A space vector modulation (SVM) scheme tailored for the proposed topology is presented, along with a carrier-based implementation. Simulation results validate that the proposed topology can achieve zero total CM voltage and neutral point current. It is also shown that the proposed inverse SgMD can reduce neutral point voltage fluctuation by about 90% and RMS current stress in the dc-link capacitors by about 43% compared to the conventional SgMD.**

Keywords—ANPC inverter, multi-phase motor drives

I. INTRODUCTION

Multi-phase motor drives are gaining more attention in automotive and aerospace applications due to their higher reliability, scalability, and fault-tolerances [1]. Segmented motor drives (SgMDs), where dual inverters drive a multi-phase motor, has emerged as a promising multi-phase topology due to their simple implementation with conventional motor drives [2], [3]. It has been shown that SgMDs can reduce the voltage ripple in DC-link capacitor [3] and common-mode (CM) voltage [4].

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Due to the increasing demand for higher dc-link voltage, there is a growing interest in employing multi-level inverters for multi-phase motor drives [5]. Among many inverter topologies, active neutral-point clamped (ANPC) inverters are gaining more attention due their controllable loss distribution, reliability, and scalability [6]. However, the ANPC inverter family suffers from unbalanced neutral-point (NP) voltage in the split DC-link capacitors, caused by the NP current, which leads to oversized DC-link capacitors [5]. Furthermore, high voltage applications generally suffer from elevated common-mode (CM) voltages v_{CM}, leading to increased electromagnetic interference (EMI) and CM current issues. Therefore, strategies to 1) reduce NP voltage unbalance (or fluctuation) in dc-link capacitors and 2) minimize v_{CM} in multi-phase motor drives with ANPC inverters are essential.

Neutral-point voltage balancing (or NP voltage fluctuation mitigation) strategies have been extensively studied in the literature. These strategies can be classified into three main categories. The first approach is to add auxiliary circuits to force NP voltage balance [7], [8], [9], [10], [11]. However, these hardware-based methods make the system bulkier and less efficient due to the losses associated with the added circuits. It is also possible to reduce NP voltage fluctuation using advanced control schemes such as model predictive control [12]. A more popular method is to inject a zero-sequence voltage into the reference voltage [13], [14], [15] or to use redundant voltage vectors [5], [16], [17], [18]. However, modifying the PWM for NP voltage balancing can degrade the output voltage waveform, leading to an overall performance reduction.

On the other hand, several approaches have been explored to mitigate v_{CM} and its impact on motor drives. One approach involves using EMI filters [19], although this often results in bulkier systems. A more common solution employs advanced PWM schemes with optimized sequences and alternative zero vectors [20], [21], [22]. However, such methods can compromise output voltage quality and reduce system efficiency.

Instead of reducing i_{NP} and v_{CM} separately, it is possible to address both in dual inverter topologies. The cancellation of i_{NP} in dual T-type inverters was first investigated in [23]. Reference [24] expanded the work presented in [23] by applying it to dual NPC inverters and demonstrated the cancellation of both i_{NP} and v_{CM} cancellation effect for a sine PWM (SPWM). However, it remains unclear whether this cancellation can be extended to other modulation schemes such as space vector modulation (SVM). Furthermore, motor winding modifications have not been investigated.

This article proposes an inverse SgMD with dual ANPC inverter, which achieves complete i_{NP} and v_{CM} cancellation using the two ANPC inverters. This results in zero total i_{NP} and v_{CM}, dramatically minimizing the NP voltage fluctuation and v_{CM} issues. The motor winding modification required for the proposed inverse SgMD is discusses in detail, showing that a conventional motor can be easily reconfigured for the proposed topology. This article reveals that i_{NP} and v_{CM} cancellation can be achieved with more general types of PWM schemes (e.g., SVM). A carrier-based implementation of SVM with i_{NP} and v_{CM} cancellation is proposed for the inverse SgMD.

The remainder of this article is as follows: Section II analyze the i_{NP} and v_{CM} of the ANPC inverter in a space vector perspective. Section III proposes the inverse SgMD and its operation to cancel both i_{NP} and v_{CM} in SVM. The modification of the motor winding for the proposed inverse SgMD is also discussed. The carrier-based implementation of the SVM that achieves zero i_{NP} and v_{CM} is presented in Section IV. The i_{NP} and v_{CM} cancellation performance of the proposed SgMD is validated in Section V, while Section VI concludes the article.

II. NP Current and CM Voltage in Segmented Motor Drives with Dual ANPC Inverters

A conventional SgMD is shown in Fig. 1(a), where two ANPC inverters, denoted as INV-1 and INV-2, are connected in parallel, sharing the dc-link. These dual ANPC inverters (i.e., INV-1 and INV-2) drive motor windings 1 and 2, respectively, as shown in Fig. 1(a). The voltage V_{dc} is the dc-link voltage, node N is the NP of the dc-link, n_y is the NP of motor winding y, where y is the inverter (or segment) number (y = 1 or 2). The current in phase x (e.g., $x = a, b$) is denoted by i_x, and the voltage of node X with respect to node Y is given by v_{XY}. For example, the node of the INV-1's c-phase is denoted as $c1$ (see Fig. 1(a)), and the voltage of the node $c1$ with respect to the node N (i.e., NP) is denoted as v_{c1N}.

In this article, when it is necessary to differentiate between INV-1 and INV-2, a double subscript is used. For example, i_a refers to an a-phase current of either INV-1 or INV-2, while i_{a2} refers to the a -phase current in INV-2. The same logic applies to voltage nodes. For example, while node b refers to a genertic b-phase node, node $b1$ refers to the b-phase node in INV-1.

Each phase of an ANPC inverter can have three voltage switching states represented by the switching function s_x, where the phase x's output voltage can be positive (i.e., s_x = P), zero

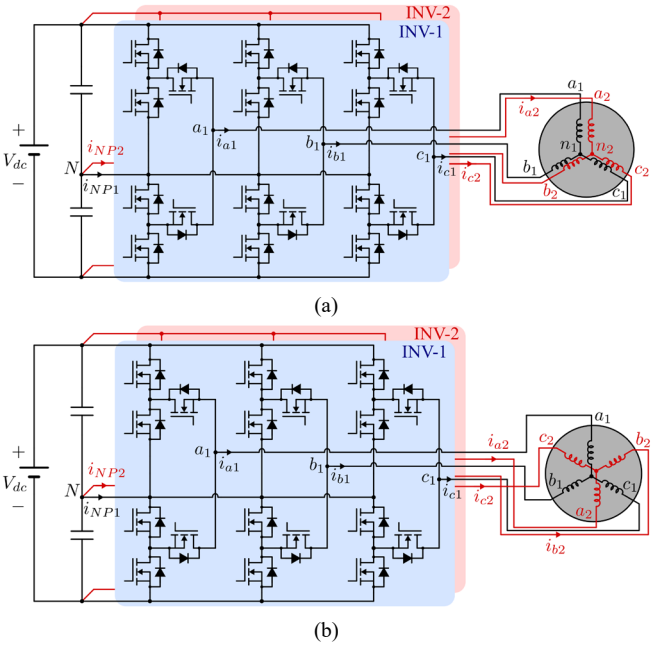


Fig. 1. Schematic of SgMD with dual ANPC inverters. (a) conventional SgMD. (b) proposed inverse SgMD with i_{NP} and v_{CM} cancelling effect.

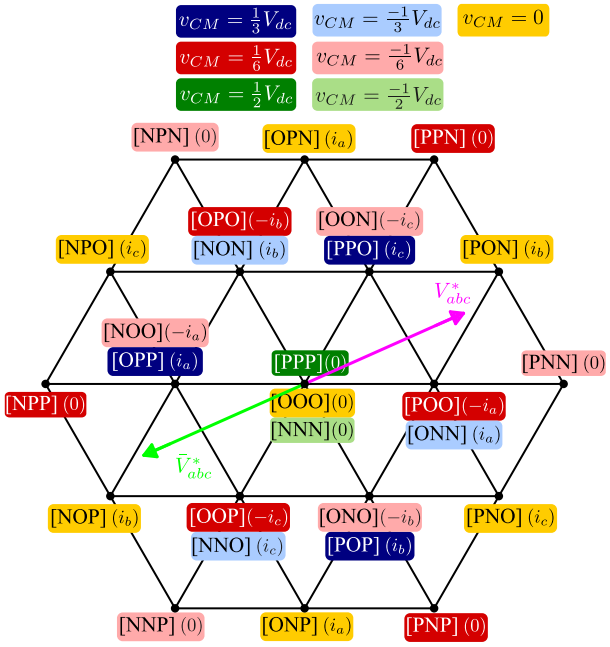


Fig. 2. Space vectors of ANPC inverter where switching states of each phase are shown in brackets (e.g., $[s_a s_b s_c]$, where s_x = P, O, N). Neutral point current i_{NP} generated from each voltage vector are shown in parenthesis. CM voltage v_{CM} generated from each voltage vector are color-coded (i.e., blue: $v_{CM} = 1/3V_{dc}$, light blue: $v_{CM} = -1/3V_{dc}$, red: $v_{CM} = 1/6V_{dc}$, light red: $v_{CM} = -1/6V_{dc}$, green: $v_{CM} = 1/6V_{dc}$, light green: $v_{CM} = -1/6V_{dc}$, yellow: $v_{CM} = 0$).

(i.e., s_x = O), or negative (i.e., s_x = N). In a three-phase ANPC inverter, different combinations of switching states result in 18 active voltage vectors and 3 zero vectors, as shown in Fig. 2.

Each switching state (e.g., [PPN] in Fig. 2) generates different NP current i_{NP} and v_{CM} . The NP current i_{NP}

associated with each switching state are shown in the parenthesis in Fig. 2, assuming

$$i_a + i_b + i_c = 0 \tag{1}$$

which is true for balanced three-phase system. The three zero voltage vectors (e.g., [PPP], [OOO], [NNN]) and six large voltage vectors (e.g., [PNN], [PPN], [NPN], [NPP], [NNP], [PNP]), results in zero i_{NP} and are indicated as "(0)" in Fig. 2. The total NP current of a SgMD is given by

$$i_{NP,tot} = i_{NP1} + i_{NP2} \tag{2}$$

where $i_{NP,tot}$ is the total i_{NP} in the SgMD, while i_{NP1} and i_{NP2} are the i_{NP} of INV-1 and INV-2, respectively.

The CM voltage v_{CM} is given by

$$v_{CM} = \frac{v_{aN} + v_{bN} + v_{cN}}{3} \tag{3}$$

and the v_{CM} values of each switching state are color-coded in Fig. 2. In an SgMD with two ANPC inverters, the total v_{CM} is

$$v_{CM,tot} = \frac{v_{CM1} + v_{CM2}}{2} \tag{4}$$

where INV-1's v_{CM} is given by

$$v_{CM1} = \frac{v_{a1N} + v_{b1N} + v_{c1N}}{3} \tag{5}$$

and v_{CM} in INV-2 is

$$v_{CM2} = \frac{v_{a2N} + v_{b2N} + v_{c2N}}{3} \tag{6}$$

where v_{xyN} denotes the voltage at node xy with respect to node N (phase $x = a, b, c$, and inverter number $y = 1, 2$).

III. Proposed Inverse Segmented Motor Drive with NP Current and CM Voltage Cancellation

A PWM sequence of a symmetric space vector PWM (SVM), synthesizing the reference voltage vector V^*_{abc}

$$V^*_{abc} = \frac{2}{3} \cdot \left(v^*_{a1n1} + v^*_{b1n1} \cdot e^{\frac{2\pi}{3}} + v^*_{c1n1} \cdot e^{\frac{4\pi}{3}} \right) \tag{7}$$

where v^*_{x1n1} is the reference voltage defined between INV-1's output node and the motor neutral point n_1 is shown in Fig. 3(a). If INV-2 is synthesizing V^*_{abc}, the reference voltages should be replaced with the voltage defined between INV-2 and the motor neutral point n_2 (e.g., replace v^*_{a1n1} with v^*_{a2n2}).

The current i_{NP1} and voltage v_{CM1} generated by this PWM sequence is also shown in Fig. 3(a). Note that only half of the switching period (denoted $T_s/2$) is shown in Fig. 3. If INV-2 is also synthesize V^*_{abc} using the same PWM sequence as the INV-1, the i_{NP} generated by INV-2 (i.e., i_{NP2}) is the same as that of INV-1 (i.e., i_{NP1}). Since i_{NP1} and i_{NP2} are identical, there is no cancellation effect on the total NP current $i_{NP,tot}$, as shown in Fig. 3(a). Similarly, if both INV-1 and INV-2 synthesize V^*_{abc} using the same PWM sequence, v_{CM1} and v_{CM2} are also the same and there is no v_{CM} cancellation.

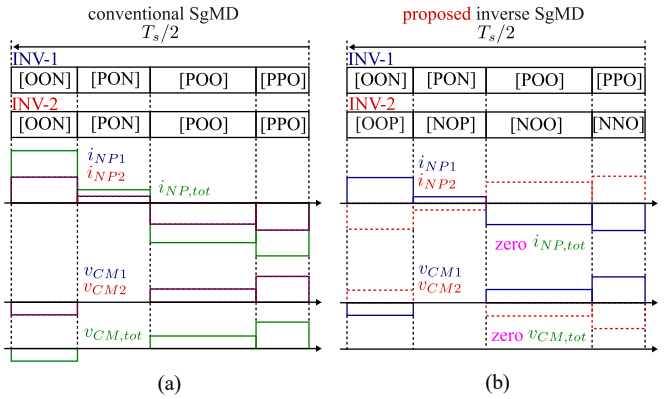


Fig. 3. PWM sequence and switching states of INV-1 and INV-2 and $i_{NP,tot}$ and $v_{CM,tot}$. (a) conventional SgMD. (b) proposed inverse SgMD achieving zero $i_{NP,tot}$ and $v_{CM,tot}$.

It is possible to *reduce* $i_{NP,tot}$ and $v_{CM,tot}$ in the conventional SgMD using more advanced PWM techniques or control methods. However, such approaches increase the implementation complexity of the system and can degrade overall performances by using the available degrees of freedom to reduce $i_{NP,tot}$ and $v_{CM,tot}$. Therefore, it is advantageous to propose a topology-level solution that can inherently cancel both i_{NP} and v_{CM} in the SgMD, leading to zero $i_{NP,tot}$ and $v_{CM,tot}$.

A. Motor Winding Modification for Proposed Inverse Segmented Motor Drive

The proposed inverse SgMD, shown in Fig. 1(b), can dramatically reduce both $i_{NP,tot}$ and $v_{CM,tot}$ (theoretically to zero) by leveraging the canceling effect between INV-1 and INV-2. This cancelling effect is achieved by inverting the direction of motor windings 1 and 2, ensuring that motor currents flowing in opposite directions contribute to the same motor flux. Such a modification can be easily implemented by inverting the direction of a one set of three-phase winding.

The cross-sectional view and winding's phasor diagram for the conventional segmented motor are shown in Fig. 4(a). Each winding is denoted as x_y, where $x = a, b, c$ represents the phase of the winding and $y = 1,2$ denotes the inverter number (or segment number). The three-phase motor windings connected to INV-1 are denoted as $a_1b_1c_1$ while those connected to INV-2 are denoted as $a_2b_2c_2$. A winding with an apostrophe (e.g. a'_2) indicates the opposite winding direction from the original winding (e.g., a_2). For example, the winding a_2 enters the motor slot, while winding a'_2 comes out of the motor slot.

The phasor diagram of both $a_1b_1c_1$ and $a_2b_2c_2$ windings for the conventional segmented motor is shown in Fig. 4(a). It is clear from the phasor diagram that the windings $a_1b_1c_1$ and $a_2b_2c_2$ and aligned, as the phasor of winding x_1 and x_2 point in the same direction. This winding arrangement indicates that the currents in the winding x_1 and x_2 contribute constructively to the same motor flux.

The cross-sectional view and winding's phasor diagram for the proposed inverse segmented motor are shown in Fig. 4(b).

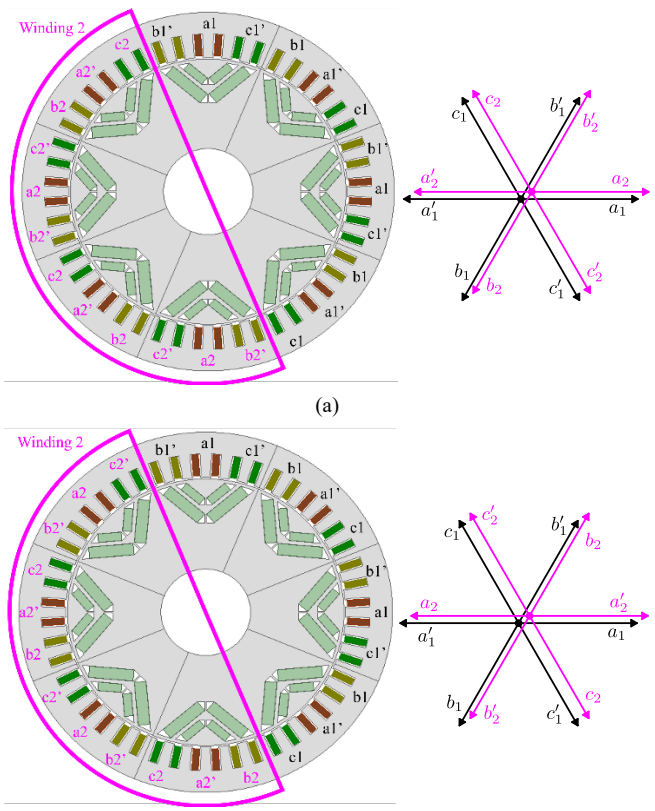


Fig. 4. Cross-sectional view and phasor diagram of segmented motor with two sets of three-phase windings (i.e., $a_1b_1c_1$ and $a_2b_2c_2$) . The winding with an apostrophe (e.g., a_1', b_2') indicates winding coming out of the motor. (a) conventional segmented motor. (b) inverse segmented motor for proposed inverse SgMD.

The stator geometry of the proposed inverse segmented motor is identical to that of the conventional motor shown in Fig. 4(a). The only difference lies in the between the direction of the $a_2b_2c_2$ winding, as shown in Fig. 4(b). For example, the winding a_2 in the conventional motor becomes winding a_2' in the proposed segmented motor, as shown in Fig. 4(b).

It is evident from the phasor diagram of the proposed segmented motor (see Fig. 4(b)) that the windings $a_1b_1c_1$ and $a_2b_2c_2$ are inversely aligned. The phasor of winding x_1 is opposite in direction to that of winding x_2, while the phasor of x_1 aligns with that of the modified winding x_2', as shown in Fig. 4(b). This winding arrangement ensures that the currents in windings x_1 and x_2' (instead of x_2) contribute constructively to the same motor flux. For example, if $i_{a1} = -i_{a2}$, the motor fluxes generated by i_{a1} and i_{a2} reinforce each other in the same direction in the proposed segmented motor. In contrast, in the conventional SgMD (see Fig. 1 (a) and Fig. 4(a)), the motor currents $i_{a1} = i_{a2}$ produce the motor flux in the same direction, which is the opposite from the proposed inverse SgMD.

B. *Neutral Point Current Canacellation Mechanism of Proposed Inverse Segmented Motor Drive*

Since the motor winding's directions are reversed in the proposed inverse SgMD, the voltage synthesized by the ANPC inverters must also be inverted. For example, if INV-1 synthesizes V_{abc}^*, then INV-2 should synthesize $\bar{V}_{abc}^* = -V_{abc}^*$, generating voltages with opposite polarity, as shown in Fig. 2.

For the proposed inverse SgMD, the PWM sequence is shown in Fig. 3(b), assuming that INV-1 synthesizes V_{abc}^* and INV-2 synthesizes $\bar{V}_{abc}^* = -V_{abc}^*$, as shown in Fig. 2. Unlike the conventional SgMD case shown in Fig. 3(a), INV-1 and INV-2 operate with different switching states. If fact, those switching states are the inverse of each other. For example, the switching state [OON] in INV-1 and [OOP] in INV-2 synthesize voltages of equal magnitude but opposite polarity, as shown in Fig. 2. These switching state both produce $i_{NP} = -i_c$, as shown in Fig. 2. However, due to the reversed winding direction in the proposed inverse SgMD, $i_{NP} = -i_c$ in INV-1 and INV-2 results in opposite polarity currents (i.e., $i_{c1} = -i_{c2}$). As a result, $i_{NP,tot} = i_{NP1} + i_{NP2} = 0$. The same logic applies to other switching states as well, leading to $i_{NP,tot} = 0$ throughout the PWM sequence, as shown in Fig. 3(b). Thus, the proposed inverse SgMD achieves complete cancellation of i_{NP}.

C. *Common-mode Voltage Canacellation Mechanism of Proposed Inverse Segmented Motor Drive*

The proposed inverse SgMD can also achieve zero $v_{CM,tot}$ as v_{CM1} and v_{CM2} always cancel each other, topologically. For example, when INV-1 operates in the switching state [OON], INV-2 operates in the switching state [OOP] for the same dwell time. The v_{CM} generated by the switching state [OON] in INV-1 is $v_{CM1} = -1/6V_{dc}$, while that generated by the switching state [OOP] of INV-2 is $v_{CM2} = 1/6V_{dc}$, as shown in Fig. 2. These voltages are equal in magnitude but opposite in polarity, resulting in $v_{CM,tot} = v_{CM1} + v_{CM2} = 0$. The same cancellation effect applies to all switching states, leading to $v_{CM,tot} = 0$ throughout the entire PWM sequence, as shown in Fig. 3(b). Thus, the proposed SgMD can achieve complete cancellation of v_{CM}.

IV. Carrier-Based Implementation of SVM for Proposed Inverce Segmented Motor Drive

Section III discussed how the proposed inverse SgMD cancels both i_{NP} and v_{CM} achieving zero $i_{NP,tot}$ and $v_{CM,tot}$. The PWM and cancellation performance of the proposed inverse SgMD are well illustrated in Fig. 3(b). Using the SVM approach, switching functions (e.g., s_{a2}) can be generated to synthesize V_{abc}^* for INV-1 and $\bar{V}_{abc}^* = -V_{abc}^*$ for INV-2. To ensure complete cancellation of i_{NP} and v_{CM} , it is essential to generate adequate PWM sequences that enforce full cancellation. While it is possible to directly implement SVM with a PWM sequence selection algorithm to guarantee zero $i_{NP,tot}$ and $v_{CM,tot}$, such an approach can be complex, and computationally demanding. Instead, this section develops that the same SVM algorithm can be realized through a carrier-based implementation [25].

Fig. 5 shows how PWM sequences for INV-1 and INV-2 can be generated using carrier-based method. The reference voltages (e.g., v_{a1N}^*, v_{b2N}^*) are the voltages between node N and the

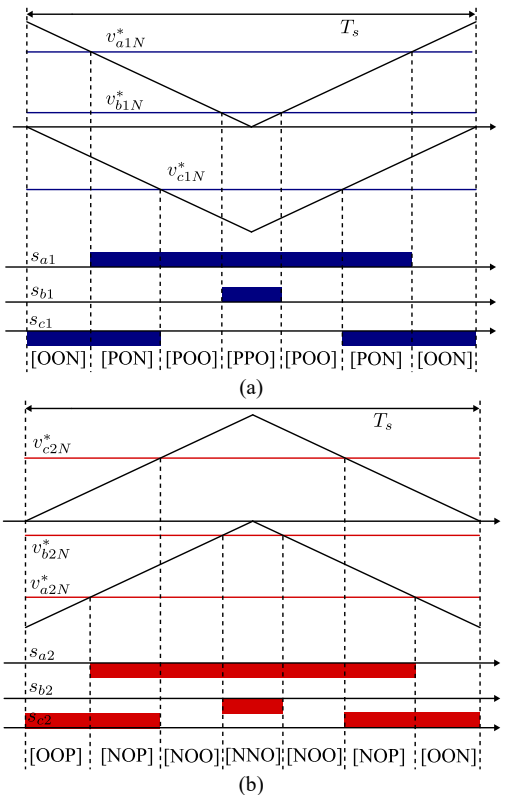


Fig. 5. Carrier-based implementation and switching functions of SVM used in proposed inverse SgMD. (a) switching functions of INV-1 (s_{a1}, s_{b1}, and s_{c1}) synthesizing V^*_{abc}. (b) switching functions of INV-2 (s_{a2}, s_{b2}, and s_{c2}) synthesizing $\bar{V}^*_{abc}$.

ANPC inverter's outputs nodes (e.g., node $a1$ in Fig. 1), which are used for the carrier-comparison.

In sine PWM (SPWM), the reference voltage v^*_{x1N} used in the carrier-comparison is the same as the reference voltage defined between the ANPC inverter's output node x_1 and the motor neutral point n_1 (denoted v^*_{x1n1}), assuming the operation of INV-1 [24], [25]. The same approach applies to INV-2 by replacing v^*_{x1N} with v^*_{x2N}.

The carrier-based SVM can be implemented by adding zero-sequence component v^*_{n1N} to the reference voltage v^*_{x1n1}, such that the reference voltage for carrier comparison becomes

$$v^*_{x1N} = v^*_{x1n1} + v^*_{n1N} \tag{8}$$

for INV-1 ($x = a, b, c$) [24], where v^*_{n1N} is given by

$$v^*_{n1N} = -\frac{v_{\max 1} + v_{min1}}{2} \tag{9}$$
$$v_{\max 1} = \max(v_{a1n1}, v_{b1n1}, v_{c1n1})$$
$$v_{min1} = \min(v_{a1n1}, v_{b1n1}, v_{c1n1}).$$

he same formulation applies to INV-2 by replacing the subscript 1 with 2. Using these modified v^*_{x1N} values, SVM can be implemented using carrier-comparison. However, simply using the modified v^*_{x1N} does not guarantee zero $i_{NP,tot}$ and $v_{CM,tot}$.

TABLE I. SgMD System Parmeters

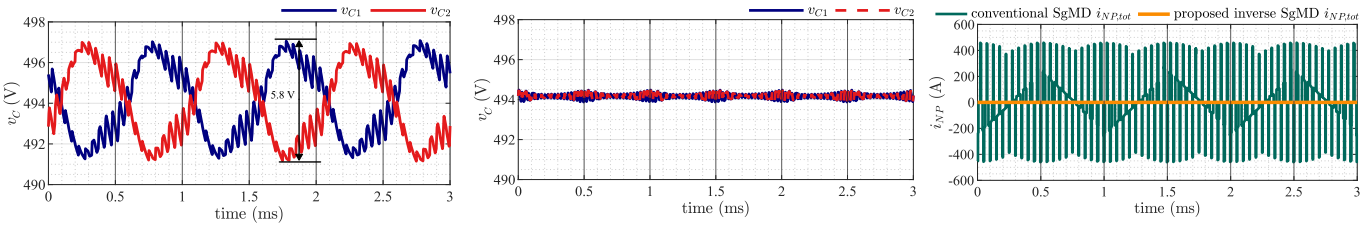
Parameter	Values	Parameter	Values
rated power (kW)	380	number of pole pairs	4
rated speed (RPM)	5000	stator resistance (Ω)	0.12
switching freq. (kHz)	20	d-axis inductance (μH)	192.8
fundamental freq. (Hz)	333.3	q-axis inductance (μH)	575.1
dc-link voltage (V)	1100	rated torque (Nm)	726
dc-link capacitance (mF)	1	PM flux (Wb)	0.2521

In the proposed inverse SgMD, INV-1 synthesizes V^*_{abc}, while INV-2 synthesizes $\bar{V}^*_{abc}$. If INV-1 and INV-2 share the same carrier, the PWM sequence for INV-2 would be [NNO]-[NOO]-[NOP]-[OOP] during the half the switching period ($T_s/2$). This PWM sequence of INV-2 cannot cancel the i_{NP1} and v_{CM1} generated by INV-1, which uses the PWM sequence [OON]-[PON]-[POO]-[PPO]. To achieve complete cancellation of i_{NP1} and v_{CM1} using i_{NP2} and v_{CM2}, the carrier signal for INV-2 must be inverted (or 180° phase-shifted) relative to INV-1, as shown in Fig. 5(b). As a result, the PWM sequence for INV-2 becomes [OOP]-[NOP]-[NOO]-[NNO], which matches the PWM sequence for INV-2 shown in Fig. 3(b). This result confirms that the carrier-based implementation can achieve full cancellation of i_{NP} and v_{CM}, as long as the carrier for INV-2 is inverted (or 180° phase-shifted) with respect to INV-1. Thus, it is shown that SVM with full i_{NP} and v_{CM} cancellation can be realized by modifying the reference voltage using (8) and by inverting the carrier used in INV-2.

V. Validation of Neutral Point Current and Common-Mode Voltage Cancellation of Proposed Inverse Segmented Motor Drive

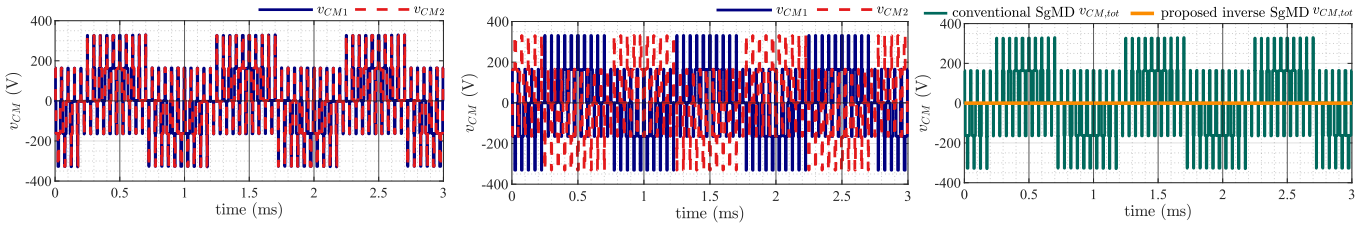
A comparative simulation analysis was conducted to validate the effectiveness of i_{NP} and v_{CM} cancellation in the proposed inverse SgMD. The conventional SgMD was used as the baseline for this study. Both the conventional and the proposed SgMD systems, along with their respective SVM schemes, were implemented in the simulation software. The switching frequency f_s was set to 20 kHz, and the fundamental frequency f_e was 333.3 Hz. The dc-link voltage V_{dc} was 1100 V. Additional SgMD system parameters are provided in TABLE I. The simulation results for i_{NP} and v_{CM} are shown in Fig. 6 and Fig. 7 respectively. The results confirm the cancellation performance of the proposed inverse SgMD.

The i_{NP} in ANPC inverter causes low-frequency voltage fluctuations at the NP of dc-link capacitors C_1 and C_2 (see Fig. 1). In the cases of the conventional SgMD, $i_{NP,tot}$ is not zero, as shown in Fig. 6(c). Consequently, the voltage of C_1 and C_2, denoted v_{C1} and v_{C2}, fluctuate with a peak-to-peak amplitude of approximately 5.8 V, as shown in Fig. 6(a). In contrast, the proposed inverse SgMD cancels i_{NP} in INV-1 and INV-2, resulting in $i_{NP,tot} = 0$, as shown in Fig. 6(c). As a result, NP of the ANPC inverter does not experience low-frequency voltage fluctuations, as shown in Fig. 6(b). The small voltage ripple in v_{C1} and v_{C2} in Fig. 6(b) corresponds to high-frequency switching ripple, which can be improved by increasing C_1 and C_2 , or by increasing f_s. The peak-to-peak



(a) (b) (c)

Fig. 6. Simulation result of dc-link capacitor voltages v_{C1}, v_{C2} and total neutral point current $i_{NP,tot}$ under SVM operation. (a) v_{C1}, v_{C2} in conventional SgMD. (b) v_{C1}, v_{C2} in proposed inverse SgMD with i_{NP} cancelation effect. (c) comparison of $i_{NP,tot}$ in conventional SgMD and proposed inverse SgMD.



(a) (b) (c)

Fig. 7. Simulation result of common-mode voltages v_{CM1}, v_{CM2}, and $v_{CM,tot}$ under SVM operation. (a) v_{CM1}, v_{CM2} *in* conventional SgMD (b) v_{CM1}, v_{CM2} in proposed inverse SgMD with v_{CM} cancellation effect. (c) comparison of $i_{NP,tot}$ in conventional SgMD and proposed inverse SgMD.

voltage ripple in Fig. 6(b) is approx. 0.6 V, which is about 90% lower than the fluctuation observed in the conventional SgMD.

Additionally, eliminating the low-frequency voltage fluctuation at the NP also reduces the low-frequency current flowing through the dc-link capacitors. Compared to the RMS current in the dc-link capacitors C_1 and C_2 in the conventional SgMD (i.e., 124.1 Arms), the proposed inverse SgMD exhibits approximately 70.3 Arms in these capacitors, reducing the RMS current stress by about 43.3%. Such a current stress reduction can substantially improve the lifetime and reliability of the dc-link capacitors.

The v_{CM} of the individual ANPC inverters in the conventional SgMD is shown in Fig. 7(a), and $v_{CM,tot}$ is shown in Fig. 7(c). Since both INV-1 and INV-2 in the conventional SgMD synthesize the same output voltage, v_{CM1} and v_{CM2} are identical, as shown in Fig. 7(a). As a result, the conventional SgMD cannot cancel v_{CM}, leading to a non-zero $v_{CM,tot}$, as shown in Fig. 7(c). On the other hand, in the proposed inverse SgMD, INV-1 and INV-2 synthesize voltages of equal magnitude but opposite polarity. Therefore, v_{CM1} and v_{CM2} have opposite polarities, resulting in cancellation of v_{CM}, as shown in Fig. 7(b). Consequently, the proposed SgMD achieves zero $v_{CM,tot}$, as shown in Fig. 7(c).

VI. Conclusions

The article proposes an inverse SgMD topology with dual ANPC inverters that is capable of achieving zero neutral point current i_{NP} and common-mode voltage v_{CM} through a cancelling effect. The required motor winding modification for the proposed inverse SgMD is discussed in detail, demonstrating that a conventional motor can be easily reconfigured for the proposed approach. The operating principle and the cancellation mechanism of i_{NP} and v_{CM} are explained using space vectors of ANPC inverters. A carrier-based implementation of the proposed space vector modulation (SVM) for realizing i_{NP} and v_{CM} cancellation in the proposed inverse SgMD is also presented. Simulation studies confirm that the proposed inverse SgMD achieves zero total i_{NP} and total v_{CM} using the proposed carrier-based SVM scheme. In addition, due to the elimination of total i_{NP}, it is shown that the proposed inverse SgMD with SVM can reduce the neutral point voltage fluctuations (or imbalance) by approximately 90% — from 5.8 V to 0.6 V — and reduce the RMS current stress in the dc-link capacitors by about 43% — from 124.1 Arms to 70.3 Arms — compared to the conventional counterpart.

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References

[1] L. de Lillo et al., "Multiphase power converter drive for fault-tolerant machine development in aerospace applications," *IEEE Trans. Ind. Electronics*, vol. 57, no. 2, pp. 575-583, Feb. 2010.

[2] X. Lyu, Y. Li and D. Cao, "DC-link RMS current reduction by increasing paralleled three-phase inverter module number for segmented traction drive," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 5, no. 1, pp. 171-181, March 2017.

[3] G. -J. Su and L. Tang, "A segmented traction drive system with a small dc bus capacitor," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Raleigh, NC, USA, 2012, pp. 2847-2853.

[4] A. M. Alcaide et al., "Common-mode voltage mitigation of dual three-phase voltage source inverters in a motor drive application," *IEEE Access*, vol. 9, pp. 67477–67487, 2021.

[5] N. Celanovic and D. Boroyevich, “A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters,” *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 242–249, Mar. 2000.

[6] S. M. Maaz and D. -C. Lee, "Common-mode voltage mitigation for dual three-phase three-level ANPC inverters using dynamic phase-shift PWM," *IEEE Access*, vol. 11, pp. 104234-104243.

[7] A. Shukla, A. Ghosh, and A. Joshi, “Control of DC capacitor voltages in diode-clamped multilevel inverter using bidirectional buck-boost choppers,” *IET Power Electron*., vol. 5, no. 9, pp. 1723–1732, Nov. 2012.

[8] S. Srikanthan and M. K. Mishra, “DC capacitor voltage equalization in neutral clamped inverters for DSTATCOM application,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2768–2775, Aug. 2010.

[9] M. K. Mishra, A. Joshi, and A. Ghosh, “Control schemes for equalization of capacitor voltages in neutral clamped shunt compensator,” *IEEE Trans. Power Del*., vol. 18, no. 2, pp. 538–544, Apr. 2003.

[10] A. V. Jouanne, S. Dai, and H. Zhang, “A multilevel inverter approach providing DC-link balancing, ride-through enhancement, and common-mode voltage elimination,” *IEEE Trans. Ind. Electron*., vol. 49, no. 4, pp. 739–745, Aug. 2002.

[11] Y. Chen, B. Mwinyiwiwa, Z. Wolanski, and B.-T. Ooi, “Unified power flow controller (UPFC) based on chopper stabilized diode-clamped multilevel converters,” *IEEE Trans. Power Electron.,* vol. 15, no. 2, pp. 258–267, Mar. 2000.

[12] A. Mora, R. Cárdenas-Dobson, R. P. Aguilera, A. Angulo, F. Donoso, and J. Rodriguez, “Computationally efficient cascaded optimal switching sequence MPC for grid-connected three-level NPC converters,” *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 12464–12475, Mar. 2019.

[13] Z. Wang, F. Cui, G. Zhang, T. Shi, and C. Xia, “Novel carrier-based PWM strategy with zero-sequence voltage injected for three-level NPC inverter,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 4, pp. 1442–1451, Dec. 2016.

[14] J. Pou, J. Zaragoza, S. Ceballos, M. Saeedifard, and D. Boroyevich, “A carrier-based PWM strategy with zero-sequence voltage injection for a three-level neutral-point-clamped converter,” *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 642–651, Feb. 2012.

[15] X. Yuan, Y. Li, and C. Wang, “Objective optimization for multilevel neutral-point-clamped converters with zero-sequence signal control,” *IET Power Electron.*, vol. 3, no. 5, pp. 755–763, Sep. 2010.

[16] A. Zorig, S. Barkat, and A. Sangwongwanich, “Neutral point voltage balancing control based on adjusting application times of redundant vectors for three-level NPC inverter,” *IEEE J. Emerg. Sel. Topics Power Electron*., vol. 10, no. 5, pp. 5604–5613, Oct. 2022, doi: 10.1109/JESTPE.2022.3186927.

[17] A. Lewicki, Z. Krzeminski, and H. Abu-Rub, “Space-vector pulsewidth modulation for three-level NPC converter with the neutral point voltage control,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 5076–5086, Nov. 2011.

[18] J. Pou, R. Pindado, D. Boroyevich, and P. Rodriguez, “Evaluation of the low-frequency neutral-point voltage oscillations in the three-level inverter,” *IEEE Trans. Ind. Electron.*, vol. 52, no. 6, pp. 1582–1588, Dec. 2005.

[19] M. Antivachis, P. S. Niklaus, D. Bortis, and J. W. Kolar, “Input/output EMI filter design for three-phase ultra-high speed motor drive GAN inverter stage,” *CPSS Trans. Power Electron. Appl*., vol. 6, no. 1, pp. 74–92, Mar. 2021.

[20] A. M. Hava and E. Ün, "A high-performance PWM algorithm for common-mode voltage reduction in three-phase voltage source inverters," *IEEE Trans. Power Electronics*, vol. 26, no. 7, pp. 1998-2008, July 2011.

[21] Z. Liu, P. Wang, W. Sun, Z. Shen, and D. Jiang, ‘‘Sawtooth carrier-based PWM methods with common-mode voltage reduction for symmetrical multiphase two-level inverters with odd phase number,’’ *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 1171–1183, Jan. 2021.

[22] X. Xu, Z. Zheng, K. Wang, B. Yang, and Y. Li, “A carrier-based common-mode voltage elimination method for back-to-back three-level NPC converters,” *IEEE Trans. Power Electron.,* vol. 37, no. 3, pp. 3040–3052, Mar. 2022.

[23] S. Bhattacharya, D. Mascarella, G. Joos, J. Cyr and J. Xu, "A dual three-level T-NPC inverter for high-power traction applications", *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 04, no. 2, pp. 668-678, Jun. 2016.

[24] S. Wang, M. Fereydoonian and W. Lee, "Six-phase three-level neutral point clamped inverter for capacitor voltage balancing and common-mode voltage cancellation," *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Phoenix, AZ, USA, 2021, pp. 1091-1096.

[25] V. Blasko, "Analysis of a hybrid PWM based on modified space-vector and triangle-comparison methods," *IEEE Trans. Ind. Appl.*, vol. 33, no. 3, pp. 756-764, May-June 1997.