Miniaturized Millimeter-Wave Multilayer Filter Design Using Additive Manufacturing

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***Abstract*— This paper presents an innovative, fully additive manufactured approach to millimeter-wave multilayer circuits. An aerosol jet printer is used to fabricate a multilayer stepped-impedance low-pass filter. By leveraging the second layer for miniaturization, we achieve a more compact design. By precisely controlling conductor separation and utilizing 3D printing technology, we were able to optimize the width of the high and low-impedance segments for optimal filter performance. Two filter types were successfully fabricated: a low-pass microstrip filter and a low-pass stripline filter, both with a cutoff frequency near 29 GHz and exhibiting excellent roll off. The stripline configuration allows for a 39 % decrease in the total stripline area. The line loss of both designs was characterized using a microstrip through line and a stripline through line. Both designs demonstrated low overall loss, with the microstrip line exhibiting a loss of 0.26 dB/mm and the stripline having a loss of 0.37 dB/mm at 29 GHz. This work demonstrates a multilayer integration solution and offers an advantage in reducing the size of RF circuits such as filter banks for next-generation integrated RF front ends.**

***Keywords*— Additive manufacturing (AM), aerosol jet printing (AJP), millimeter-wave (mm-wave), Filter.**

I. Introduction

As consumer devices push for higher data rates and increased compactness of devices, a packaging solution is needed to keep up with this demand. Another issue is that operation at higher frequencies requires tighter system integration to maintain performance. Additive manufacturing (AM) has been proven as a promising and competitive alternative in the field of RF and mm-wave electronics [1], [2], [3], [4]. The ability to deposit both conductive and dielectric material at smaller scales and with high accuracy makes AM an attractive packaging solution compared to traditional integration processes. Along with this, AM can deposit material in 3 dimensions making it a candidate process for 3D heterogeneous integration (3DHI) in sixth-generation (6G) devices.

Aerosol jet printing (AJP) is a promising style of AM and a good alternative to already existing manufacturing techniques. Some advantages of aerosol jet printing include easier customization, rapid prototyping, high resolution, and reduced non-recurring manufacturing costs. This process allows for the conformal printing of circuits on uniform and nonuniform surfaces alike, and can produce routing layers without the need for additional processes such as bumps, wire bonding, or via-based transitions. It also covers a large range of feature sizes from 10 μm to 10 mm. Unlike other AM techniques, the AJP process can print both metal and dielectrics on 3D surfaces with the same machine. Ongoing research in multilayer circuits utilizing AJP will help lay the foundation for the realization of 3DHI.

It is common for RF front-end modules to include filter banks that occupy a large portion of the integrated space. These filters are often difficult to make smaller when constrained to planar designs. In this work, we will focus our efforts on reducing the filter size through a 3D multilayer design which will enable higher-performance systems. [1]

Previous work has demonstrated the ability to fully 3D print passive components while integrating semiconductor chips in a package. In [4], bypass capacitors were printed. This technique proved that capacitive elements can be created using additive manufacturing. This approach demonstrates AJP as an attractive process for the development of System on Package (SOP) designs for RF front ends. The work in [5] demonstrates a low pass filter on single-crystalline diamond. The filter design in [5] achieves a 40 GHz cutoff frequency, demonstrating that a filter could utilize the exceptional properties of diamond as a substrate. These properties include having high thermal conductivity and having a small loss tangent over a wide range of frequencies. The diamond AJP filter demonstrates great scalability upwards in frequency as well as potentially better heat handling. The present work will build on this previous AJP work and improve the performance already shown.

One way other works have accomplished size reduction of filters is by utilizing the third dimension through the ability to create a thickness-modulated transmission line. A mix of stereolithography (SLA) 3D printing and aerosol jet printing was used to fabricate the structure shown in [6]. [6] demonstrated that additive manufacturing can create a structure with a higher rejection ratio than its planar counterpart. Reference [6] successfully displayed the operation of the "rollercoaster" filter at lower frequencies. The "rollercoaster" design introduces improvements by introducing a thickness-modulated transmission line filter which allows for the reduction of width for the capacitive segments. This design was also successful creating a filter with a higher rejection ratio compared to a comparable planar filter design. The main disadvantage of this design was the large size of the structure and not being able to scale upwards in frequency to cover

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microwave and millimeter bandwidths due to SLA printer limitations.

[2] While extensive research has focused on single-layer AM packages, there hasn't been much development in terms of techniques that leverage the advantages of multilayer 3D AM circuits. This research aims to demonstrate a multilayer filter circuit using the AJP process that is compatible with SOP designs for RF applications. The availability of 3D design through the AJP process allows changes to the physical layout of the circuit that are not easily achievable with other methods. This work will build on the idea of the thickness modulation technique shown in [6] while being significantly smaller. Three additional techniques that the AJP process easily enables are: adding a customizable printed ground plane, adding serpentine lines to the filter design, and adding an additional layer of silver on top. With the multilayer techniques that AJP enables, we will demonstrate that these techniques can reduce the overall conductor area of the filter.

II. Transmission Line & Filter Design

Prior to fabricating the filter, a microstrip through line was constructed using the concept of incorporating a printed ground plane between two layers of polyimide shown in Figure 1a. This basic design serves as a proof-of-concept for incorporating a customizable printed ground plane, which is utilized in all subsequent designs. The conductor line length in this design was 4.5mm. A stripline wave guide was also designed by adding a second printed ground plane on top. The fabricated wave guide can be seen in Figure 2a for a through line. The line loss of both the microstrip through line and the stripline through line was characterized. ANSYS HFSS was used to validate the broadband performance of these transmission lines. A unique feature of this filter is its fully 3D-printed ground plane, which eliminates the reliance on a specific substrate. This increases the options for integration, thus enhancing its versatility.

A Chebyshev low-pass filter was selected for integration into a multi-layer package due to its sharp cutoff and easy implementation in microstrip and stripline configurations. The filter circuit was initially designed using lumped elements in Keysight's Advanced Design System (ADS). The chosen shunt capacitors and series inductors were simulated to achieve the desired low-pass filter cutoff frequency of 27 GHz and its expected roll-off.

To fabricate the filter using waveguides, the lumped elements were replaced with high- and low-impedance waveguide sections. A high ratio of high to low impedance segments is needed for optimal filter performance. From the Telegrapher's equations, we determine that low-Z line segments can be used as a lumped shunt capacitor while high-Z line segments are used as lumped series inductors:

$$Z = \sqrt{\frac{(R + j\omega L)}{(G + j\omega C)}} \tag{1}$$

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The electrical lengths of the elements were calculated based on the desired inductance and capacitance values:

$$L = \frac{\beta \cdot l \cdot Z_h}{R_0} \tag{2}$$

$$C = \frac{\beta \cdot l \cdot R_0}{Z_l} \tag{3}$$

Where L and C represent the desired inductance and capacitance values of the respective segments. R_0 is the nominal system impedance of 50Ω. Z_H and Z_L represent the characteristic impedance of the waveguide segments being used to generate the desired inductance, L, and capacitance, C, for the filter.

A filter with a traditional planar layout was designed using the concept of low-Z and high-Z line segments, the full process is highlighted in [7]. High-impedance line segments were designed at 120 ohms, while low-impedance segments were designed at 20 ohms. The designed plate separation was chosen with the smallest feature size in mind, which is the width of the high-Z 120 Ω segment.

Once the performance of the planar microstrip filter was successfully verified in ADS, segments of alternating high and low-impedance lines were used to create a low-pass microstrip filter. This stepped impedance planar filter was fabricated shown in Figure 1b. The filter design consisted of seven stages. ANSYS HFSS was used to simulate the cutoff performance of the design. A planar stripline filter was also designed in the same fashion, enabling a reduction in the area of the middle conductor shown in Figure 2b. The spacing between the middle conductor and the top ground was designed to be identical to the spacing in the bottom region. Both ends of the filter were connected to a microstrip launch, which was impedance-matched to 50 Ω, as shown in Figure 3.

Using the same design methods a multilayer stepped-impedance low-pass microstrip filter was designed using ANSYS HFSS. To create a low-pass microstrip filter alternating segments of high and low impedance lines are used shown in Figure 4. For the capacitive segments, the area can be calculated using the following equation:

$$C = \frac{\epsilon \cdot A}{d}$$

This shows that reducing the height of the segment can maintain the same capacitance with less conductor area. Low-impedance segments were placed on 20μm dielectric segments to enable a more compact capacitor width of 162 μm compared to the original 300 μm. Similarly, the inductive segments were positioned on 68μm raised dielectric regions, allowing for wider traces of 18 μm. Increasing the elevation allows for the inductive segments to reach higher inductance without having to increase the length of the line. We demonstrate a design of a multilayer filter much like [6].

We improve upon this design by decreasing the size of the filter conductor area using additional techniques that are easily implemented with AJP. Figure 5 shows the full HFSS stack-up for the microstrip filter design. The inductance of

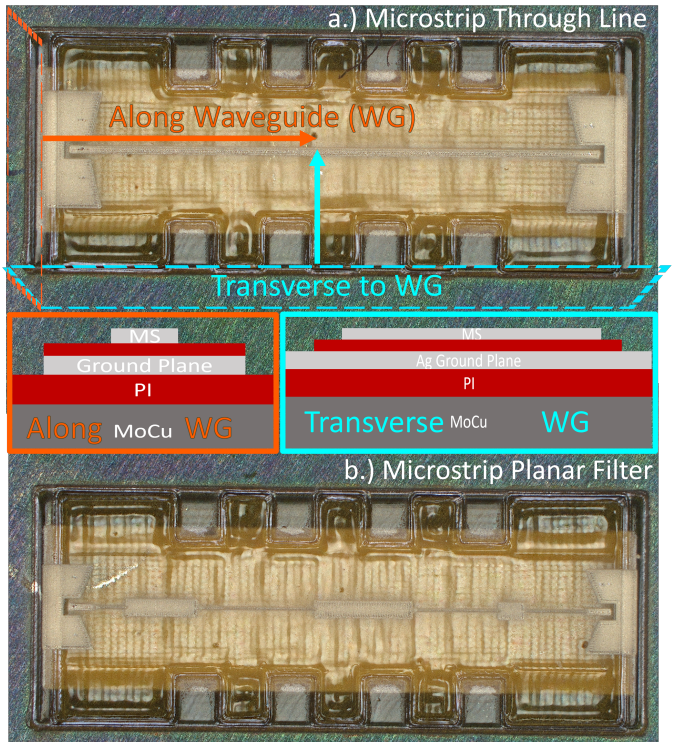

Fig. 1. Fabricated printed a.) thru microstrip line b.) planar microstrip filter sharing similar side profiles. Where the orange arrow represents the front cross-sectional plane along the waveguide and the blue arrow represents the side cross-sectional plane transverse to the waveguide. Anchoring structures are unused in both microstrip cases.

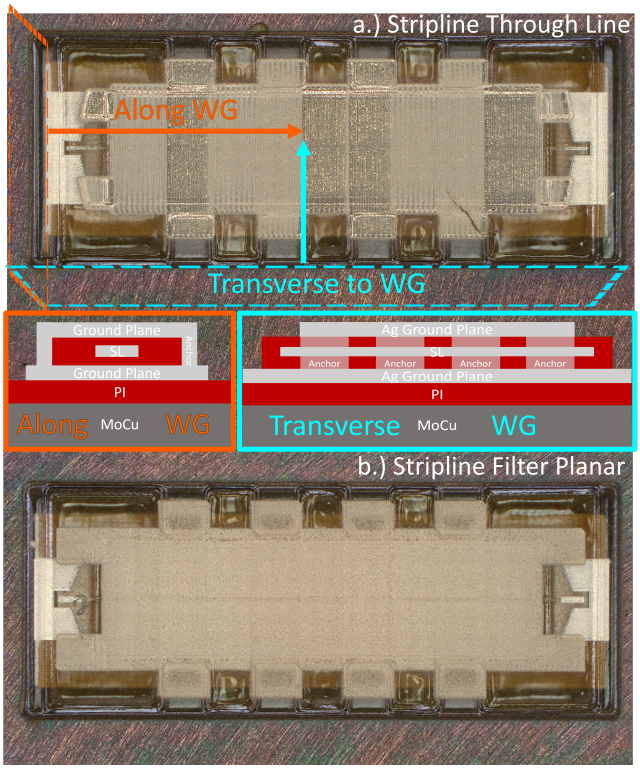

Fig. 2. Fabricated printed a.) thru stripline line b.) planar stripline. Where the orange arrow represents the front cross-sectional plane along the waveguide and the blue arrow represents the side cross-sectional plane transverse to the waveguide. Anchoring structures are used for silver-silver contact between printed grounds.

the lower impedance segments can be further increased by using serpentine lines. This method increases the effective inductance by adding length to the line segment without increasing the overall filter footprint. Figure 6 shows the fabricated model of the multilayer microstrip. Additionally, the ground underneath the inductive segment was removed which reduces the capacitance of the line, increasing effective inductance. This was fine-tuned to match the ideal inductor in the ADS design. The ground can be easily patterned in the electronic files for the direct-write AJP process and is not limited to any particular layout.

The final addition to this stepped impedance multilayer filter was converting the design into a stripline configuration. Figure 7 shows the stack-up design of the stripline multilayer filter. Figure 8 shows the fabricated model of the multilayer stripline. The dielectric was designed to maintain equal separation between the waveguide and the top and bottom ground plane on each side. This design also uses serpentine lines and patterned grounds to fine-tune the high-Z segments. The addition of a top ground plane allows electromagnetic fields to interact with both the top and bottom ground planes, like a stripline, and the area of the low-impedance segments can now be reduced. This process reduced the area of both the high- and low-Z segments by 39%.

By utilizing serpentine lines, a patterned ground plane, and a stripline configuration we achieved a 39% reduction in the total area of the waveguide conductor. This approach allowed us to significantly decrease the size of the low-Z segments, leading to an overall wave guide area reduction. [3]

III. Fabrication

This multilayer filter design was fabricated using an Aerosol Jet 5X Optomec system. All printed components were fabricated on a molybdenum copper substrate (a high thermal conductive substrate to be used for direct chip mounting in our future designs). A base layer of polyimide dielectric was printed using a pneumatic atomizer. HD Microsystems PI2611 was selected due to its relatively close coefficient of thermal expansion (CTE) match to molybdenum copper. PI2611 has a relatively high solid loading content making it an ideal foundational dielectric material for building up structures. A 0.1% solution of VM651 in water was used as an adhesion promoter and applied to the surface of the molybdenum copper sheet, enabling the PI2611 to adhere to the surface. The dielectric constant of PI2611 has been verified through a Beatty line experiment.

A silver ground plane was printed on top of the polyimide. An ultrasonic atomizer was used to aerosolize the Clariant silver ink. To create openings in the ground plane between the inductive regions, silver material was intentionally not printed

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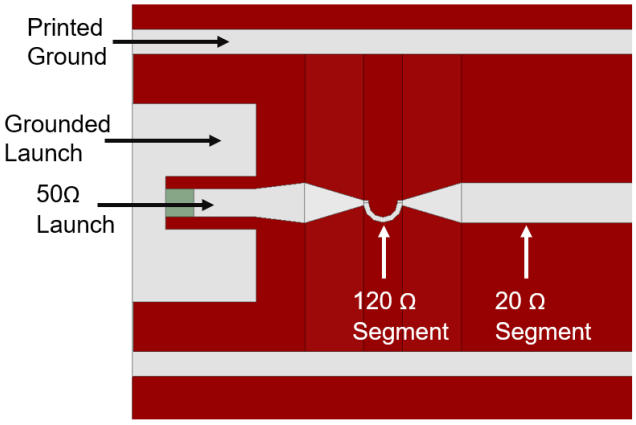

Fig. 3. Designed top view of filter launch. The launch was designed to be 50 Ω. 120Ω waveguide segments are shown on the raised areas while the 20 Ω waveguide segments are shown on the lower areas.

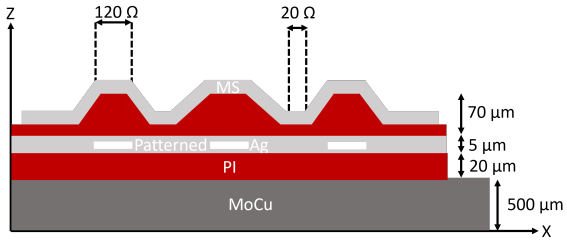

Fig. 4. Microstrip multilayer filter side cross section traverse to waveguide. Part designed in units of μm. Inductive 120Ω waveguide segments are on the raised areas while the capacitive 20 Ω waveguide segments are on the lower areas.

in those areas. The sintering profile of this ink was 180°C for 5 hours, to get improved conductivity. The print parameters of all of the materials used are shown in Table 1.

A second layer of polyimide was deposited on top of the silver ground plane as the waveguide dielectric layer. For the high impedance segments, polyimide reached a height of 68 μm above the printed ground plane, while the lower impedance segments were printed at a distance of 20 μm from the ground plane. Finally, the wave guide conductors were printed on top of the previous polyimide layers in a similar fashion to the ground plane completing the microstrip filter design. All waveguide conductor area measurements are shown in Table 2.

For the stripline design, an additional $15\mu m$ polyimide layer was printed over the impedance segments, which were already pre-designed for dielectric loading. The height of this layer was printed to match the height of the previous dielectric layer as closely as possible for a optimal stripline configuration. A final printed silver ground plane was fabricated on top of the dielectric layer, replicating the features of the first printed ground plane, and completing the full stripline design.

The stripline design encountered the challenge of weak adhesion between the first silver ground plane and the underlying polyimide dielectric. This weak connection led to

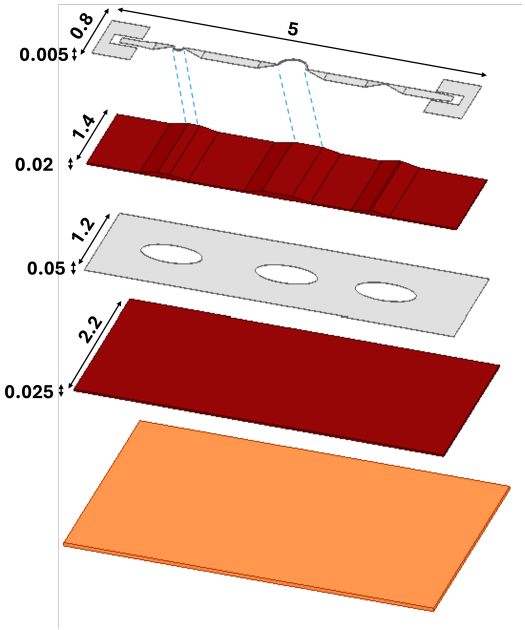

Fig. 5. Layer by layer stack of multilayer microstrip filter with designed dimensions. Layers are printed from bottom to top with their respective curing/sintering profiles in between.

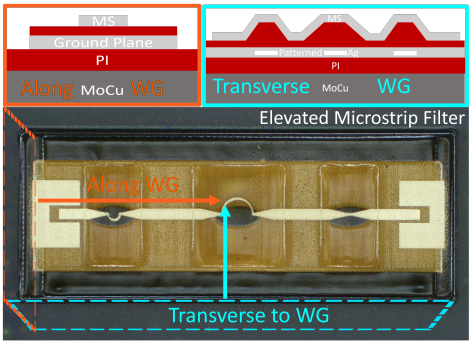

Fig. 6. Fabricated printed multilayer microstrip filter. No anchoring structures are present due to the design being a microstrip.

delamination of the silver layer when a subsequent polyimide layer was printed on top. To address this issue, polyimide anchors were added on top of the second polyimide layer. These anchor-like structures facilitated a connection between the two polyimide layers, providing anchoring for the middle silver layer. Full polyimide coverage was maintained at both launch ends, which are more prone to delamination. The implementation of polyimide anchoring structures resulted in an improvement in the yield rate, eliminating failures during this fabrication step. [4]

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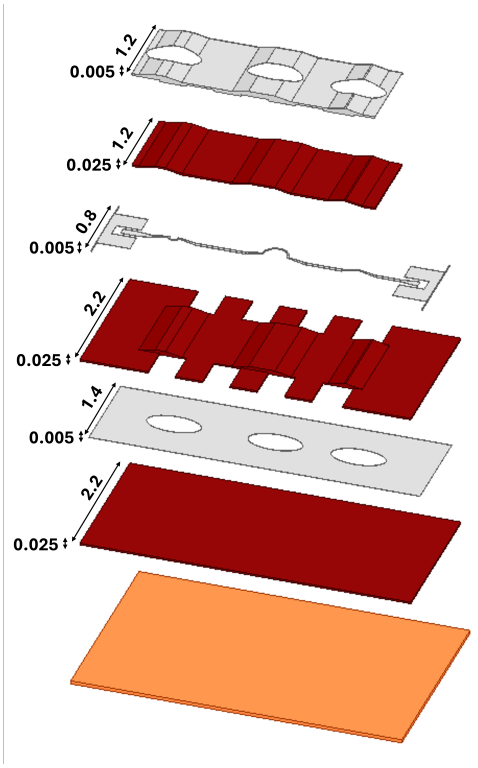

Fig. 7. Layer by layer stack of multilayer stripline filter with designed dimensions. Layers are printed from bottom to top with their respective curing/sintering profiles in between.

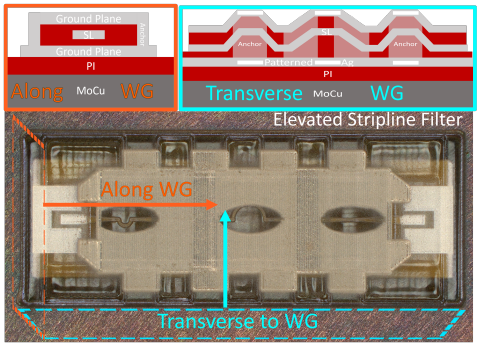

Fig. 8. Fabricated printed multilayer stripline filter. Anchoring structures are present for better silver-silver contact.

IV. Measurements & Discussion

Using a Keyence VK-X3000 3D Surface Profiler, height measurements of each layer were taken and verified before the final silver layer was printed. The dimensions were compared to those in the EM models, then models were backfit to reflect the measured dimensions. This process was repeated for both the filter and the through-line fabrication. All width measurements of the conductive line are shown in Table 3. Height and dielectric constant are the two most important parameters for accurate back fitting. As a result, precise profile measurements are vital for guaranteeing accurate simulation and measurement agreement. The heights of the planar through line, planar filter, and multilayer filter are presented in Table 4 for both configurations. It is important to note that the height elevation in the patterned ground plane was not fully compensated for in the subsequent polyimide layer. The resulting height difference in the polyimide layer above these circles was a small $5\mu m$, which may have contributed to some mismatch loss. [5]

RF measurements were performed using GBB 50A-GSG-250 probes, which were connected to an N5245B PNA-X. A GGB CS5 calibration substrate was used, which places the measurement reference plane at the probe tips. The calibration method that was employed was short-open-load-through (SOLT).

Table 1. Printer Parameters

	PI 2611	Ag (Fine Feature)	Ag (Wide Feature)
Nozzle Diameter	300 μm	150μm	200μm
Steath Flow Rate	65 sccm	40 sccm	65 sccm
Areosol Flow Rate	33 sccm	23 sccm	25 sccm
Single Trace Width	70 μm	16 μm	40 μm
Ink temperature	35°C	25°C	25°C
Platform Temperature	60°C	55°C	55°C

Table 2. Areas of Fabricated Middle Conductors

	Tx/Impedance Conductor Area
MS Thru	0.29 mm^2
SL Thru	0.14 mm^2
MS Planar Filter	0.31 mm^2
SL Planar Filter	0.19 mm^2
MS Multilayer Filter	0.28 mm^2
SL Multilayer Filter	0.16 mm^2

Table 3. Widths of Fabricated Line and Filters

Configuration	Through Line	Planar Filter	Multilayer Filter
Microstrip	63 μm	250 μm	162 μm
Stripline	30 μm	160 μm	55 μm

The microstrip design exhibited excellent broadband performance in terms of its mismatch being below -20dB for the full 50 GHz measurement range. While its insertion loss was slightly higher than previously reported for aerosol-printed packages in the literature, the difference was not substantial. The stripline design added a moderate amount of insertion loss, which was very good given the good impedance matching. The

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Table 4. Heights of Multilayer Filter Designs

	MS Multilayer Filter	SL Multilayer Filter
1st Polyimide	22 μm	23 μm
1st Ground	6 μm	7 μm
2nd Polyimide	11 μm	16 μm
Tx Line	4 μm	5 μm
3rd Polyimide	N/A	14 μm
2nd Ground	N/A	7 μm

insertion loss per length was characterized for both the stripline and microstrip lines using the following equation:

$$S_{21}^{il} = S_{21}^{m}/l$$

Where S_{21}^{il} represents the insertion loss per length, S_{21}^{m} is the measured insertion loss, and l is the total conductor line length excluding launches. The insertion loss is calculated and shown in Table 5, where it is compared to previous literature. The microstrip through line performed comparably to other works, with a slightly higher line loss than reported in [5]. The insertion loss per length is plotted in Figure 9 for both the microstrip line and the stripline.

The measured cutoff frequency for the planar microstrip filter design was 28 GHz. As shown in Figure 10a, the measured cutoff frequency matches closely with the simulated results. The cutoff frequency was determined by using the slope of the passband line to account for the material losses. The roll-off of the measured filter matches the simulated roll-off well. Figure 11a displays the stripline measurements for the planar stepped impedance filter. The simulated roll-off and cutoff frequency in this stripline configuration fits very well with the measured data.

For the multilayer microstrip filter shown in Figure 10b, the measured cutoff frequency occurs at approximately 26.9 GHz. We observe a stopband roll-off of 23 dB/octave, reasonably matching our expected roll-off of 20 dB/octave. The cutoff frequency for the multilayer stripline matched well with the backfit simulations at 31.4 GHz, while the roll-off value was still high at 17.2 dB/octave. The multilayer stripline measurements are shown in Figure 11b. The stripline filter involved higher design complexity, requiring tighter tolerances in the dielectric heights. The fabricated heights of both the microstrip and stripline multilayer filters are shown in Table 4, demonstrating a reasonable amount of accuracy in the layer deposition process.

It is noted that in terms of the planar filter, the high-Z waveguide width was reduced from $250\mu m$ to $160\mu m$. For the same designs, the impedance areas were successfully shrunk from 0.3092 mm^2 in total area to $0.1973mm^2$, which was a 36% reduction

The end product of this work involved the design and fabrication of a 3D stepped-impedance low-pass filter. This design builds upon the success of the planar filter by incorporating much smaller capacitors and further maximizing conductor miniaturization, achieving a reduced conductor width of 52 μm from the already shrunk 162 μm. As with the previous design, serpentine lines were utilized in the inductive segments to enhance inductance. This multilayer stepped impedance filter demonstrates the application of the additional shielding ground plane concept to a non-planar surface. Compared to traditional non-3D printed techniques, this fully 3D-printed filter design offers high accuracy in fabricating small, 18 μm high impedance segments while simultaneously reducing the size of low-impedance segments to 162 μm. Compared to the original "roller coaster" design [6], which was approximately 37.5 mm^2 of total area, the improved aerosol jet-printed version achieves a smaller total area of only $6.55mm^2$.

Table 6 demonstrates the total electrical size of the multilayer stripline filter, comparing it to previous literature. Compared to other works, the overall size is highly competitive at mm^2. We also note that [8] uses MEMS technology to help miniaturize the size. Despite having a lower dielectric constant, which can make miniaturization more challenging due to the need to compensate with increased area, our filter offers a small filter area of $6.55mm^2$ while maintaining desirable filter properties such as a high roll-off. Although the cutoff frequency and unit cells may not be exactly the same in some cases, our filter provides a large reduction in size while preserving desirable filter characteristics. [6]

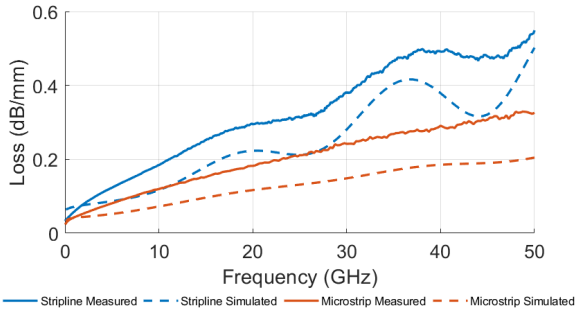

Fig. 9. Planar microstrip and stripline insertion loss per length. Simulations are shown with dotted lines while measured results are shown with solid lines. Where the total length of both through lines is 4.5mm.

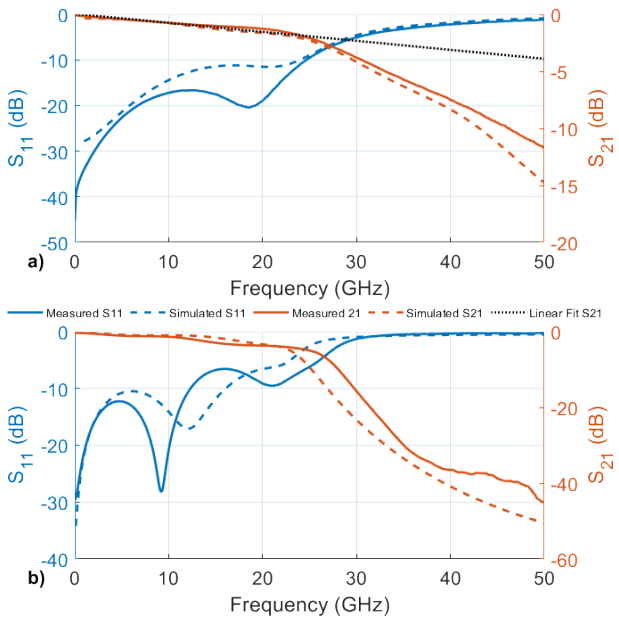

Fig. 10. Simulated Vs. Measured Results of a.) Planar microstrip filter b.) multilayer microstrip filter. Measurements were taken using SOLT-calibrated GBB 50A-GSG-250 probes with an PNA-X

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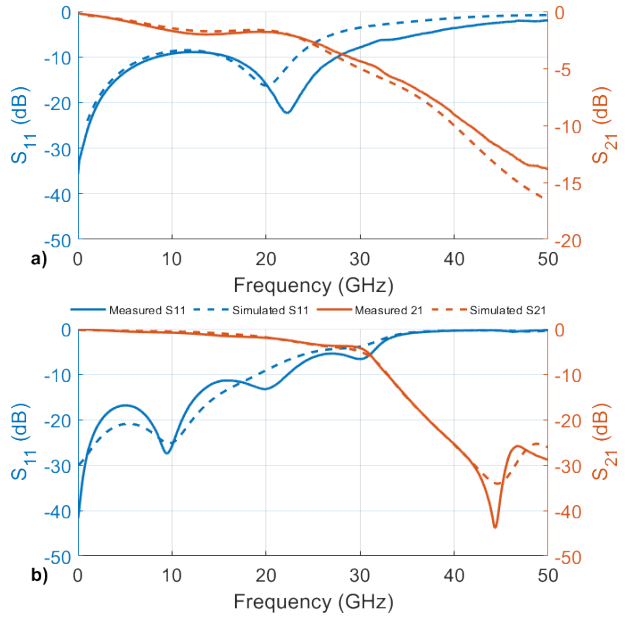

Fig. 11. Simulated Vs. Measured Results of a.) Planar Stripline Filter b.) Multilayer Stripline Filter.

Table 5. Line Loss of Microstrip & Stripline

	[21]	[21]	[5]	MS Thru	SL Thru
Printer Type	AJP	AJP	AJP	AJP	AJP
Loss 20 GHz (dB/mm)	0.09	0.10	0.13	0.18	0.28
Loss 30 GHz (dB/mm)	0.11	0.12	0.19	0.27	0.38
Loss 40 GHz (dB/mm)	0.15	0.21	0.20	0.29	0.47

Table 6. Comparison of Filter Total Area

Work	Cutoff (GHz)	Unit Cells	Area (mm^2)	ϵr	Material
Multilayer	31.4	7	6.55	3.5	Polyimide
[5]	40	7	7.34	6.7	Diamond
[6]	6-14*	5	37.5	3.65	GPCL02
[8]	26.6-34.4**	6	5.76	7.5	PECVD

The demonstrated solution combines the advantages of 3D printing on the molybdenum copper (non-planar) and the high resolution of AJP metal and dielectric printing. Building off of the roller coaster filter and the resolution advantages of the fully 3D printed filter on diamond, results in a smaller footprint. Table 2 shows the widths of the through line and low impedance segments for the filters. Table 4 shows the calculated areas of the transmission line width and all high and low impedance segments. By converting the microstrip through line into a stripline, we achieved a 52% reduction in conductor area. This approach also applies to the planar filter, demonstrating a 36% reduction in stepped impedance areas. The multilayer filter initially had the smallest stepped impedance areas, which were further reduced by 39%. With the reduction in conductor area, our initial objective is proven, and filter parallelization becomes a possibility through the use of this method for future applications.

The demonstrated method of capacitor shrinkage has significant advantages over previous methods. Compared to [5] the width of the capacitor has dramatically decreased as a direct result of the raised segments. Another main difference between this and the demonstrated method is that the ground plane is printed and not reliant on the carrier substrate. The carrier substrate is electrically isolated from the filter design and instead, the patterned printed ground plane determines the design. In the case of [5] diamonds are used for the substrate and electrically is part of the filter design.

[7] Our proposed method also compares favorably to [6]. Since the substrate was fabricated using stereolithography (SLA) printer for [6] the thinnest height that was used was 2.73mm. The AJP process gives a significant advantage by depositing thin films allowing for the minimum height for our proposed design to be 20μm. It is noted that this width can be shrunk even further but it is limited by the resolution of the smallest feature size, in this case, the width of the inductor. The process of our solution is fully AJP opposed to a combination of inkjet and SLA printed.

V. Conclusion

By utilizing the optimization available with AJP, we have successfully fabricated a fully 3D-printed, miniaturized stepped impedance filter. To the author's knowledge, this is the first of a fully 3D-printed filter structure that utilizes multiple layers to minimize the total conductor area of the passive components. We successfully fabricated a multilayer microstrip filter with a cutoff frequency of 26.8 GHz and a multilayer stripline filter with a cutoff frequency of 31.4 GHz.

The area of the capacitor on the microstrip planar design was originally 0.028 mm^2 and was shrunk down to 0.016 mm^2 for the final multilayer stripline design, which is a 39 % reduction in area. The implementation of the stripline design yielded significant miniaturization benefits when it came to reducing the width of capacitive elements. Comparing both planar printed filter designs, the width of the capacitors was shrunk in area. The multilayer advantage allowed for extra capacitance to be added in the lower filter segments. In combination with this multilayer component, three additional techniques were introduced to further miniaturize the filter which include adding a customizable printed ground plane, adding serpentine lines to the filter design, and adding an additional layer of silver on top. To the best of the author's knowledge, this is the smallest stepped impedance stripline filter that has been fabricated using a multilayer process with aerosol jet printing technology. A relevant application is to miniaturize bulky filter designs for more compact integration.

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