

High Energy Density Capacitors for Power Electronic Applications Using Nano-Structure Multilayer Technology

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WHITEPAPER

BAA Title: Power Electronics Building Block (PEBB)

HIGH ENERGY DENSITY CAPACITORS FOR POWER ELECTRONIC APPLICATIONS USING NANO-STRUCTURE MULTILAYER TECHNOLOGY

Submitted by

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OBJECTIVE

Power electronics applications are currently limited by capacitor size and performance. Only incremental improvements are anticipated in existing capacitor technologies, while significant performance advances are required in energy density and overall performance to meet the technical needs of the applications which are important for U.S. economic competitiveness. One application, the Power Electronic Building Block (PEBB), promises a second electronics revolution in power electronic design. High energy density capacitors with excellent electrical thermal and mechanical performance represent an enabling technology in the PEBB concept.

We propose a continuing program to research and develop LLNL's *nano-structure multilayer* technologies for making high voltage, high energy density capacitors. Our controlled deposition techniques are capable of synthesizing extraordinarily smooth sub-micron thick layers of dielectric and conductor materials. We have demonstrated that, with this technology, high voltage capacitors with an order of magnitude improvement in energy density are achievable. U.S. patent No. 5,414,588 was issued in May, 1995, covering the structure of these capacitors. Well-understood dielectrics and new dielectric materials will be investigated for use with this technology.

There are many advantages to capacitors produced by nano-structure multilayer technology. They are inherently solid state, exhibiting superior mechanical and thermal properties when compared to conventional electrolytic, oil-filled, or polymer construction. Their compact, flat profiles are well-suited to surface mounting and to integration into the packages of power semiconductor devices, offering performance, volume, and cost advantages over discrete capacitors. An additional advantage of this capacitor technology is its applicability to perform as a mechanical structure. The proposed capacitors could be formed in sheets that would serve double duty. For instance, in a power supply, they could serve as both an energy storage device and as an electrical power bus while conforming to the shape of the power supply's case. This would further reduce the bulk of the packaged system. A conceptual capacitor design for power electronics applications is discussed to illustrate capacitor design techniques, materials, and the performance that is expected with this technology.

The concept of capacitors integrated onto substrates and/or packaged with semiconductors can be taken a step farther. Our colleagues at the University of California have devised techniques whereby inductors of substantial size can be deposited on silicon, thus producing a completely integrated high-frequency (10 MHz) switching power supply with power densities exceeding 100 W/in³. Our capacitors are an important part of this concept.

Our long-term plans, with sufficient funding and the help of industrial partners, include NMC dielectric materials research; engineering design and evaluation for power electronics applications; building a prototype manufacturing capability for NMC production; designing a full-scale manufacturing system; and moving this technology to industry for commercial production.

TECHNICAL PROBLEM

Rugged, high-performance, high-voltage capacitors are needed in many industrial and military applications. In power electronics, they are needed in several major areas:

- *Snubber capacitors* in power semiconductor devices, such as IGBTs and MCTs. High-amplitude, high-frequency transient currents—as high as 40 A/ns—must be absorbed. This demands capacitors with the lowest possible effective series resistance (ESR) and effective series inductance (ESL).

- *Filter capacitors* on the DC power bus of inverters, converters, and many *custom power* regulation systems. High capacitance and high energy density is desired to maximize noise and ripple rejection and to promote longer holdup time. Again, low ESR and ESL are important.

These applications require high-voltage, high energy-density capacitors with good circuit performance. LLNL's NMCs have strategic advantages when compared to existing technologies. New power electronics applications demand better capacitor performance than presently available. Low ESR and ESL with high temperature capability are available (but not always in combination) only from the very finest film and ceramic devices. Requirements for capacitors used in power electronics are listed in Table 1, and are barely obtainable at any price. Issues to be addressed in achieving these difficult objectives include:

- Increased dielectric breakdown voltage, V_b
- High dielectric constant, k , that is stable with temperature and voltage
- Managing electromagnetic field gradients and edge effects
- Current density and the action integral for the conductors
- Loss mechanisms: dipole relaxation and resonance, ionization, structural inhomogeneity, and conductor loss
- Equivalent series resistance and inductance (ESR / ESL)
- Mechanical, thermal, and chemical integrity under stress
- Interconnection and integration
- Self healing

Table 1. Some requirements for electrical power applications that are not achievable with existing capacitor technology.

Temperature range	-40 to +150 °C
Energy density:	$\geq 10 \text{ J/cm}^3$
Device voltage:	500 to 1200 V
ESR	$< 1 \text{ m}\Omega$
ESL	$< 2 \text{ nH}$
Ripple current (at 50 KHz):	200 A

Current capacitor technologies suffer from defects and inhomogeneity introduced in the dielectric material and in capacitor manufacturing which contributes to voltage breakdown. Important voltage breakdown mechanisms include electronic or avalanche breakdown, electrochemical breakdown and thermal breakdown as dielectric loss increases under intense electric field stress and with aging.

Rolled paper-conductor or polymer film capacitors are characterized by high breakdown voltage but lower dielectric constant. They suffer from material and manufacturing defects such as pinholes and particle contamination, and can fail under mechanical and thermal shock. They experience chemical degradation with aging, temperature, and high ripple currents. They are bulky and are not expected to achieve the performance required for the envisioned power electronics applications.

Capacitors with ferroelectric ceramic dielectrics such as BaTiO₃ have a much higher dielectric constant than polymer or paper capacitors. However, large geometry ceramic capacitors still have lower breakdown voltage and often high dielectric loss. Performance of today's ceramic capacitors is limited by ceramic powder quality, capacitor design and the manufacturing process. Furthermore, there are thermal and mechanical problems with the larger ceramic devices, making them difficult to solder, unreliable at high temperatures, and causing unreliable shelf life statistics.

Electrolytic Double Layer Capacitors (EDLCs) are characterized by very high capacitance and specific energy (J/kg). However, they are limited to 1-3 V per cell, have relatively high ESR and ESL, and require elaborate packaging to contain the liquid electrolyte. Double layer capacitor technology such as the *Carbon Aerogel* capacitors (*Aerocapacitors*) developed at LLNL are well-suited to bulk energy storage capacitor role, augmenting batteries and other energy sources.

NANOSTRUCTURE MATERIALS BACKGROUND

Nano-engineered multilayer materials are characterized by a near-atomic scale and thus, uniquely large interfacial area to volume ratios. Successful capacitor structures fabricated using multilayer technology will give us the ability to engineer high performance capacitors. We can optimize properties by materials selection, design of the synthesis process, and materials processing. Multilayer materials are widely known in the materials community for scientific study and physics application. Their use has been demonstrated at many laboratories, including LLNL. The multilayer effort at LLNL is among the strongest in the world as it is a core technology supporting many programmatic and scientific activities.

Nano-structure or nano-phase multilayer materials are dense, low contamination solids synthesized using atom by atom processes. They are characterized by a high concentration of material interfaces. The most notable of such materials are semiconductor superlattices fabricated using molecular beam epitaxy (MBE). However, multilayers may be synthesized using elements from all parts of the Periodic Table using MBE, evaporation, sputtering and electrochemical deposition technologies. At this time, multilayer structures have been fabricated by physical vapor deposition from at least 75 of the 92 naturally occurring elements in elemental form, as alloys or as compounds. The structure of multilayer materials is determined in synthesis by control of the thicknesses of the individual layers during deposition. These thicknesses vary from one monolayer (0.2 nm) to thousands of monolayers (>1000 nm).

Until recently, the macroscopic thickness of nano-structure multilayer materials has been generally limited to less than a few microns, and more typically to 0.5 μm or less. Recently, processes for deposition of thick macroscopic nano-structure multilayer materials have been developed at LLNL and used to fabricate free standing high quality structures up to 300 μm thick containing up to 50,000 individual layers. Our existing research synthesis system produces samples having periods uniform to 2% of the individual layer thickness and areas of $\sim 400 \text{ cm}^2$. These macroscopic nano-structure multilayer samples enable use of standard diagnostic techniques for material property characterization and open a path to develop devices with performance that approaches theoretical limits.

The through film and lateral perfection of these macroscopic multilayer materials have been determined using surface roughness measurements, cross-section transmission electron microscopy (TEM) and standard x-ray diffraction analysis. The surfaces of macroscopic multilayers ($t > 20 \mu\text{m}$) have demonstrated surface perfection essentially equal to the substrate roughness: multilayers deposited on super polished substrates with roughness of $\sim 0.02 \text{ nm RMS}$ and $0.14 \text{ nm peak to valley (PV)}$ had roughness of $\sim 0.04 \text{ nm}$ and 0.29 nm PV . Cross-section TEM shows that the multilayer structure $\sim 17 \mu\text{m}$ from a substrate is identical to that $1 \mu\text{m}$ from that same surface and that this uniformity extends laterally over several microns. X-ray analysis demonstrates that the multilayer period of a 5 nm period 25 μm thick free standing structure varied by less than 1% top to bottom through 10,000 individual layers and is constant over 10 cm on single substrates. The perfection shown by these characterization results is unique in that it is atomic in scale but extends over macroscopic thicknesses. These materials exhibit exceptional application specific performance as a result of their nano-structures and atomic

distributions. Structural flaws that characteristically limit performance are controlled so that the full potential of the nano-structure multilayer materials is achievable.

There are several potential advantages inherent to fabrication of high energy density capacitors by multilayer synthesis technologies. First, the processes used are generic in that a wide range of materials may be deposited as thin films. Therefore, it will be possible to apply new materials as they are developed, potentially enhancing the dielectric properties of the insulating spacer (i.e. *technology insertion*). The designs presented here are based on simple metaloxide dielectrics, such as amorphous ZrO_2 , and Al_2O_3 with dielectric constants of $k=21$ and 9 , respectively, and a maximum standoff field of $V_b = 4$ to 6 MV/cm. Enhanced performance can be expected if $CaTiO_3$ ($k \approx 165$), for example, is applied. Standoff fields of these materials in thin film form are not currently well known but are expected to be substantially larger than those observed for commercial bulk materials formed using powder compaction/sintering processing (~ 0.1 MV/cm). This optimistic opinion is based on our ability to fabricate fully dense layers having controlled surface roughness less than 5 Å on a routine basis. This is demonstrated in Figure 1 where a cross section transmission electron micrograph of an $Al-Al_2O_3$ multilayer having a periodicity of 920 Å is shown at a magnification of $100,000x$.



Figure 1. Transmission Electron Microscope (TEM) image of an $Al-Al_2O_3$ multilayer. In this case, the crystalline aluminum conductor layers and amorphous alumina dielectric layers are both 460\AA ($0.046\text{ }\mu\text{m}$) thick. Surface roughness at the interfaces is 12\AA RMS.

Note the uniformity of the layers and the interfacial quality; the interfaces in this structure are smooth to approximately two to four atomic diameters (5 - 10 Å). Second, these structures are thermally and mechanically robust. Strengths approaching the theoretical limits of the component materials in metal/metal multilayers have been experimentally demonstrated for several alloy systems. Also, these materials are observed to be stable in multilayer form to temperatures in excess of 500°C in most cases. Thus, nano-engineered multilayer structures have several strategic advantages in developing high performance capacitors.

There are also manufacturing advantages. It is possible to design and fabricate a capacitor structure to *near net form*. This manufacturability and the atom-by-atom nature of the deposition processes can facilitate engineering design. The conductor structures can be formed in a variety of configurations allowing applications-specific geometries and sizing to minimize anticipated capacitor performance limitations. For instance, the thin, flat sheets of multilayer material that form capacitors will also have significant mechanical strength and robustness, possibly enabling their use as a structural component.

CONCEPTUAL ENGINEERING DESIGN

We introduce a conceptual design addressing a power electronics application. An NMC snubber capacitor is designed for use with high-frequency switching semiconductors. Compatibility with surface mounting or other low-inductance interconnections is mandatory. Integration of the device into a semiconductor device case would offer a significant improvement in performance and a cost saving. The goal is to design a 5 μF , 1000 V device. ESR and ESL must be exceptionally low, 1 $\text{m}\Omega$ and 2 nH respectively.

NMC Snubber Capacitor Design

A snubber capacitor form factor amenable to multilayer fabrication is 1.54 mm thick and 2 cm by 2 cm (Fig. 2). Terminals at each end of the device are solid copper, suitable for brazing and direct surface mounting onto power switching transistor packs, which guarantees low contact resistance and inductance and high durability. Finished devices (all deposited in net form) as small as 1 mm square are feasible for applications in electronic systems. Thin capacitors with a smaller outline can be readily stacked to accommodate arbitrary space limitations.

A cross section of a capacitor element is shown in Fig. 3. We chose a proprietary mixture of metal oxides ($\text{Al}_2\text{O}_3/\text{ZrO}_2$) as the dielectric for this conceptual design because we have recent experience with this combination; our research would surely point towards other non-ferroelectric materials with higher dielectric constants. Working characteristics of the dielectric used in this design are listed in Table 2.

Table 2. Working characteristics for $\text{Al}_2\text{O}_3/\text{ZrO}_2$.

Breakdown voltage, V_b :	$4 \times 10^6 \text{ V/m}$ (10 kV/mil)
Dissipation factor ($\tan \delta$):	3×10^{-4}
Relative permittivity (k):	15

The breakdown voltage, in particular, is a conservative value. Because of the very thin layers, breakdown performance modes are expected to improve. One such effect, avalanche breakdown, is reduced because of rapid electron recapture. Extensive testing will be required to determine a realistic safety factor on breakdown voltage rating; a factor of 1.33 is applied here. The dissipation factor is lower than that of film and ceramic dielectrics found in the most commonly-used high energy capacitors. Losses are guaranteed to be low because

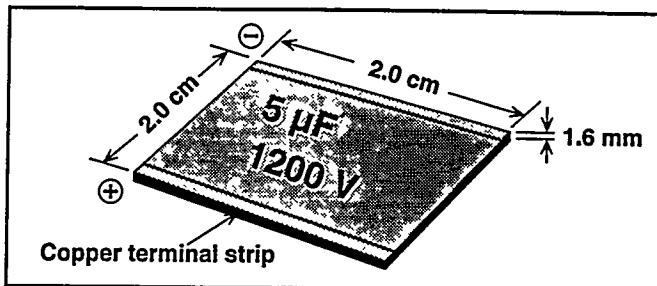


Figure 2. Form factor for a conceptual design of an NMC snubber capacitor. This form factor can be reshaped almost arbitrarily.

of the very high purity of the deposited material. These metaloxide materials are also free from dipole losses and the high effective inductance of high- k ferroelectric ceramics like BaTiO₃. In applications where high capacitance (as opposed to high voltage) is the most important factor, high- k materials could certainly be used.

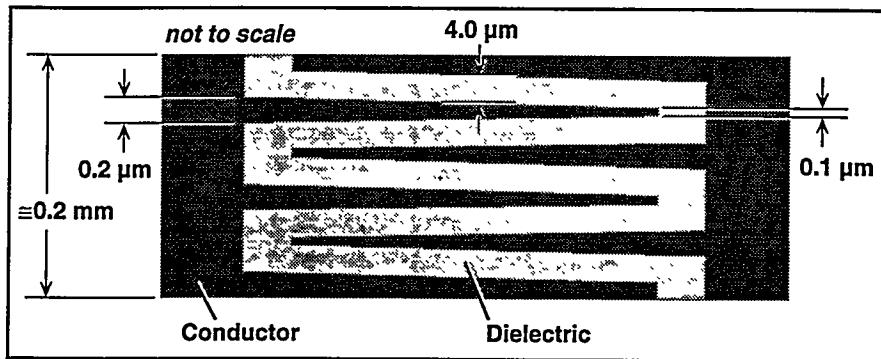


Figure 3. Cross section of a typical multilayer capacitor element for a 1200 V application. Several of these elements would be stacked in parallel to produce the desired capacitance.

From Figure 3, you will note another engineering advantage of the multilayer technique: tapered conductors are feasible. Since the current density in any plate is proportional to the distance from the tip, the required cross section of conductor can also vary proportionally. This reduces the amount of metal in the assembly, saving weight and bulk. The minimum practical thickness for metal deposition is about 0.1 μm and the maximum is about 1.0 μm. Metals such as aluminum and copper are likely candidates for this design.

In ordinary foil capacitors, breakdown at the edges of the foils is a nagging problem. In our NMC design, the edges, or plate tips, are completely buried in the multilayer dielectric. Electromagnetic modeling indicates that full burial reduces field enhancement by 15%. We hope to demonstrate how multilayer dielectric material can be engineered to defocus the electric field gradient and reduce edge effects, improving capacitor voltage breakdown characteristics.

Capacitance for one layer of this parallel-plate capacitor is calculated from

$$C = k\epsilon_0 \frac{a}{d} \quad (1)$$

where C is the capacitance in Farads, k is the relative permittivity for the dielectric, ϵ_0 is the permittivity of free space (8.854×10^{-12} F/m), a is the plate area and d is the dielectric thickness. For a 1600 V breakdown rating, 4.0 μm of dielectric is required. The conductors would be about 0.1 μm thick, accounting for 8% of the volume and 20% of the mass of this capacitor. Minimizing the quantity of copper maximizes the volume of dielectric, improving energy density. This 5 μF capacitor will occupy about 0.62 cm³. Fig. 2 indicates a possible set of dimensions: 2 by 2 by 0.15 cm, about the size of a postage stamp. Of course, the finished device can easily be assembled from a stack of thinner elements to achieve almost any form factor. Thin capacitors have several advantages: lower inductance, easier surface mounting, and better heat dissipation (larger surface area to volume ratio).

Energy stored in a capacitor is calculated from

$$W = \frac{1}{2} CV^2 = \frac{1}{2} k\epsilon_0 V^2 \frac{a}{d} \quad (2)$$

where W is the energy in Joules, and V is the voltage. This capacitor ($5 \mu\text{F}$, 1200 V) can store 6.4 J if it is charged to its breakdown voltage of 1600 V . When designing a capacitor, it is apparent that dielectrics with high- k and high breakdown voltage increase energy density, but there may be other tradeoffs: dielectric absorption (loss), capacitance voltage coefficient, temperature coefficient, thermal conductivity, mechanical properties, etc., all affect the choice of the dielectric material.

Effective series resistance for this device is determined primarily by the bulk resistance of the copper. ESR can be computed from the standard resistance formula

$$R = \rho \frac{l}{a} \quad (3)$$

where R is the resistance, ρ is the resistivity of copper ($1.7 \times 10^{-6} \Omega \text{ cm}$), l is the length and a is the area. There are 377 layers of copper, each $0.1 \mu\text{m}$ thick. Current flows through a path 2 cm long and 2 cm wide. The dc ESR is then $0.5 \text{ m}\Omega$, an excellent figure. Note that conductor thickness can be varied as desired to control ESR and other properties.

The inductance of a thin parallel plate capacitor is extremely small because the magnetic fields in adjacent plates cancel one another. We expect the ESL of these devices to be a fraction of a nanohenry, similar to that of a sheet conductor with similar dimensions. Inductance will be challenging to measure and will be dominated by interconnection effects in real applications. A summary of specifications for this design appears in Table 3. Using our current estimates for large-scale production, this capacitor should cost about one dollar to produce.

Table 3. Snubber capacitor specifications.

Capacitance:	$5 \mu\text{F}$
Maximum voltage:	1600 V
Working voltage:	1200 V
Maximum energy storage:	6.4 J
Dimensions	$2 \times 2 \times 0.15 \text{ cm}$
Volume	0.6 cm^3
Weight:	3.0 g
Energy density:	10 J/cm^3
Specific energy:	2.3 J/g
Effective Series Resistance:	$0.5 \text{ m}\Omega$
Effective Series Inductance	$< 1 \text{ nH}$

Summary

This conceptual design uses novel materials to engineer an extraordinary capacitor. Alternative material choices for dielectrics and conductors will certainly improve these specifications. High energy and power density, low loss, good thermal and mechanical properties, and low inductance make the nano-structure multilayer capacitor an excellent candidate for power electronics applications.

TECHNICAL STATUS AND ISSUES

Our nanostructure multilayer technology is well established. Facilities and equipment capable of proof-of-principle and small scale capacitor fabrication and testing are available. We have begun to retrofit and add to the existing systems to carry out this proposed program. Our scientific and engineering staff is currently in place and available. We are prepared to draw on the collective materials, electronics, and related expertise at LLNL needed to succeed in this program. As of this writing, we have made significant progress in the fabrication of NMC capacitors.

Small-scale test films with dielectrics composed of various compositions of metal oxides have been deposited and characterized. A typical specimen is illustrated in Figure 4. An array of small capacitors are deposited to permit statistical sampling and destructive evaluation of individual capacitors. Figure 5 shows a scanning electron microscope cross section of a test film and its analogy to a parallel-plate capacitor.

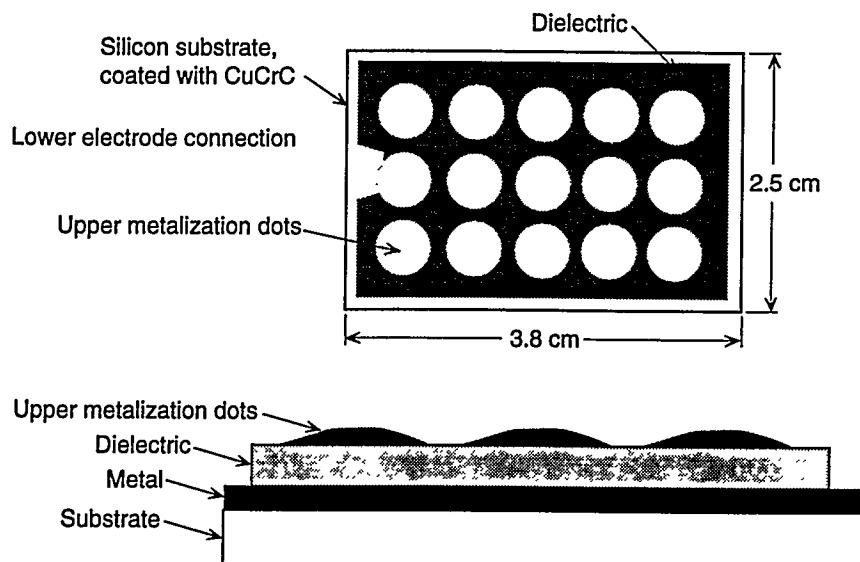


Figure 4. Top view and cross section illustration of an NMC test films

High energy density has been demonstrated as summarized in Table 3. The metaloxide dielectric studied here could be supplanted by a higher- k material, such as calcium titanate, to increase energy density by as much as a factor of 10 without significantly impacting other specifications. Use of ferroelectric materials, such as barium titanate, may increase energy density by a factor of 100 with some loss of efficiency. Such materials are currently under study. These results are very encouraging and indicate that NMCs represent a new state of the art in capacitor technology.

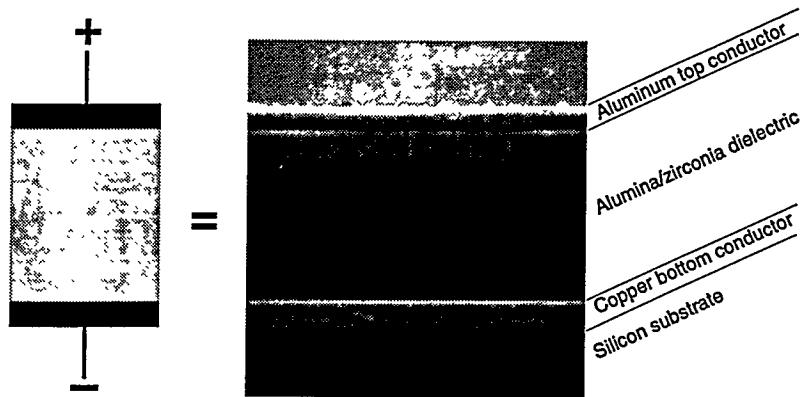


Figure 5. Scanning electron microscope cross section of an NMC test film.

Table 3. Test Film Specification Summary

Dielectric	Zirconia/alumina
Conductors	CuCrC multilayer base, Al dots
Dielectric thickness	3.0 μm
Dielectric constant, k	15.5
Dielectric density	4.75 g/cm ³
Dielectric volume	5.34X10 ⁻⁵ cm ³
Dielectric resistivity	10 ¹⁵ ohm-cm
Capacitance	813 pF
Breakdown voltage	1200 V
Breakdown field	4.0 MV/cm
ESR	0.4 Ω (instrumentation limited)
Energy density	11 J/cm ³ (3.1 Whr/l)
Specific energy	2.3 J/g (0.64 Whr/kg)

The NMC manufacturing process is environmentally benign. Solid metal or ceramic materials are deposited in a vacuum chamber. Waste materials are predominantly metals in solid or oxide forms. The resulting capacitors are solid-state with no seals to fail or corrosive fluids to leak. They are expected to have excellent mechanical and thermal properties: resistance to vibration, stress, and elevated temperatures.

Masking is one of the challenges in the fabrication process. One or more masks must be precisely located in intimate contact with the substrate for each deposition step. The mask(s) must be easy to replace and fairly low cost, even for a research system. Also, the masking apparatus must operate within the vacuum chamber, which limits the choice of materials and fabrication methods. We have designed an automated apparatus that meets the needs of multilayer capacitors masking. Stepper and servo motors move the actuators under computer control. A computer-based measurement and control system is operational, enabling us to program the deposition sequences and automatically record important parameters for later analysis.

The high dielectric deposition rates required for economical manufacturing are projected to be greater than 30 \AA/s (0.18 $\mu\text{m/min}$). This is achieved in our work using a unique reactive sputtering process developed at LLNL.

This process has recently been improved so that rates of 25 to 30 Å/s are attainable with ZrO_2 . The acceptable range of process parameters is also broad, indicating that process scaling is possible.

Some important technology issues remain to be investigated. Time-dependent dielectric breakdown of nano-structure multilayer capacitors needs to be well understood for a variety of materials and capacitor designs. Interfacial reactions (e.g., diffusion) between dielectrics and conductors are important to understanding voltage breakdown phenomena. Complex dielectric/conductor structures and multiple dielectric-dielectric interfaces that are expected to provide very high voltage holdoff will be studied. Complex-composition dielectrics may offer advantages. Voltage breakdown resulting from electromagnetic field gradients at the edges of conductors requires continuing study.

Program issues include development and fabrication of additional multilayer capacitors designed for high voltage holdoff. Substrates and substrate removal to fabricate free standing capacitors have to be developed. Full capacitor performance characterizations need to be done. We need a better understanding of engineering design of near-net-form capacitors with consideration for electromagnetic gradients and edge effects, mechanical properties and interconnection for integration into capacitor banks. Scale up of this nano-structure capacitor technology will require investment in facilities and equipment, and will present new fabrication and processing problems.

PLANNED WORK

Our initial efforts, under the presently-funded DOE Energy Efficiency and Renewable Energy program, were dedicated to proof-of-principle dielectric film depositions (single-layer capacitors). That project was limited to metaloxide dielectrics.

In the current phase, we will fabricate and characterize small-scale multilayer capacitors using metal oxide dielectrics. This will validate the mechanical aspects of our multilayer capacitor designs and allow us to develop design rules for NMC capacitors. We will also fabricate and characterize single-layer test films with high- k dielectrics such as CaTiO_3 . These test films will prove the viability of NMC capacitors in bulk energy storage applications where energy density is the most important specification.

Future efforts, in cooperation with our industrial partners, will include the design and construction of a scaled-up capacitor fabrication facility, design and testing of commercially-practical capacitors, and the design of high-volume manufacturing equipment for industry. LLNL is pursuing several industrial contacts who have expressed interest in manufacturing NMCs.

The PEBB design team at Harris Semiconductor Corporation believes that a commercially-viable NMC technology will have a major impact on PEBB objectives, and on the future of power electronics in general. Expected NMC characteristics—high energy density, high performance and reliability, and competitive cost—make NMCs an enabling technology. Harris will test laboratory prototype NMCs under realistic conditions to evaluate transient discharge performance and reliability. They will also supply design requirements and evaluate design tradeoffs to integrate NMCs into the PEBB package.

We propose a multi-year program to develop NMC technology for power electronics applications. Our industrial partners will:

- provide device requirements and specifications and evaluate designs;
- perform comprehensive testing;

- > materially participate in the design and construction of a pilot-scale fabrication system;
- > move NMC technology to commercial production.

Phase 1: Demonstration capacitors

1. High-k test films: A deposition process will be developed and optimized for high-*k* dielectrics including various ferroelectric materials. Test films will be deposited in the form of arrays of single-layer capacitors for parametric testing and process characterization. The films will be characterized for capacitance, ESR, efficiency, energy density, and specific energy at applied voltage, frequency, and temperature. Deliverables: Sample films and test report.

2. Materials Studies & Modeling: Throughout this project, we will be improving our physical models and understanding of nano-structure multilayer dielectrics, accumulating a database of dielectric characteristics, and performing electrical system analyses. These models will effect capacitor design and improve performance. Deliverables: Report.

3. Demonstrate small-scale NMCs: Using optimal dielectric materials and our existing deposition systems, we will fabricate capacitor assemblies of about 20 cm³ with a capacitance of several microfarads. These devices will be subjected to electrical and environmental testing as prescribed by our industrial partners. Deliverables: Small-scale NMCs.

Phase 2: Process scale-up

1. Large substrate development: Substrate materials and substrate handling techniques will be investigated with the goal of selecting methods for fabrication of full-scale NMCs. Techniques to remove devices from the substrate will also be evaluated. A large deposition system will be used to evaluate designs by depositing dielectrics on various substrates.

2. Fabricate NMCs on large substrates: Existing deposition systems will be modified to deposit material over large areas of approximately 10 x 25 cm. This will help to determine scale-up limitations. Deliverables: Quantities of capacitors on large substrates.

3. Masking development: In conjunction with the development of large substrates, appropriate masking techniques will be investigated. Prototype designs will be exercised along with the substrate handling equipment. Deliverables: Design report.

Phase 3: Prototypical manufacturing system

In this phase, our industrial partner in manufacturing will work with LLNL to design, build, and operate a plant-scale fabrication system.

1. Design: Using the materials, substrate, and masking designs evolved in Phase 2, a full-scale system for use in a pilot plant will be designed. Extensive interaction with our partner in the capacitor industry will be required. Deliverables: Design documents.

2. Construction: The full-scale pilot plant system will be constructed at LLNL. It is expected that this machine would be paid for and owned by the capacitor manufacturer and would eventually be shipped to their plant for installation after initial use at LLNL. Deliverables: Completed system.

3. Fabricate full-scale NMCs : The pilot plant system will be operated and improved as necessary to produce full-scale NMC devices which can then be assembled into stacks for applications. At the end of this phase, a revised design would be proposed for replication by the capacitor manufacturer. Deliverables: Full-scale NMCs; revised design; delivery of pilot plant system to capacitor manufacturer.

Budget, schedule, and cost sharing

Figure 6 summarizes the development plan and shows the estimated costs for each phase. It is assumed that costs will be shared approximately equally between government and industry over the course of the program. Ownership of the pilot system is contingent on the industrial partner paying for all procurements. For that reason, financial responsibility for phase 3 of the program falls primarily on industry.

Task		Milestone cost (k\$)	
		Gov't.	Industry
Demonstration Capacitor	<u>12 months</u>		
High-k dielectric research		\$800	\$100
Breakdown/reliability research			
Demonstrate microfarad caps			
Process Scale-up	<u>18 months</u>		
Fabricate large-area NMCs		\$700	\$200
Large substrate development			
Masking development			
Pilot Facility	<u>36 months</u>		
Design		\$1000	\$2200
Construction			
Fabricate full-scale NMCs			
		Total milestone costs	\$2500
			\$2500

Figure 6. NMC development budget and schedule.

To date, our progress has been budget-limited. Funding has come from LLNL internal sources and from DOE Energy Efficiency's Ultracapacitor Program (EE-51, Pat Davis). This DOE funding is expected to continue at a moderate level (\$250k) through FY96. Additional LLNL internal funds may also be available, primarily through Defense Programs, though the exact amount is unknown at this time. We also leverage the efforts of other LLNL multilayer materials projects including cooperative agreements (CRADAs) with industry. This is especially appealing because much of the apparatus, materials, and manpower is shared which eliminates overhead and increases synergy.

RELATED ON-GOING WORK

LLNL is an applied physics laboratory with a well-established materials and engineering technology base. We expect to draw on the collective capabilities and expertise at LLNL to better understand power electronics applications and be in the best position to meet our industrial partners' capacitor performance goals. Core materials technologies include the nano-structure multilayers, interatomic materials diagnostics, and carbon and silica Aerogels. Multilayers are currently being developed as physics diagnostic and optical devices. Research is proceeding to take advantage of their remarkable mechanical and thermal properties for DOE programs and applications in aerospace and related industries. Transmission electron microscopes, x-ray diffraction, and similar diagnostic capabilities at LLNL are needed tools to understand and develop nano-structure multilayer

materials. Carbon Aerogels are extremely low density, high surface area foams developed for DOE programs. We are currently developing low voltage, very high capacitance electrochemical double layer capacitors and lithium ion batteries with carbon Aerogels for automotive applications.

LLNL also has well-developed engineering thrust areas in pulse power, microwave, laser and semiconductor technologies, and electromagnetic and device modeling. Very large capacitor banks have been developed for electric gun, rail gun and x-ray applications. LLNL originated the concept of small pulse power slapper detonators for weapon initiation. Microwave broad band sources and vulnerability assessment at LLNL rely on high performance capacitor technology. Pulsed, high power lasers developed at LLNL for DOE and DoD programs similarly rely on high performance capacitors banks. Research has been done on laser and electron beam initiated fast semiconductor switches for pulse power applications. Our electromagnetic and device modeling expertise is a resource used by DOE and DoD programs.

EXPECTED PAYOFFS

We are proposing research and development of an important enabling technology. The nano-structure multilayer capacitor technology can open up many new opportunities for industry and the military. An order of magnitude or more improvement in energy density with very high efficiency will be significant. We expect immediate use of this capacitor technology in power electronics, as demonstrated by the intense interest from our industrial partners.

The proposed technology may enable capacitor designs that approach theoretical limits of the dielectric and conductor materials used. New capacitor design techniques are made possible to control field gradients, edge effects and current densities in the capacitor, and enable rugged, high density capacitor packaging for commercial, military, and space applications. Spin-offs include other dielectric applications such as millimeter wave ICs, radar, and instrumentation. We plan to move this technology to our industrial partners for large-scale production as soon as possible.

The revitalization of the American electronics and industrial base is also important. The proposed capacitor technology can make a needed difference in a variety of industrial fields. Communication, transportation, and power distribution systems envisioned today can be enabled and made practical by high energy density capacitor technology. Electric automobiles with reasonable acceleration and effective energy recovery through dynamic braking may become a reality with this technology. Medical systems, such as defibrillator implants, and high density electronics packaging, are also possible.

CURRICULA VITAE

TROY W. BARBEE, JR.

Materials Scientist, Chemistry & Materials Science Department, LLNL

Birth Date: July 7, 1937 Citizenship: USA

PROFESSIONAL MEMBERSHIP

M.R.S., A.P.S., S.P.I.E., A.A.A.S.

EDUCATION

B.S. '60, M.S. '62, Ph.D. '65, Stanford University, Stanford CA

PROFESSIONAL EXPERIENCE

Materials Scientist, Stanford Research Institute, '65-'70; Laboratory Director, Center for Materials Research, Stanford Univ., '70-'77; Facility Head, Vapor Phase Synthesis, Stanford Univ., '71-'77; Technical Advisor, Center for Materials Research, '77-'82; Senior Research Associate, Center for Materials Research and Materials Science and Engineering Department, Stanford Univ., '77-'84; Metallurgist, LLNL, '84-present; Multilayer Synthesis and Properties Group Leader, '87- Present.

HONORS

Sigma Xi, IR 100 - X-Ray Beam Splitter (1986), R&D 100 - New Class of Diffraction Grating (1989).

GENERAL RESEARCH INTERESTS

Atomic engineering; nano-engineered multilayer structure, synthesis and properties; multilayer x-ray optic elements; multilayer x-ray optics instrumentation; micro-metrology; micro-analytical techniques.

PUBLICATIONS (The following are a selection of those related to this proposal)

1. T. W. Barbee, Jr., "Multilayer Structures: Atomic Engineering in Its Infancy," in *Physics, Fabrication and Application of Multilayer Structures*, ed. by P. Dhez and C. Weisbach, Plenum Press, New York, NY (1988) p. 17.
2. Troy W. Barbee, Jr., "Nano-structure Multilayer Materials," in "State of the Laboratory, Lawrence Livermore National Laboratory (1991)," UCRL-5200-91-718 (1991).
3. R. Frahm, T. W. Barbee, Jr., and W. K. Warburton, "In-situ Structural Study of Thin Film Growth by QEXAFS," *Phys. Rev. B* 44, 2822 (1991).
4. T. W. Barbee, Jr., and J. Wong, "EXAFS of Near Monolayer Hafnium Film," *Physica B* 158, 670 (1989).
5. T. W. Barbee, Jr., "X-ray Evanescent -Standing Wave Fluorescence Studies Using a Layered Synthetic Microstructure," *Mat'l. Lett.* 3, 17,(1984).
6. T. W. Barbee, Jr., "Combined Microstructure X-Ray Optics," *Rev. Sci. Instrum.* 60, 1588 (1989).
7. T. W. Barbee, Jr., "Multilayer Optics for the Soft X-ray and Extreme Ultra-Violet," *Physica Scripta T31*, 147 (1990).
8. Troy W. Barbee, Jr., "Multilayer Optics for the Soft X-ray and Extreme Ultraviolet," *MRS Bulletin* XV, 37 (1990).

GARY W. JOHNSON

Engineer, Electronics Engineering Department, LLNL

Birth Date: January 27, 1958

Citizenship: USA

PROFESSIONAL MEMBERSHIP

IEEE, ISA

EDUCATION

B.S. '81, University Illinois

PROFESSIONAL EXPERIENCE

Mr. Johnson currently serves as an instrumentation engineer supporting C&MS research and programs.

Mr. Johnson's past assignments include service in the Isotope Separation and Materials Processing Program as lead engineer, '87-'92, responsible for all aspects of instrumentation, data acquisition, process control, and power conditioning in a plasma physics research environment. He also served as project engineer for the Liquefied Gaseous Fuels Spill Safety Program, '81-'87, where he was responsible for design and deployment of hundreds of sensors and associated data acquisition equipment, as well as the control and data acquisition systems during design, construction, and startup of the National Spill Safety Test Center (Mercury, NV).

GENERAL RESEARCH INTERESTS

Mr. Johnson's recent activities include data acquisition and process control system design (hardware and software); design, interfacing, and applications of instrumentation and transducers of all kinds; analog circuit design; and electro-optical systems applications.

PUBLICATIONS

Johnson, Gary W., *LabVIEW Graphical Programming*, NY: McGraw-Hill (1994).

Published papers covering LLNL facility and system designs. Publication list available upon request.