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Final Scientific/Technical Report

20 kV Gallium Nitride pn Diode Electro-Magnetic Pulse Arrestor for Grid Reliability

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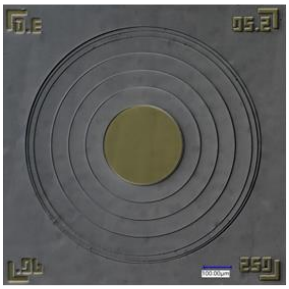

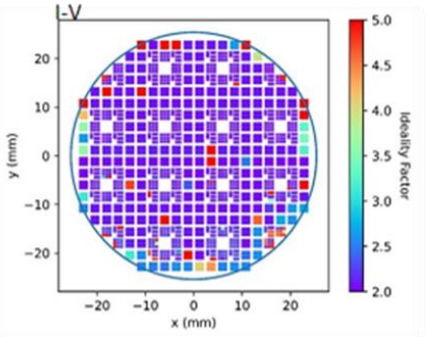

Award:	18/CJ000/10/01
Lead Recipient:	Sandia National Laboratories
Project Title:	20 kV Gallium Nitride pn Diode Electro-Magnetic Pulse Arrestor for Grid Reliability
Program Director:	Isik Kizilyalli
Principal Investigator:	Bob Kaplar
Contract Administrator:	Kelly Harper
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Public Executive Summary

This project developed vertical Gallium Nitride (GaN) pn diodes under two main thrusts: (1) A focus on relatively higher-voltage devices for use as fast EMP arrestors to protect the electric grid; and (2) A focus on a Foundry effort to establish the manufacturability of relatively lower-voltage devices. For the first thrust, the aim was to develop devices that go into avalanche breakdown to clamp the voltage across sensitive grid equipment subject to voltage transients induced by electromagnetic pulses (EMPs). Devices with breakdown voltages exceeding 6.5 kV were achieved, and breakdown times shorter than 1 ns were demonstrated, which is sufficiently fast to protect against the fast component of an EMP-induced signal. Key challenges included the epitaxial growth of thick (50 um or more), low-doped (low 10^{15} cm^{-3} range) GaN layers comprising the drift regions of the diodes, as well as the design and fabrication of edge termination structures (step-etched junction termination extensions) to prevent premature breakdown. Midway through the project, an additional emphasis was put on large-area, high-current devices, and forward currents of approximately 400 A were achieved in composite devices towards the end of the project. Experimental and theoretical studies of impact ionization and avalanche ruggedness were also conducted. For the second thrust (the Foundry), the focus was primarily on 1.2-kV-class devices, although towards the end of the project outstanding results on 3.3-kV-class devices were also achieved. The aim of the Foundry was to develop a high-yield, reliable, and economic vertical GaN pn diode process. The Foundry conducted characterization of incoming epitaxial material and correlated this information with the yield and performance of fully processed devices. Wafer maps of diode characteristics such as forward and reverse current as well as capacitance-voltage curves were measured using auto-probing. Several mask sets comprising different-area devices as well as multiple edge termination designs (implanted junction termination extensions, guard rings, and combinations thereof) were studied, and machine-learning-based approaches were utilized to analyze the data. Packaging and reliability efforts were also undertaken for the Foundry diodes, which are necessary for a viable commercial process.

Acknowledgements

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Accomplishments and Objectives

A summary of the tasks, milestones, deliverables, and their final status is provided in the table below.

Table 1. Key Milestones and Deliverables.

Tasks	Milestones and Deliverables
Task 1: Development of work plan 1.1: Refine tasks and milestones for the work plan	• Development of interim/lower level tasks and milestones. **Project Q1** • 1.1: Refine tasks and milestones for the work plan (if applicable). **Due project Q1** **Actual Performance: Completed Q1 (FY19Q4).** Reviewed and verified milestones at the program kickoff meeting in Philadelphia on June 20, 2019 as well as at the project kickoff meeting in Washington DC on October 7, 2019.
Task 2: Epitaxial Materials Growth 2.1: (Go/No-Go) Develop growth conditions for 5 kV PN diode 2.2: Develop growth conditions for 10 kV PN diode 2.3: Develop growth conditions for 20 kV PN diode	• The final objective of this project element is to grow epitaxial GaN layers of sufficiently low net doping and sufficiently high thickness to achieve a prototype 20 kV PN diode fabricated at Sandia for the EMP arrestor, and 6.5 kV diodes fabricated with high yield at the NRL/NIST nanofab. **Project Q1-Q9** • 2.1: Demonstrate controllable n-type doping <8×10^{15} cm^{-3}, evaluated by capacitance-voltage measurements, in a >30-um-thick epitaxial GaN layer on a GaN substrate suitable for 5 kV device processing as justified through simulations and edge termination. Perform studies of compensating deep level defects in the GaN layer and correlate to growth conditions. Concurrently develop growth conditions necessary for a 1.2 kV diode to be fabricated at the NRL/NIST nanofab. **Due project Q3** **Actual Performance: Completed project Q2 (FY20Q1).** Drift layers of thickness >40 um with doping as low as 1-2×10^{15} cm^{-3} were achieved. • 2.2: Demonstrate controllable n-type doping <4×10^{15} cm^{-3}, evaluated by capacitance-voltage measurements, in a >50-um-thick epitaxial GaN layer on a GaN substrate suitable for 10 kV device processing as justified through simulations and edge termination. Perform studies of compensating deep level defects in the GaN layer and correlate to growth conditions. Concurrently develop growth conditions necessary for a 3.3 kV diode to be fabricated at the NRL/NIST nanofab. **Due project Q6** **Actual Performance: Completed project Q6 (FY21Q1).** The team measured carrier concentrations of 1-3×10^{15} cm^{-3} by CV measurements of fabricated PN diodes with 45- and 50-um-thick drift layers. Similar carrier concentrations were measured by Hg-probe CV of n-GaN epitaxial calibration layers. • 2.3: Demonstrate controllable n-type doping <2×10^{15} cm^{-3}, evaluated by capacitance-voltage measurements, in a >100-um-

Tasks	Milestones and Deliverables
	thick epitaxial GaN layer on a GaN substrate suitable for 20 kV device processing as justified through simulations and edge termination. Perform studies of compensating deep level defects in the GaN layer and correlate to growth conditions. Concurrently develop growth conditions necessary for a 6.5 kV prototype diode to be fabricated with high yield at the NRL/NIST nanofab. **Due project Q9** **Actual Performance: Estimated to be 50% complete at the end of the project.** A trial thick epi run using the TNSC reactor at Sandia was not successful and resulted in severe build-up in the reactor. This prompted the team to re-consider the feasibility of MOCVD for 10- and 20-kV-class epi, and investigations have been on-going regarding the possible use of HVPE growth instead. As a result of this, the focus of the project shifted to large-area (>10 mm^2) devices in the 1-5 kV range.
Task 3: Materials 3.1: Impact ionization characterization	• The final objective of this project element is to establish the semiconductor materials understanding necessary to enable a prototype 20 kV GaN PN diode fabricated at Sandia for the EMP arrestor, and a 6.5 kV diode fabricated with high yield at the NRL/NIST nanofab. **Project Q1-Q9** • 3.1: Determine impact ionization coefficients in GaN based on optically-induced avalanche multiplication experiments at Stanford. Approximately 4 wafers with epi per quarter will be provided by Sandia to Stanford for this task/milestone, plus other processing tasks performed there. Acceptance of an impact ionization characterization report by ARPA-E Program Director. **Due project Q8** **Actual Performance: Completed project Q8 (FY21Q3).** Measurements of the ionization coefficients were made and compared to processed device breakdown voltage data.
Task 4: Device Fabrication 4.1: Establish baseline high-yield pilot 1.2 kV diode manufacturing line. 4.2: Demonstrate 5 kV GaN diode 4.3: Establish high-yield pilot 3.3 kV diode production line 4.4: Demonstrate 10 kV GaN diode	• The final objective of this project element is to fabricate a prototype 20 kV GaN PN diode at Sandia for the EMP arrestor, and to establish a 6.5 kV GaN PN diode in a high-yield pilot production line at the NRL/NIST nanofab. **Project Q4-Q12** • 4.1: Establish a baseline, high-yield pilot manufacturing capability for a 1.2 kV GaN PN diode with avalanche breakdown. Develop back-side ohmic contacts suitable for 1.2, 3.3, and 6.5 kV GaN PN diodes. Develop back-side thinning processes for GaN diodes in support of impact-ionization studies. Demonstrate reliable high-yield production of this diode at the NRL/NIST NanoFab with >50% yield on at least one wafer per lot, where yield is defined as GaN PN diodes with area >1 mm^2, forward current density >500 A/cm^2, differential specific on-resistance in the forward direction <1.3 $m\Omega\ cm^2$, turn-on voltage <3.5 V, and leakage current density <1 mA/cm^2 at 80%

Tasks	Milestones and Deliverables
4.5: Establish high-yield pilot 6.5 kV diode production line 4.6: Demonstrate 20 kV GaN diode	of rated breakdown voltage. Approximately 12 wafers with epi per quarter will be provided by Sandia to NRL for this task/milestone. Acceptance of a baseline 1.2 kV process report by ARPA-E Program Director. **Due project Q5** **Actual Performance: Completed project Q7 (FY21Q2).** Many of the 1.2-kV-class, 1 mm^2 devices met the yield target for most metrics. However, a problematic issue was the thick metallization, which significantly impacted R_{ON} and was unavailable due to the COVID-imposed closure f the NIST nanofab. The addition of thick Au metallization at NRL enabled an estimated reduction in R_{ON} for the best Foundry devices such that the 1.3 $m\Omega\ cm^2$ target was met with the appropriate use of wafer thinning and back-side processing. • 4.2: Fabricate and characterize 5 kV GaN PN diode and verify >5 kV avalanche breakdown. The diode must also have: Area >1 mm^2, forward current density >330 A/cm^2, differential specific on-resistance in the forward direction <7.7 $m\Omega\ cm^2$, turn-on voltage <3.5 V, and leakage current density <1 mA/cm^2 at 80% of rated breakdown voltage. **Due project Q6** **Actual Performance: Completed project Q7 (FY21Q2).** As of the previous quarter, all of the metrics had been met except for the forward turn-on criterion, and this final metric was met in project Q7. A detailed investigation of the dependence of the forward characteristics of the device with duty cycle was conducted, which allowed the turn-on metric to be satisfied. • 4.3: Establish high-yield pilot manufacturing capability for a 3.3 kV GaN PN diode with avalanche breakdown. Demonstrate reliable high-yield production of this diode at the NRL/NIST NanoFab with >30% yield on at least one wafer per lot, where yield is defined as GaN PN diodes with area >1 mm^2, forward current density >400 A/cm^2, differential specific on-resistance in the forward direction <3.8 $m\Omega\ cm^2$, turn-on voltage <3.5 V, and leakage current density <1 mA/cm^2 at 80% of rated breakdown voltage. Approximately 12 wafers with epi per quarter will be provided by Sandia to NRL for this task/milestone. Acceptance of a 3.3 kV pilot production process report by ARPA-E Program Director. **Due project Q8** **Actual Performance: Estimated to be 50% complete at the end of the project.** This milestone was not completed primarily due to the closure of the NIST fab. However, good progress was made, particularly towards the end of the project – devices were designed, epi was delivered to NRL, and initial device results were very promising, with breakdown voltages up to 3.8 kV demonstrated.

Tasks	Milestones and Deliverables
	• 4.4: Fabricate and characterize 10 kV GaN PN diode and verify >10 kV avalanche breakdown. The diode must also have: Area >1 mm^2, forward current density >200 A/cm^2, differential specific on-resistance in the forward direction <28 $m\Omega\ cm^2$, turn-on voltage <3.5 V, and leakage current density <1 mA/cm^2 at 80% of rated breakdown voltage. **Due project Q9** **Actual Performance: Estimated to be 50% complete at the end of the project.** While progress was made and breakdown voltages >6 kV were achieved, given the reconsideration of the drift region growth mentioned above, the 10 kV device work was delayed as the focus of the project shifted to large-area (>10 mm^2) 1-5 kV diodes. • 4.5: Establish high-yield pilot manufacturing capability for a 6.5 kV GaN PN diode with avalanche breakdown. Demonstrate reliable high-yield production of this diode at the NRL/NIST NanoFab with >10% yield on at least one wafer per lot, where yield is defined as GaN PN diodes with area >1 mm^2, forward current density >280 A/cm^2, differential specific on-resistance in the forward direction <13 $m\Omega\ cm^2$, turn-on voltage <3.5 V, and leakage current density <1 mA/cm^2 at 80% of rated breakdown voltage. Approximately 12 wafers with epi per quarter will be provided by Sandia to NRL for this task/milestone. Acceptance of a 6.5 kV pilot production process report by ARPA-E Program Director. **Due project Q11** **Actual Performance: Estimated to be 0% complete at the end of the project.** This milestone was delayed due to the unavailability of 6.5 kV class epi coupled with the closure of the NIST nanofab, resulting in the focus of the Foundry processing efforts on 1.2 and 3.3 kV class device fabrication. • 4.6: Fabricate and characterize 20 kV GaN PN diode and verify >20 kV avalanche breakdown. The diode must also have: Area >1 mm^2, forward current density >110 A/cm^2, differential specific on-resistance in the forward direction <110 $m\Omega\ cm^2$, turn-on voltage <3.5 V, and leakage current density <1 mA/cm^2 at 80% of rated breakdown voltage. **Due Project Q12** **Actual Performance: Estimated to be 0% complete at the end of the project.** This milestone was delayed due to the unavailability of 20-kV-class epi as discussed above, resulting in a shift in focus of the project to large-area (>10 mm^2) 1-5 kV diodes.
Task 5: Device Modeling 5.1: Evaluate edge terminations and down-select to best design	• The final objective of this project element is to design an edge termination that enables 6.5 kV breakdown in a high-yield GaN PN diode and 20 kV breakdown in a prototype GaN PN diode, without sacrificing switching speed. **Project Q1-Q10**

Tasks	Milestones and Deliverables
5.2: Finalize edge termination for 3.3 and 10 kV diodes 5.3: Finalize edge termination for 6.5 and 20 kV diodes 5.4: EMP switching simulation	• 5.1: Evaluate the suitability of different edge termination approaches for high voltage diodes based on numerical simulation and compatibility with processing capability. Down-select to most suitable design and optimize for 1.2 and 5 kV diodes. Acceptance of an edge termination simulation report by ARPA-E Program Director. **Due project Q3** **Actual Performance: Completed project Q4 (FY20Q3).** For the Foundry, the primary path was established to use implanted guards/rings and/or JTEs, with a secondary plan to use a bevel termination. Simulations and experiments at Stanford determined that a 1° edge termination is a highly efficient edge termination design. For the high-voltage EMP arrestor diodes, the path was established to utilize a multi-zone JTE implemented either by etching. • 5.2: Finalize edge termination design for 3.3 and 10 kV diodes using numerical simulation. Acceptance of an edge termination simulation report by ARPA-E Program Director. **Due project Q6** **Actual Performance: Completed project Q6 (FY21Q1).** Simulations were performed of both the drift layers and the anodes/edge terminations required for the 10 kV EMP diodes and the 3.3. kV Foundry diodes. The 10 kV diodes will utilize a multi-step JTE, and the 3.3 kV diodes will utilize various combinations of guard rings and JTEs as a primary path, and bevel termination as a secondary path. This follows the approach used for the 5 kV EMP diodes and 1.2 kV Foundry diodes. • 5.3: Finalize edge termination design for 6.5 and 20 kV diodes using numerical simulation. Acceptance of an edge termination simulation report by ARPA-E Program Director. **Due project Q9** **Actual Performance: Estimated to be 75% complete at the end of the project.** While substantial progress on this task was made, it was put on hold due to the thick epi and NIST nanofab challenges described above, and the resulting shift in the project focus to large-area (>10 mm^2) 1-5 kV diodes. • 5.4: Perform simulation studies to ensure that diode design is compatible with switching performance required for use in EMP applications. Acceptance of an EMP switching simulation report by ARPA-E Program Director. **Due project Q10** **Actual Performance: Estimated to be 75% complete at the end of the project.** Electro-thermal considerations under high-voltage/high-current avalanche conditions were examined, and TCAD simulations of avalanche structures were also conducted.

Tasks	Milestones and Deliverables
Task 6: Reliability and Failure Analysis 6.1: Reliability test set-up 6.2: Reliability testing and failure analysis of 1.2 kV NRL/NIST diodes 6.3: Reliability testing and failure analysis of 3.3 and 6.5 kV NRL/NIST diodes	• The final objective of this project element is to understand and improve the reliability and failure modes of GaN PN diodes fabricated in the NRL/NIST NanoFab. **Project Q2-Q11** • 6.1: Set up HTRB and HTOL reliability testing capability for diodes up to 6.5 kV breakdown. Test system using existing 1.2 kV vertical GaN PN diodes. Acceptance of a baseline reliability testing report by ARPA-E Program Director. **Due project Q2** **Actual Performance: Completed project Q3 (FY20Q2).** This was slightly delayed due to difficulties in placing the Sandia subcontract with EDYNX. Testing capabilities for 1.2 through 6.5 kV diodes were completed. • 6.2: Conduct HTRB and HTOL reliability testing and advanced failure analysis using novel spectroscopic and imaging techniques of 1.2 kV GaN PN diodes fabricated in the NRL/NIST NanoFab and provide feedback to fab process. Acceptance of a 1.2kV reliability testing report by ARPA-E Program Director. **Due project Q7** **Actual Performance: Completed project Q7 (FY21Q2).** HTRB and HTOL reliability testing and advanced failure analysis using novel spectroscopic and imaging techniques of 1.2 kV GaN PN diodes fabricated in the NRL/NIST NanoFab was conducted, and feedback was provided to the fab process. • 6.3: Conduct HTRB and HTOL reliability testing and advanced failure analysis using novel spectroscopic and imaging techniques of 3.3 kV GaN PN diodes fabricated in the NRL/NIST NanoFab, and provide feedback to fab process. If possible, conduct similar testing for initial 6.5 kV diodes. Acceptance of a 3.3 and 6.5 kV reliability testing report by ARPA-E Program Director. **Due project Q11** **Actual Performance: Estimated to be 75% complete at the end of the project.** While test capabilities and procedures were established, this milestone was delayed due to the unavailability of 3.3 kV and 6.5 kV Foundry diodes as discussed above.
Task 7: EMP Arrestor Demonstration 7.1: Develop EMP arrestor test capability 7.2: Demonstrate EMP robustness	• The final objective of this project element is to verify that a 20 kV GaN PN diode can be effectively utilized as an EMP arrestor for the electric grid. **Project Q4-Q12** • 7.1: Modify existing reverse-recovery setup into an EMP test/demo circuit for avalanche breakdown characterization and perform experiments to simulate EMP event using existing 1.2 kV GaN PN diodes. The response time must be <10 ns and the avalanche energy tolerated must exceed 1.0 J/cm^2 over a 500 ns pulse. **Due project Q4** **Actual Performance: Completed project Q4 (FY20Q3).** The previously existing reverse-recovery setup was converted to

Tasks	Milestones and Deliverables
	measure reverse breakdown, and the time response of the breakdown of a vertical GaN diode was characterized. • 7.2: Perform experiments to simulate EMP event using 20 kV GaN PN diode. The response time must be <10 ns and the avalanche energy tolerated must exceed 10 J/cm2 over a 500 ns pulse. **Due project Q12** **Actual Performance: Estimated to be 50% complete at the end of the project.** This milestone was delayed due to the unavailability of 20 kV diodes for the reasons discussed above. However, several successful experiments were performed on lower-voltage diodes.
Task 8: Tech to Market 8.1: Initial T2M Plan and Impact Sheet drafted 8.2: Product / First-Market Fit 8.3: Techno-Economic Analysis (TEA) 8.4: Manufacturing and Scalability 8.5: Follow-On Funding and Stakeholder Adoption	• The final objective of this project element is to determine the best path to bring the GaN EMP arrestor to market. **Project Q1-Q11** • 8.1: The goal of this milestone is to develop and demonstrate an understanding of the various key considerations in attempting to commercialize this new technology. The initial T2M plan will be completed per the template and instructions provided by ARPA-E. An IP strategy for the project will be included. Patent applications including inventions reduced to practice stemming from work performed in this project will be entered into the Federal iEdison system. Submission of draft Impact Sheet that describes the desired impact the project team would like to have by the end of the project. Deliverable: Submit T2M plan to ARPA-E and present it to program director and T2M Advisor for approval. **Due project Q1** **Actual Performance: Completed project Q2 (FY20Q1).** Completed initial T2M plan and impact sheet. • 8.2: Prepare GaN arrestor product hypotheses and test them through direct conversation with potential adopters of the technology. Include a draft datasheet with target specifications. Include an analysis of competitive products or approaches and compile a list of new technology attributes for comparison. Deliverable: Present product hypotheses requirements to program director and T2M Advisor for approval. **Due project Q4** **Actual Performance: Completed project Q4 (FY20Q3).** The characteristics of a prototype GaN EMP arrestor product were specified and compared to existing technology. • 8.3: Generate a model that provides insight into the trade-offs and interactions between GaN arrestor product design, cost (including bill of materials), and performance. Deliverable: Present TEA model to program director and T2M Advisor for approval**. Due project Q6** **Actual Performance: Completed project Q6 (FY21Q1).** A techno-economic analysis report was completed, which was

Tasks	Milestones and Deliverables
	included in project Q6 report, and the key elements of which are also included in this final report. • 8.4: Develop the expected arrestor production processes. Identify risks in processes and supplies to manufacture first market product. Demonstrate the manufacturing process. Include reliability testing for devices to validate GaN arrestor robustness. Identify and engage suppliers for materials and production equipment/processes. Update product datasheet if needed. Deliverable: Present a report which describes the validated process and arrestor performance to program director and T2M Advisor for approval. **Due project Q8** **Actual Performance: Estimated to be 75% complete at the end of the project.** The analysis of device cost that was conducted is a major component of this, and the fabrication process was demonstrated, albeit below 20 kV. Reliability testing of GaN diodes was delayed due to the closure of EDYNX. While progress was made on identification of markets and suppliers, commercial vertical GaN diode production is required. • 8.5: The PI and T2M PoC will identify and engage with internal & external entities to identify the best first market applications for the technology. The team will provide the PD and T2M advisor with quarterly updates of progress including feedback they receive from the interactions with stakeholders. Final transition and next stage planning report is due at M8.5. **Due project Q8-Q11** **Actual Performance: Estimated to be 25% complete at the end of the project.** Some conversations occurred with potential commercial adopters of the technology, although was been judged that these are likely not good options, and alternatives must be identified. • Identify appropriate next-stage funding sources. Address both long-term and near-term, first-market applications. Describe plan to engage with potential funding sources and map out next-stage goals and resource needs. Deliverable: Analysis of potential next-stage funding presented to program director and T2M Advisor for approval. **Due project Q11** **Actual Performance: Estimated to be 25% complete at the end of the project.** Similar to M8.5 this was delayed, with analogous activities.

Project Activities

This project had two main thrusts. The first, led by Sandia, was the development of vertical GaN diodes targeted at Electromagnetic Pulse (EMP) mitigation applications. The project aimed

to develop 1 mm^2 devices with breakdown voltage ratings of 5, 10 and 20 kV. The second thrust of the project, led by NRL, was to demonstrate the manufacturability of 1.2, 3.3, and 6.5 kV diodes and to demonstrate an open Foundry process (in conjunction with the NIST nanofab). This portion of the project focused on wafer screening and mapping of diode performance and yield for various device designs. Other efforts in the project focused on reliability (EDYNX), avalanche robustness (Stanford), and the theory of impact ionization in GaN (Boston University).

Mid-way through the project, the focus at Sandia was shifted from the attainment of 10-20 kV devices to large-area, high-current devices in the voltage range up to 5 kV. A 10 kV device was retained as a stretch goal, but was not achieved due to difficulties in growing GaN drift layers thicker than 50 um. However, a large-area (>13 mm^2), high-current device was demonstrated at 400 A pulsed forward current, which also had 1600 V breakdown and low reverse leakage current. Additionally, as a result of the closure of the NIST nanofab (due to COVID), the Foundry effort was run exclusively at NRL and the 6.5 kV device was transitioned to a stretch goal (which was not achieved, largely due to unavailability of sufficient amounts of thick GaN epi). Godd 3.3. kV Foundry devices were achieved, however.

EMP Arrestor Diode Development

In pursuit of a 20 kV vertical GaN PN diode, several milestones were set to demonstrate the ability to provide thick, device-quality epitaxial material with sufficiently low net n-type doping. This required developing growth conditions necessary for 5 kV, 10 kV, and 20 kV epilayers corresponding to milestones M2.1, M2.2, and M2.3. In the 3rd year of the project the SOPO was updated to remove the 20 kV milestone and focus instead on large-area, high-current devices. Based on TCAD simulation data, a design space was explored that indicated a 10 kV diode would require at least a 50 µm drift layer with an N_d-N_a carrier concentration < 4×10^{15} cm^{-3}. Initial epitaxial growth was pursued using Sandia's Veeco MOCVD reactor. Commercially available 2" HVPE GaN substrates were used and both the LED- and-LD grade options were explored. The LED substrates consistently resulted in a rough surface morphology that was determined to not be suitable for device development. The LD-grade substrates tended to provide stable growth with significantly less concerning surface morphology as compared to the LED-grade. In FY20 we demonstrated a 60 µm thick epilayer with controlled doping on the order of 6×10^{15} cm^{-3}. A Nomarski image map of the as-grown 60 µm drift layer along with Hg probe CV results demonstrating controlled doping is shown in Figure 1.

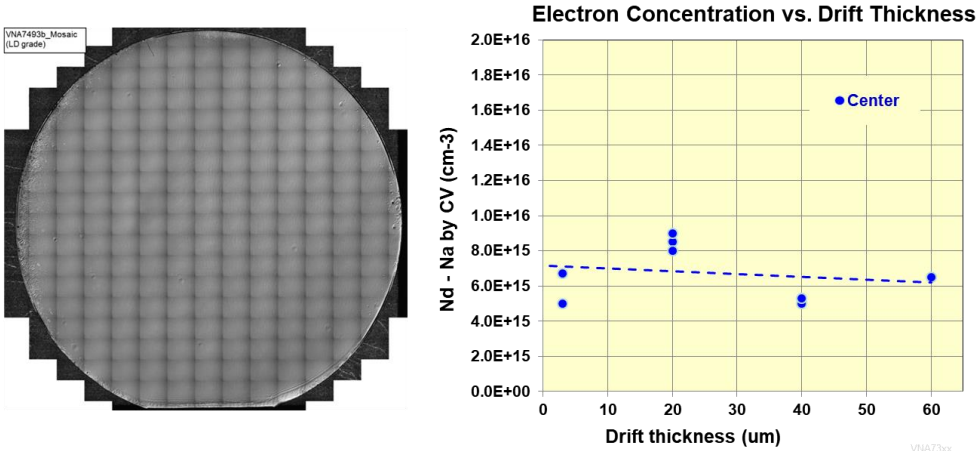

Figure 1. (left) Nomarski image of 2" HVPE LD-grade GaN wafer with an additional 60 µm epitaxial drift layer grown using Sandia's Veeco MOCVD reactor. (right) Carrier concentration as measured by Hg probe CV for several different drift thicknesses, up to 60 µm.

In conjunction with the development of thick, low-doped, device-quality epitaxy, proper junction termination extensions (JTEs) were explored. While several methods were utilized throughout the program, the development of the high-voltage diode at Sandia relied on a multi-zone step-etched approach to mitigate the electric field in the device. Early efforts consisted of a three-zone design on a 14 µm thick, 1×10^{16} cm^{-3} concentration drift layer. The etch depths were determined by considering the breakdown electric field anticipated in the device and the doping in the p-region to estimate the net dose required to fully deplete the outer zone and sustain the breakdown field in the inner zone. This analysis followed Gauss's Law and was also verified via TCAD modeling. Overall, the goal was to provide a window that accounted for process and doping variations, as well as potential etch damage impacts. The width of the steps required to sustain the highest possible breakdown also had to be explored. Our initial design on the 14 µm drift layer indicated that a 50 µm step width (3.5x the drift thickness) was sufficient to achieve consistent, low-leakage, 2 kV breakdown. A diagram of the design along with an image of a processed diode and a reverse breakdown result is shown in Figure 2.

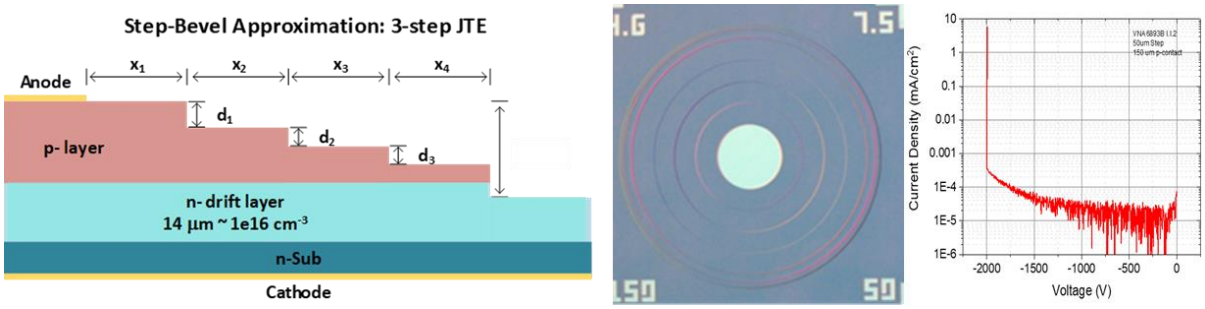

Figure 2. (left) Axisymmetric diagram of device with included JTE structure. Multiple variations of the x and d dimensions were explored. (middle) Optical image of a fabricated device with a 150 µm diameter anode contact and 50 µm wide JTE steps. (right) Reverse IV characteristic of a typical well-performing device from this design lot. Multiple devices demonstrated noise floor leakage out to 2 kV breakdown.

Further understanding of the JTE design was pursued on a thicker 50 µm drift layer with ~2×10^{15} cm^{-3} net doping. A four-zone design was implemented with JTE step widths ranging from 0 to 100 µm. Multiple device types were evaluated for forward and reverse IV characteristics. Those that maintained a reasonable forward IV were considered when looking at how the JTE step width impacted the device breakdown. Figure 3 provides an annotated image of the processed wafer alongside a plot of average breakdown vs. step width. A "quick fab", or no JTE device with only an isolation etch is included in the middle of the array to ensure variations were not due to the devices' position on the wafer. It is clear that with no JTE structure, a significant reduction is breakdown is observed. Additionally, increasing the JTE step width tended to show an increase in breakdown up to about 1.5x the drift region thickness. It should be noted that the Veeco reactor used to perform these early studies was known to have variations in doping uniformity across the 2" wafer. So, even while a clear trend is observed, it was still rather difficult to definitively understand at which point the JTE step width was sufficient to maximize the device breakdown.

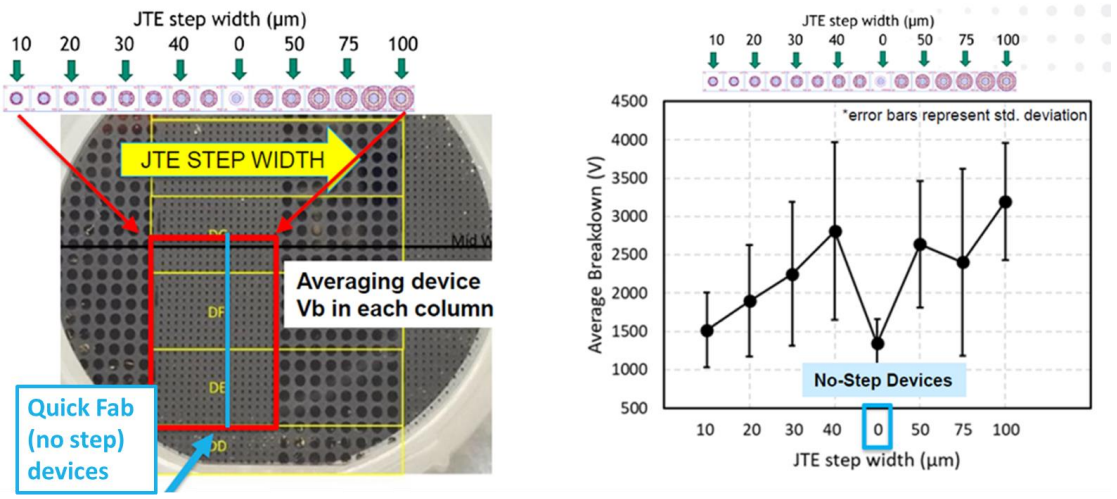

Figure 3. (left) Annotated optical image of a processed 2" wafer with a 50 µm drift region and varying JTE step widths and anode sizes. (right) Average breakdown of different device columns, each with varying JTE step widths.

While the Veeco MOCVD reactor was able to provide valuable insight into both the ability to grow low-doped, thick epi layers and proper JTE design, an opportunity to attempt a thick, low-doped drift region on Sandia's newer TNSC SR4000HT reactor presented itself. This tool had been shown to provide significantly better uniformity in the epitaxial growth across the 2" HVPE GaN substrates. An LD-grade substrate with a threading dislocation density of ~10^6 cm^{-2} and electron concentration of ~2×10^{18} cm^{-3} was used to grow a 50 µm thick, lightly-doped n^- drift region, followed by a standard p-type region. Significantly more detail can be found in the Yates *et al.* IEEE TED publication listed under the journal articles. The as-grown wafer was found to have good surface morphology with few particle defects. PN diodes were processed on multiple quarter wafers that consisted of both four- and two-zone JTE designs. 75 and 150 µm step widths were implemented for the four- and two-zone designs, respectively. Two anode sizes were incorporated into the design, consisting of total areas of either 0.063 mm^2 or 1.0 mm^2. An

axisymmetric schematic of the diode design is shown in Figure 4. Device CV curves were measured to determine the carrier concentration in the drift region, which was found to vary between ~5×10^{14} and 1×10^{15} cm^{-3}. This is also shown in Figure 4. This epi growth and device design resulted in multiple 6 kV class devices with both the 0.063 mm^2 and 1.0 mm^2 anode contacts, with differential specific on-resistances of 10.2 and 8.3 $m\Omega\text{-}cm^2$, respectively, when considering current spreading at a 45° angle through the drift region and pulsed I-V measurements for the 1.0 mm^2 device. Figure 5 contains the both the reverse and forward I-V characteristics for the devices. Excellent low leakage was demonstrated, with a measurement-limited noise floor of 100 pA. Initial breakdown characterization was performed in fluorinert on devices without additional passivation.

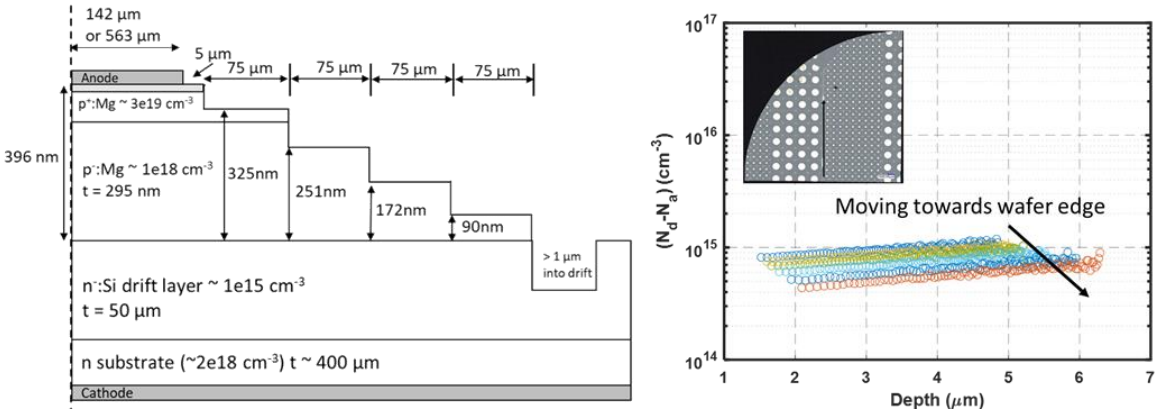

Figure 4. (left) Axisymmetric schematic of vertical PN diode with four-zone JTE design. (right) Extracted carrier concentration of measured devices in the n-GaN drift layer. A frequency of 1 MHz was used for the CV measurements.

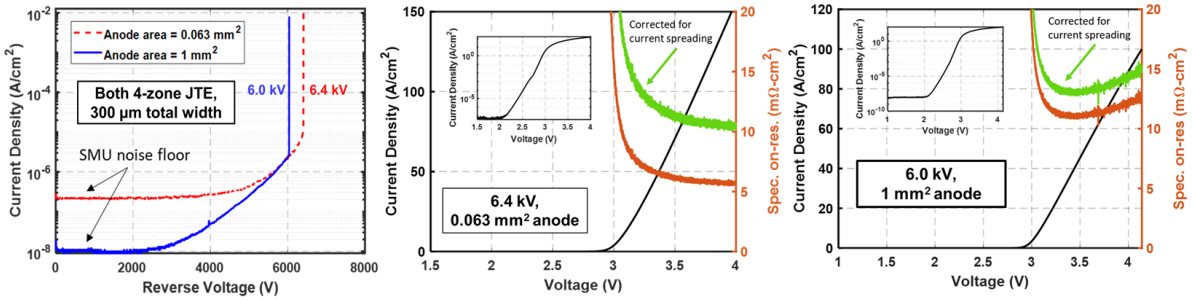

Figure 5. (left) Reverse I-V characteristics and breakdown voltage of two PN diodes with anode areas of 0.063 mm^2 and 1.0 mm^2. The noise floor change is a result of different anode areas and not due to the characterization equipment. (middle) Forward I-V characteristics of a 6.4 kV diode with a 0.063 mm^2 anode area. (right) Forward I-V characteristics of a 6.0 kV diode with a 1.0 mm^2 anode area. Both the middle and right figures were taken to a maximum of 1 A DC current, and the specific on-resistance is shown using both the anode area and assuming a 45° current spreading through the drift region. Insets show the forward I-V on a semilogarithmic scale.

Further interrogation of the devices demonstrated a near-equivalent performance between the four- and two-zone JTEs. A temperature-dependent breakdown analysis was also performed to check for indications of avalanche breakdown. Due to the use of fluorinert, we were limited

to 100°C during our temperature-dependent tests. However, we were still able to clearly see an increase in both leakage and breakdown as a function of temperature (Figure 6).

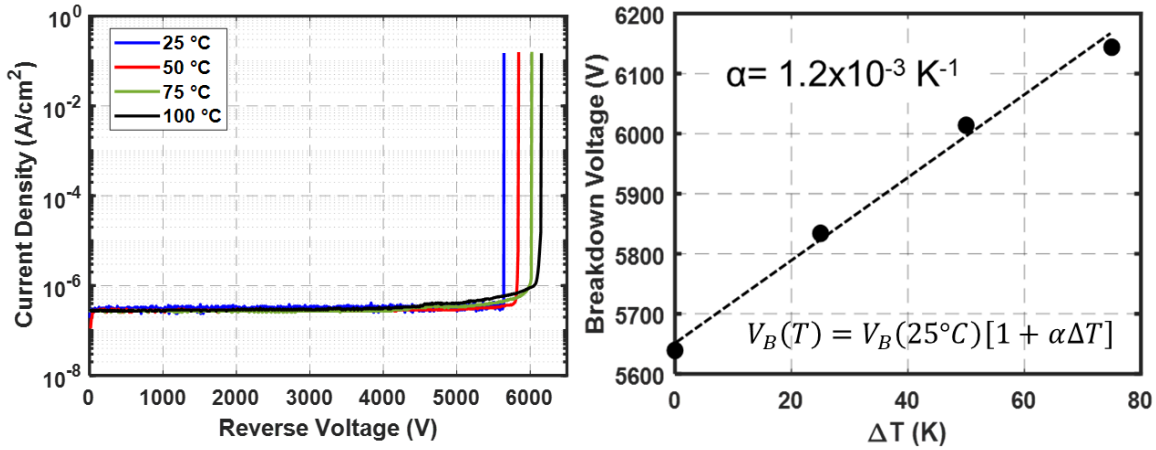

Figure 6. (left) Temperature dependence of the reverse I-V characteristics of a PN junction diode with an anode area of 0.063 mm^2. (right) Linear relationship of breakdown with change in temperature as indicated by the inset equation. A temperature coefficient of 1.2×10^{-3} K^{-1} was fit and is consistent with literature for this doping level.

A passivation process was developed and implemented with the 6 kV class devices. Our initial designs included a bi-layer approach, consisting of a 100 nm thick layer of ALD-deposited Al_2O_3 followed by a 2 µm thick layer of PECVD-deposited SiN. Our studies have shown that the inclusion of the additional ALD Al_2O_3 layer achieves lower reverse leakage currents than observed for devices solely using a PECVD SiN deposition, likely due to surface damage during the PECVD process. We have also explored the use of an LPCVD-deposited film, but we were unable to complete this process before the end of the program. In Figure 7a, we present a simple schematic of the passivation with our four-zone JTE design. Figure 7b shows reverse I-V characteristics of one of our 1 mm^2 anode contact devices with a four-zone JTE before and after the addition of the bi-layer passivation. Both tests were performed in fluorinert. It is shown that the inclusion of the passivation resulted in a slight increase in leakage current, but also increased the breakdown voltage of the device by ~10%. It is postulated that the passivation aids in the effectiveness of the JTE by reducing surface charges that would otherwise be present when handling and testing the wafer in air. Even though fluorinert is used during the reverse I-V characterization, there are not typically additional surface cleaning or treatment steps performed as there is with the passivation deposition procedure. Finally, in Figure 7c and Figure 7d we compare the reverse I-V characteristics of 24 of the 0.063 mm^2 anode area devices. All devices were found to have an increased breakdown voltage, and 20 out of the 24 tested devices maintained excellent low leakage < 1 nA out to 80% of breakdown. Although it is not shown here, the impact on forward I-V characteristics was found to be minimal, with a very slight change in the sub-threshold voltage slope.

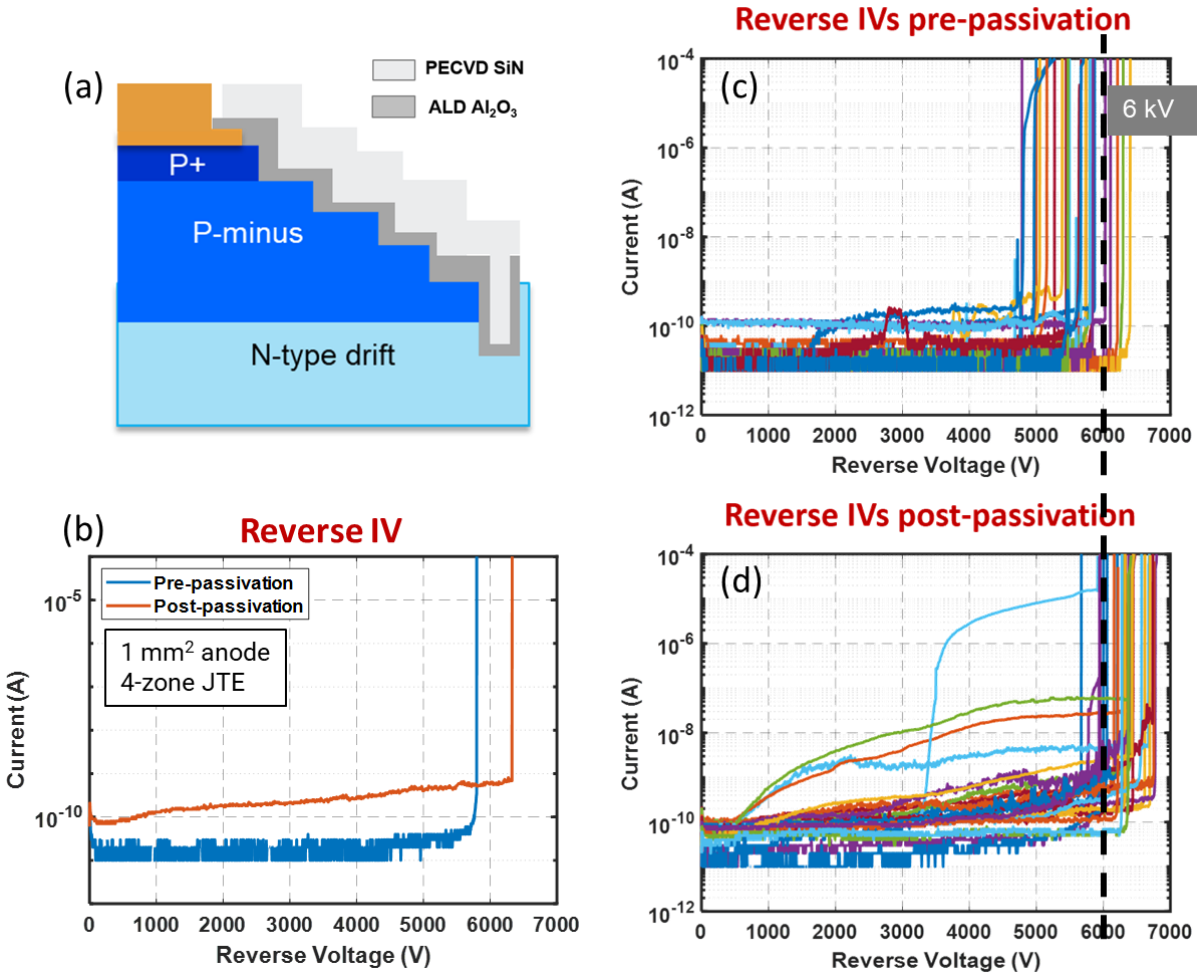

Figure 7. (a) Schematic of implemented passivation consisting of 100 nm ALD Al_2O_3 and 2 µm PECVD SiN. (b) Reverse IV characteristics of a PN diode with 1 mm^2 anode contact. A slight increase in leakage current is observed with an almost 10% increase in breakdown voltage. (c) & (d) Comparison of 24 devices with 0.063 mm^2 anode contacts. A total of 20 devices maintained <10 nA leakage current up to 80% of breakdown, with all the devices demonstrating an increase in absolute breakdown voltage. This resulted in multiple devices breaking down at 6.7 kV.

The successful demonstration of a 5 kV class device with an effective passivation layer paved the way to focus on scaling device area to enable high current capabilities. Milestone M4.5 was modified in year 3 to reflect this new effort to scale size and current capabilities for a 5 kV class device. In pursuit of this new goal, an initial study was undertaken to gain a better understanding of how device yield was impacted by both the total anode area and the total device area (including the JTE and isolation). An 1800 V epi design was used to facilitate the initial studies. All devices consisted of a four-zone JTE design. The layout of devices was randomized on the mask in an effort to provide meaningful statistics over the eight different designs. A total of 256 devices were evaluated for forward and reverse characteristics, which meant that each of the eight device types had 32 devices characterized. All devices sustained DC forward conduction up to 1

A and an ~1800 V breakdown. A yield criterion of < 1µm/cm^2 at a V_R > 1600 V was implemented. The forward I-V characteristics underwent visual inspection. We found that our yield criterion seemed to depend on total device area more so than anode area. For the devices with a constant anode area of 0.243 mm^2, the device pass rate decreased as the JTE width was increased. The 100 µm JTE devices had an 84% yield, the 200 µm JTE devices had a 72% yield, the 300 µm and 400 µm devices both had a 69% yield, and the 550 µm JTE devices had a 53% yield. Moving to the constant total area (2.47 mm^2) devices, the devices with an anode area of 0.111 mm^2 had a 59% yield, the 0.243 mm^2 anode devices had a 53% yield, the 0.49 mm^2 anode devices had a 59% yield, and the 1 mm^2 anode devices had a 50% yield. Figure 8 shows the above information in graphical form. There appeared to be a clear trend that demonstrated a reduced yield with increasing area. However, as we reach our maximum total area of 2.47 mm^2 the pass rate did not vary as significantly, even though the anode area was increasing.

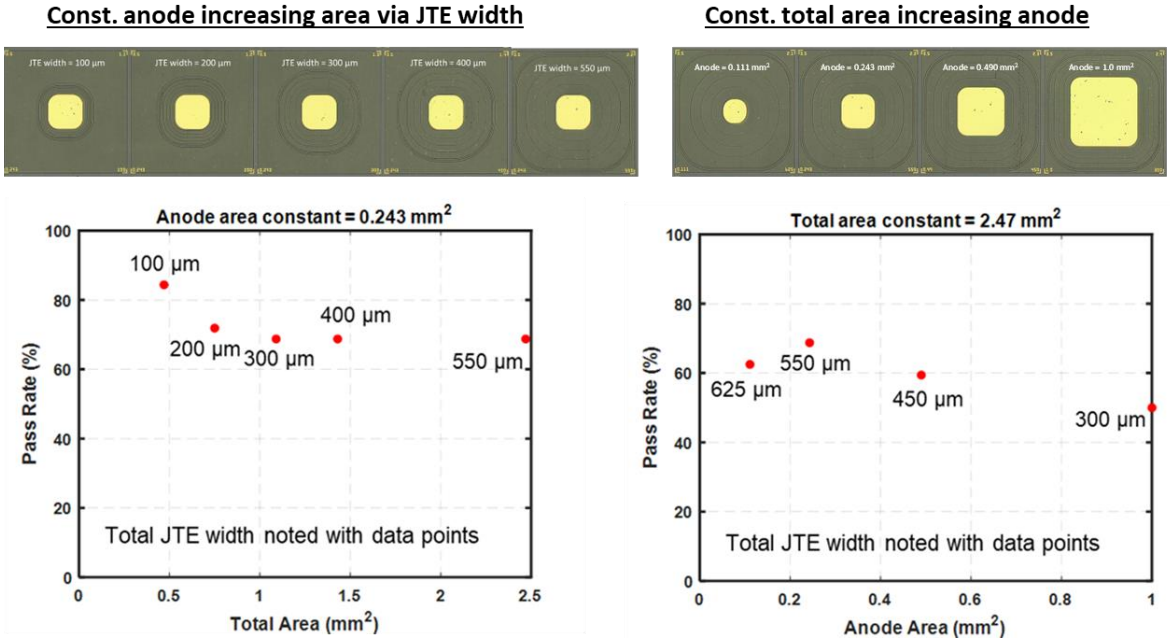

Figure 8. (left) The pass rate vs. total area for the devices with a constant anode area and increasing JTE width. The JTE width is noted on the data points, and an image of the completed diodes is shown above the plot. (right) The pass rate for devices with a constant total area vs. anode area. An image of the diodes is shown above the plot. Increasing the device total area reduces the pass rate, with a combination of large anode and large total area leading to the lowest yield.

Rather than focus on single devices with very large anode areas that are capable of 100's of amps of current conduction, we decided to utilize an interconnected approach to parallel multiple devices to create a large effective anode area. This was primarily due to the randomness of critical defects in GaN and previous attempts that failed to yield 4 mm^2 and larger devices. Based on results from our anode vs. total area studies, we developed a quad cell array mask that consisted of four cells with either a 10x10, 8x8, 6x6, or 4x4 total device array. This design resulted in single anode areas in the respective cells of 0.243 mm^2, 0.48 mm^2, 1.04 mm^2, and 2.77 mm^2. A four-zone 100 µm total width JTE was used for all devices in this effort. A full 2" wafer was

fabricated with the quad cell design. Our bi-layer passivation was included from the start. Once fabrication was completed, all devices underwent an initial screening to allow for the identification of "good" devices that passed our yield criteria of < 1μm/cm^2 at a V_R > 1600 V. In parallel, a TCAD study was performed to understand the impact of placing a contact metal over isolation trenches between the devices. This was required to connect the devices and was thought to create a MOS capacitor, which led to the question of how thick our passivation would need to be to sustain not only the 1600 V devices, but our eventual > 5 kV devices. It was discovered that as long as the isolation is continuous between devices and the etch depth is fairly shallow, the PN junction provides field protection to the dielectric, allowing our bi-layer passivation to maintain electric fields well below the dielectric breakdown limit. This was shown to be valid experimentally with our 1600 V devices.

The completed quad cell wafer post-characterization and interconnection is shown in Figure 9a. Devices were evaluated initially prior to the interconnect metallization, post-interconnection, and post packaging/ribbon bonding. Figure 9b shows a cell with the 2.77 mm^2 anode devices that has been singulated, die-attached, and ribbon-bonded into a TO-254 package. The singulated device with the interconnected devices is approximately 8 mm x 8 mm. A total of 20 ribbon bonds (each ribbon bond was 25.4 μm x 76.2 μm) were used to interconnect approximately 13.85 mm^2 total anode area. Figure 9c consists of the initial on-wafer reverse I-V characterization of the 16 devices found in this cell. A total of six devices from the screening in Figure 9c were found to pass our yield criteria, and five of those were chosen to be interconnected and ribbon-bonded as seen in Figure 9b. The final reverse I-V characterization of the packaged device is show in Figure 9d as compared to the five connected devices as evaluated on-wafer. While a slight increase in leakage current and a reduction in breakdown is observed post-interconnection and packaging, the paralleled device is able to maintain < 1 nA leakage current out to a 1600 V breakdown voltage. This was a non-destructive breakdown and was shown to be repeatable.

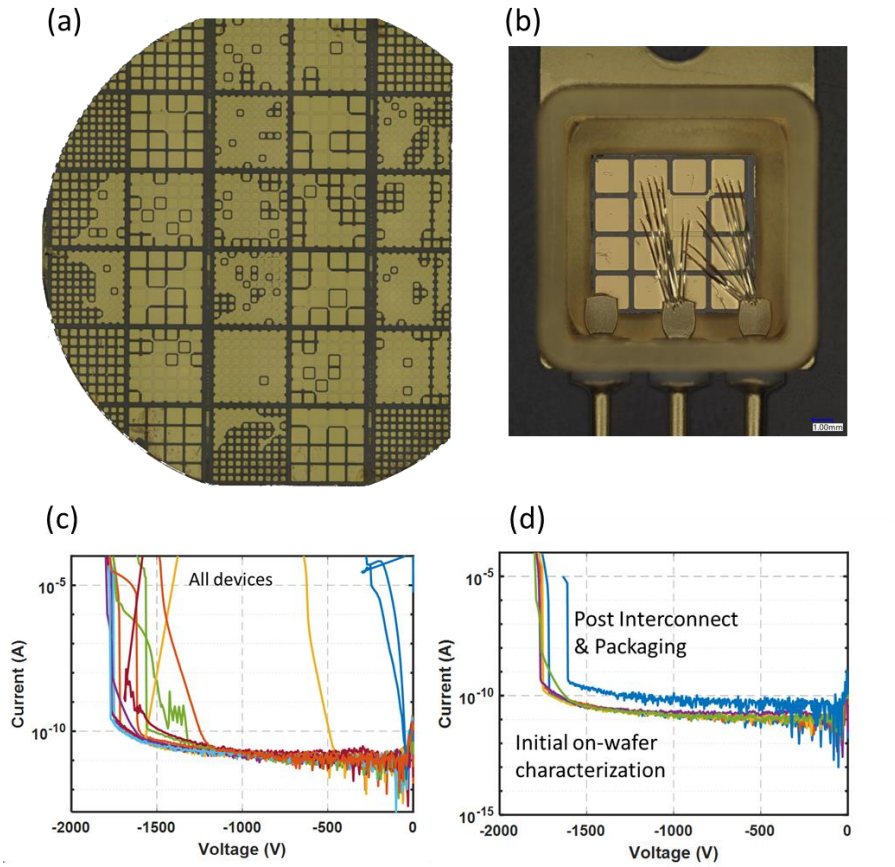

Figure 9. (a) Completed 2" quad cell wafer post-screening and interconnect metallization. The right edge was diced off prior to interconnect for initial wire/ribbon bonding tests. (b) A 4 x 4 cell with five of the largest 2.77 mm^2 anode devices connected in parallel and ribbon-bonded into a TO-254 package. (c) Initial reverse I-V characterization of the on-wafer devices from the same cell shown in (b). (d) A comparison of the reverse I-V characteristics of the paralleled devices on-wafer and post interconnect and packaging.

Three of the completed interconnected, paralleled, and packaged diodes are shown in Figure 10a. While we attempted to account for chipping and dicing artifacts, we found that the 300 µm dicing lanes still led to several of the singulated cells suffering damage to the outer JTE structures on some of the devices. Because they were paralleled with the inner devices, this led to the entire cell suffering from elevated reverse I-V leakage or complete failure. The first of the three devices shown in Figure 10a appeared to have edge damage due to the dicing process. Future efforts will use wider dicing lanes and/or implement substrate thinning, followed by a scribe and break approach. Regardless, we were able to demonstrate up to 400 A current conduction using a 50 µs pulse width and 0.1% duty cycle. Additionally, the 13.85 and 7.53 mm^2 samples maintained low reverse I-V leakage and 1600 V breakdown (Figure 10b). The forward I-V characterization shown in Figure 10c indicates that increased total anode area is reducing the on-resistance of the device, however, the small change with a 2x increase in anode area further indicates that the current is now limited by the conduction capabilities of the ribbon bonds and/or the resistance associated with the die-attach on the backside of the die. This process is currently being

transferred to our 5 kV class epitaxial material, but at the time of this report has not yet completed processing and characterization. This effort will continue with follow-on funded projects that also maintain an interest in both high-voltage and high-current vertical GaN PN diodes.

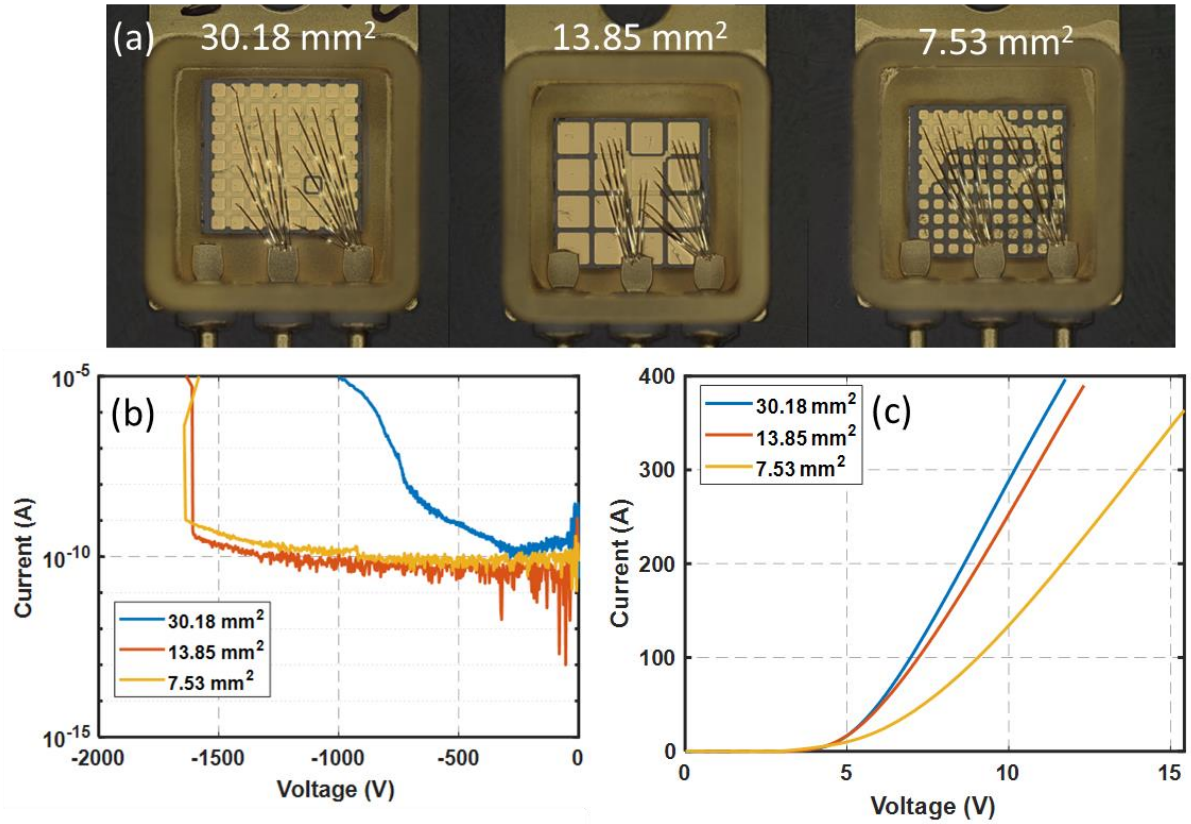

Figure 10. (a) Optical images of three paralleled packaged diodes of varying individual anode areas. (b) The reverse I-V characteristics of the packaged diodes in (a). The 13.85 and 7.53 mm^2 devices maintained low leakage and 1600 V breakdown, while the largest 30.18 mm^2 device exhibited elevated leakage. (c) The forward I-V characteristics showing a reduction in resistance for the larger paralleled anode contact areas and ~400 A forward current conduction. Testing was performed using a 50 µs pulse width with a 0.1% duty cycle.

Finally, we are continuing our efforts to realize a 10 kV class diode by utilizing low doped (< 1×10^{15} cm^{-3}), thick (~100 µm) HVPE-grown epitaxial drift layers. This material has been accompanied with thinner drift samples to allow for some development of our p-GaN regrowth process on the HVPE material. At the time of this report, the wafers with the HVPE drift regions have been received, and initial regrowth attempts on the thinner sister wafers have not provided device-quality material. This effort will continue through follow-on funded projects.

Foundry Process Development

Process Overview

This program developed a pilot-production-scale manufacturing process for 1.2 and 3.3 kV class diodes. The process modules consisted of optimization of the epitaxial layer stack to include an appropriate substrate vendor, drift layer and anode design, p-ohmic metallization, n-ohmic metallization, planar implant and edge termination processes utilizing nitrogen ion implantation, and surface passivation. We identified that the most relevant substrate materials were readily available from Mitsubishi Chemical at the beginning of the program, and in layer years we were able to procure ammonothermal substrates as well, which exhibited reduced dislocation density. The diode structure utilized for the 1.2 kV process node was an 8 um, N_D-N_A = 1E16 cm^{-3} drift layer with a 400 nm / [Mg] = 1E18 cm^{-3} anode layer grown in-situ on top of the diode. As shown in Figure 11, a hybrid edge termination region was formed utilizing both a junction termination extension (JTE) and superimposed guard ring (GR) structure to precisely control the charge laterally from the anode to the isolation edge, essentially digitizing the linear shape of a bevel edge. The process is completely planar utilizing nitrogen ion implantation to form semi-insulating GaN regions. It is important to note that the edge termination is formed in the remaining active p-GaN (not the implanted regions). Isolation regions are formed via a deeper and higher-dose implant. All implants are designed as a multi-energy box profile to the desired depth. Following implantation and cleaning, the top-side and back-side metals were deposited. Passivation processes such as both PECVD and LPCVD SiO_2 and SiN_x films were also evaluated in the program, but the results were inconclusive in identifying an appropriate technique. All fabrication was completed at NRL, because NIST facilities were unavailable from March 2020 to June 2023 due to COVID-related access restrictions.

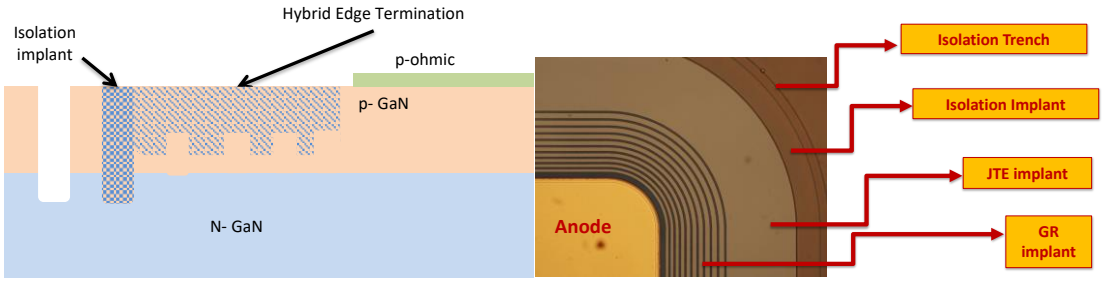

Figure 11. GaN diode cross-section and optical image.

Incoming Metrology

Techniques were developed to assess the quality of incoming epitaxial films and identify appropriate wafers for fabrication and assignment to experiments. Initially, a Hg-probe technique was applied to quantify drift layer carrier concentration. This was later expanded to a mapping service utilizing commercially available tools at NIST, enabling 32-point maps on a 50 mm wafer. In addition to C-V mapping, we also developed optical profilometry processes based on mapping using a commercial Zygo interferometer tool. By taking the optical profilometry data, binning regions of the wafer to areas approximating the device regions, and performing statistical analysis of the data, we were able to generate a distribution of average RMS roughness as well

as percent area covered by bumps (corresponding to extreme roughness due to surface hillocks) and pits (pinholes in the epitaxial layer or wafer due to particles or surface defects on the wafer). We have correlated the presence of such defects to device performance and thus are able to statistically predict the yield of devices fabricated on-wafer. Experimental data is ~90% accurate compared to modeled yield, which is acceptable given the presence of fab defects and yield as well. An example of predictive algorithm data on "good" and "bad" wafers is shown in Figure 12.

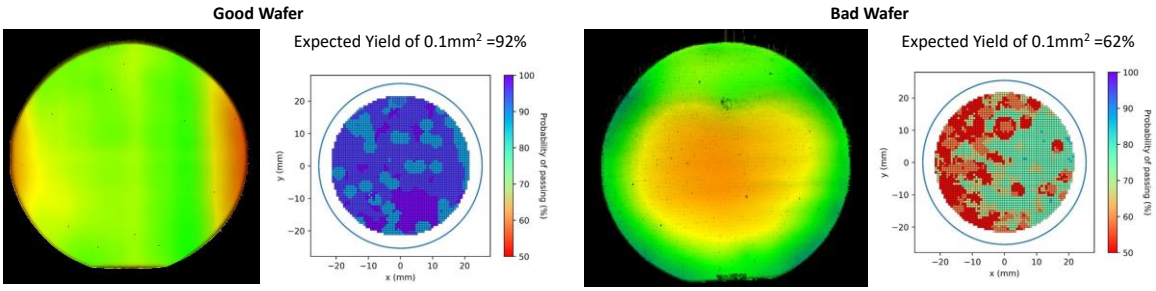

Figure 12. Optical profilometry image and predicted yield for multiple wafers.

Electrical Testing

The wafers were tested under DC and pulsed forward I-V, resulting in maximum current of 18 A for a 1 mm^2 device and on-resistance of 1.2 mOhm-cm^2. The maximum current capability was relatively consistent, though testing was later limited to 10 A to avoid damaging the diodes during testing. We performed many systematic evaluations to assess the appropriate probe configuration and metallization thickness for large-area devices. We also performed limited studies to scale device area to >1 mm^2 and potentially up to full wafer by selectively removing the "failed" areas predicted above from the metallization pattern. Typical I-V results from a "good" wafer are shown in Figure 13. We were able to clearly achieve avalanche breakdown at 1.4 kV using an optimized termination design (discussed below).

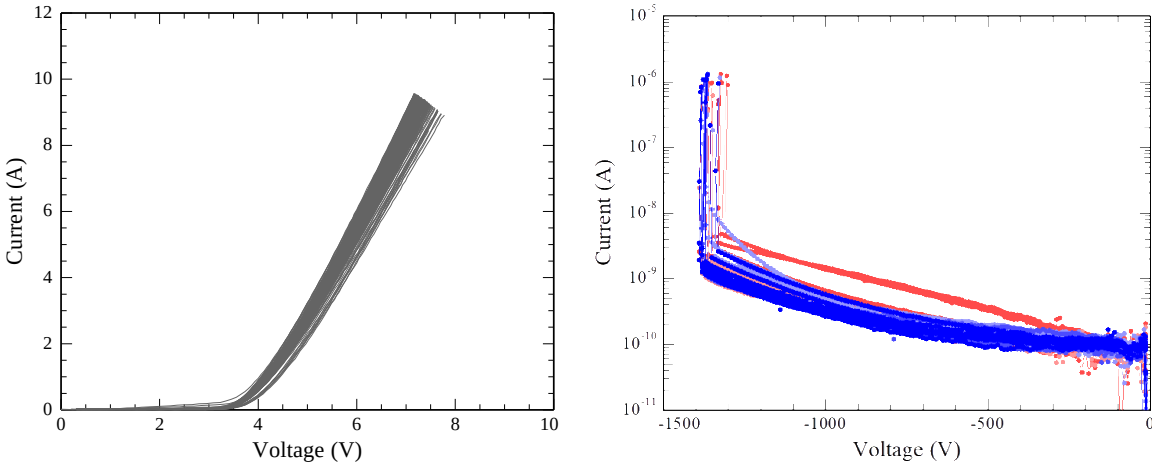

Figure 13. Typical I-V behavior of 1 mm^2, 1.2 kV-class Foundry diodes.

The device behavior was quantified using NRL-developed auto-probing techniques. We were able to successfully fabricate 48 wafers over 12 Lots, meeting the metrics of the program, and fabricating >25,000 devices. We observed a spread in ON-resistance from 1-4 mOhm-cm^2, which we attribute to both variations in the anode p^{++} cap process due to epitaxial layer variability as

well as instability in the NRL metallization process due to the inherent nature of a multi-user facility. We also observed a spread in breakdown voltage from 600-1400 V, which we have determined is a function of the drift layer doping, anode doping, anode thickness, and edge termination design. In some cases we observed significant variation within-wafer for reverse I-V performance, which we attribute to a localized variation in miscut angle. It is important to note that the drift layer doping and forward I-V behavior was generally relatively constant. An example of this is shown in Figure 14.

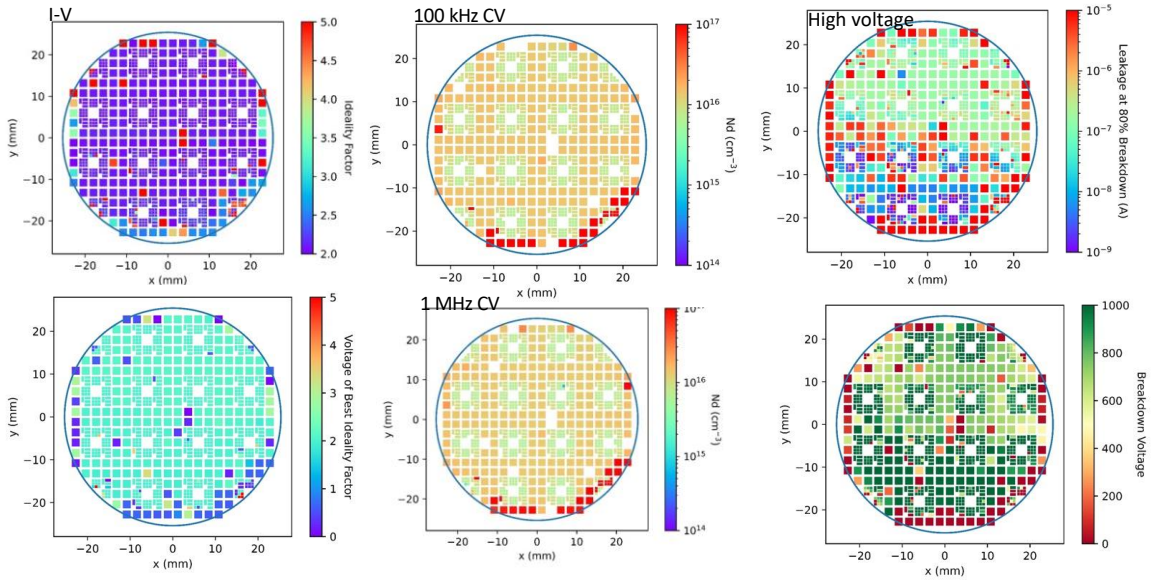

Figure 14. Typical auto probe map of Foundry wafer.

Optimization of edge termination design is critical to achieve abrupt, avalanche breakdown in the Foundry process. To study this, we developed several controlled experiments to implement in the production process. By varying the anode thickness, we were able to systematically vary the thickness of the remaining p-GaN layer, since the implant depth is constant and the wafers are processed in parallel. Since the implant depth is ~300 nm, we varied the anode thickness from 500 nm to 300 nm. In doing so, we observed that by making the anode thin, and thus the underlying p-GaN layer constituting the JTE/GR region <10 nm, we were able to achieve >100x reduction in leakage current under reverse bias conditions. In addition, the temperature dependence of the reverse I-V behavior changed to show an increased breakdown voltage at elevated temperature. Finally, we also observed the electroluminescence spot moving from the edge of the isolation implant to the edge of the anode. The latter two observations are consistent with avalanche breakdown. We performed a similar experiment holding the anode thickness constant at 400 nm while varying the Mg doping level from 2E19 cm^{-3} down to 5E17 cm^{-3}. In this case, the optimal Mg concentration was 1E18 cm^{-3}, which also resulted in an abrupt avalanche breakdown confirmed by its temperature dependence and electroluminescence imaging. These results are all consistent with simulation results reported in the literature. A summary of the I-V behavior is shown in Figure 15.

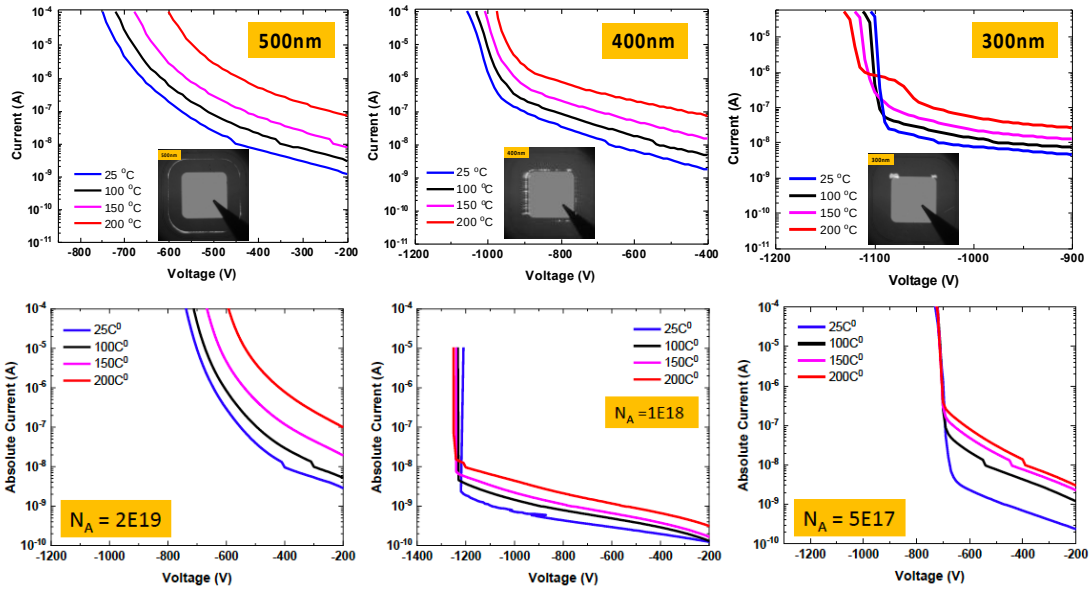

Figure 15. Temperature-dependent reverse I-V behavior of six different anode designs.

Second-Generation Device (3.3 kV-Class Diode)

We successfully designed a second-generation diode targeted at 3.3 kV-class operation, utilizing a ~25 um epitaxial drift layer with a doping target of 4E15 cm^{-3}. In the initial fabrication Lots (10-12), there were no additional alterations to the anode design or edge termination process. We successfully demonstrated 3.6-3.8 kV operation with forward current capability of 8 A and specific ON-resistance of <7 mOhm-cm^2 as shown in Figure 16. Electroluminescence imaging confirmed a similar signature as the 1.2 kV-class diodes. A second wafer with higher drift layer doping resulted in inferior performance, which indicates the importance of the doping specification.

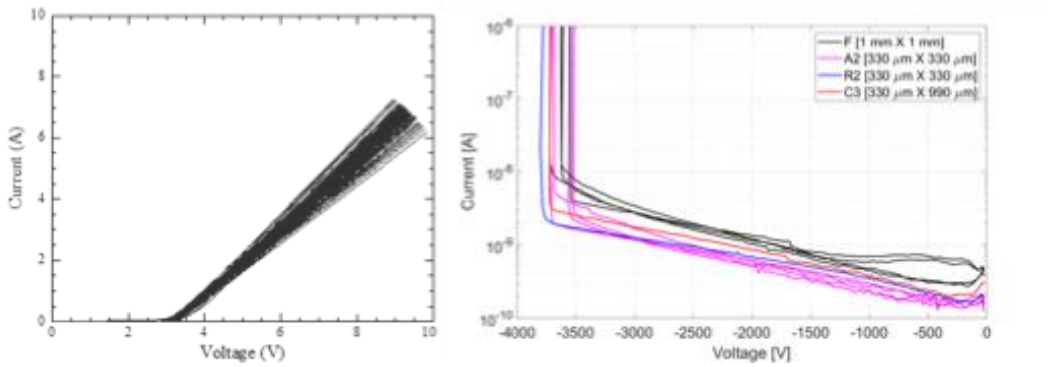

Figure 16. Typical I-V behavior of 1 mm^2 3.3 kV-class Foundry diodes.

Packaging Development

The NRL team engaged with Integra to procure services for mounting and wire-bonding Foundry parts using a surface-mount package from Spectrum Semiconductor (SMD10003). Given

the geometry of the package we expect it to be capable of 2-3 kV, but further testing is required. The dicing is performed in-house at NRL using a pattern determined by auto-probe testing, followed by separation of known good parts, cleaning, and shipping for packaging. Following wire-bonding, the cavities are potted with Hysol. The supplier was able to place ~16 wire-bonds on a 0.1 mm^2 device and ~64 wire-bonds on a 1mm^2 device. A picture of the wire-bonded devices and the completed parts is shown in Figure 17. Forward and reverse I-V testing on die before and after packaging has identified no obvious degradation in performance following singulation and packaging.

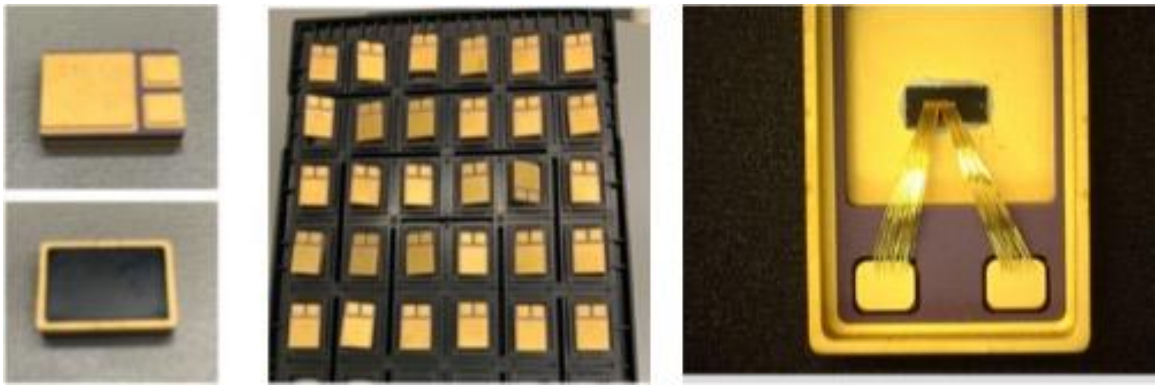

Figure 17. Optical images of packaged parts from 1.2 kV-class diode wafer.

Reliability Evaluation

Reliability testing was conducted primarily at EDYNX, although some also occurred at NRL and at Sandia. Much of this consisted of High-Temperature Operating Life (HTOL) testing of Foundry diodes. As a typical example, Figure 18 shows forward voltage drop versus time for four GaN diodes subjected to HTOL testing at 24 W constant power. The test was conducted at ambient temperature, but self-heating raised the temperature of the diodes to the 150-160°C range. Three of the devices show relatively stable forward voltage followed by an abrupt increase, while one device shows a higher initial forward voltage that does not experience an abrupt increase during the time period measured. The observed behavior and its variation between devices was postulated to be due to variation p-conductivity and/or contact resistance across the device, resulting in localized heating and eventual degradation. Additionally, in this experiment none of the diodes showed appreciable change in the reverse current.

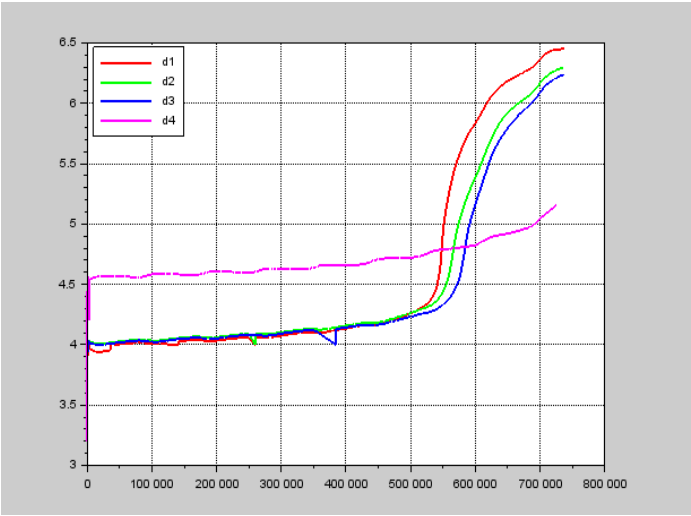

Figure 18. Forward voltage versus time for four GaN diodes during HTOL testing.

Impedance-based techniques were also utilized to study the GaN diodes. For example, representative capacitance-frequency curves at room temperature and 150°C are shown in Figure 19. The high-temperature capacitance-frequency characteristics indicate a general increase in capacitance at high temperature. This is of consequence for devices that are designed to operate at high temperatures and may be correlated with reduced breakdown at high temperature. Further, from the high-temperature characteristics at 1 V bias (red curves) it is clear that there is an additional increase in low-frequency capacitance beyond what is observed at room temperature, suggesting that there is a residual issue that continues to exist close to the junction.

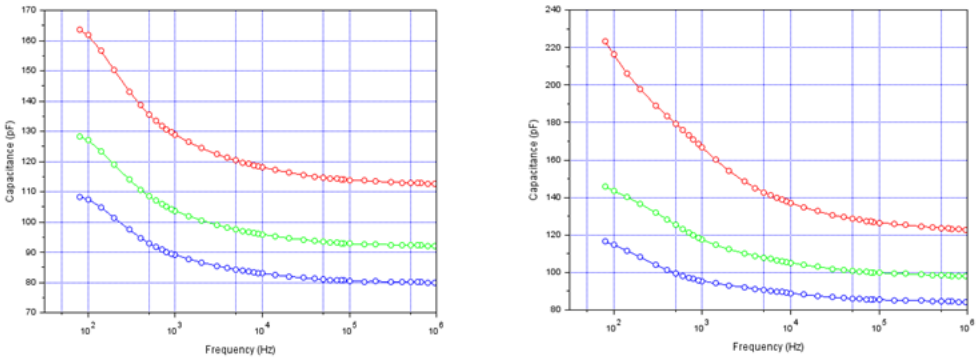

Figure 19. Capacitance-frequency curves at -1 V (blue), 0 V (green), and 1 V (red) for representative GaN diode at (left) room temperature and (right) 150°C.

Avalanche Ruggedness

Stanford University conducted a number of experiments, first by developing a bevel edge termination process and then conducting avalanche ruggedness tests on the fabricated devices. Unclamped Inductive Switching (UIS) was used to evaluate the avalanche ruggedness. As a representative example, circular PN diodes of 300 μm anode diameter were fabricated on a GaN epi-stack as shown in Figure 20(a), which was realized on a highly doped 2-inch n^+ GaN substrate

using MOCVD. A 20 μm n-drift region was grown with Si-doping of 6-9E15 cm^{-3}, followed by a 500 nm p-GaN layer with 5E17 cm^{-3} Mg doping to form the PN junction. A Ni/Au/Ti/Au metal stack was used as the anode on top while a Ti/Au stack was used as the cathode on the backside. All devices possess a field plate with a 5° bevel at the anode for edge termination as shown in Figure 20(b). 300 nm thick spin-on-glass (SOG) was used as the field plate dielectric and for surface passivation. DC characterization of diodes was done using a power device analyzer. This particular diode studied had a turn-on voltage of ~4 V owing to an extra drop at the p-type contact, and an ON-current of up to 2.2 A @ 13 V as depicted in Figure 20(c) with low reverse leakage of 10 pA. The diode showed a reverse breakdown voltage (V_{BD}) of ~2.8 kV @ 1μA, Figure 20(d), with a positive temperature coefficient of 2V/°C as shown in the inset, confirming an avalanche breakdown.

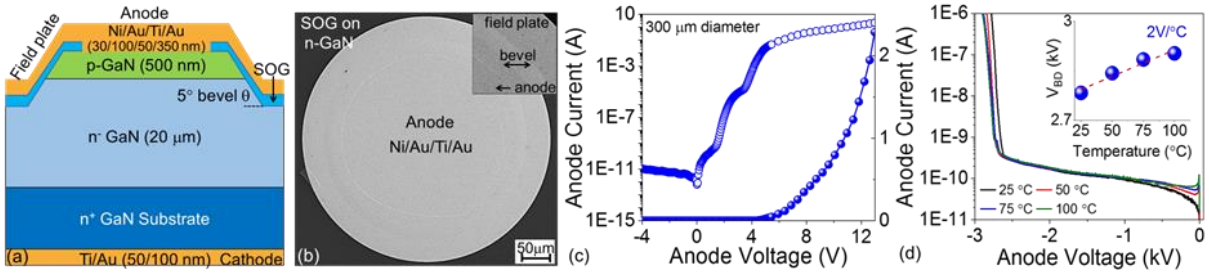

Figure 20. (a) Cross-sectional schematic of 3 kV GaN vertical PN diode depicting different layers of the device stack. Field plate with 5° bevel was used as edge termination at anode. (b) Top view SEM image of diode, with magnified view of field plate and bevel shown in the inset. (c) I-V characteristics of 3 kV GaN vertical PN diode. (d) Reverse breakdown voltage V_{BD} @ 1 μA measured at different temperatures.

The avalanche behavior of the diode was investigated using a UIS test circuit integrated with the wafer chuck under a high-speed CCD camera as shown in Figure 21(a). The diode was probed on-chuck using thick needle probes and connected in anti-parallel to a SiC MOSFET, which has a higher breakdown voltage (3.3 kV) than the diode. The MOSFET is turned on to energize the inductor and later turned off to interrupt the current flow through it. The interruption to the inductor current generates a voltage overshoot at the diode's cathode terminal which pushes the diode into avalanche. Cathode voltage and current waveforms were recorded using high-bandwidth current/voltage probes and a digital storage oscilloscope. During avalanche, the cathode voltage clamped to 2.9 kV and a peak current of 1.4 A flowed through the GaN diode for 1 μs as seen in Figure 21(b). The diode showed avalanche robustness of 1.72 mJ/pulse. In contrast, a bevel-terminated 1.3 kV GaN vertical PN diode without a field plate avalanched at 1.3 kV with a higher current of 2.2 A flowing through the diode for a duration of t_{AV} = 550 ns as depicted in Figure 21(c). The higher current resulted from the diode's uniform avalanche behavior which possibly distributed the thermal stress uniformly across the device. Uniform avalanche is a sign of superior edge termination which was achieved in the 1.3 kV diode. While the 3 kV diode demonstrated avalanche based on the positive temperature coefficient, UIS stress testing suggests that avalanche was not uniform.

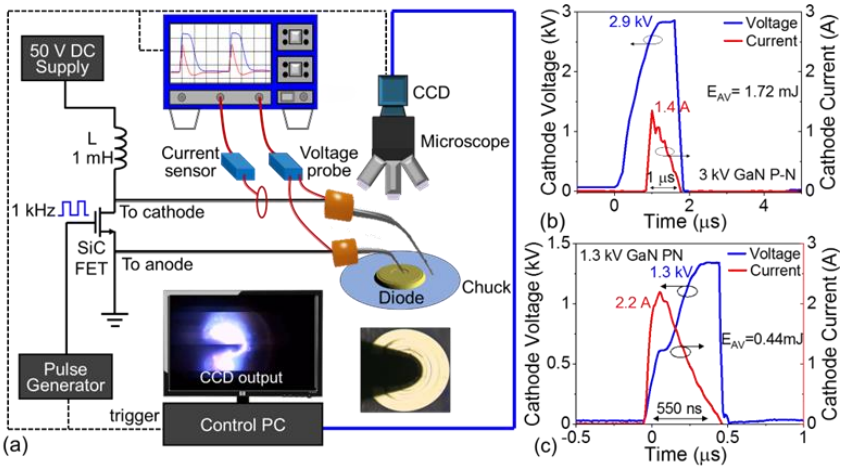

Figure 21. (a) Experimental setup with integrated CCD for on-wafer UIS testing and avalanche study of GaN vertical PN diodes. The diode is probed on-chuck using thick needle probes and is connected anti-parallel to the MOSFET. (b) Cathode voltage and current waveforms recorded for 3 kV GaN vertical PN diode in a UIS cycle. (c) Cathode voltage and current waveforms recorded for 1.3 kV GaN vertical PN diode in similar test.

Avalanche Response Time

To determine the GaN PN diodes' suitability as an EMP arrestor, the breakdown time for various devices was measured. For example, a fully packaged GaN diode produced by NRL was evaluated in a Sandia cable line pulser to measure the time to reverse breakdown. The NRL device had a static breakdown voltage of 800 V (measured by NRL) and was wire-bonded into a ceramic package (shown in Figure 17). This ceramic package was then soldered onto a pulser strip-line board for measurement. The diode was evaluated in a Pulse Arrested Spark Discharge (PASD) setup (Figure 22), which is capable of up to 15 kV pulsed operation in 100 V steps. In this test setup, a fast pulse (5 ns width) is applied to a diode device under test (DUT) which is placed in the blocking configuration. The current and voltage measurement equipment is located behind the diode, and the cable pulser is terminated to ground through a 50 Ω load. This configuration means that the current measurement will only see current flow upon breakdown. Similarly, the 50 Ω terminating load and the DUT form a resistive ladder. While the DUT is in blocking mode, R_{DUT} >> 50 Ω and almost all of the voltage is dissipated across the DUT. When the DUT is in a conducting state, however, R_{DUT} << 50 Ω and almost all of the voltage is dropped across the terminating impedance. This means that both current and voltage measurements will peak upon breakdown of the DUT.

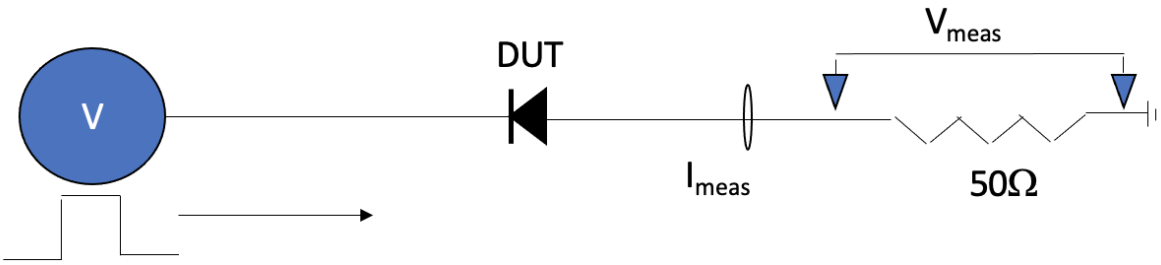

Figure 22. Pulse Arrested Spark Discharge testing diagram for GaN diode.

The results of pulse measurement for the NRL GaN diode are shown in Figure 23 for applied voltages of 1000 V to 1300 V in 100 V increments[1]. The diode is in blocking mode for the pulses at 1000, 1100, and 1200 V (blue, orange, yellow). This is characterized by an incident voltage peak, followed by a flat regime of zero voltage and then a negative reflected peak. The incident peak is due to capacitive depletion region formation in the diode upon the application of the voltage. The current traces for these pulses are dominated by ringing for the first 10 ns after the applied voltage pulse, before damping out to zero at around 10 ns. The pulse at 1300 V (purple trace) shows the beginnings of breakdown in the device, although the magnitude of the change is small, indicating that the device is just on the threshold of breakdown. In this trace, the incident peak dies to zero, then increases linearly over time. At 25 ns, there is a discrete jump in the measured voltage across the terminating resistor, indicating more significant leakage through the diode. This increase in voltage just prior to the reflected wave is confirmed through the current measurement. Unlike the previous voltage traces, the current does not decay to zero at 10 ns, but has a small leakage current (~0.1 A). Corresponding to the time of the voltage increase at 25 ns, there is also an increase in current flow through the diode to a peak value of 1 A that is terminated by the reflected wave.

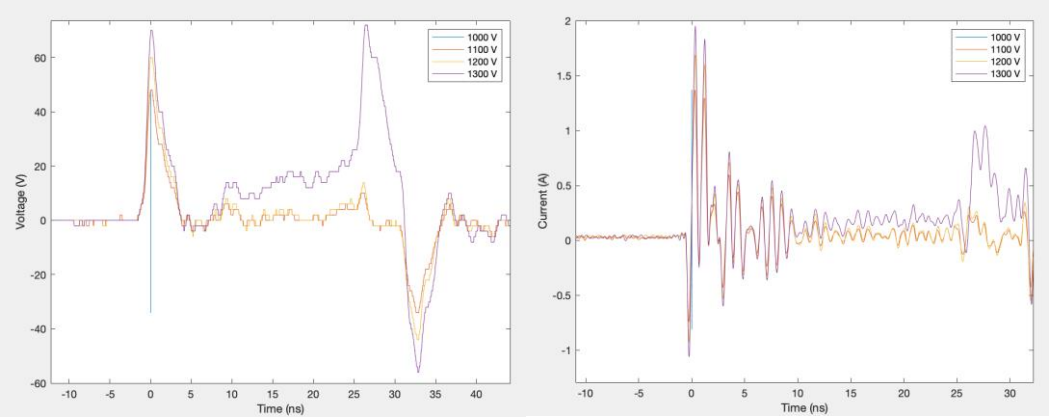

Figure 23. (left) Voltage profile of the PASD pulser from 1000 V to 1300 V. (right). Current profile of the terminating 50 Ω resistor of the PASD pulser.

[1] This voltage level represents the *charge level* of the pulser, which considers open-circuit voltage doubling. The actual applied voltage of the pulse is approximately ½ of the charge level. So, the actual applied voltage to the device is ~500-650 V.

Design of EMP Diodes

Sonrisa Research developed designs for GaN PN diodes specific for use as EMP arrestors, as opposed to general-purpose power electronics applications. For such a diode to survive an avalanche event, the structure should be designed to ensure broad-area avalanche throughout the interior of the diode, rather than at the edge termination. This is typical done by inserting structures under the anode that either concentrate the field locally, reduce the epilayer thickness, or both. Figure 24 illustrates two possible structures to accomplish this. Both structures contain regions under the anode where the drift region thickness T_{Anode} is less than under the edge termination T_{Edge}.

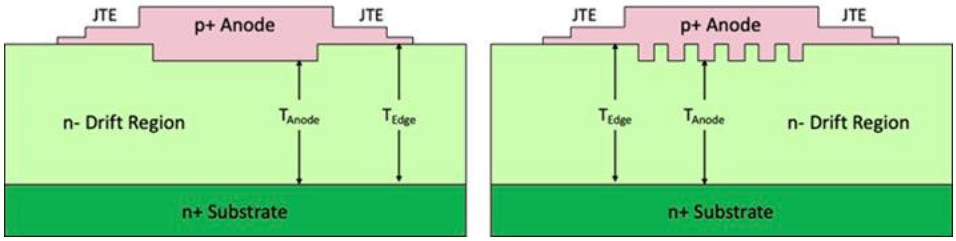

Figure 24. Two diode structures designed for broad-area avalanche rather than edge breakdown.

Suppose we wish to design a 20 kV diode, taking into account the inefficiency of the edge termination. Assuming our edge termination goes into avalanche at 80% of the theoretical one-dimensional breakdown voltage, T_{Edge} must be chosen to have a theoretical breakdown voltage of 25 kV. This can be achieved with a doping of $2x10^{14}$ cm^{-3} and thickness T_{Edge} = 140 µm. Now suppose we want the broad area of the anode to go into avalanche at 20 kV. This gives the thickness of the drift region under the anode T_{Anode} as 110 µm. This creates a 30 µm vertical offset between the pn junction under the anode and the pn junction under the edge termination. These results are obtained from a one-dimensional analysis, and it is important to verify the results using numerical simulations. In either structure in Figure 24, we expect field crowding at the corners of the anode trenches, and this can only be investigated by 2-D (or 3-D) numerical simulations.

High-Field Transport and Impact Ionization

Boston University conducted computational studies of high-field transport and impact ionization in GaN. Early models for impact ionization based on a full-band description utilized a carrier-phonon interaction model affected by uncertainty in the deformation potentials. As a result, a significant uncertainty in the calculated values of the ionization coefficients was also present. While some of these sets were able to predict electron and hole multiplication gains in several avalanche photodetector structures, not unexpectedly the theoretical data differ from the measured data. As pointed out, the main source of uncertainty is the strength of the carrier-phonon scattering rates. To overcome this problem one can directly compute the interaction coefficients that determine the rates. In the past, this was accomplished using different approaches. Empirical models used Fermi's Golden Rule and ad-hoc values of deformation potentials were initially considered. A further improvement of the model is the pseudo-rigid-ion

(PRI) model that is free of empirical/fitting parameter but is non-self-consistent. This approach neglects the change in crystal potential resulting from the atomic displacement. In other words, atoms are assumed to move rigidly with their potential distribution. The latest model is based on an *ab-initio* approach where the energy bands, phonon dispersion, and carrier-phonon interaction are evaluated self-consistently within the density functional theory (DFT) and HSE hybrid functional. From Figure 25, one can immediately see that that while for electrons the *ab-initio* deformation potential scattering rates from DFT-HSE and PRI are similar, there is a significant difference for the hole scattering rate, as the hole-phonon scattering shows a decrease in total rate calculated with DFT-HSE.

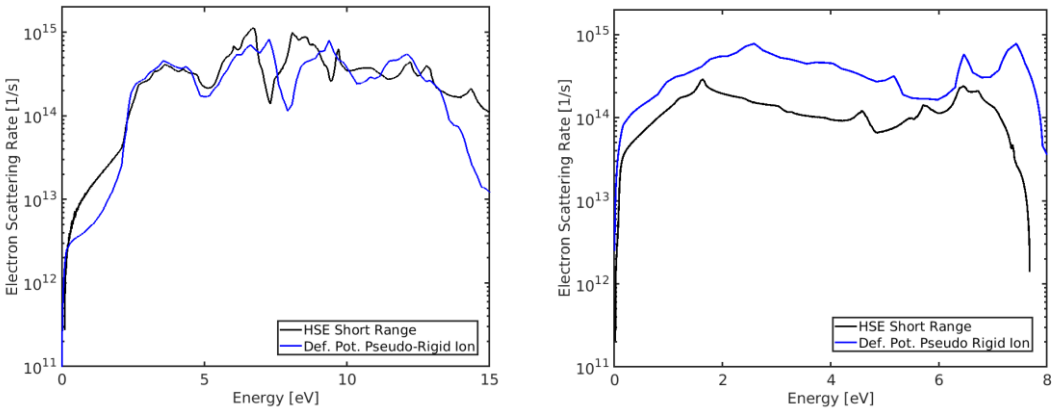

Figure 25. (left) Comparison between the electron-phonon deformation potential scattering calculated with the pseudo-rigid-ion (blue line) and DFT-HSE (black line) models. (right) Comparison between the hole-phonon deformation potential scattering calculated with the pseudo-rigid-ion (blue line) and DFT-HSE (black line) models.

Using the carrier-phonon scattering rates obtained from DFT-HSE, it is possible to re-evaluate the ionization coefficients for electrons and holes. We expect that, due to the lower total scattering rates for holes, the corresponding ionization coefficient will be higher than what was previously computed. Figure 26 presents both the experimental data and calculated hole (open black squares) and electron (open black diamonds) ionization coefficients. We can immediately appreciate that the theoretical values for holes match reasonably well with the experimental data. On the other hand, the values calculated for electrons are an overestimate of the experimental data.

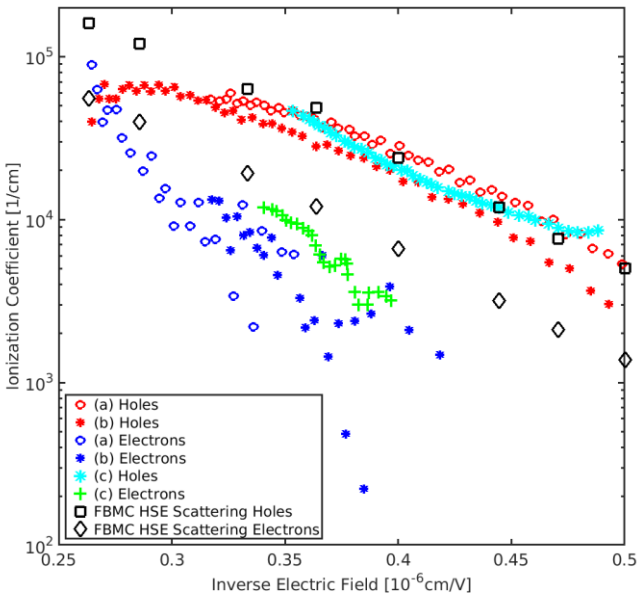

Figure 26. Comparison between the measured and computed electron and hole ionization coefficients for GaN. The data sets are from: (a) and (b) Cao et al., APL 112, 262103 (2018), (c) Maeda et al., Maeda et al., JAP 129, 185702 (2021). The calculated hole and electron ionization coefficients are represented by open black squares and open black diamonds respectively.

Tech-to-Market

Cost Model

A cost model for GaN PN diode EMP arrestors we developed. The cost model identifies the cost components that are expected to determine the price of the GaN arrestor devices, and represents the dependence of the primary cost components on important design, performance, and production parameters.

Production Costs

The full production cost of the GaN arrestors includes the direct production cost (materials and labor) and production overhead. The cost of the GaN diodes themselves is treated as a materials cost in the overall arrestor model; the diode production cost is based on a separate cost model.

Material Cost: The materials inputs to arrestor production include the GaN diodes and the packaging materials. As noted above, a separate cost model was constructed to estimate the GaN diode cost.

GaN Diodes: GaN diodes are produced at a semiconductor fabrication plant (fab) using standard epitaxy and wafer processing steps. The process begins with the epitaxial growth of GaN on GaN

substrate wafers. These wafers are then subjected to approximately 30 fab processing steps, followed by thinning-lapping and finally dicing to yield the individual diode devices. The GaN diode cost model represents materials costs (including the GaN substrate wafers), direct labor, and depreciation/fab overhead, and includes expected yields at both the fab line and die level.

Packaging Materials: Existing packaging cost is based on a custom power-module type package that utilizes a ceramic baseboard and a custom-machined high-temperature polymer enclosure. The present packaging scheme can incorporate large-area diodes including 1 cm^2 devices. The present packaging scheme uses wire-bonds to package devices that are approximately 1 mm^2. For the larger 1 cm^2 devices, the anode connection will need to be changed to a soldered connector, and the die attach process and the soldering of the connector will need to be optimized.

Labor Cost: A detailed estimate of labor requirements (excluding labor to produce the GaN diodes) is not possible due to the lack of a fully developed production process. However, based on manufacturing data for rectifiers, inverters, solid-state lighting (LEDs), and smartphones, labor costs are expected to be approximately 4-12% of the materials cost. The cost model assumes that labor costs for a fully scaled process will be 10% of the materials cost.

Production Overhead: The arrestor production overhead cost includes indirect labor cost, indirect material cost, maintenance, depreciation, taxes, and insurance related to assets. Based on similar industries, production overhead is assumed to be 12 percent of the total material cost for a high-volume process.

Non-Production Costs

The non-production cost of the GaN arrestors includes selling, general, and administrative (SG&A) costs, research and development (R&D), interest, warranty and risk, shipping, and profit. These factors may vary significantly across companies; based on similar industries, the non-production cost in the cost model is assumed to be 25 percent of the full production cost (material, labor, and factory overhead costs).

Cost Analysis

Initial Cost Estimate

An initial cost estimate of $6,900 for a single 1 cm^2, 1 kA, 20 kV GaN arrestor was generated based on a low-volume production process yielding 800 devices per month, with the following cost contributions:

- Materials: $4,500
    - GaN diode: $4,000/device, based on the following contributions and assumptions:
        - 2” GaN wafer: $2000/wafer
        - Epitaxial growth of GaN on the GaN substrate: $2000/wafer

        - Fab costs based on 4-wafer lots, 15 days of fab time, and 15 simultaneous lots, running in 2 shifts with 5 technicians in each shift results in ~25 worker-hours/wafer. The estimated hourly cost of each technician is $100/hour after benefits, taxes, and insurance.
            - Fab labor: $2500/wafer
            - Fab overhead: $2000/wafer
        - Thinning-lapping: $500/wafer
        - Dicing: $500/wafer
        - Testing: $500/wafer
        - 50% line-yield, 50% die-yield (assuming 10 devices/wafer)
    - Packaging materials: $500/device, based on custom production
- Labor: $450
- Production overhead: $550
- Non-production costs: $1400

Cost Reduction Opportunities

The initial cost estimate presented in the preceding section is based on a low-volume process that has not been fully optimized. As the arrestor production process is scaled up, efficiencies and economies of scale will decrease costs. In addition, potentially greater cost reductions will be achieved by leveraging technology advances that are driven by existing (and growing) markets such as LEDs.

Project Outputs

A. Journal Articles

A. Haque et al, "Improving Vertical GaN p-n Diode Performance with Room Temperature Defect Mitigation," accepted to *Semiconductor Science and Technology* (November 2023).

M. Liao et al., "Microstructural Evolution of Extended Defects in 25 um Thick GaN Homoepitaxial Layers," *Applied Physics Letters* 122, 242101 (2023), DOI: 10.1063/5.0152720.

J. C. Gallagher et al., "Using Machine Learning with Optical Profilometry to Estimate the Yield of Vertical GaN Diodes," *Scientific Reports* 13, 3352 (2023). DOI: 10.1038/s41598-023-29107-9.

T. Nelson et al., "Hybrid Edge Termination in Vertical GaN: Approximating Beveled Edge Termination via Discrete Implantations," *IEEE Transactions on Electron Devices* 69(12), 6940 (2022), DOI: 10.1109/TED.2022.3215107.

R. Khanna et al., "A Simple Edge Termination Design for Vertical GaN PN Diodes," *IEEE Transactions on Electron Devices* 69(9), 5096 (2022), DOI: 10.1109/TED.2022.319279.

D. Ji et al., "A Discussion on Various Experimental Methods of Impact Ionization Coefficient Measurement in GaN," *AIP Advances* 12, 030703 (2022), DOI: 10.1063/5.0083111.

L. Yates et al., "Demonstration of >6.0 kV Breakdown Voltage in Large Area Vertical GaN PN Diodes with Step-Etched Junction Termination Extensions," *IEEE Transactions on Electron Devices* 69(4), 1931 (2022), DOI: 10.1109/TED.2022.3154665.

M. Ebrish et al., "Impact of Anode Thickness on Breakdown Mechanisms in Vertical GaN PiN Diodes with Planar Edge Termination," *Crystals* 12(5), 623 (2022), DOI: 10.3390/cryst12050623.

J. C. Gallagher et al., "Optimizing Performance and Yield of Vertical GaN Diodes Using Long Range Optical Techniques," *Scientific Reports* 12, 658 (2022), DOI: 10.1038/s41598-021-04170-2.

J. C. Gallagher et al., "Effect of GaN Substrate Properties on Vertical GaN PiN Diode Electrical Performance," *Journal of Electronic Materials* 50, 3013 (2021), DOI: 10.1007/s11664-021-08840-9.

M. A. Ebrish et al., "A Study on the Impact of Mid-Gap Defect States on Vertical GaN Diodes," *IEEE Transactions on Semiconductor Manufacturing* 33(4), 546 (2020), DOI: 10.1109/TSM.2020.3019212.

B. Conference Talks and Proceedings

L. Yates et al., "Recent Progress in Medium-Voltage Vertical GaN Power Devices," *244th Meeting of the Electrochemical Society*, Gothenburg, Sweden (October 2023).

M. E. Liao et al., "Origins of Epitaxial Surface Haze on GaN Substrates for kV Power Devices," *American Conference on Crystal Growth and Epitaxy / US Workshop on Organometallic Vapor Phase Epitaxy (ACCGE/OMPVE)*, Tucson, AZ (August 2023).

J. C. Gallagher et al., "Using Machine Learning Models to Locate Defective Regions on GaN Epi-Wafers," *Lester Eastman Conference on Advanced Devices*, Chicago, IL (August 2023).

J. C. Gallagher et al., "Accuracy of Machine Learning Models on Predicting the Properties of Vertical GaN Diodes," *International Conference on Compound Semiconductor Manufacturing Technology (CS Mantech)*, Orlando, FL (May 2023).

T. J. Anderson et al., "Scalable Manufacturing of Planar, Large-Area 1.2 kV and 3.3 kV Vertical GaN PiN Diodes," *International Conference on Compound Semiconductor Manufacturing Technology (CS Mantech)*, Orlando, FL (May 2023).

M. Ebrish et al., "Impact of Anode Doping on Avalanche in Planar 1.2 kV Vertical GaN PiN Diodes," *Government Microcircuit Applications and Critical Technology Conference (GOMAC)*, San Diego, CA (March 2023).

J. C. Gallagher et al., "Predicting Breakdown Failures in GaN Diodes Using Machine Learning Models with Optical Profilometry," *Government Microcircuit Applications and Critical Technology Conference (GOMAC)*, San Diego, CA (March 2023).

L. Yates et al., "Development of High-Current, Large-Area Vertical GaN Power Devices," *Workshop on Compound Semiconductor Materials and Devices (WOCSEMMAD)*, San Antonio, TX (February 2023).

R. Kaplar et al., "Progress in Medium-Voltage Vertical GaN Power Devices," *Workshop on Compound Semiconductor Materials and Devices (WOCSEMMAD)*, San Antonio, TX (February 2023).

J. Flicker and R. Kaplar, "Reverse Breakdown Time of Wide-Bandgap Diodes," *IEEE Workshop on Wide-Bandgap Power Devices and Applications (WiPDA)*, Redondo Beach, CA (November 2022).

B. Shankar et al, "Study of Avalanche Behavior in 3 kV GaN Vertical PN Diode Under UIS Stress for Edge Termination Optimization," *IEEE International Reliability Physics Symposium (IRPS)*, Dallas, TX (March 2022).

S. Chowdhury et al., "Current Status of GaN Vertical Technology Development for High Voltage Applications," *Government Microcircuit Applications and Critical Technology Conference (GOMAC)*, Miami, FL (March 2022).

M. Ebrish et al., "Edge Termination Design for Planar 1.2 kV Vertical GaN PiN Diodes", *Government Microcircuit Applications and Critical Technology Conference (GOMAC)*, Miami, FL (March 2022).

R. Kaplar et al., "Progress in Fabrication and Characterization of Vertical GaN Power Devices," *Workshop on Compound Semiconductor Materials and Devices (WOCSEMMAD)*, Destin, FL (February 2022).

R. Kaplar et al., "Progress in Vertical Gallium Nitride Power Devices," *PowerUp Conference* Virtual (December 2021).

B. Shankar et al., "On-Wafer Investigation of Avalanche Robustness in 1.3 kV GaN on GaN PN Diode under Unclamped Inductive Switching Stress," *IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Virtual (November 2021).

R. Kaplar et al., "Vertical Gallium Nitride PN Diodes for Grid Resiliency and Medium-Voltage Power Electronics," *240th Meeting of the Electrochemical Society*, Virtual (October 2021).

R. Kaplar et al., "Vertical Gallium Nitride Devices for Medium Voltage Power Electronics," *IEEE Electrical Conversion Congress and Exposition*, Virtual (October 2021).

M. A. Ebrish et al., "Investigation of Hybrid Edge Termination Designs for Vertical 1.2kV GaN PiN Diodes," *Lester Eastman Conference on High Performance Devices*, South Bend, IN (August 2021).

J. C. Gallagher et al, "Using Long Range Optical Techniques to Predict Vertical GaN Diode Performance," *Lester Eastman Conference on High Performance Devices*, South Bend, IN (August 2021).

R. Kaplar et al., "Vertical GaN Power Electronics – Opportunities and Challenges," *American Physical Society March Meeting*, Virtual (March 2021).

R. Kaplar et al., "Development of High-Voltage Vertical GaN PN Diodes," *PowerAmerica Webinar* (December 2020).

R. Kaplar et al., "Development of High-Voltage Vertical GaN PN Diodes," *IEEE International Electron Devices Meeting (IEDM)*, Virtual (December 2021).

R. Kaplar et al., "Development of High-Voltage Vertical GaN PN Diodes," *Materials Research Society Spring/Fall Meeting*, Virtual (November 2020).

G. M. Foster et al., "Recovery of Sidewall Etch Damage in p-type Gallium Nitride," *Electronic Materials Conference*, Virtual (June 2020).

J. C. Gallagher et al., "Predicting the Quality of Vertical GaN Devices Using Long-Range Optical Techniques," *Electronic Materials Conference*, Virtual (June 2020).

C. Status Reports

Quarterly status reports were submitted for FY19Q4 through FY23Q3.

D. Media Reports

R. Kaplar et al., "Record-Breaking Grid Protection Switches," Sandia National Laboratories Advanced Science and Technology Labs Accomplishments (2023).

R. Kaplar et al., "Targeting Medium-Voltage Power Electronics with Vertical GaN Devices", *Compound Semiconductor* 27(7), 54 (2021).

E. Invention Disclosures

iEdison disclosure 687308-22-001, "High Voltage Gallium Nitride vertical PN Diode" (Sandia, January 2022).

iEdison disclosure 10067820-22-0001, "Ohmic Contacts to N -Face n-type GaN" (EDYNX, January 2022).

iEdison disclosure 10067820-22-0002, "High RelabilityGaN pn Diode Structures" (EDYNX, January 2022).

F. Patent Applications

T. J. Anderson, et al. "Multi-Layer Hybrid Edge Termination for III-N Power Devices," U.S. Patent Application 17876163, filed 7/2022.

T. J. Anderson et al., "Selective-Area Doping of III-N Materials Utilizing Diffused Dopant Species and Method of Fabricating Devices," U.S Patent Application 63326296, filed 4/2022.

L. Yates et al., "Selective-Area Doping of III-N Materials Utilizing Diffused Dopant Species and Method of Fabricating Devices," U.S. Patent Application 17/572360, filed 1/2022.

J.C. Gallagher et al., "Surface Profile Mapping Techniques for Evaluating III-N Device Performance and Yield," U.S. Patent Application 17/345012, filed 6/2021.

T. J. Anderson et al., "Mapping and Evaluating GaN Wafers for Vertical Device Applications," U.S. Patent 11,415,518, filed 6/2020.

G. Licensed Technologies

N/A

H. Networks/Collaborations Fostered

The partner institutions (Sandia, NRL, Stanford, Boston University, EDYNX, and Sonrisa) had a very strong collaboration on this project, and some collaborations are expected to continue.

I. Websites Featuring Project Work Results

N/A

J. Other Products (e.g. Databases, Physical Collections, Audio/Video, Software, Models, Educational Aids or Curricula, Equipment or Instruments)

N/A

K. Awards, Prizes, and Recognition

N/A

Follow-On Funding

Additional funding committed or received from other sources (e.g. private investors, government agencies, nonprofits) after effective date of ARPA-E Award.

Table 2. Follow-On Funding Received.

Source	Funds Committed or Received
DOE/DoD Joint Munitions Program	FY24 $500K, FY25 $500K
DOE NNSA	Proprietary
Naval Research Lab	FY25-FY27 $1650K total (tentative)