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Journal:	*Electron Device Letters*
Manuscript ID	EDL-2025-02-0330
Manuscript Type:	Letters
Date Submitted by the Author:	14-Feb-2025
Complete List of Authors:	Wang, Yifan; Virginia Polytechnic Institute and State University Xiao, Ming; Xidian University Yang, Zineng; Virginia Polytechnic Institute and State University Porter, Matthew; Virginia Polytechnic Institute and State University cheng, Kai; Enkris Semiconductor Inc Song, Qihao; Virginia Polytechnic Institute and State University Kravchenko, Ivan; Oak Ridge National Laboratory Center for Nanophase Materials Sciences Zhang, Yuhao; The University of Hong Kong Department of Electrical and Electronic Engineering
Keyword:	Avalanche breakdown, Circuit testing, Gallium compounds, Power electronics, Power semiconductor devices, Sapphire, Semiconductor device fabrication

Robust Avalanche (1.5 kV, 2 kA/cm^2) in Vertical GaN Diodes on Patterned Sapphire Substrate

Yifan Wang, Ming Xiao, Zineng Yang, Matthew Porter, Kai Cheng, Qihao Song, *Student Member, IEEE*
Ivan Kravchenko, Yuhao Zhang, *Senior Member, IEEE*

***Abstract*— The lack of avalanche capability is a key limitation of current lateral GaN devices. Despite the report of avalanche in vertical GaN-on-GaN devices, the high wafer cost hinders device commercialization. Here we demonstrate a circuit-level avalanche in vertical GaN diodes on low-cost patterned sapphire substrate (PSS), with the avalanche voltage (1.57 kV) and avalanche current density (>2 kA/cm^2) both being the highest reported in GaN devices on foreign substrates. The PSS enables a lower dislocation density than conventional sapphire substrate and is employed in high-voltage GaN devices for the first time. The avalanche voltage in the circuit test reaches 98% of the parallel-plane limit, further affirming that near-ideal avalanche breakdown can be realized on GaN devices on foreign substrates. These results show the promise of the GaN-on-PSS platform for low-cost, robust power devices.[1]**

***Index Terms*— power electronics, gallium nitride, patterned sapphire substrate, avalanche, breakdown voltage, circuit test**

I. Introduction

Gallium nitride (GaN) lateral power devices on sapphire and Si substrates have been commercialized with a market size exceeding $1 billion. However, a key limitation of these devices is the lack of avalanche capability, which disallows devices to dissipate the surge energy in circuits and requires a large margin in breakdown voltage (BV) design and thereby a higher specific on-resistance [1]. A solution to this issue is deploying the p-n junction in vertical GaN devices with an optimal design of edge termination. Avalanche-capable vertical GaN p-n diodes [2]–[18] and transistors [19] has been reported recently.

However, two key gaps persist on the avalanche robustness of GaN devices. First, in most early reports, avalanche is only verified by the positive temperature coefficient (η_T) of the BV extracted at a low current compliance (e.g., 0.1 A/cm^2) in the static I-V sweep. In contrast, the avalanche required in circuit applications has to withstand a concurrence of high avalanche voltage (BV_{AVA}) and high avalanche current (I_{AVA}), as well as respond in sub-μs dynamic switching [1]. Very recently, such avalanche robustness has been reported by a few groups [10], [13], [15], [17], [18], [20] through inductive circuit tests.

The second gap is regarding the avalanche robustness in GaN on foreign substrates. While most avalanche GaN devices are reported on native substrates, the high wafer cost hinders device commercialization. To date, there are only a few reports [17], [18] of circuit-level avalanche (i.e., concurrence of high I_{AVA} and BV_{AVA} that can only be measured by circuit method) in GaN-on-sapphire devices, but their BV_{AVA} and I_{AVA} are much inferior to GaN-on-GaN. It is unknown if a comparable avalanche can be realized in low-cost GaN on Si/sapphire, which suffer a higher dislocation density.

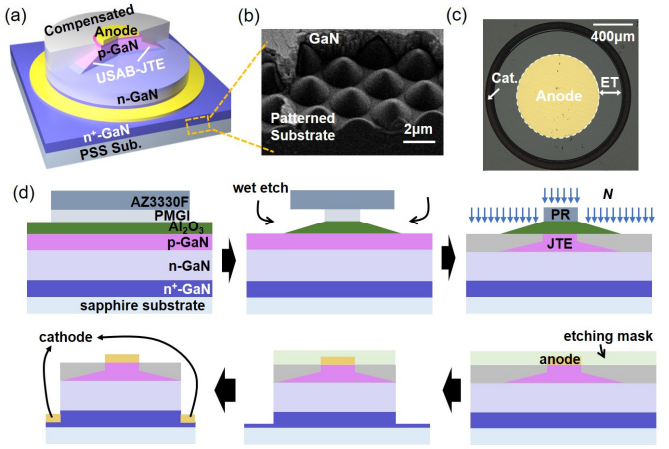

Fig. 1 (a) 3D schematics of quasi-vertical GaN-on-PSS p-n diode with JTE. (b) SEM image of the cleaved PSS showing the patterned growth seed. (c) Top view optical microscopic image of the fabricated device. (d) Key fabrication steps including Al_2O_3 mask wet etch, nitrogen implantation, quasi-vertical device deep etch, and contact formation.

This work addresses this gap by demonstrating a record high avalanche capability in vertical GaN diodes on sapphire. Here we adopt the cost-effective patterned sapphire substrate (PSS), which enables a lower dislocation density in GaN as compared to the conventional sapphire substrate. The PSS is widely used in GaN light-emitting diodes [21] but has not been explored in power devices. Here we fabricate the GaN-on-PSS diode with an ultra-small angle beveled junction termination extension (USAB-JTE) and characterize it in the unclamped inductive switching (UIS) circuit. The fabricated device exhibits an I_{AVA} over 2 kA/cm^2 at BV_{AVA} >1.5 kV, with the I_{AVA} and avalanche energy comparable to the best reports in GaN-on-GaN devices.

II. Epi Growth and Device Fabrication

Fig. 1(a) shows the 3D schematic of the fabricated device. The epitaxial structure consists of 20 nm p^{++}-GaN ([Mg] = 10^{20} cm^{-3}), 500 nm p$^+$-GaN ([Mg] = 10^{19} cm^{-3}), 10 μm n-GaN ([Si] ~ 10^{16} cm^{-3}), 4 μm n$^+$-GaN ([Si] = 2×10^{18} cm^{-3}), and a buffer layer, all grown on the PSS by Enkris Semiconductor. C-V analysis reveals the net donor concentration in n-GaN (N_D-N_A) to be 1.6×10^{16} cm^{-3}. Fig. 1(b) shows the scanning electron microscopy (SEM) image of the pyramidal PSS after the sample cleaving. The full-width at half-maximum (FWHM) of the (002) and (102) X-ray diffraction rocking curves is 246 and 307

[1]Y. Wang, Z. Yang, M. Porter, and Q. Song are with the Center of Power Electronics Systems, Virginia Tech, Blacksburg, VA 24060 USA.
Y. hang was with Virginia Tech, Blacksburg, VA 24060 USA, and is now with the Department of Electrical and Electronic Engineering, University of Hong Kong, Hong Kong, China. (Email: yuhzhang@hku.hk)
M. Xiao is with Xidian University, Xi'an, 710071 China.
K. Cheng is with Enkris Semiconductor Inc., Suzhou 215123 China.
I. Kravchenko is with the Center for Nanophase Materials Sciences, Oak Ridge National Laboratory, Oak Ridge, Tennessee 37830 USA.

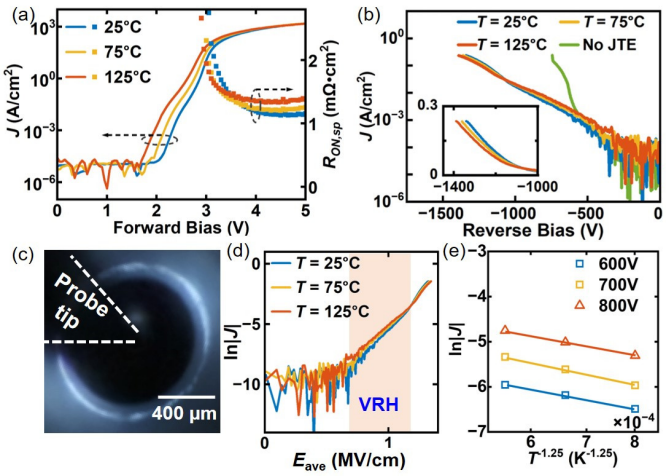

Fig. 2. (a) Forward I-V characteristics and the extracted differential $R_{ON,SP}$ of the GaN-on-PSS JTE p-n diode at different temperatures. (b) Reverse I-V characteristics at different temperatures up to a 0.2 A/cm^2 current compliance; (inset) zoom-in view of the breakdown regime. (c) Electroluminescence image taken for the JTE device under 1500 V stress for 10 seconds. (d) ln|J| versus average E-field in the depletion region with the VRH regime marked. (e) ln|J| versus $T^{1.25}$ at temperatures of 300, 350 and 400 K for three reverse biases.

arcsec, respectively, for the GaN epi layer grown on this PSS. The screw dislocation density, which is related to bulk leakage current in GaN devices, is estimated to be 1.2×10^8 cm^{-2} from the (002) FWHM [22], [23], which is lower than the usual value (>10^{18} cm^{-3}) reported for the GaN epi on sapphire [24].

The quasi-vertical GaN-on-PSS p-n diode deploys a USAB-JTE edge termination, which realizes the spatially-distributed E-field by reducing the JTE bevel angle [15]. Fig. 1(c) shows the top-view optical microscopic image of the fabricated device with an anode radius of 400 μm and a JTE length of ~100 μm. Moreover, the USAB-JTE formation only requires a single planar implantation with a wide process window for the implant depth, as illustrated in Fig. 1(d) for main fabrication steps.

The fabrication starts with a deposition of 250 nm Al_2O_3 at 200 °C in a plasma-enhanced atomic layer deposition, followed by coating a bilayer photoresist that consists of 2 μm PMGI-SF11 and 3 μm AZ3330F. After hard-bake, samples are immersed in AZ300MIF solution (i.e., diluted TMAH) for wet etch. The etch rate of PMGI is found to be over 600 times higher than Al_2O_3, producing a large PMGI undercut and a small Al_2O_3 bevel angle below 1°. This beveled Al_2O_3 serves as the dielectric mask for nitrogen implantation, transferring the small bevel angle to the uncompensated p-GaN to form a JTE. A five-energy combination of 25, 80, 150, 240 and 320 keV with doses of 8.54, 1.51, 1.36, 5.81 and 4.48×10^{12} cm^{-3} are used to create a box-like profile that fully compensate p$^+$-GaN uncovered by the Al_2O_3 mask. This full compensation allows a process robustness against the implant depth variation, which is known to be a challenge of the prior bi-layer, partially-implanted JTE that requires an accurate control of the compensation depth down to nm-scale [3], [25]. A post-implantation annealing at 560 °C is performed in N_2. After this JTE formation, a quasi-vertical structure is etched, with anode and cathode formed on p$^+$-GaN and n$^+$-GaN, respectively. A thick anode metal stack Pd/Ni/Au (50/80/180 nm) is used to ensure effective current spreading during the avalanche circuit test.

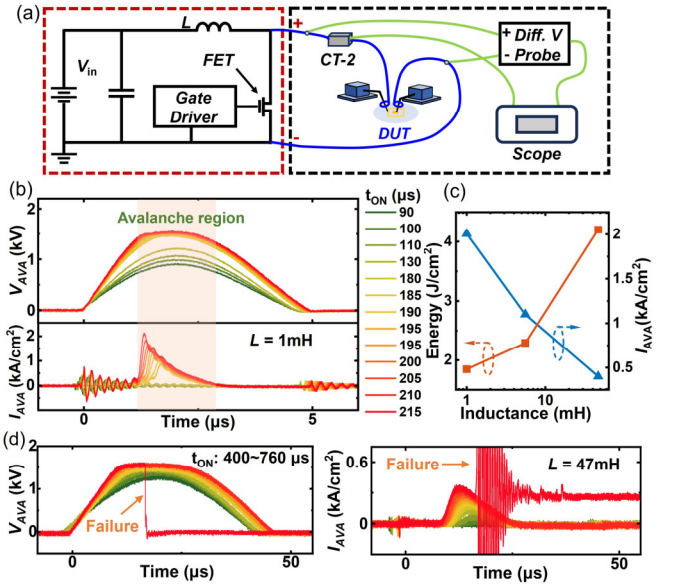

Fig. 3. (a) Illustration of the on-wafer UIS test setup, including the UIS circuit schematics, DUT, probes, and current/voltage measurement setups. The CT-2 current transformer is used for current measurement and is connected to the probes in contact with cathode and anode. (b) UIS waveforms of the fabricated diode with varying on-state time to charge the load inductor (t_{on}) under 1 mL load inductance. (c) The measured critical I_{AVA} and E_{AVA} at device failure as a function of load inductance. (d) UIS waveforms under varying t_{on} and 47 mH load; the voltage and current waveforms at device failure are also included.

III. Device Characterization and Circuit Test

Fig. 2(a) shows forward I-V characteristics of the fabricated device at 25-125 °C. The current density is normalized to anode area in this work. The differential specific resistance ($R_{ON,SP}$) is 1.1 mΩ·cm^2 at 25 °C and 1.3 mΩ·cm^2 at 125 °C. The on/off ratio is over 10^9 at 25 °C. The turn-on voltage is at about 3.2V.

Fig. 2(b) shows the reverse I-V characteristics of the device at 25-125 °C up to a current compliance of 0.2 A/cm^2. The non-destructive BV extracted at such a leakage current compliance increases from 770 V for the device without JTE to 1350 V for the device with JTE. In the JTE device, at bias above 1000 V, the leakage current reduces at higher temperature, and the non-destructive BV exhibits a positive η_T. These phenomena suggest the avalanche breakdown. Note that, as compared to the steep avalanche I-V in GaN-on-GaN devices, the I-V characteristics in our GaN-on-PSS device show a flatter pattern. This can be ascribed to the superposition of dislocation-associated leakage current, which features a gradual increase with voltage.

As a further proof, Fig. 2(c) shows the top-view electroluminescence image of the JTE device taken under a 10 seconds stress at 1500 V. Such luminescence is produced from the recombination of electrons and holes generated in impact ionization (I.I.). The uniform luminescence in the device periphery confirms a non-localized avalanche, which indicates the potential to achieve a high I_{AVA} [20]. Note that the luminescence signal in the active region is not visible due to the thick and opaque anode metals.

Below the avalanche bias regime, the device leakage current is found to agree with the variable range hopping (VRH) model. The VRH model features $J \propto \exp\left(E_{ave}/T^{1.25}\right)$ [24], where J is the current density, E_{ave} is the average E-field in the depleted region, and T is temperature. The E_{ave} can be derived by $E_{ave} =$

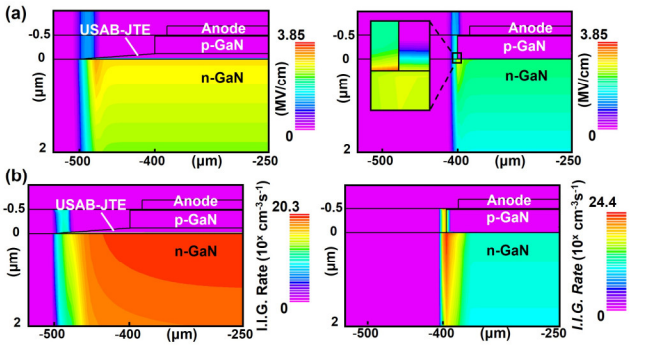

Fig. 4. Simulated (a) *E*-field contours and (b) I. I. generation rate contours of the devices with and without JTE at their respective *BV*.

$\sqrt{qN_D\,V/2\varepsilon}$ at the reverse bias (V) below the punch-through. Fig. 2(d) and 2(e) shows the derived ln|J| *vs.* E_{ave} and ln|J| *vs.* $T^{1.25}$ plots based on experimental data, revealing a good linearity in both plots, which verifies the VRH model.

The UIS circuit is the JEDEC standard to evaluate the I_{AVA} and avalanche energy of power devices [1]. Here we develop an UIS circuit board integrated with the probe station to directly test bare-die devices (Fig. 3(a)), which is similar to the setup in [26]. The circuit board comprises banana plug cables that are attached to the probe tip via an alligator clip. A 3D-printed holder places the circuit board in proximity to the device. A FET (3.3 kV SiC MOSFET) is placed in parallel with the GaN diode. The FET is first turned on to charge the inductor (L). Subsequently, it is turned off, and the energy stored in L is withstood by the FET and diode, driving the latter into avalanche (as it has a lower BV_{AVA}).

Fig. 3(b) shows the voltage and current waveforms in the UIS tests with the increased turn-on time under L of 1 mH, which corresponds to the increased energy dissipated via avalanche. Device voltage is clamped at BV_{AVA}~1570 V while dissipating an I_{AVA} >2 kA/cm^2, exhibiting a signature avalanche waveform. Fig. 3(c) shows the I_{AVA} and E_{AVA} at device failure measured under three different L, revealing a peak avalanche energy over 4 J/cm^2. At a lower L, I_{AVA} decreases, enabling a longer avalanche time before thermal failure; this further results in a higher E_{AVA}. Fig. 3(d) shows the avalanche waveforms under L of 48 mH, as well as the waveform at device failure. The device shows a mid-avalanche thermal failure at the critical E_{AVA}.

TCAD simulations are performed based on the I. I. models described in [15]. Fig. 4 shows the simulated contours of E-field and I. I. generation rates of the devices with and without the JTE, at their respective BV. The JTE not only suppresses the peak E-field but also transforms a highly localized I. I. into spatially distributed I. I., enabling high I_{AVA}.

Fig. 5(a) compares the differential $R_{ON,SP}$ *vs.* BV_{AVA} for the state-of-the-art avalanche-capable GaN p-n diodes on GaN [3], [4], [9], [15], sapphire [17], [18], and Si [16] substrates. Our GaN-on-PSS diode exhibits one of the best $R_{ON,SP}$ *vs.* BV_{AVA} trade-offs in avalanche GaN diodes on foreign substrates. Fig. 5(b) benchmarks the circuit-level I_{AVA} *vs.* BV_{AVA} reported in GaN-on-GaN [10], [15], [20], GaN-on-sapphire [17], [18], SiC [27], [28] and Ga_2O_3 [29] diodes. Our diode shows one of the highest I_{AVA} in kilovolt GaN devices, comparable to the best reports in GaN-on-GaN. Though the I_{AVA} is lower than the best report in SiC, GaN-on-PSS device can provide a cost advantage (up to 65% [31]) over the SiC counterparts.

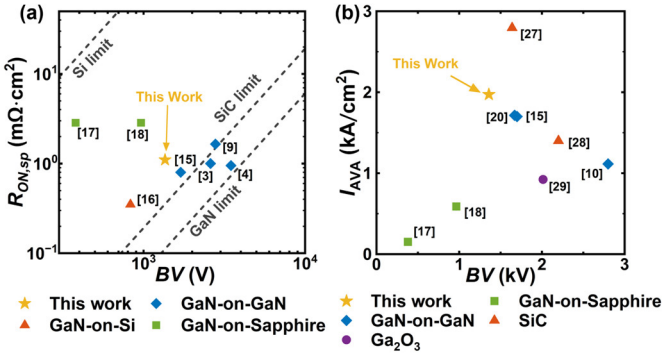

Fig. 5. (a) Benchmark of differential $R_{ON,SP}$ versus BV_{AVA} for the state-of-the-art avalanche-capable vertical GaN diodes on GaN, sapphire, and Si substrates. (b) Benchmark of circuit-level I_{AVA} versus BV_{AVA} for our device and GaN-on-GaN and GaN-on-sapphire devices, as well as SiC and Ga_2O_3 devices. Here we mainly include the reports of devices with an anode area over 0.2 mm^2.

Table I lists key metrics of the reported vertical GaN p-n diodes with circuit-level avalanche. The BV_{AVA}/BV_{AVA}^{pp} is the ratio between BV_{AVA} and the parallel-plane limit BV_{AVA}^{pp}. Based on the punch-through design, BV_{AVA}^{pp} is calculated by $BV_{AVA}^{pp} = E_C t - qN_D t^2/2\varepsilon$, where t is the drift region thickness and E_C is the avalanche breakdown field of GaN. The E_C dependence on N_D can be described by $E_C = E_{co}/[1 - a\log_{10}(N_D/10^{16})]$, where E_{co} and a are two fitting parameters; their values for GaN are reported in [30]. The BV_{AVA} of our GaN-on-PSS diodes extracted in the UIS test reaches ~98% of the BV_{AVA}^{pp}, revealing that a near ideal avalanche breakdown can be realized in low-cost vertical GaN devices on foreign substrates.

IV. Summary

This work demonstrates a robust avalanche in vertical GaN-on-PSS p-n diodes with an USAB-JTE. The device exhibits positive η_T in the non-destructive BV extracted at a low current compliance, as well as a uniform electroluminescence at the device periphery. The device avalanche is validated in the UIS tests with BV_{AVA} over 1.5 kV and I_{AVA} over 2 kA/cm^2. The BV_{AVA} is 98% of the parallel-plane limit and I_{AVA} is among the highest in vertical GaN devices. These results suggest the great potential of GaN power devices on the low-cost PSS platform.

TABLE I. Comparison of the key metrics of GaN, SiC and Ga_2O_3 diodes reported with circuit-level avalanche capability.

Material	Ref	Active Area (mm^2)	I_{AVA} (kA/cm^2)	BV_{AVA} (kV)	BV_{AVA}/BV_{PP}^{AVA} [a]
GaN-on-GaN	[10]	0.13	1.12	2.8	85%
	[15]	0.79	1.7	1.7	83%
	[20]	1.4	1.71	1.67	83%
GaN-on-PSS	**This work**	**0.79**	**2**	**1.57**	**98%**
GaN-on-sapphire	[17]	0.031	0.15	0.38	58%
	[18]	1.9	0.59	0.96	N/A
SiC	[27]	0.64	2.8	1.5	N/A
	[28]	1	1.4	2.2	N/A
Ga_2O_3	[29]	9	0.92	2.01	N/A

[a] The drift region thickness and doping are not fully disclosed in some devices or more advanced designs are used in some devices, resulting in the difficulties to accurately estimate BV_{PP}^{AVA}.

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