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Fermi National Accelerator Laboratory
Computer Division
Data Acquisition Electronics Department

Draft Specification
Fiberoptic Data Transmission Link

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1.0 General Information

1.1 Overview

This fiberoptic data link can be thought of as a general purpose, optically isolated, point-to-point port through which information can be transmitted at relatively high data rates. A commercially available transmitter/receiver chipset, manufactured by Advanced Micro Devices (AMD) and called TAXI, is used. The transmitter chip encodes up to 10 parallel data bits, serializes them, and outputs the result at 125 Mbits/sec. This serial data stream is then fed to an optical transmitter which passes the data through a fiberoptic cable to a remote optical receiver. This optical receiver then converts the optical signal into an electrical bit stream that is applied to the input of the AMD receiver chip. The receiver chip decodes the data, performs a serial-to-parallel conversion, and then outputs the data in parallel along with a strobe which occurs at a data valid point. The result of this operation is the transfer of parallel data over a serial optical link that is basically transparent to the user.

In the Silicon Strip Detector (SSD) application, the fiberoptic data link is configured to transfer data at 50 Mbytes/sec. This rate requires that four individual fiber links be used, each transmitting 10 data bits (a total of 40 bits; 32 bits of data, 8 bits of status), at a rate of 10.42 Mbytes/sec.

1.11 Standard Bus System Used

The SSD readout system is being implemented in the FASTBUS standard. The fiberoptic data link aquires power (+5V) from the FASTBUS crate. Both the optical transmitter and receiver are physically mounted on FASTBUS auxiliary boards but have no physical connection to the FASTBUS backplane.

1.12 Number of Channels

Basically, the fiberoptic data link is a single channel port, connecting a transmitting node to a receiving node operating at a data transfer rate of 41.68 Mbytes/sec. Word width at the transmitting and receiving node is 40 bits (32 bits of data, 8 bits of status).

1.2 Application

The fiberoptic data link is a point-to-point pipelined data mover presently capable of transmitting data at 41.68 Mbytes/sec. Any application that may require data transfers at this rate or higher is a potential customer for this link.

1.3 Packaging

The fiberoptic data link requires no special packaging, and may be implemented in any system that provides the proper voltages. In the SSD case, the transmitting node is packaged on a FASTBUS auxiliary board. The receiving node can be implemented in any appropriate configuration or system capable of accepting 40 bits of parallel data and a strobe every 96 ns.

1.32 Pinout

The connections between the FASTBUS board and the auxiliary board containing the fiberoptic data link components will be as defined in Table I of this specification. The connection to the outside world will be through 5 fiberoptic cable connectors located on the auxiliary backplane board.

Table 1 : Sequencer Module Pin List

(Viewed From Front of Crate-3/7/89)

,Ø1 Clock, Slot 25,23,21	B01-Reset	A01-53MHZ,Ø1 Clock, Slot 12,10,8
,Ø1 Clock, Slot 19,17,15	B02-S0	A02-53MHZ,Ø1 Clock, Slot 6,4,2
ata 0, Slot 24	B03-S1	A03-Hit Data 0, Slot 1
ata 1, Slot 24	B04-S2	A04-Hit Data 1, Slot 1
ata 2, Slot 24	B05-S3	A05-Hit Data 2, Slot 1
ata 3, Slot 24	B06-S5	A06-Hit Data 3, Slot 1
ata 4, Slot 24	B07-LINK ERROR	A07-Hit Data 4, Slot 1
ata 5, Slot 24	B08-SSTROBE	A08-Hit Data 5, Slot 1
ata 6, Slot 24	B09-Sync	A09-Hit Data 6, Slot 1
ata 7, Slot 24	B10-Sync Err	A10-Hit Data 7, Slot 1
Valid, Slot 24	B11-D00	A11-Data Valid, Slot 1
-5.2 Volts	B12-D01	A12-VEE, -5.2 Volts
Data 0, Slot 20	B13-D02	A13-Hit Data 0, Slot 5
ata 1, Slot 20	B14-D03	A14-Hit Data 1, Slot 5
Data 2, Slot 20	B15-D04	A15-Hit Data 2, Slot 5
Data 3, Slot 20	B16-D05	A16-Hit Data 3, Slot 5
Data 4, Slot 20	B17-D06	A17-Hit Data 4, Slot 5
Data 5, Slot 20	B18-D07	A18-Hit Data 5, Slot 5
ata 6, Slot 20	B19-D08	A19-Hit Data 6, Slot 5
a 7, Slot 20	B20-D09	A20-Hit Data 7, Slot 5
lid, Slot 20	B21-D10	A21-Data Valid, Slot 5
	B22-D11	A20-GND
ata 0, Slot 16	B23-D12	A23-Hit Data 0, Slot 9
ata 1, Slot 16	B24-D13	A24-Hit Data 1, Slot 9
ata 2, Slot 16	B25-D14	A25-Hit Data 2, Slot 9
Data 3, Slot 16	B26-D15	A26-Hit Data 3, Slot 9
Data 4, Slot 16	B27-D16	A27-Hit Data 4, Slot 9
Data 5, Slot 16	B28-D17	A28-Hit Data 5, Slot 9
Data 6, Slot 16	B29-D18	A29-Hit Data 6, Slot 9
Data 7, Slot 16	B30-D19	A30-Hit Data 7, Slot 9
Valid, Slot 16	B31-D20	A31-Data Valid, Slot 9
	B32-D21	A32-VEE, -5.2 Volts
26 MHZ Clock	B33-D22	A33-Right 26 MHZ Clock
Data 0, Slot 14	B34-D23	A34-Hit Data 0, Slot 11
Data 1, Slot 14	B35-D24	A35-Hit Data 1, Slot 11
Data 2, Slot 14	B36-D25	A36-Hit Data 2, Slot 11
Data 3, Slot 14	B37-D26	A37-Hit Data 3, Slot 11
Data 4, Slot 14	B38-D27	A38-Hit Data 4, Slot 11
Data 5, Slot 14	B39-D28	A39-Hit Data 5, Slot 11
Data 6, Slot 14	B40-D29	A40-Hit Data 6, Slot 11
Data 7, Slot 14	B41-D30	A41-Hit Data 7, Slot 11
Valid, Slot 14	B42-D31	A42-Data Valid, Slot 11
	B43-D32	A43-VCC, +5.0 Volts
Data 0, Slot 18	B44-D33	A44-Hit Data 0, Slot 7
Data 1, Slot 18	B45-D34	A45-Hit Data 1, Slot 7
Data 2, Slot 18	B46-D35	A46-Hit Data 2, Slot 7
Data 3, Slot 18	B47-CLOCK	A47-Hit Data 3, Slot 7
Data 4, Slot 18	B48-Event Address Valid	A48-Hit Data 4, Slot 7
Data 5, Slot 18	B49-Event Address Wrt. En.	A49-Hit Data 5, Slot 7
Data 6, Slot 18	B50-Event Address 0	A50-Hit Data 6, Slot 7
Data 7, Slot 18	B51-Event Address 1	A51-Hit Data 7, Slot 7
Valid, Slot 18	B52-Event Address 2	A52-Data Valid, Slot 7
+5.0 Volts	B53-Event Address 3	A53-GND
Data 0, Slot 22	B54-Event Address 4	A54-Hit Data 0, Slot 3
Data 1, Slot 22	B55-Event Address 5	A55-Hit Data 1, Slot 3
Data 2, Slot 22	B56-Event Address 6	A56-Hit Data 2, Slot 3
Data 3, Slot 22	B57-Event Address 7	A57-Hit Data 3, Slot 3
Data 4, Slot 22	B58-D36	A58-Hit Data 4, Slot 3
Data 5, Slot 22	B59-D37	A59-Hit Data 5, Slot 3
Data 6, Slot 22	B60-D38	A60-Hit Data 6, Slot 3
Data 7, Slot 22	B61-D39	A61-Hit Data 7, Slot 3
Valid, Slot 22	B62-STROBE	A62-Data Valid, Slot 3
-5.2 Volts	B63-ACKNOWLEDGE	A63-GND
Z,Ø2 Clock, Slot 24,22,20	B64-GND	A64-53MHZ,Ø2 Clock, Slot 11,9,7
Z,Ø2 Clock, Slot 18,16,14	B65-VTT, -2 Volts	A65-53MHZ,Ø2 Clock, Slot 5,3,1

1.33 N/A

1.4 Power Requirements

The auxiliary card implementation will require the following voltages and currents:

Receiver	+5v @ 1.75A
Transmitter	+5v @ 1.5A

1.41 Control and Monitoring Requirements

The fiberoptic data link uses a simple standard protocol to communicate between transmitting and receiving nodes.

1.5 Cooling Requirements

The fiberoptic data link auxiliary board will be cooled by air passing over the surface of the auxiliary board.

1.6 Unusual Requirements N/A

2.0 Theory of Operation

2.1 Basic Operation

The fiberoptic data link is a data pipeline port through which parallel data is encoded, serialized, and transmitted optically over fiberoptic cable. At the receiving node the data is optically received, converted to electrical signals, decoded, de-serialized and then made available as parallel multi-bit words.

A block diagram of the fiberoptic data link is shown in Figure 1. This description assumes that there is a one-to-one correspondence between the transmitting node and the receiving node. In other words, there is one receiver connected to one transmitter. An alternative arrangement might be to connect multiple transmitting nodes to a single receiving node. In this case a Permit to Transmit is used at each SEQ or FSCC to control the number of nodes transmitting and the data is or'ed optically or electrically at the receiver.

In either case, the fiberoptic data link is operated according to a protocol that defines a very simple communication interchange between a transmitting and receiving node. The protocol does not stipulate a data transfer rate since future implementations of this link will likely be at higher data transfer rates.

The link itself has no intelligence. Data is applied to the link in parallel, received at the remote end, and then presented in parallel as though a multiconductor cable were connecting the two devices.

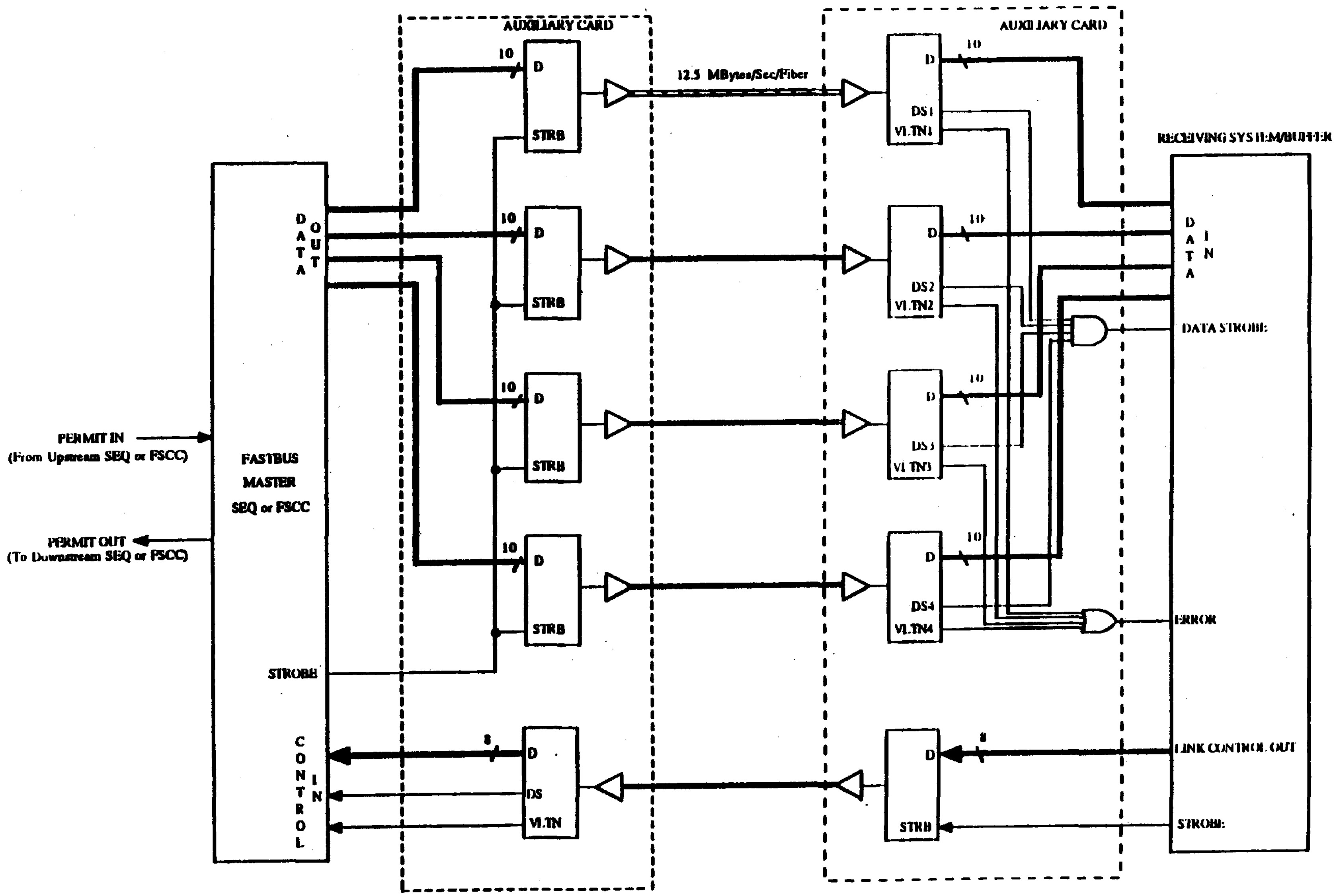

Figure 1; Fiberoptic ˈnk Block Diagram

The fiberoptic data link contains five separate fiberoptic channels, each operating at 10.42 Mbytes/sec. Four of the fibers carry pipeline data and status information to the remote node. The fifth fiber is used to transmit acknowledge or error information from the remote node back to the originating node. The four fibers carrying data to the remote node are operating at an aggregate rate of 41.68 Mbytes/sec, with the acknowledge link operating at 12.5 Mbytes/sec. Commercially available communication chips and optical components are used in the implementation of the link.

Appendix A of this document details the communication chips (AMD TAXI Chips) as well as the optical components used in this implementation.

2.2 N/A

2.3 Addressing Modes

The fiberoptic data link contains no system interface and is therefore not addressable.

2.31 Data Transfer Description and Transfer Rates

The FASTBUS data acquisition system communicates with the fiberoptic link through the FASTBUS auxiliary backplane. A FASTBUS module connects to the link through an auxiliary backplane connector. The fiberoptic data link components are mounted on a FASTBUS auxiliary board that plugs into the auxiliary backplane at the back of a standard FASTBUS crate. The link accepts 40 bit wide (32 bits of data, 8 bits of status) data words and a strobe using TTL logic levels. The FASTBUS transmitting module is responsible for implementing the simple communication protocol as detailed in Appendix A. through the use of the 8 status bits. The module must also supply the link with 32 bits of parallel data and a strobe. The rate of data transfer to the fiberoptic link is controlled by the FASTBUS transmitting module. A maximum rate of transfer between the module and the link is a 40 bit word every 80 ns. The transmitting link has the ability to signal the FASTBUS transmitter that is cannot accept data. This status flag can be used by the module to time the transmissions over the link. The optical receiving node can output a 40 bit data word and strobe at a maximum data rate of one per 80 ns.

An example of a data transfer using the link protocol is shown in Figure 2. The transmitter begins the communication session by transmitting a Start of Message (SOM) control code. The transmitting node waits for an acknowledge transmission from the receiving node for a specific amount of time (timeout protection). If and when the acknowledge signal arrives at the transmitter, data transmission begins. At the end of data an End of Message (EOM) is transmitted to the receiving node. The receiving node acknowledges that it has received the EOM code. Additional data transmissions could follow without waiting for the initial SOM/acknowledge again. The SOM merely tests the integrity of the link before transmitting data.

Figure 2 also contains an example of a communication session in which the receiving node detects an error. In this case an error message is transmitted back to the transmitting node. The transmitting node will continue to transmit data during the time it takes for the receiving node to detect an error and transmit that information back to the transmitting node. When the transmitting node realizes that an error message has arrived, an error handling routine must be activated that resolves the problem based on system level considerations.

3.0 Input/Output Specifications

3.1 Communication Interfaces

This link is in itself a communication port between a transmitting and receiving no implemented in almost any system. The fiberoptic link and a simple data pipeline communicatio.. protocol provides both electrical and logical system isolation. The transmitting node accepts data in parallel, transmits the data, receives the data at the remote node, and makes the data available in parallel as though a muticonductor cable were connected between the two points. This transparency makes the connection of two different systems relatively easy. The "bridge" between different systems is implemented in the design of the transmitting and receiving node interfaces to the fiber link.

3.11 Description and Operation of Ports

The fiberoptic link has a 40 bit (32 bits of data, 8 bits of status) parallel input port at the transmitting node and a 40 bit (32 bits of data, 8 bits of status) parallel output port at the receiving node. The link input port is accessed through a connection between a FASTBUS module and the FASTBUS auxiliary card containing the fiberoptic link components. The link output port will be available for use in any system implementation that is capable of accepting a 40 bit parallel data word.

3.12 Communication Protocol

The communication protocol will be implemented according to the emerging fiberoptic data link standard presently under review by the FASTBUS Standards Committee.

3.2 Analog/Digital Signals

3.21 Logic Levels

Digital signal levels at the input to the optical transmitting node and at the output of the opt... receiving node are at TTL levels.

4.0 System Software

4.1 Initialization N/A

4.2 System Software

Control of the link both at the transmitting and receiving end is the responsibility of the devices to which the link is interfaced. The SSD FASTBUS Smart Crate Controller and/or Sequencer will contain the required link control logic.

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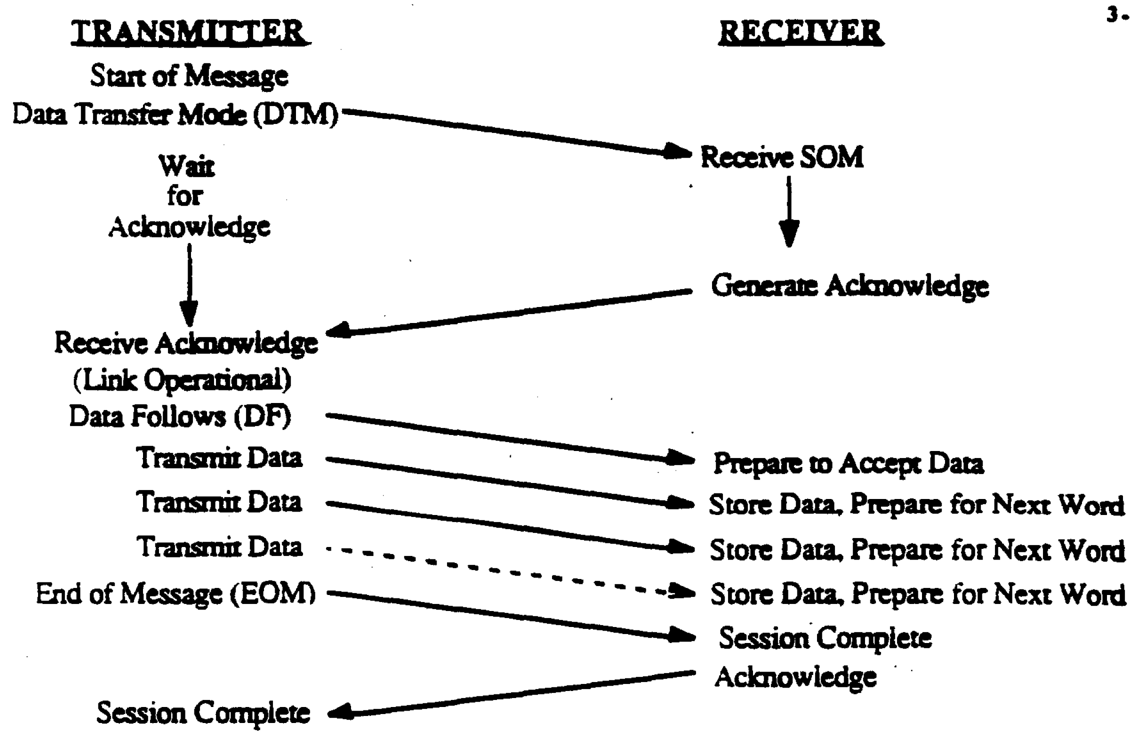
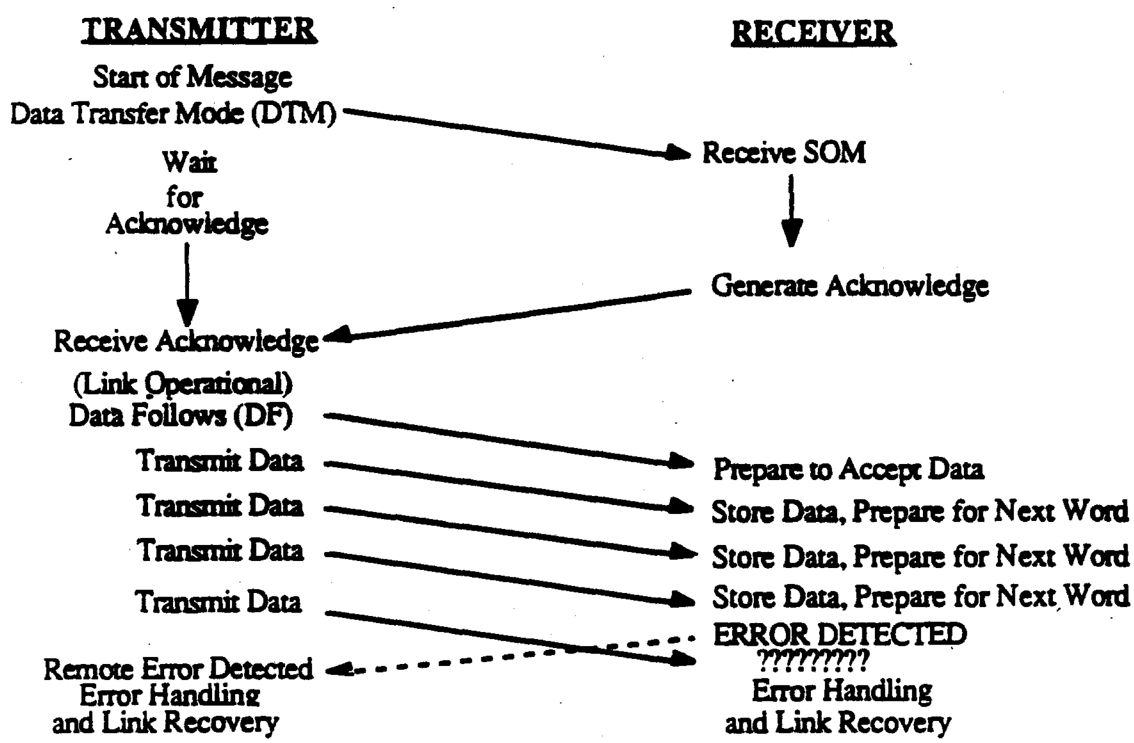


Normal Communication Session



Communication Session With Remote Error Detected

Figure 2: Communication Session Example